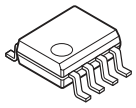
Precision Operational Amplifier

■ FEATURES

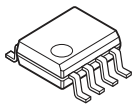
●Precision	V_{IO}=60 μV max.
	V_{IO}=100 μV max. (Ta= -40°C to +85°C)
●Low Offset Drift	$\Delta V_{IO}/\Delta T$=1.2μV/°C max. (Ta= -40°C to +85°C)
●CMR	115dB min.
●Low Noise	V_{NI}=80nVrms typ. at f=1 to 100Hz
	en=8nV/√Hz typ. at f=100Hz
●Open Loop Gain	Av=126dB min.
●Operating Temperature	Topr=-40°C to +105°C
●Guaranteed Temperature	Topr=-40°C to +85°C
●Unity Gain Stable	
●Operating Voltage	Vopr=±3V to±18V
●Unity Gain Frequency	f_T=1.1MHz typ.
●Package	NJMOP177GE(Single): SOP8 JEDEC 150mil
	NJMOP1772E(Dual): SOP8 JEDEC 150mil

●REPLACES INDUSTRY-STANDARD OPAMPS OP-07, OP-77, OP-177, OPA-177, AD707, etc.

■ PACKAGE OUTLINE



NJMOP177GE
(Single)



NJMOP1772E
(Dual)

■ GENERAL DESCRIPTION

The NJMOP177/NJMOP1772 are high precision operational amplifier features very low offset voltage and drift.

It also achieves high common mode rejection, low noise and high open loop gain. DC characteristics are 100% tested and specified from −40 to 85ºC.

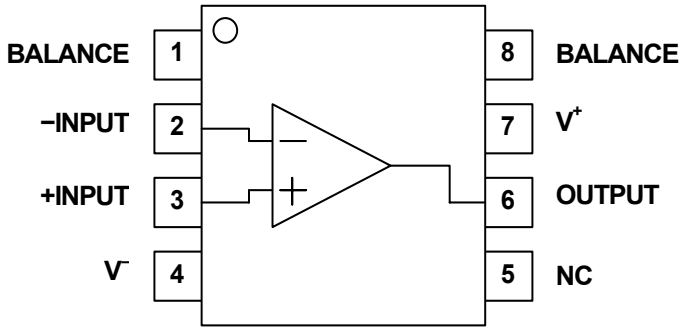
The NJMOP177/NJMOP1772 are suitable for high gain circuit amplified small signal and sets required stable behavior over a wide temperature range.

■ APPLICATION

●Thermocouple sensor
●Bridge Amplifier
●Current Sensor
●Instrumentation Amplifier
●Reference Voltage Circuit

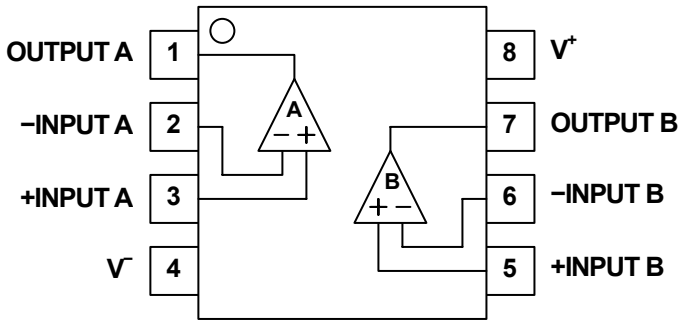
■ PACKAGE DESCRIPTION

(Top View)



NJMOP177GE

(Top View)



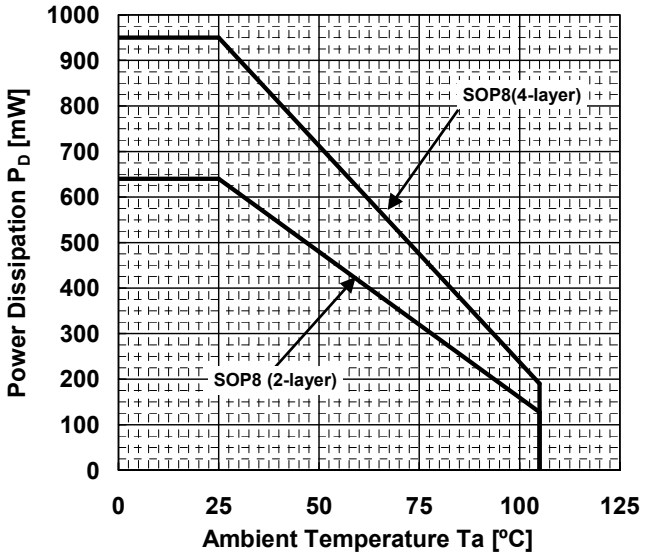
NJMOP1772E

■ ABSOLUTE MAXIMUM RATING(Ta=25ºC Unless Otherwise Specified)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+/V^-	±20	V
Common Mode Input Voltage (Note1)	V_{ICM}	±20	V
Differential Input Voltage	V_{ID}	±30	V
Power Dissipation	P_D	640(Note 2) 950(Note 3)	mW
Operating Temperature	Topr	-40～+105	℃
Storage Temperature	Tstg	-50～+125	℃

(Note1) For supply voltage less than ±20V, the maximum input voltage is equal to the supply voltage.
(Note2) Mounted on the EIA/JEDEC standard board (76.2×114.3×1.6mm, two layer, FR-4).
(Note3) Mounted on the EIA/JEDEC standard board (76.2×114.3×1.6mm, four layer, FR-4).
Refer to following Fig. A for a permissible loss when ambient temperature (Ta) is Ta≥25°C.

Fig. A Power Dissipation Derating Curve



■ RECOMMENDED OPERATING VOLTAGE

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+/V^-		±3	-	±18	V

■ ELECTRONIC CHARACTERISTICS (V^+/V^- = ±15V, Ta = +25ºC, V_{CM} = 0V unless otherwise specified)

● DC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Characteristics						
Input Offset Voltage	$V_{IO}1$		—	20	60	μV
	$V_{IO}2$	Ta = -40 to +85°C	—	20	100	μV
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$	Ta = -40→+25°C / Ta = +25°C→+85°C	—	0.3	1.2	μV/°C
Common Mode Input Voltage Range	$V_{ICM}1$		±13	±14	—	V
	$V_{ICM}2$	Ta = -40 to +85°C	±13	±13.5	—	V
Common Mode Rejection Ratio	CMR1	V_{CM} = 0V→-13V / V_{CM} = 0V→+13V	115	140	—	dB
	CMR2	Ta = -40 to +85°C, V_{CM}=0V→-13V / V_{CM}=0V→+13V	110	140	—	dB
Supply Voltage Rejection Ratio	SVR1	V^+/V^- = ±3V to ±18V	110	125	—	dB
	SVR2	Ta = -40 to +85°C, V^+/V^- = ±3V to ±18V	106	120	—	dB
Input Bias Current	I_B1		-2.8	1.2	2.8	nA
	I_B2	Ta = -40 to +85°C	-6	1.7	6	nA
Input Bias Current Drift	$\triangle I_B/\triangle T$	Ta = -40→+85°C	—	8	60	pA/°C
Input Offset Current	$I_{IO}1$		—	0.3	2.8	nA
	$I_{IO}2$	Ta = -40 to +85°C	—	0.3	4.5	nA
Input Offset Current Drift	$\triangle I_{IO}/\triangle T$	Ta = -40→+85°C	—	1.5	72	pA/°C
Differential Input Impedance	R_{ID}	(Note 4)	—	90	—	MΩ
Common-Mode Input Impedance	R_{IC}	(Note 4)	—	800	—	GΩ
Voltage Gain	Av1	R_L = 2kΩ, Vo = -10V→0V / 0V→+10V / -10V→+10V	126	142	—	dB
	Av2	Ta = -40 to +85°C, R_L = 2kΩ, Vo = -10V→0V / 0V→+10V / -10V→+10V	120	136	—	dB
Input Offset Voltage Trim (only NJMOP177)	Viotri	Rp = 20kΩ	—	±3	—	mV
Channel Separation (only NJMOP1772)	CS	DC	—	0.01	—	μV/V
Output Characteristics						
Maximum Output Voltage	$V_{OM}1$	R_L=10kΩ	±13.5	±14.0	—	V
	$V_{OM}2$	Ta = -40 to +85°C, R_L = 10kΩ	±13.0	±14.0	—	V
	$V_{OM}3$	R_L = 2kΩ	±12.5	±13.0	—	V
	$V_{OM}4$	Ta = -40 to +85°C, R_L = 2kΩ	±12.0	±13.0	—	V
	$V_{OM}5$	R_L = 1kΩ	±12.0	±12.5	—	V
Output Impedance	R_O	Open-Loop	—	60	—	Ω

(Note 4) Theoretical value by design

● DC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Characteristics						
Supply Current	$I_{CC}1$	A_V = +1, R_L = ∞	—	1.6	2.0	mA
(only NJMOP177)	$I_{CC}2$	Ta = -40 to +85°C, A_V = +1, R_L = ∞	—	1.7	2.5	mA
	$I_{CC}3$	V^+/V^- = ±3V, A_V = +1, R_L = ∞	—	0.70	0.75	mA
	P_D1	A_V = +1, R_L = ∞	—	50	60	mW
	P_D2	V^+/V^- = ±3V, A_V = +1, R_L = ∞	—	4.2	4.5	mW
Supply Current	$I_{CC}1$	A_V = +1, R_L = ∞	—	2.6	3.2	mA
(only NJMOP1772)	$I_{CC}2$	Ta = -40 to +85°C, A_V = +1, R_L = ∞	—	2.7	3.4	mA
	$I_{CC}3$	V^+/V^- = ±3V, A_V = +1, R_L = ∞	—	1.3	1.6	mA
	P_D1	A_V = +1, R_L = ∞	—	78	96	mW
	P_D2	V^+/V^- = ±3V, A_V = +1, R_L = ∞	—	7.8	9.6	mW

● AC CHARACTERISTICS

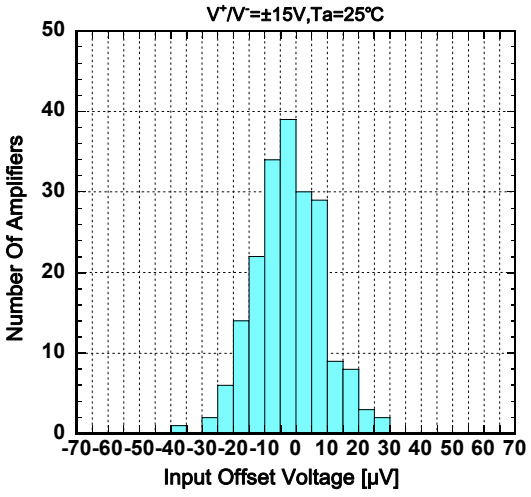
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Frequency Characteristics						
Unity Gain Frequency	f_T	A_V = +100, R_L = 2kΩ, C_L = 10pF	—	1.1	—	MHz
Slew Rate	+SR	RISE, A_V = +1, V_{IN} = 1Vpp, R_L = 2kΩ, C_L = 10pF	0.1	0.3	—	V/μs
	-SR	FALL, A_V = +1, V_{IN} = 1Vpp, R_L = 2kΩ, C_L = 10pF	0.1	0.3	—	V/μs
Noise Characteristics						
Equivalent Input Noise Voltage	V_{NI}	fo = 1Hz to 100Hz	—	80	—	nVrms
Equivalent Input Noise Current	I_{NI}	fo = 1Hz to 100Hz	—	3	—	pArms

●EXPLANATION OF MEASUREMENT CONDITION

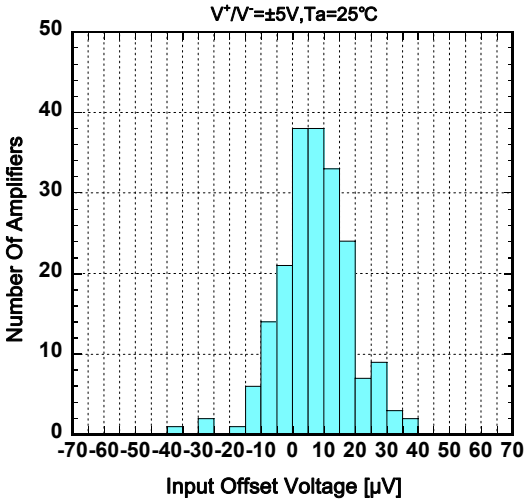
PARAMETER	Explanation
Input Offset Voltage Drift	Input Offset Voltage Drift = $\Delta V_{IO} / \Delta T$ ΔT : Amount of Temperature Change. ΔV_{IO} : Amount of Input Offset Voltage.
Common Mode Input Voltage range	A range of input voltage at which the operational amplifier can function.
Common Mode Rejection Ratio	$CMR = 20\log \lvert (\Delta V_{CM} / \Delta V_{IO}) \rvert$ ΔV_{CM} : Amount of Input Voltage. ΔV_{IO} : Amount of Input Offset Voltage.
Supply Voltage Rejection Ratio	$SVR = 20\log \lvert (\Delta V_S / \Delta V_{IO}) \rvert$ ΔV_S : Amount of Supply Voltage. ΔV_{IO} : Amount of Input Offset Voltage.
Common Mode Input Impedance	$R_{IC} = \Delta V_{CM} / \Delta I_B$ ΔV_{CM} : Amount of Input Voltage. ΔI_B : Amount of Input Bias Current.
Voltage Gain	$AV = 20\log \lvert (\Delta V_O / \Delta V_{IO}) \rvert$ ΔV_O : Amount of Output Voltage. ΔV_{IO} : Amount of Input Offset Voltage.

■TYPICAL CHARACTERISTICS

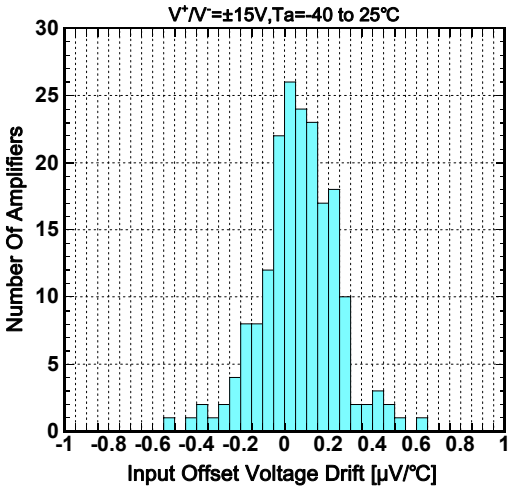
Input Offset Voltage Distribution



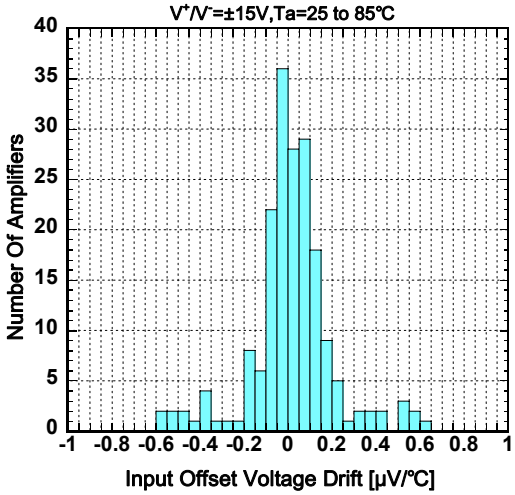
Input Offset Voltage Distribution



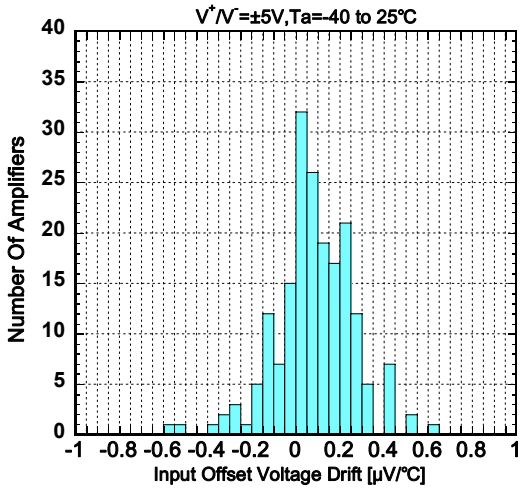
Input Offset Voltage Drift Distribution



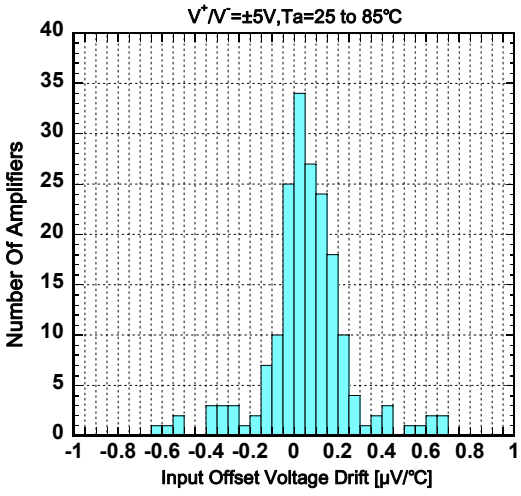
Input Offset Voltage Drift Distribution



Input Offset Voltage Drift Distribution

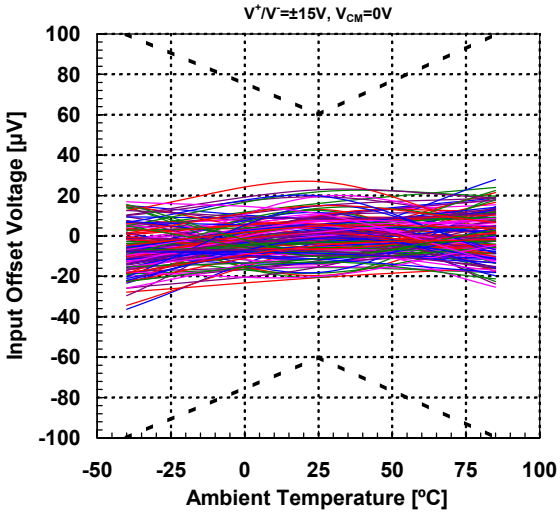


Input Offset Volotage Drift Distribution



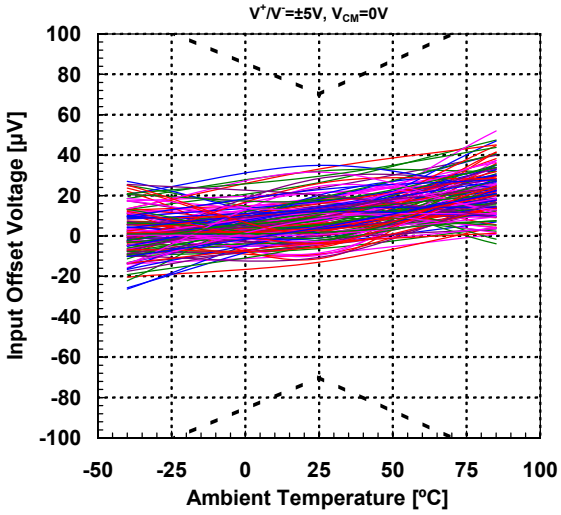
Input Offset Voltage vs. Temperature

V^+/V^-=±15V, V_{CM}=0V



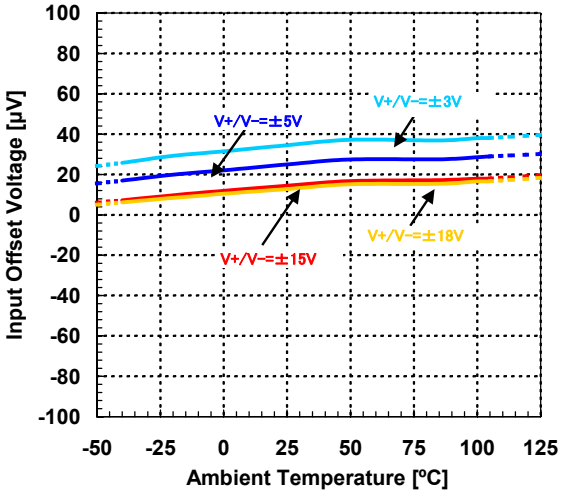
Input Offset Voltage vs. Temperature

V^+/V^-=±5V, V_{CM}=0V



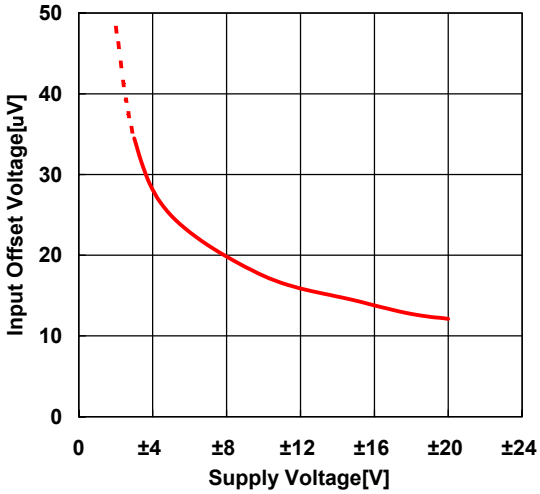
Input Offset Voltage vs. Temperature (Supply Voltage)

V_{ICM}=0V

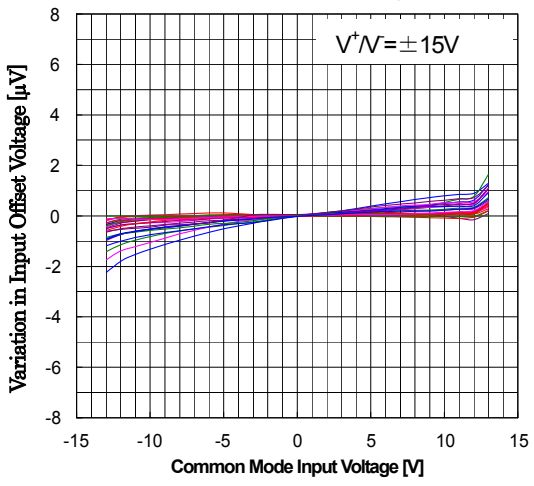


Input Offset Voltage vs. Supply Voltage

V_{CM}=0V



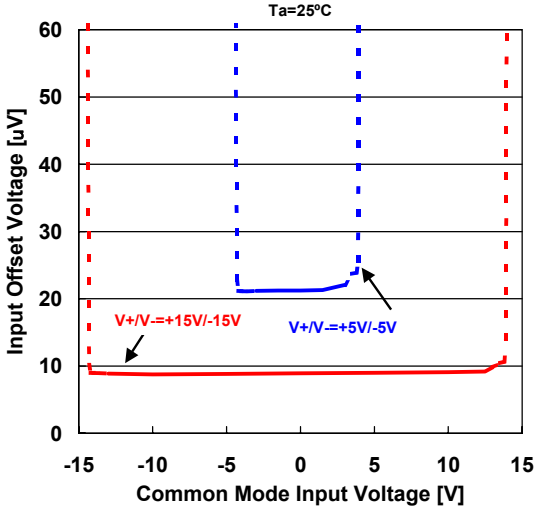
Variation in Input Offset Voltage vs. Common Mode Input Voltage



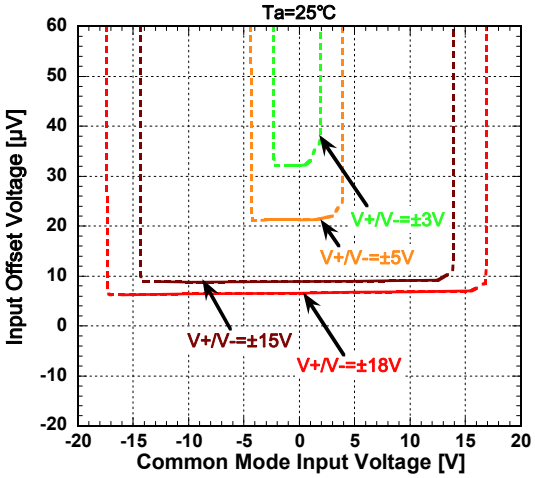
Input Offset Voltage vs. Common Mode Input Voltage

(Supply Voltage)

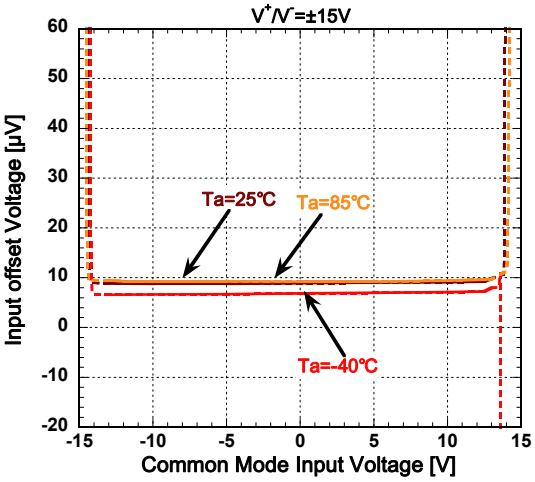
Ta=25ºC



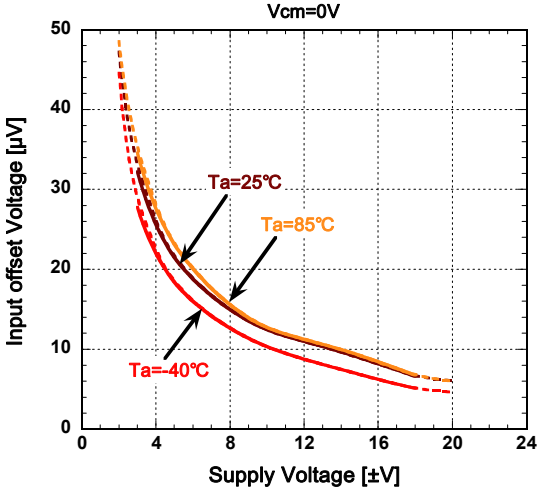
Input Offset Voltage vs. Common Mode Input Voltage
(Supply Voltage)
Ta=25℃



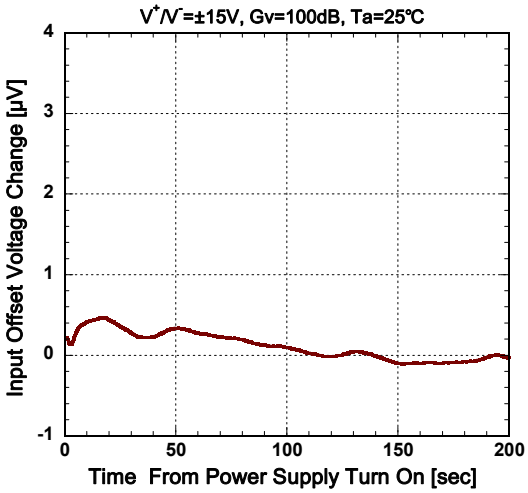
Input Offset Voltage vs. Common Mode Input Voltage
(Temperature)
V+/V-=±15V



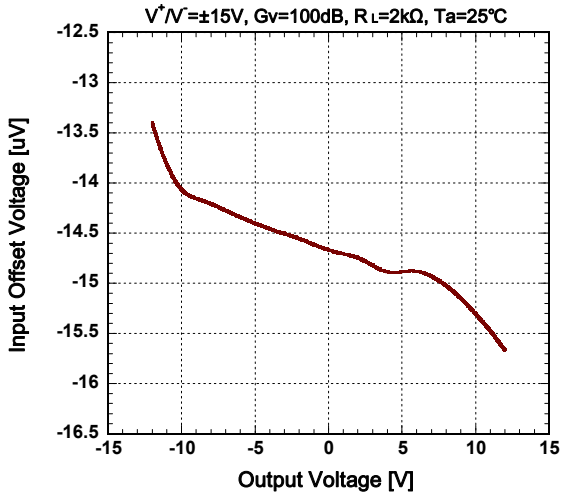
Input Offset Voltage vs. Supply Voltage
(Temperature)
Vcm=0V



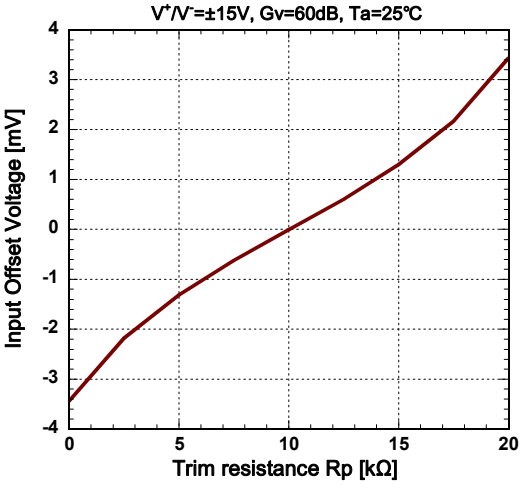
Warm Up Input Offset Voltage Drift
V+/V-=±15V, Gv=100dB, Ta=25℃

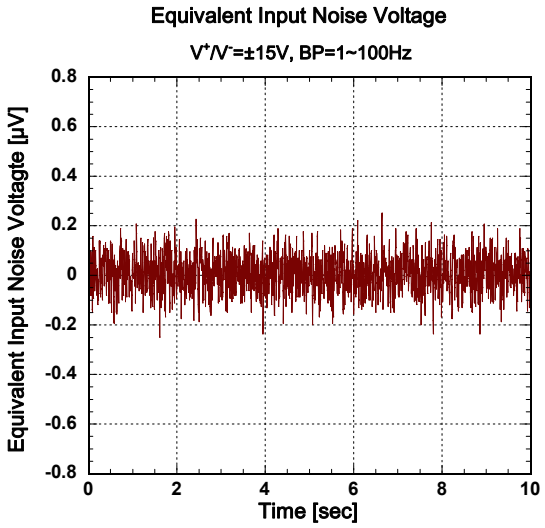


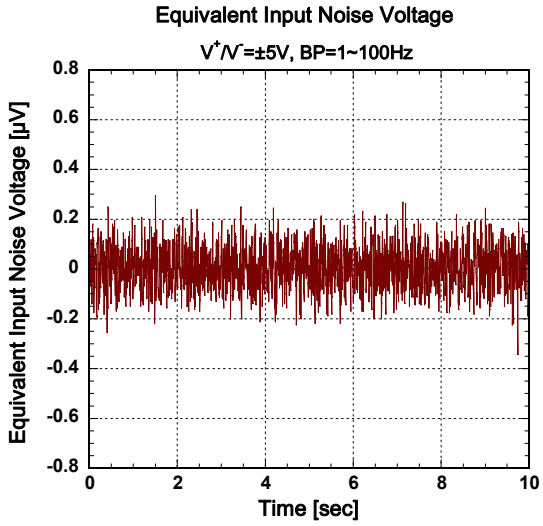
Input Offset Voltage vs. Output Voltage
V+/V-=±15V, Gv=100dB, RL=2kΩ, Ta=25℃

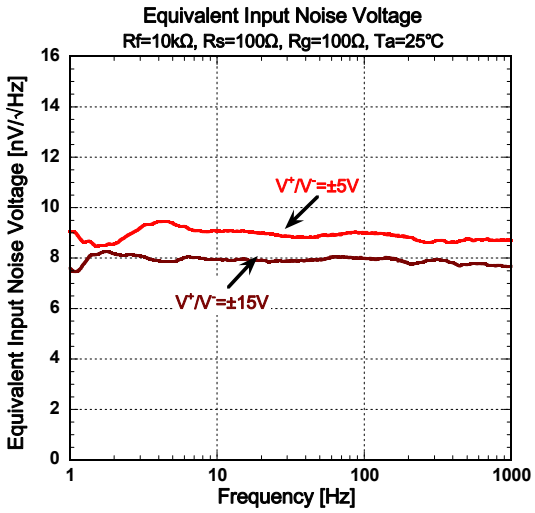


Input Offset Voltage vs. Trim Resistance
V+/V-=±15V, Gv=60dB, Ta=25℃

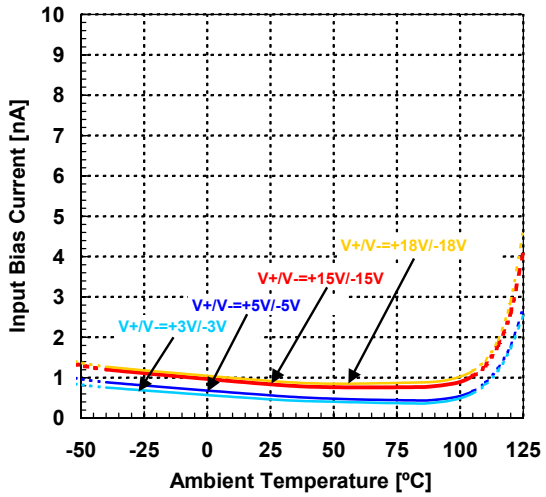



Equivalent Input Noise Voltage
V+/V-=±15V, BP=1~100Hz
Equivalent Input Noise Voltagte [μV]
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
0
2
4
6
8
10
Time [sec]

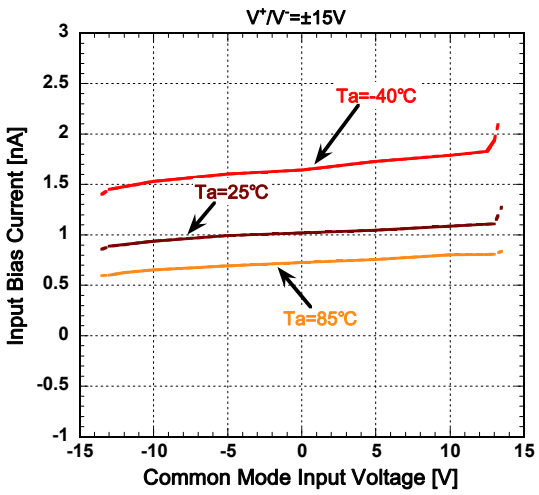

Equivalent Input Noise Voltage
V+/V-=±5V, BP=1~100Hz
Equivalent Input Noise Voltage [μV]
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
0
2
4
6
8
10
Time [sec]


Equivalent Input Noise Voltage
Rf=10kΩ, Rs=100Ω, Rg=100Ω, Ta=25℃
Equivalent Input Noise Voltage [nV/√Hz]
16
14
12
10
8
6
4
2
0
V+/V-=±5V
V+/V-=±15V
1
10
100
1000
Frequency [Hz]

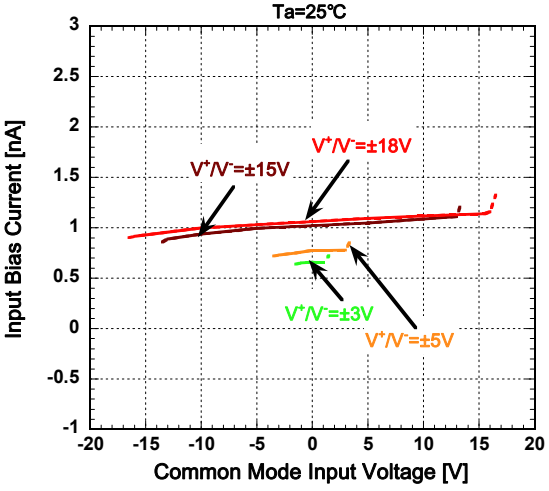
Input Bias Current vs. Temperature



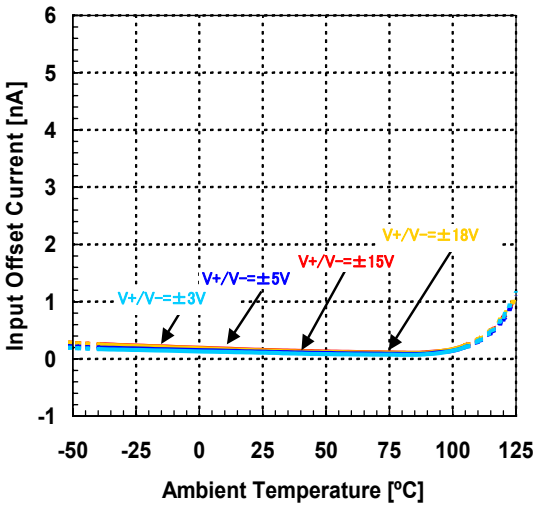
Input Bias Current vs. Common Mode Input Voltage
(Temperature)



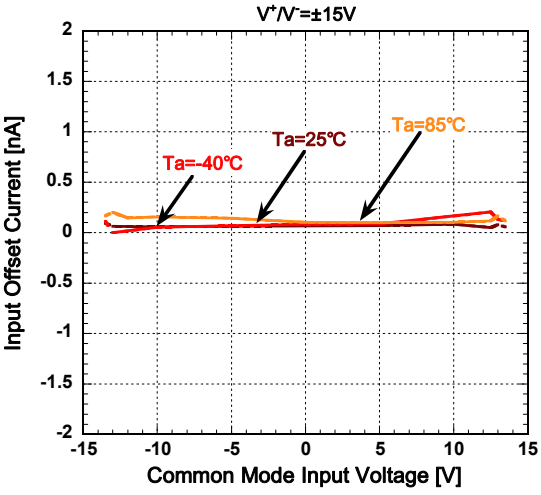
Input Bias Current vs. Common Mode Input Voltage
(Supply Voltage)
Ta=25°C



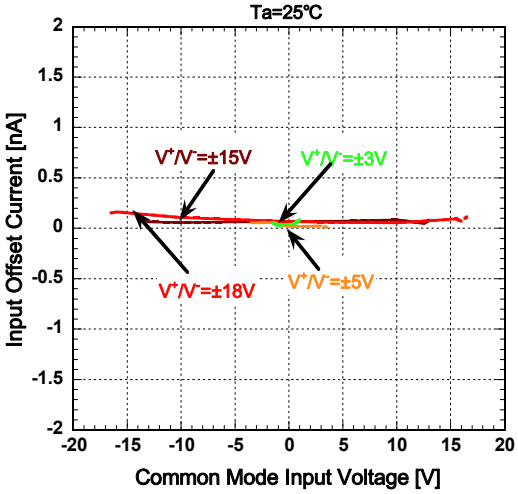
Input Offset Current vs. Temperature

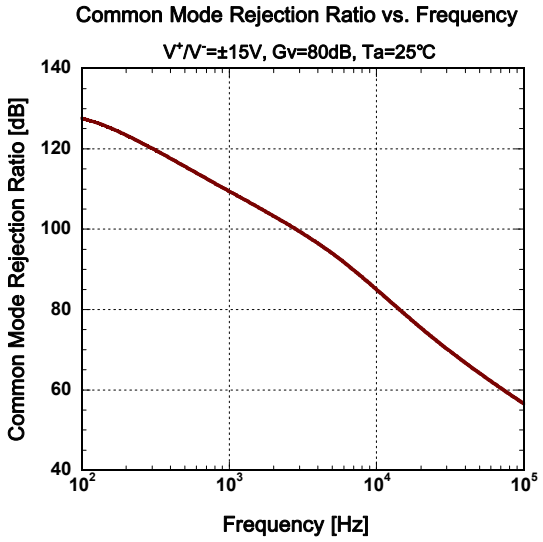


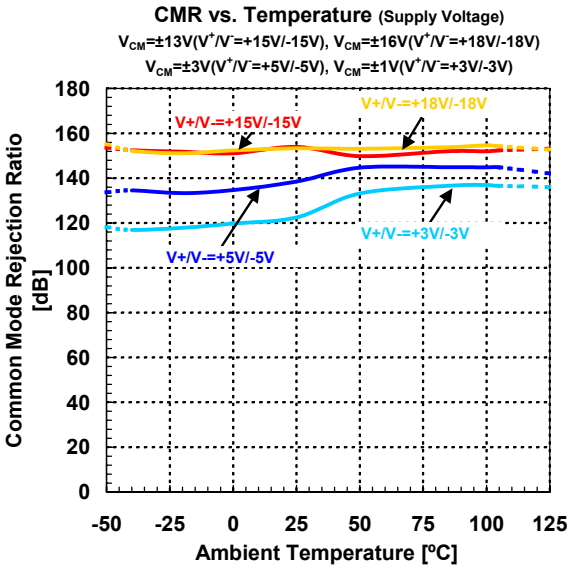
Input Offset Current vs. Common Mode Input Voltage
(Temperature)
V+/V-=±15V

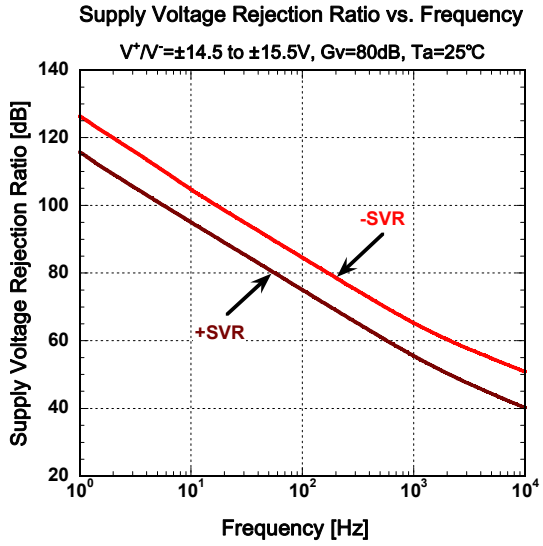


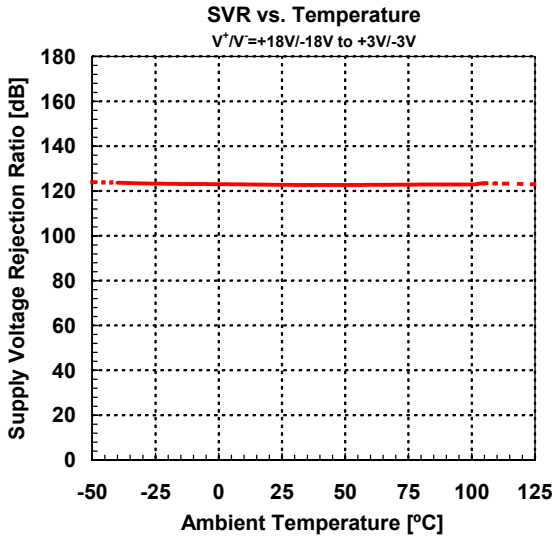
Input Offset Current vs. Common Mode Input Voltage
(Supply Voltage)
Ta=25°C



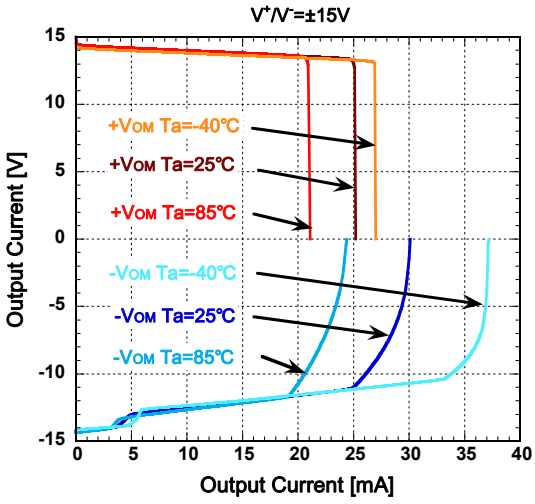

Common Mode Rejection Ratio vs. Frequency
V+/V-=±15V, Gv=80dB, Ta=25℃
Common Mode Rejection Ratio [dB]
140
120
100
80
60
40
10^2
10^3
10^4
10^5
Frequency [Hz]


CMR vs. Temperature (Supply Voltage)
VCM=±13V(V+/V-=+15V/-15V), VCM=±16V(V+/V-=+18V/-18V)
VCM=±3V(V+/V-=+5V/-5V), VCM=±1V(V+/V-=+3V/-3V)
Common Mode Rejection Ratio [dB]
180
160
140
120
100
80
60
40
20
0
V+/V-=+18V/-18V
V+/V-=+15V/-15V
V+/V-=+3V/-3V
V+/V-=+5V/-5V
-50
-25
0
25
50
75
100
125
Ambient Temperature [ºC]

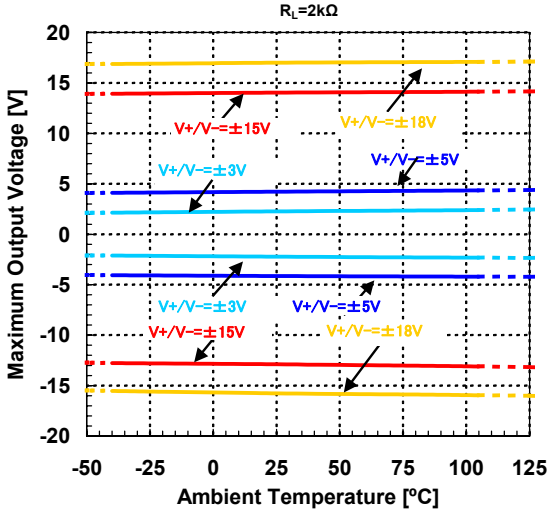

Supply Voltage Rejection Ratio vs. Frequency
V+/V-=±14.5 to ±15.5V, Gv=80dB, Ta=25℃
Supply Voltage Rejection Ratio [dB]
140
120
100
80
60
40
20
-SVR
+SVR
10^0
10^1
10^2
10^3
10^4
Frequency [Hz]


SVR vs. Temperature
V+/V-=+18V/-18V to +3V/-3V
Supply Voltage Rejection Ratio [dB]
180
160
140
120
100
80
60
40
20
0
-50
-25
0
25
50
75
100
125
Ambient Temperature [ºC]

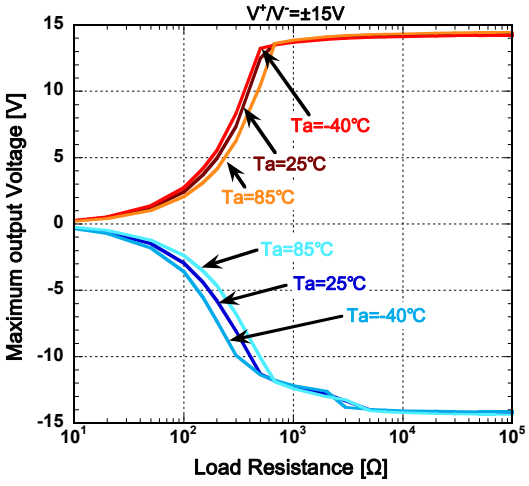
Output Voltage vs. Output Current



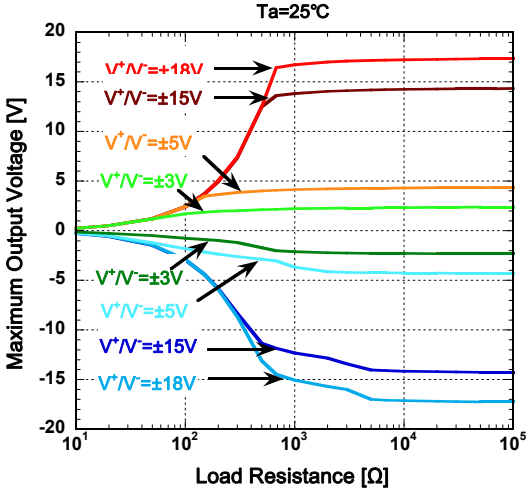
Maximum Output Voltage vs. Temperature



Maximum Output Voltage vs. Load Resistance
(Temperature)

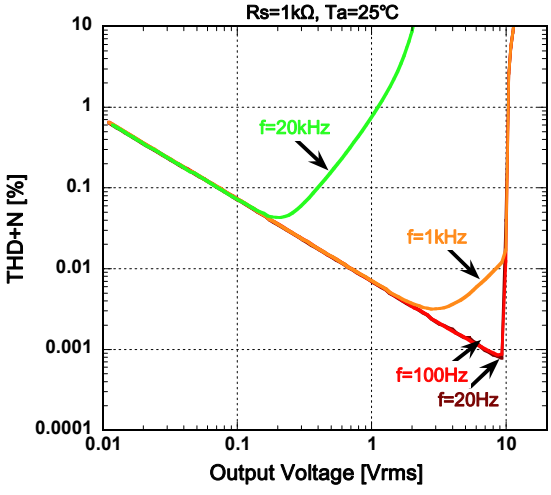


Maximum Output Voltage vs. Load Resistance
(Supply Voltage)
Ta=25℃



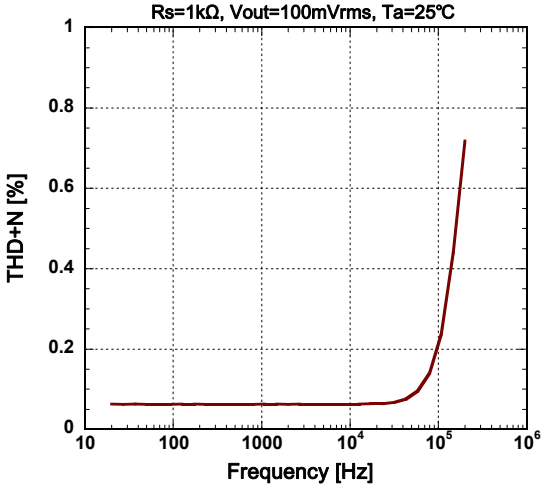
THD+N vs. Output Voltage

V+/V-=±15V, Gv=20dB, RF=10kΩ,
Rs=1kΩ, Ta=25℃

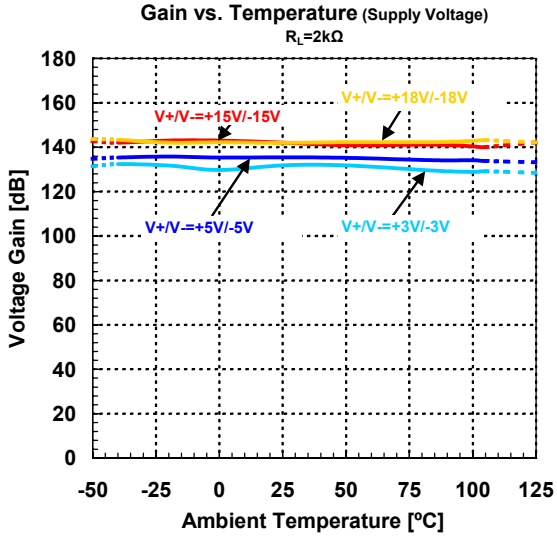


THD+N vs. Frequency

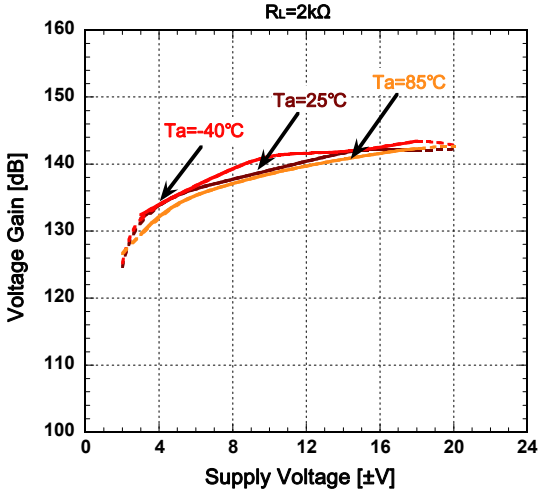
V+/V-=±15V, Gv=20dB, RF=10kΩ,
Rs=1kΩ, Vout=100mVrms, Ta=25℃



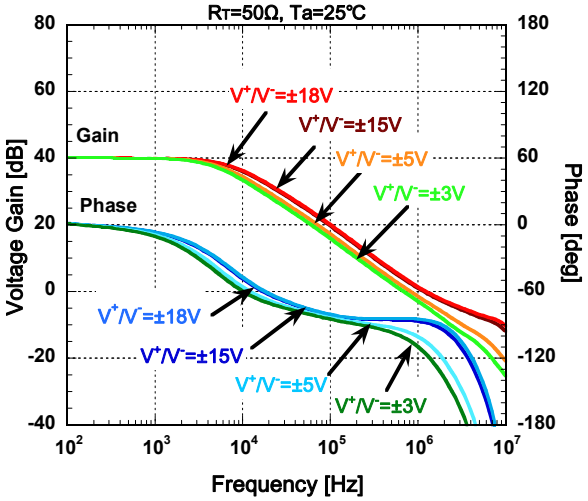
Gain vs. Temperature (Supply Voltage)



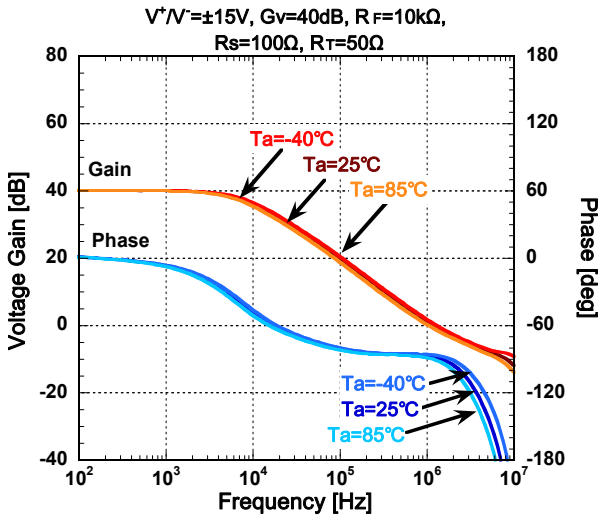
Voltage Gain vs. Supply Voltage (Temperature)



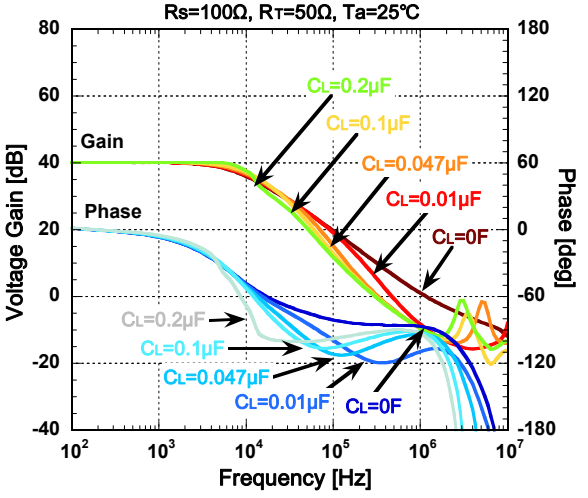
40dB Gain/Phase vs. Frequency (Supply Voltage)



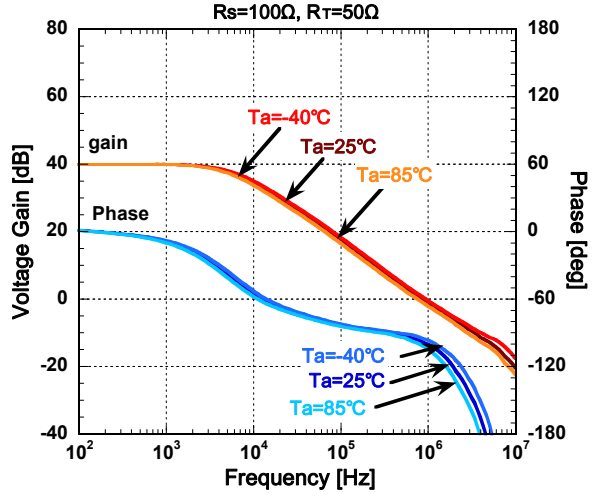
40dB Gain/Phase vs. Frequency (Temperature)



40dB Gain/Phase vs. Frequency (Load Capacitance)

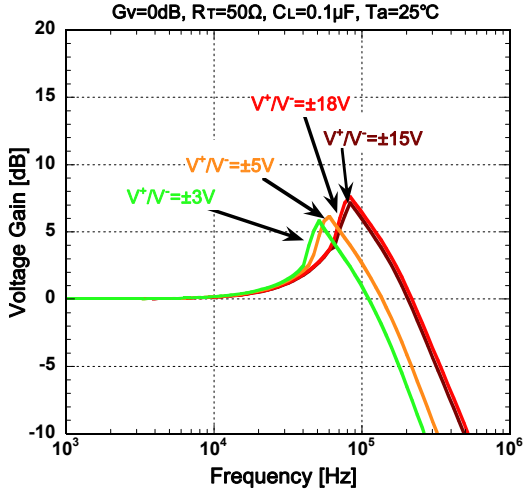


40dB Gain/Phase vs. Frequency (Temperature)



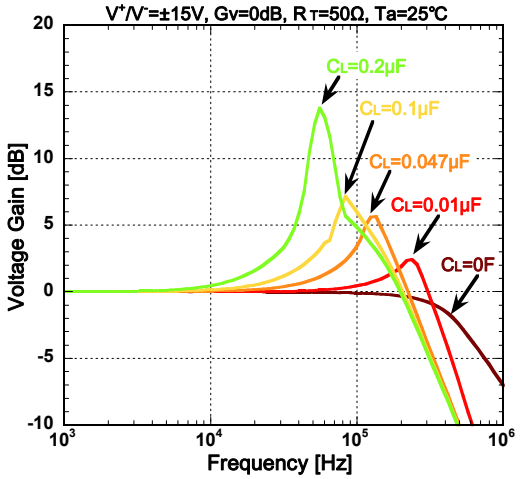
V.F. Peak (Supply Voltage)

Gv=0dB, RT=50Ω, CL=0.1μF, Ta=25℃



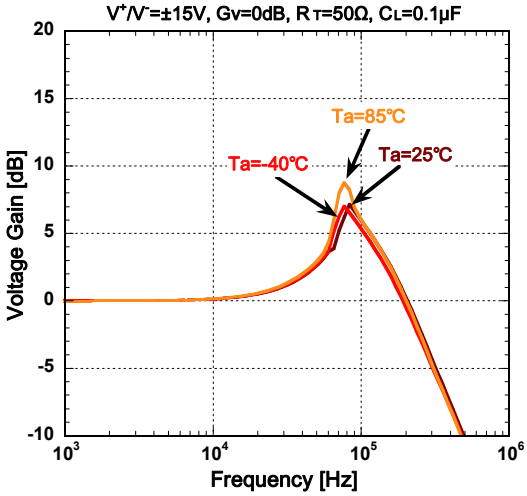
V.F.Peak (Load Capacitance)

V+/V-=±15V, Gv=0dB, RT=50Ω, Ta=25℃



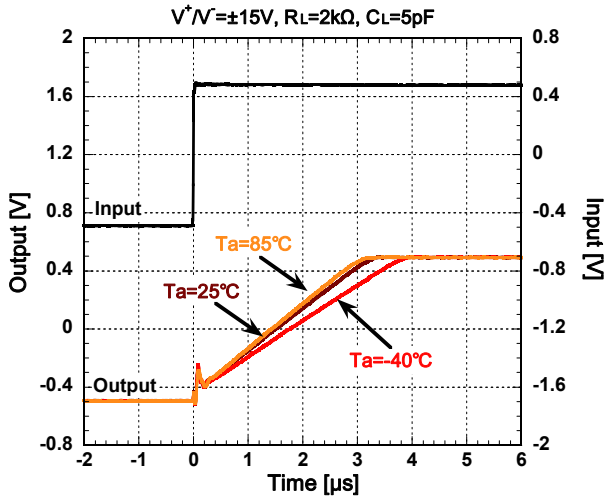
V.F.Peak (Temperature)

V+/V-=±15V, Gv=0dB, RT=50Ω, CL=0.1μF



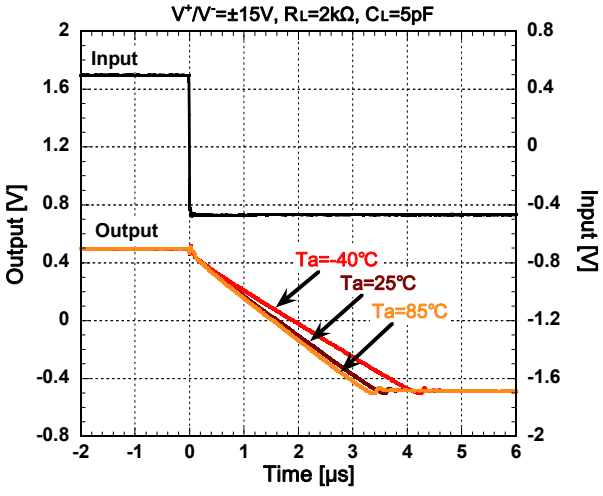
Pulse Response (Temperature)

V+/V-=±15V, RL=2kΩ, CL=5pF



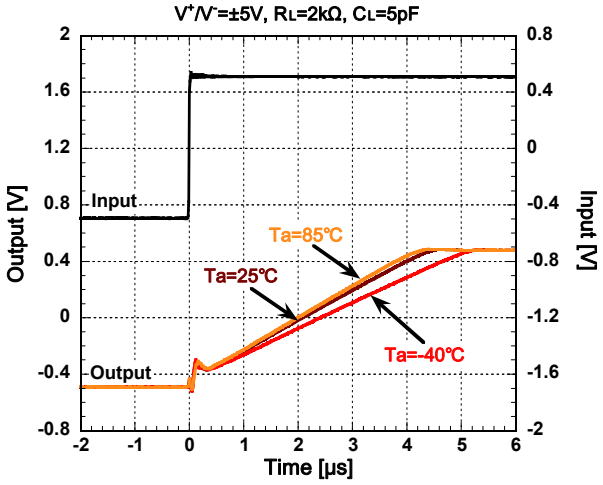
Pulse Response (Temperature)

V+/V-=±15V, RL=2kΩ, CL=5pF



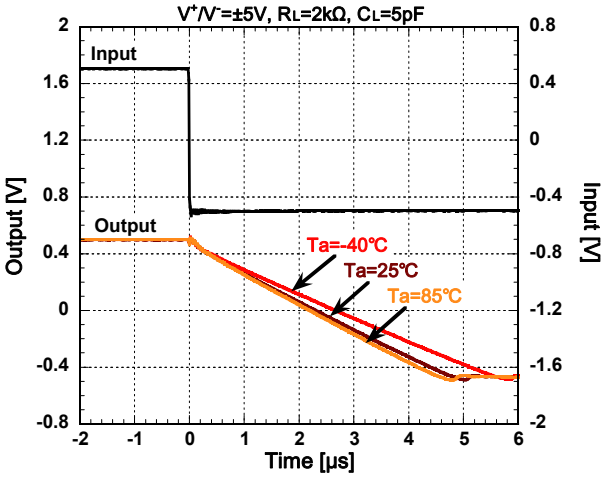
Pulse Response (Temperature)

V^+/V^-=±5V, R_L=2kΩ, C_L=5pF

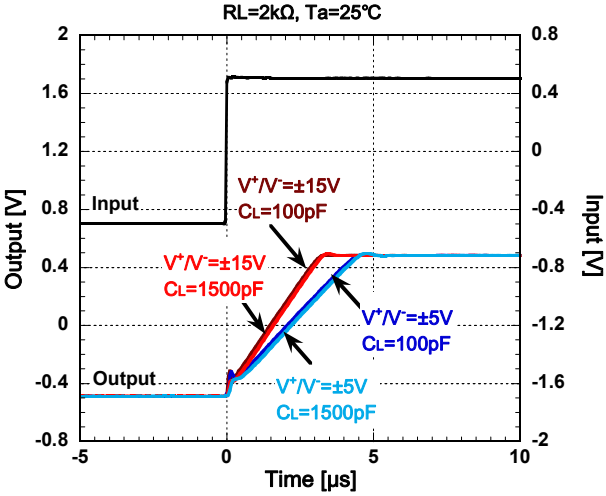


Pulse Response (Temperature)

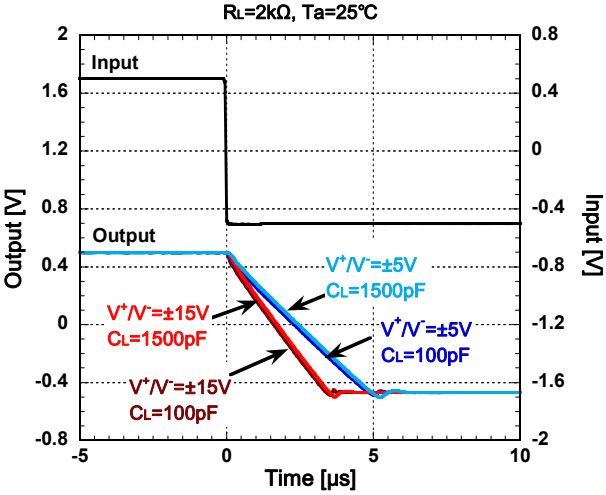
V^+/V^-=±5V, R_L=2kΩ, C_L=5pF



Pulse Response
(Supply Voltage, Load Capacitance)
R_L=2kΩ, Ta=25℃

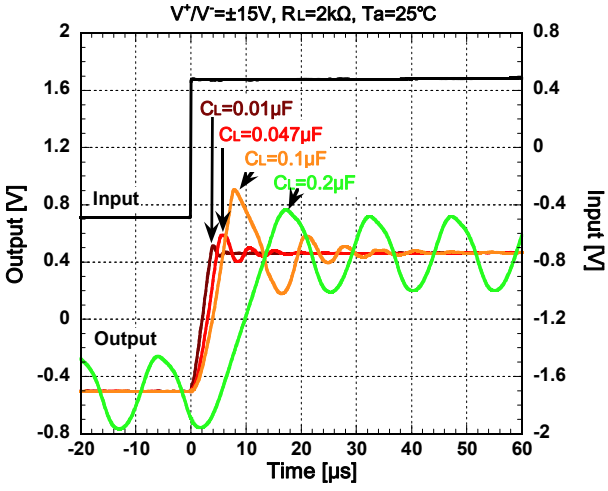


Pulse Response
(Supply Voltage, Load Capacitance)
R_L=2kΩ, Ta=25℃



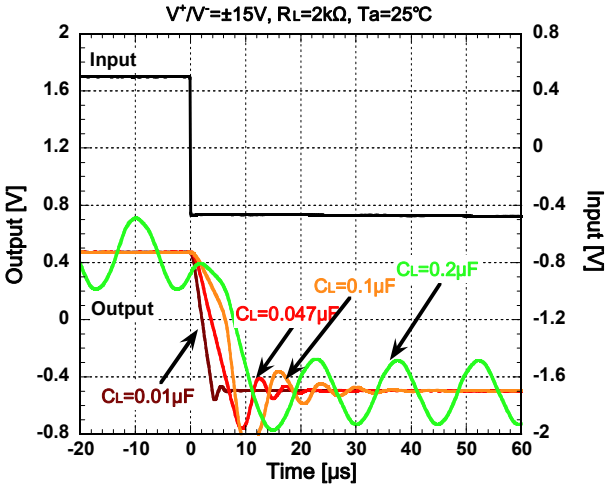
Pulse Response (Load Capacitance)

V^+/V^-=±15V, R_L=2kΩ, Ta=25℃



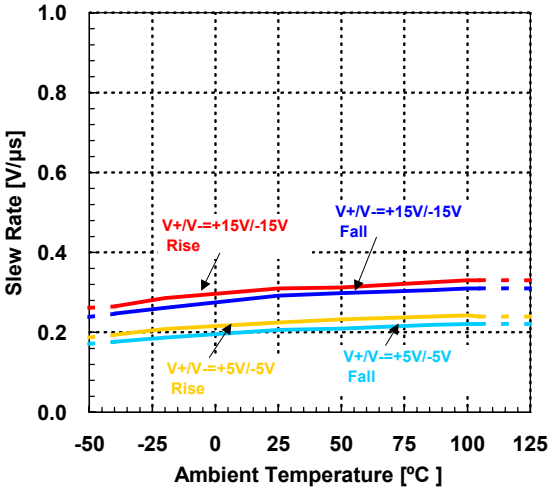
Pulse Response (Load Capacitance)

V^+/V^-=±15V, R_L=2kΩ, Ta=25℃



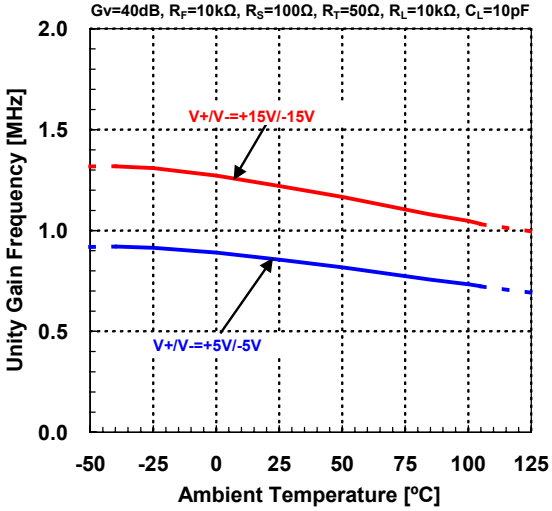
Slew Rate vs. Temperature

R_L=2kΩ



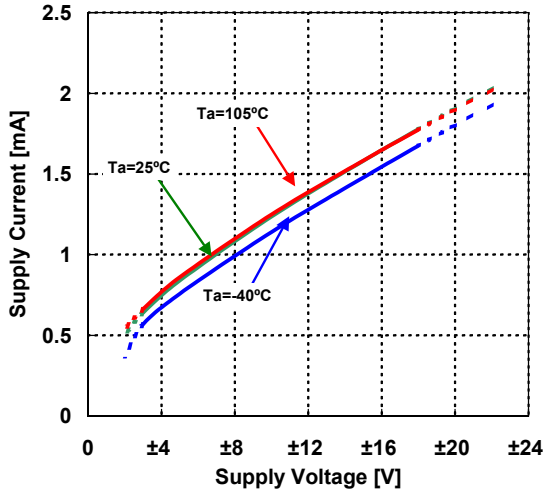
Unity Gain Frequency vs. Temperature

Gv=40dB, R_F=10kΩ, R_S=100Ω, R_T=50Ω, R_L=10kΩ, C_L=10pF



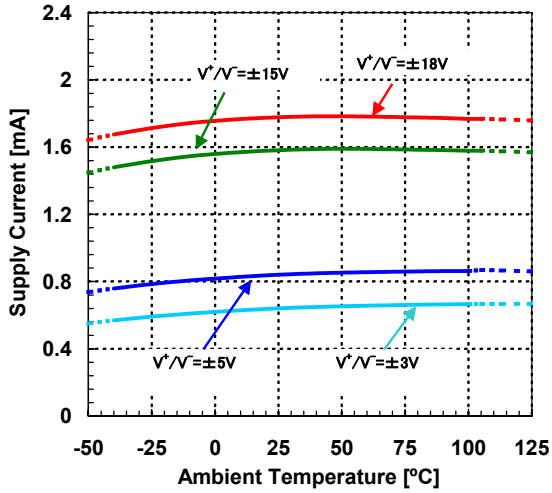
Supply Current vs. Supply Voltage (NJMOP177)

R_L=OPEN



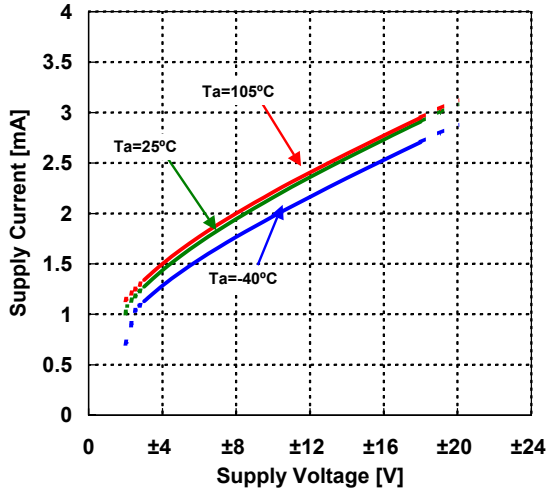
Supply Current vs. Temperature (NJMOP177)

R_L=OPEN



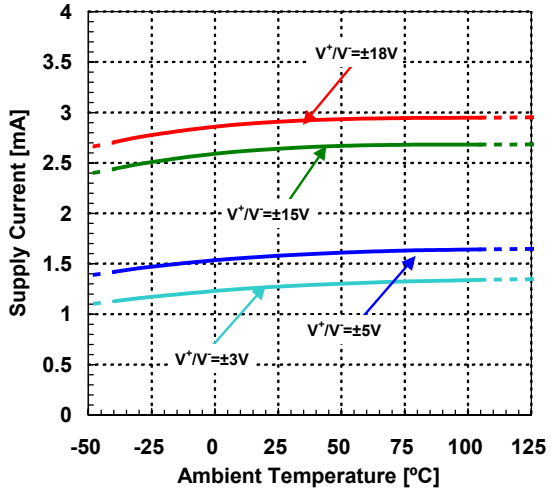
Supply Current vs. Supply Voltage (NJMOP1772)

R_L=OPEN



Supply Current vs. Temperature(NJMOP1772)

R_L=OPEN



■Application Information

●Power Supply Bypassing

The NJMOP177/NJMOP1772 are high precision operational amplifiers featuring low offset voltage, high voltage gain, high CMR, high SVR and so on. To maximize such a high performance with stable operation, theNJMOP177/NJMOP1772 should be operated by clean and low impedance supply voltage. So, the bypass capacitor should be connected to the NJMOP177/NJMOP1772's both power supply terminals (V+ and V-) as shown in Fig.1. The bypass capacitors should be placed as close as possible to IC package.

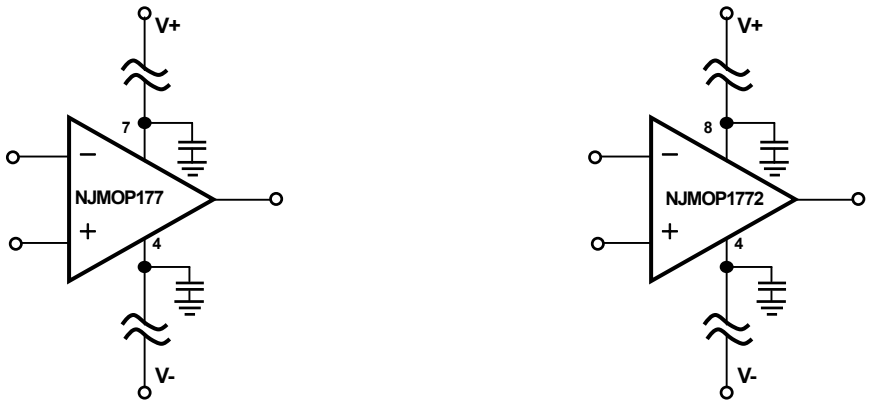


Fig.1 Power Supply Bypassing Circuit

●Thermoelectric Effect

The NJMOP177/NJMOP1772 are high precision operational amplifiers featuring low offset voltage and low offset voltage thermal drift.

To achieve such a high performance, take care about thermoelectric effect possibly occurs on each input terminal of the NJMOP177/NJMOP1772. Generally, if there are thermal mismatches at the junction of different types of metals, the thermoelectric voltage (Seebeck effect) occurs at the junction. The thermoelectric voltages possibly occur at the junction of PCB metal patterns and NJMOP177/NJMOP1772's each input terminal metal. If there is thermal mismatch in-between NJMOP177/NJMOP1772's each input terminal metal, the thermoelectric voltages generated on each input terminal possibly have different voltage each. This voltage difference causes offset voltage and offset voltage thermal drift of the NJMOP177 /NJMOP1772.

To minimize this voltage difference, the thermal mismatch in-between NJMOP177/NJMOP1772's each input terminal and PCB metal should be minimized.

●Offset Voltage Adjustment (only NJMOP177)

The NJMOP177 has offset voltage trim terminals (pin1 and pin8) as shown in below Fig.2. By connecting external potentiometer in the range of 20Kohm, the offset voltage trim range is ±3mV. This offset voltage trim is effective only for offset voltage at room temperature, not for offset voltage thermal drift.

If offset voltage adjustment is not in use, leave pin1 and pin8 open (un-connected).

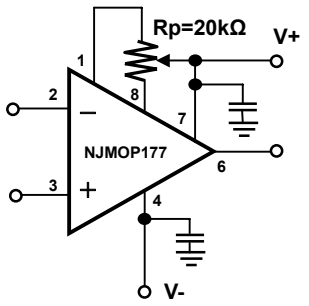


Fig.2 Offset Voltage Trim Circuit

●Differential Amplifier

Differential amplifier (see below Fig.3) is used in high accuracy circuit to improve common mode rejection ratio (CMR). A matching between the ratio R1/R2 = R3/R4 and R1=R3 makes the high CMR.

For example, acceptable error range to obtain CMR of 130dB or more is about 0.1ppm.

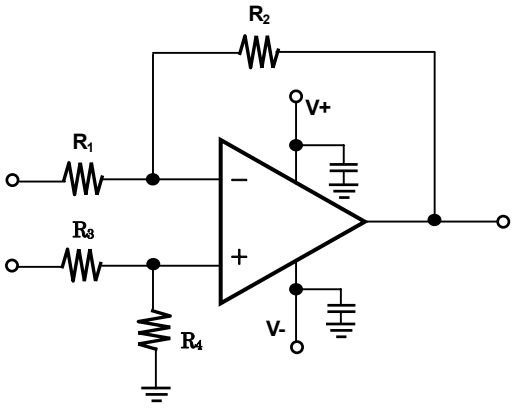
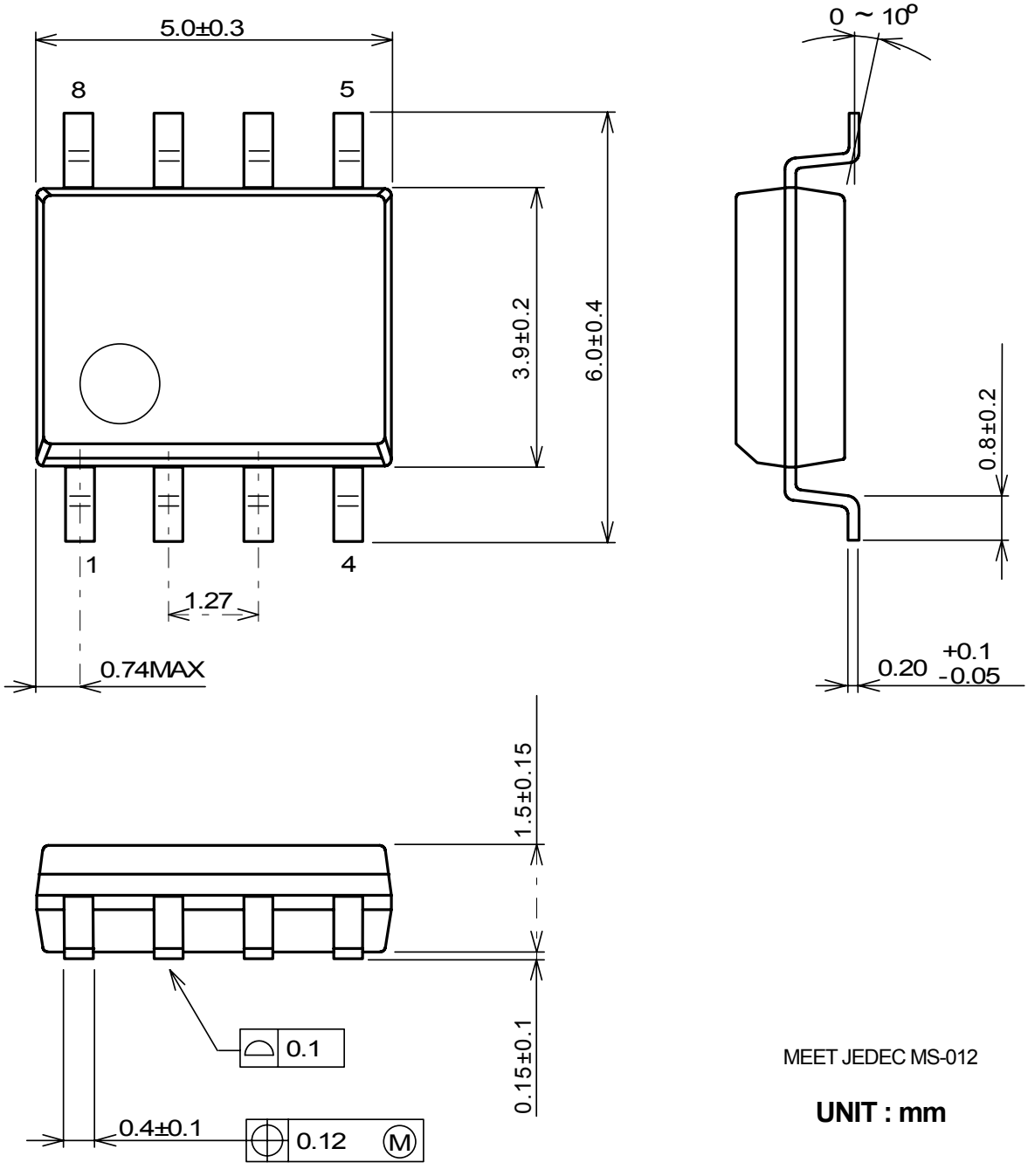


Fig.3 Differential Amplifier

■ **PACKAGE DIMENSIONS**

SOP8 JEDEC 150 mil



MEET JEDEC MS-012

UNIT : mm

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