MP2932

6-Phase PWM Controller with 8-Bit DAC Code for VR10 and VR11

The Future of Analog IC Technology

DESCRIPTION

The MP2932 is a 6-phase, synchronous buck switching regulator controller for regulating microprocessor core voltage. MP2932 also uses dual edge PWM mode to realize fast load transient with fewer capacitors.

For meeting the requirement of microprocessor output voltage drops tightly as load current increases, output current is sensed to realize voltage droop function. Accurate current balancing is included in MP2932 to provide current balance for each channel.

8-bit ID input with selectable VR11 code and extended VR10 code can set output voltage dynamically.

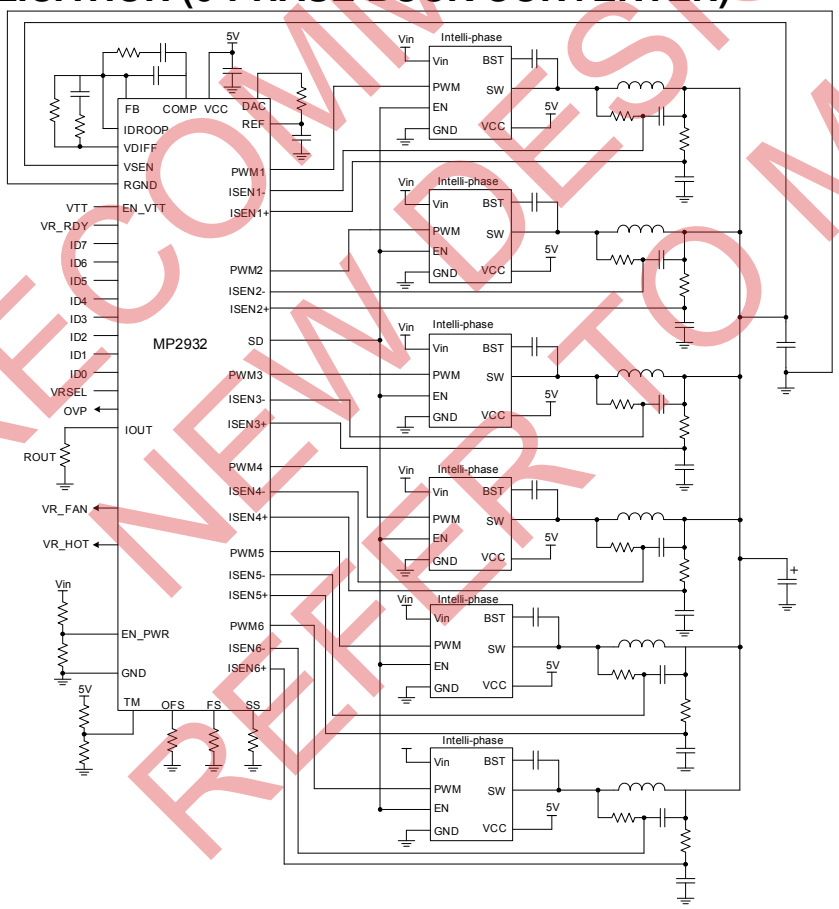
FEATURES

- 2-, 3-, 4-, 5- or 6-phase Operation
- Channel-Current Balancing
- Voltage Droop vs. Load Current
- Precision Resistor or DCR Current Sensing
- Adjustable Switching Frequency
- Over Current Protection
- Available in a 48-pin QFN6x6 Package

APPLICATIONS

- Power Modules
- Desktop, Server, Core Voltage
- POLs (Memory)

TYPICAL APPLICATION (6-PHASE BUCK CONVERTER)

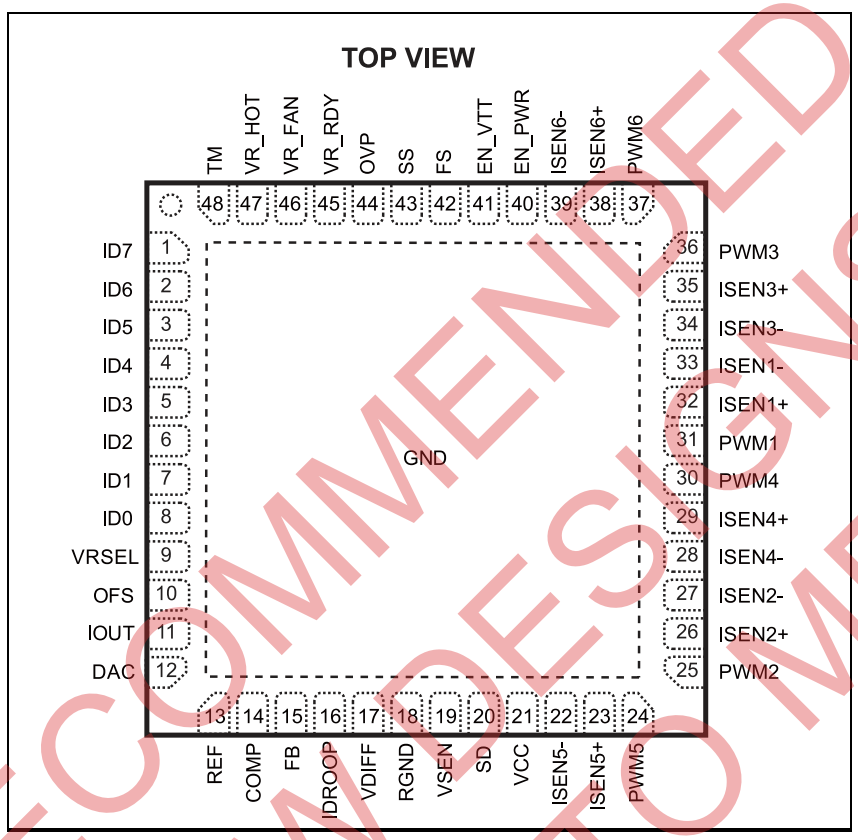


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP2932GQK	QFN (6 x 6mm)	MP2932	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP2932GQK–Z);
For RoHS compliant packaging, add suffix –LF; (e.g. MP2932GQK –LF–Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage VCC 6V
All Other Pins ..... -0.3V to VCC + 0.3V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 3.9W
Junction Temperature ..... 150°C
Storage Temperature ..... –65°C to +150°C
ESD Rating
Human Body Model 2kV
Machine Model 200V
Charged Device Model 1.5kV

Recommended Operating Conditions (3)

Supply Voltage VCC ..... +5V ±5%
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
QFN48 (6mm x 6mm)	32	3.5 .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J\ (MAX)}$, the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\ (MAX)} = (T_{J\ (MAX)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

Operating conditions: V_{CC} = 5V, unless otherwise noted.

Parameter	Test conditions	Min	Typ	Max	Units
V_{CC} Supply Current					
Nominal Supply	V_{CC}=5VDC; EN_PWR=5VDC; R_T=100kΩ, I_{SEN1}=I_{SEN2}=I_{SEN3}=I_{SEN4}= I_{SEN5}= I_{SEN6}=-70μA		18	26	mA
Shutdown Supply	V_{CC}=5VDC; EN_PWR=0VDC; R_T=100kΩ		14	21	mA
Power-on Reset and Enable					
POR Threshold	V_{CC} Rising	4.3	4.5	4.7	V
	V_{CC} Falling	3.7	3.9	4.2	V
EN_PWR Threshold	Rising	0.850	0.88	0.910	V
	Hysteresis		130		mV
	Falling	0.71	0.745	0.78	V
EN_VTT Threshold	Rising	0.850	0.88	0.910	V
	Hysteresis		130		mV
	Falling	0.71	0.745	0.78	V
Reference Voltage and DAC					
System Accuracy of MP2932 (ID =1V to 1.6V, TJ=0°C to +70°C)		-0.5		0.5	%ID
System Accuracy of MP2932 (ID =0.5V to 1V, T_J=0°C to +70°C)		-0.9		0.9	%ID
ID Pull-Up		-60	-40	-20	μA
ID Input Low Level				0.4	V
ID Input High Level		0.8			V
VRSEL Input Low Level				0.4	V
VRSEL High Low Level		0.8			V
DAC Source Current			4	7	mA
DAC Sink Current				320	μA
Pin-adjustable Offset					
Voltage at OFS Pin	Offset resistor connected to ground	380	400	420	mV
	Voltage below V_{CC}, offset resistor connected to V_{CC}	1.55	1.600	1.65	V
Oscillators					
Accuracy of Switching Frequency setting	R_T=100kΩ	225	250	275	kHz
Adjustment Range of Switching Frequency		0.08		1.0	MHz
Soft-Start Ramp Rate	R_S=150kΩ		1.563		mV/μs
Adjustment Range of Soft-Start Ramp Rage		0.625		6.25	mV/μs

ELECTRICAL CHARACTERISTICS *(continued)*

Operating conditions: V_{CC} = 5V, unless otherwise noted.

Parameter	Test conditions	Min	Typ	Max	Units
Error Amplifier					
Maximum Output Voltage		3.8	4.2	4.6	V
Output High Voltage @ 2mA		3.6			V
Output Low Voltage @ 2mA				1.8	V
Remote-sense Amplifier					
Bandwidth			20		MHz
Output High Current	VSEN-RGND=2.5V	-100		100	µA
Output High Current	VSEN-RGND=0.6	-100		100	µA
PWM Output					
PWM Output Voltage Low Threshold	ILOAD=±500µA			0.5	V
PWM Output Voltage High Threshold	ILOAD=±500µA	4.3			V
Current Sense and Over-current Protection					
Sensed Current Tolerance(IDROOP)	ISEN1=ISEN2=ISEN3=ISEN4= ISEN5=ISEN6=50µA	47	50	53	µA
Overcurrent Trip level for Average Current		72	85	98	µA
Peak Current Limit for Individual Channel			120		µA
Maximum Voltage at IDROOP and IOUT Pins		1.98	2.01	2.04	V
Thermal Monitoring and Fan Control					
TM Input Voltage for VR_FAN TRIP		1.55	1.65	1.75	V
TM Input Voltage for VR_FAN Reset		1.85	1.95	2.05	V
TM Input Voltage for VR_HOT Trip		1.3	1.4	1.5	V
TM Input Voltage for VR_HOT Reset		1.55	1.65	1.75	V
Leakage current of VR_FAN	With externally pull-up resistor connected to VCC			30	µA
VR_RAN Low Voltage	IVR_FAN=4mA			0.4	V
Leakage Current of VR_HOT	With externally pull-up resistor connected to VCC			30	µA
VR_HOT Low Voltage	IVR_HOT=4mA			0.4	V
VR Ready and Protection Monitors					
Leakage Current of VR_RDY	With externally pull-up resistor connected to VCC			30	µA
VR_RDY Low Voltage	IVR_RDY=4mA			0.4	V
Undervoltage Threshold	VDIFF Falling	48	50	52	%ID
VR_RDY Reset Voltage	VDIFF Rising	58	60	62	%ID
Overvoltage Protection Threshold	Before Valid ID	1.250	1.275	1.300	V
	After valid ID, the voltage above ID	150	175	200	Mv
Overvoltage Protection Reset Hysteresis			100		mV

PIN FUNCTIONS

Pin #	Name	Description
1	ID7	ID inputs from microprocessor. These codes determine output regulation voltage.
2	ID6	
3	ID5	
4	ID4	
5	ID3	
6	ID2	
7	ID1	
8	ID0	
9	VRSEL	Select internal ID code. When it is tied to GND, the extended VR10 is selected. When it's floated or tied to high, VR11 code is selected.
10	OFS	Offset between REF and DAC program pin. The OFS pin can be used to program a DC offset current which will generate a DC offset voltage between the REF and DAC pins. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unconnected.
11	IOUT	A resistor needs to be placed between IOUT and GND to ensure the proper operation. The voltage at IOUT pin will be proportional to the load current.
12	DAC	Internal DAC reference output determined by ID codes
13	REF	Error amplifier input. A capacitor 0.1uF is used between REF and GND to smooth the voltage transition during Dynamic ID operations.
14	COMP	Error amplifier output pin. Tie to compensation network
15	FB	Output voltage feedback pin.
16	IDROOP	Current proportional to load current is flowed out through this pin
17	VDIFF	Remote sense amplifier output. VDIFF-GND=VSEN-RGND
18	RGND	Remote sense amplifier input. Remote output GND
19	VSEN	Remote sense amplifier input. Remote output.
20	SD	Shutdown Intelli-phase @ Hiz state. MP2932 cooperates with MPS Intelli-phase and SD pin is connected to the EN of Intelli-phase.
21	VCC	Power supply. Connect this pin directly to a +5V supply.
22	ISEN5-	Phase 5 current sense amplifier differential inputs.
23	ISEN5+	
24	PWM5	Phase 5 PWM output.
25	PWM2	Phase 2 PWM output.
26	ISEN2+	Phase 2 current sense amplifier differential input.
27	ISEN2-	
28	ISEN4-	Phase 4 current sense amplifier differential input.
29	ISEN4+	
30	PWM4	Phase 4 PWM output.
31	PWM1	Phase 1 PWM output.
32	ISEN1+	Phase 1 current sense amplifier differential input.
33	ISEN1-	

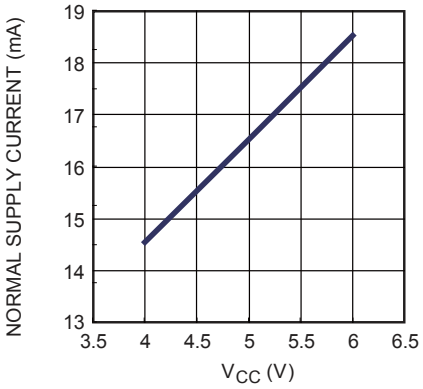
PIN FUNCTIONS *(continued)*

Pin #	Name	Description
34	ISEN3-	Phase 3 current sense amplifier differential input.
35	ISEN3+	
36	PWM3	Phase 3 PWM output.
37	PWM6	Phase 6 PWM output.
38	ISEN6+	Phase 6 current sense amplifier differential input
39	ISEN6-	
40	EN_PWR	Enable pin. It is used to synchronize power-up of the controller and MOSFET driver ICs.
41	EN_VTT	Enable pin. It is controlled by output of VTT voltage regulator in the mother board.
42	FS	PWM frequency set pin. A resistor from FS to GND will set the switching frequency.
43	SS	Soft start oscillator frequency set pin. A resistor from SS to GND will set up the soft-start ramp rate.
44	OVP	Overvoltage protection output indication pin. It can be pulled to VCC and is latched when an overvoltage condition is detected.
45	VR_RDY	Open drain logic output. When soft start completed and output voltage is regulated in the value determined by ID setting, VR_RDY is logic high.
46	VR_FAN	Open drain logic output. It is open when VR temperature reaches certain value
47	VR_HOT	Open drain logic output. It is open when VR temperature reaches certain value
48	TM	NTC resistor in this pin is used to monitor inductor temperature. Connect this pin through an NTC thermistor to GND and a resistor to VCC of the controller. The voltage at this pin is reverse proportional to the VR temperature.

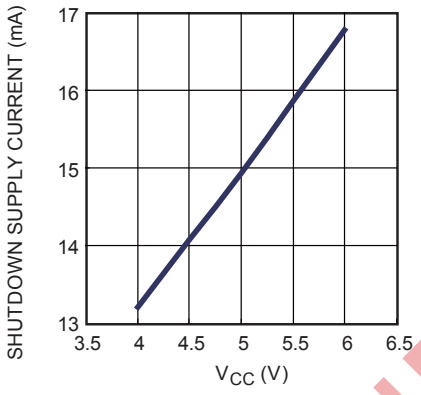
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{ID}=1.2V, L=0.3µH, F_{SW}=600kHz, 6-Phase Operation, T_A = +25ºC, unless otherwise noted.

Normal Supply Current vs. V_{CC}

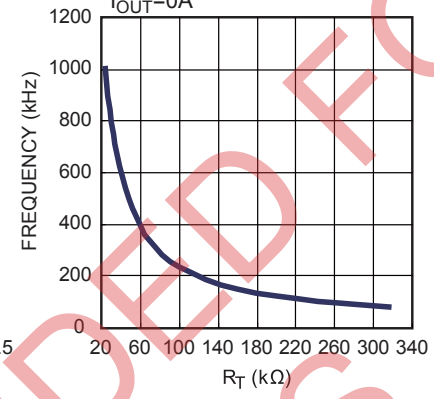


Shutdown Supply Current vs. V_{CC}



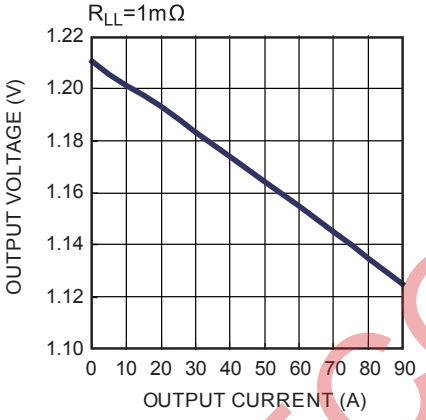
Switching Frequency vs. R_T

I_{OUT}=0A



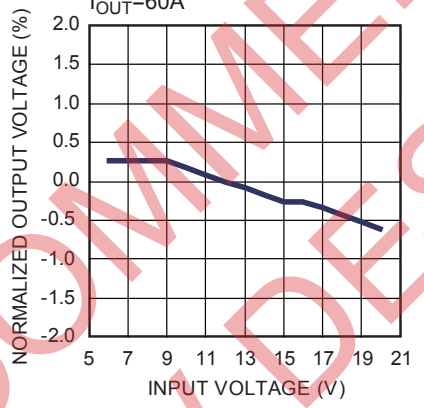
Load-Line

R_{LL}=1mΩ



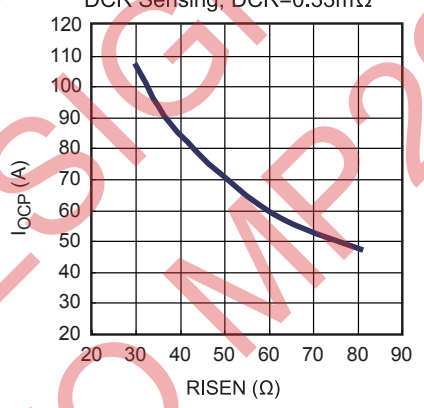
Line Regulation

I_{OUT}=60A



Overcurrent Trip Point vs. RISEN

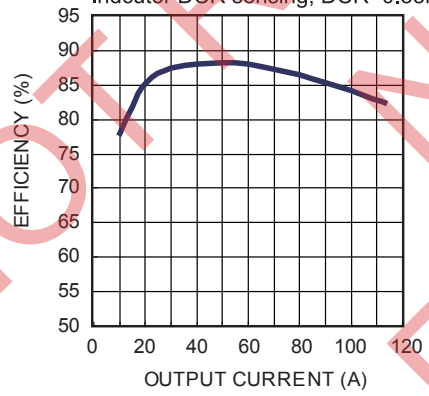
DCR Sensing, DCR=0.33mΩ



Efficiency

V_{IN}=12V, V_{OUT}=1.2V

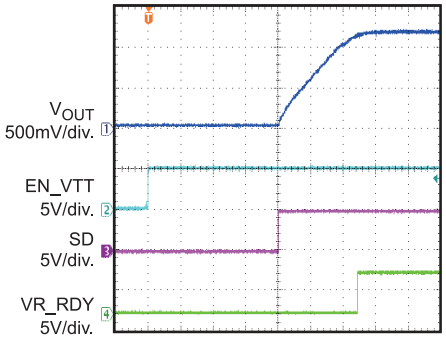
Indcutor DCR sensing, DCR=0.33mΩ



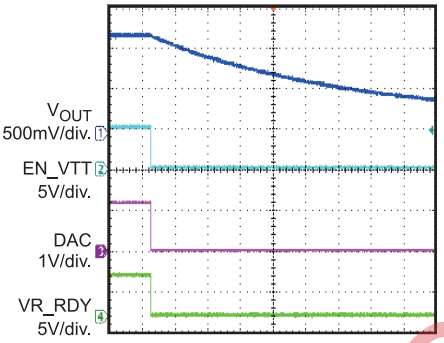
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{ID}=1.2V, L=0.3µH, F_{SW}=600kHz, 6-Phase Operation, T_A = +25ºC, unless otherwise noted.

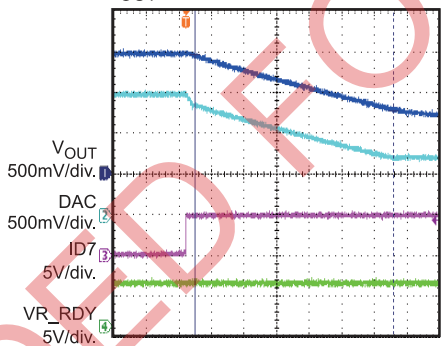
EN_VTT Startup
I_{OUT} = 0A



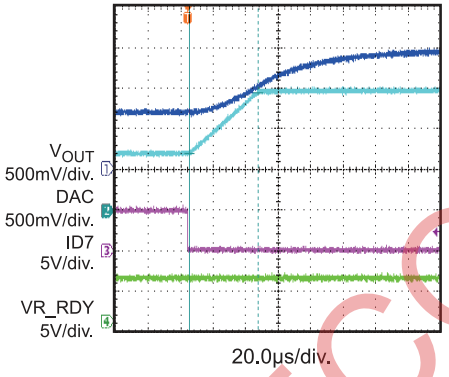
EN_VTT Shutdown
I_{OUT} = 0A



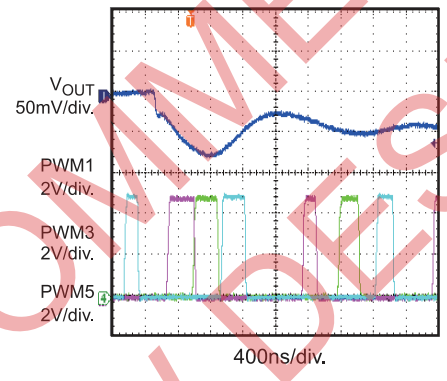
V_{ID}=1.5V to 0.7V, 6-Phase
I_{OUT} = 0A



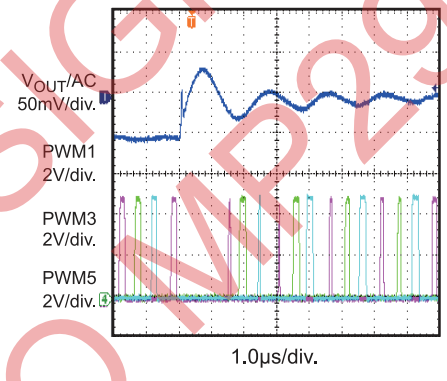
V_{ID}=0.7V to 1.5V, 6-Phase
I_{OUT} = 0A



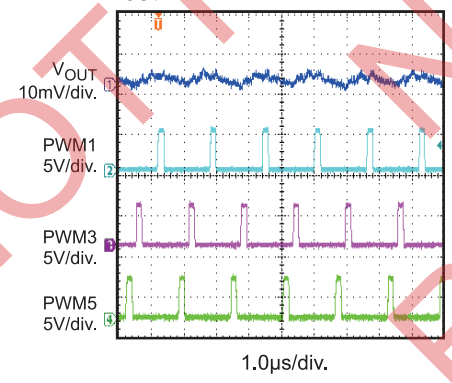
Load Transient Response @ load step up
I_{OUT}=0A-60A @ 500A/µs



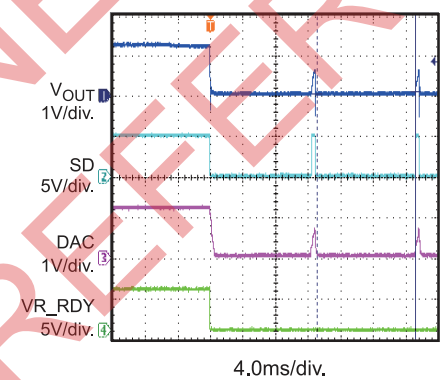
Load Transient Response @ load step down
I_{OUT}=60A-0A @ 500A/µs



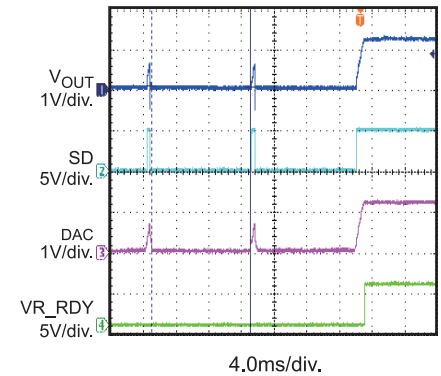
Output Ripple
I_{OUT} = 50A



OCP Entry



OCP Recorvey



BLOCK DIAGRAM

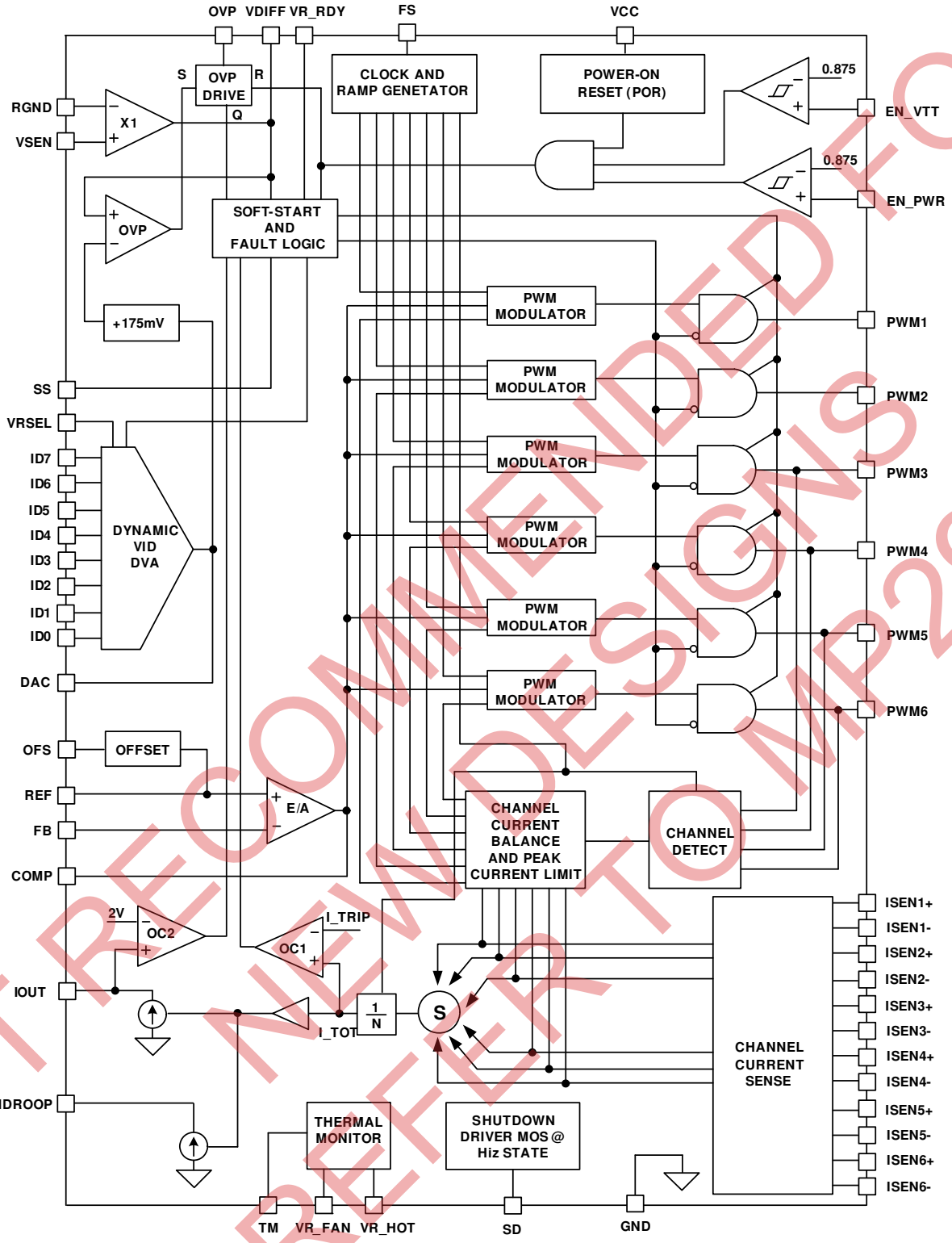


Figure 1—Functional Block Diagram

OPERATION

Multiphase Power Conversion

The MP2932 is a multiphase VR controller for Intel VR11 or VR10. It can be programmed for 2-, 3-, 4-, 5- or 6 channel operation for micro-processor core supply power converters with interleaved switching. The interleaving work of each phase can help to reduce of ripple current amplitude in the multiphase circuit and to reduce input ripple current.

The MP2932 control system is based on Dual-Edge PWM providing the fastest load response.

Under load transition condition, the MP2932 can turn on all phase together to improve the load transient. It can achieve excellent transient performance and reduce the demand on the output capacitors.

Number of Phases

The number of operational phases is determined by internal circuitry that monitors the PWM outputs. Normally, the MP2932 operates as a 6-phase controller. The number of active channels is determined by the state of PWM3, PWM4, PWM5, and PWM6. For 2-phase operation, connect PWM3 to VCC; similarly, PWM4 for 3-phase, PWM5 for 4-phase, and PWM6 for 5-phase operation. Table 1 shows the phase firing sequence.

Table 1—Phase firing sequence

Configuration	Phase Sequence
6-Phase	1 - 2 - 3 - 4 - 5 - 6
5-Phase	1 - 2 - 3 - 4 - 5
4-Phase	1 - 3 - 4 - 2
3-Phase	1 - 2 - 3
2-Phase	1 - 2

Switching Frequency

The clock frequency is set by an external resistor R_T connected from the FS pin to GND.

The resistor R_T can be estimated by Equation (1).

$$R_T = \frac{2.5 \times 10^{10}}{F_{SW}} - 600 \quad (1)$$

Where F_{SW} is the switching frequency of each phase.

Current Sensing

MP2932 has cycle by cycle current sense for fast response. MP2932 adopts inductor DCR sensing, or resistive sensing techniques. The sense current, I_{SEN}, is proportional to the inductor current. The sensed current is used for current balance, load-line regulation, and overcurrent protection.

Inductor DCR Sensing

The MP2932 can adopt a lossless current sensing scheme, commonly referred to as inductor DCR sensing, as shown in Figure 2.

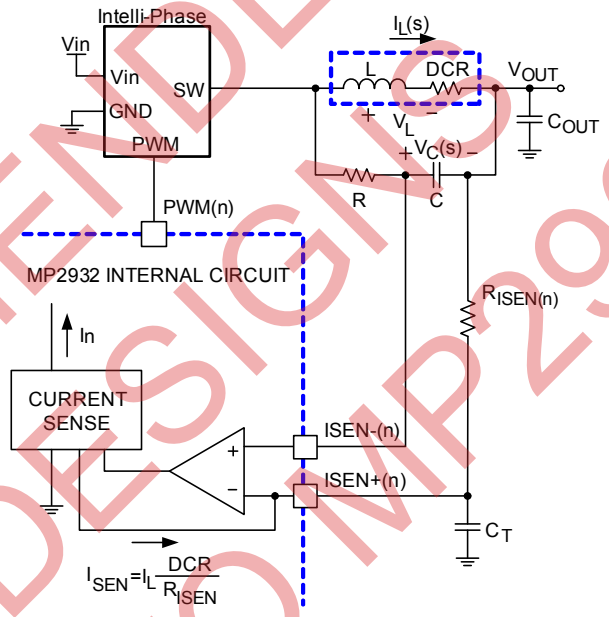


Figure 2—DCR Sensing Configuration

Equation (2) shows the s-domain equivalent voltage across the inductor V_L.

$$V_L = I_L \cdot (s \cdot L + DCR) \quad (2)$$

A simple RC network across the inductor extracts the DCR voltage, as shown in Figure 2.

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L, see Equation (3).

$$V_C = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \quad (3)$$

If the RC network components are selected such that the RC time constant (=R*C) matches the inductor time constant (=L/DCR), the voltage across the capacitor V_C is equal to the voltage drop across the DCR, i.e., proportional to the channel current.

Therefore, the current out of ISEN+ pin (I_{SEN}), is proportional to the inductor current and it can be seen form Equation (4).

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} \quad (4)$$

Resistive Sensing

For accurate current sense, a current-sense resistor R_{SENSE} in series with each output inductor can also be adopted (see Figure 3). This technique reduces overall converter efficiency due to the additional power loss on R_{SENSE}.

Equation (5) shows the relationship between the channel current to the sensed current I_{SEN}.

$$I_{SEN} = I_L \cdot \frac{R_{SENSE}}{R_{ISEN}} \quad (5)$$

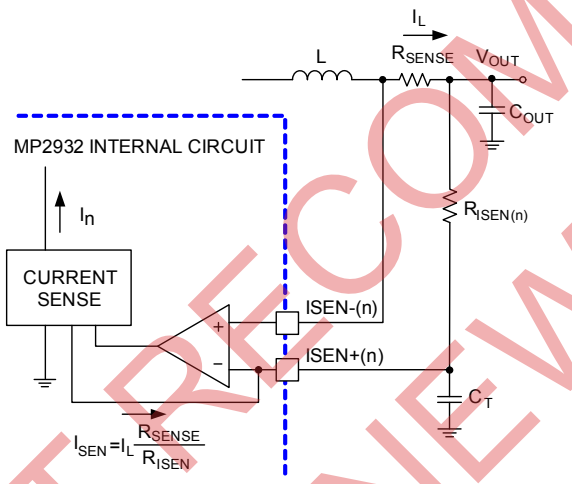


Figure 3—Sense Resistor in Series with Inductors

Channel-Current Balance

The sensed current from each active channel is summed together and divided by the number of active channels. The resulting average current (I_{AVG}) provides a measure of the total load current. Channel current balance is achieved by comparing the sensed current of each channel to the average current to make an appropriate adjustment to the PWM duty cycle of each channel.

Output Voltage and Load-Line Regulation

The MP2932 uses an internal differential remote-sense amplifier as shown in Figure 4. The microprocessor voltage is sensed between the VSEN and RGND pins.

The output of the error amplifier (V_{COMP}) is compared to sawtooth waveforms to generate the PWM signals. The typical open-loop gain of error amplifier is no less than 80dB, and the typical open-loop bandwidth is no less than 20MHz. The PWM signals control the timing of the MPS Intelli-phase and regulate the converter output to the specified reference voltage.

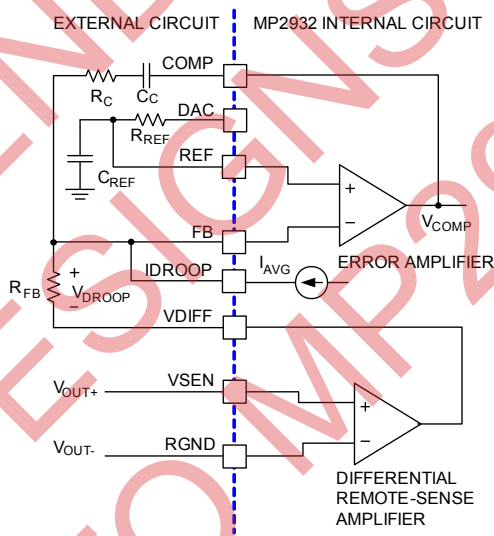


Figure 4—Output Voltage and Load-line Regulation

The load-line is realized by a resistor R_{FB} connected between FB pin and the remote sense output (VDIFF). As shown in Figure 4, the average current of all active channels (I_{AVG}) flows from FB through the load-line regulation resistor R_{FB}. The resulting voltage drop across R_{FB} can be seen form Equation (6):

$$V_{DROOP} = I_{AVG} R_{FB} \quad (6)$$

The output voltage is reduced by the droop voltage V_{DROOP}, and it is a function a load current. It's derived by combining Equation (6) with the appropriate sensing current expression defined by the current sense method.

$$V_{OUT} = V_{REF} - V_{OFS} - \left(\frac{I_{OUT}}{N} \frac{R_X}{R_{ISEN}} R_{FB} \right) \quad (7)$$

Where V_{REF} is the reference voltage, V_{OFS} is the programmed offset voltage, I_{OUT} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the ISEN+ pin, and R_{FB} is the feedback resistor, N is the active channel number, and R_X is the DCR, or R_{SENSE} depending on the sensing method.

Therefore, the loadline is defined as:

$$R_{LL} = \frac{R_{FB}}{N} \frac{R_X}{R_{ISEN}} \quad (8)$$

Output Voltage Offset Programming

In Figure 5, OFS pin is used to generate no-load offset. A resistor RREF between DAC and REF is selected, and the product (I_{OFS} x R_{OFS}) is equal to the desired offset voltage.

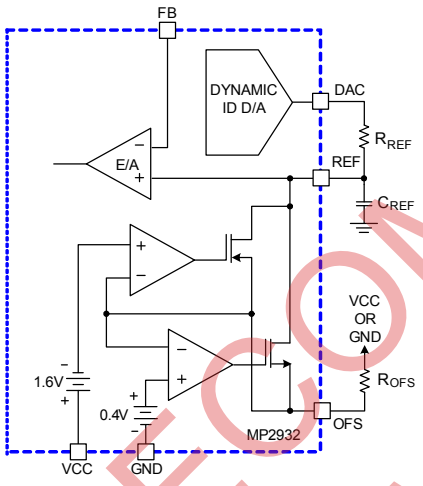


Figure 5—Offset Voltage Programming

Connect a resistor R_{OFS} between OFS to VCC to generate a positive offset. The voltage across it is regulated to 1.6V. This causes a proportional current (I_{OFS}) to flow into OFS. The positive offset is:

$$V_{OFFSET} = \frac{1.6 \times R_{REF}}{R_{OFS}} \quad (9)$$

Connect a resistor R_{OFS} between OFS to GND to generate a negative offset. The voltage across it is regulated to 0.4V, and I_{OFS} flows out of OFS. The negative offset is:

$$V_{OFFSET} = \frac{0.4 \times R_{REF}}{R_{OFS}} \quad (10)$$

Enable and Disable

While in shutdown mode, the PWM outputs are held in a Hi-Z state, and the SD signal is pulled low to assure the Intelli-phase remain off. The following input conditions must be met to start MP2932.

1. VCC must reach the internal power-on reset (POR) rising threshold.
2. EN_PWR is used to coordinate the power sequencing between VCC and another voltage rail. The enable comparator holds the MP2932 in shutdown until the voltage at EN_PWR rises above 0.875V.
3. The voltage on EN_VTT must be higher than 0.875V to enable the controller. This pin is typically connected to the output of VTT VR.
4.

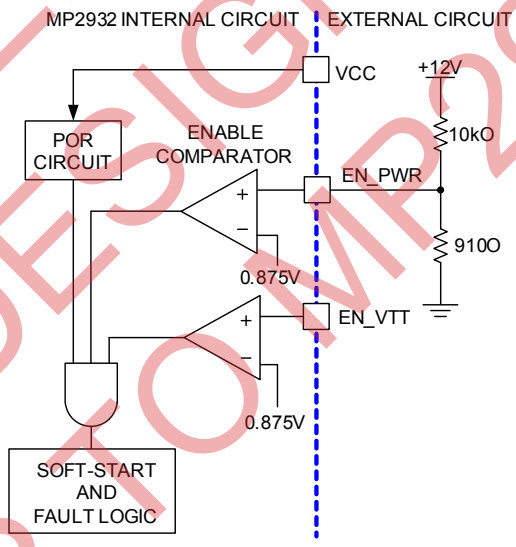


Figure 6—Power Sequencing Using Threshold Sensitive Enable (EN) Function

When all conditions are satisfied, MP2932 begins the soft-start and ramps the output voltage to 1.1V first. After remaining at 1.1V for some time, MP2932 reads the ID code at ID input pins. If the ID code is valid, MP2932 will regulate the output to the final ID setting. If the ID code is OFF code, MP2932 will shutdown, and cycling VCC, EN_PWR or EN_VTT is needed to restart.

Soft-Start

MP2932 has 4 periods during soft-start as shown in Figure 7. After VCC, EN_VTT and EN_PWR reach their POR/enable thresholds, the controller will have fixed delay period t_{d1} 1.36ms. After the delay period, the VR will begin first soft-start ramp until the output voltage reaches 1.1V. Then, the controller will regulate the VR voltage at 1.1V for another fixed period t_{d3}. At the end of t_{d3} period, MP2932 reads the ID signals. If the ID code is valid, MP2932 will initiate the second soft-start ramp until the voltage reaches the ID voltage minus offset voltage.

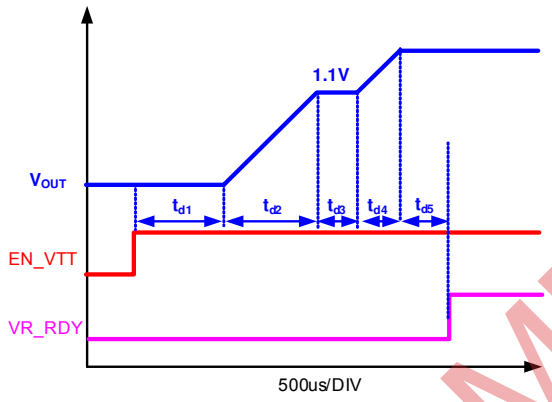


Figure 7—Soft-Start Waveforms

The soft-start time is the sum of the 4 periods, as shown in Equation (11):

$$t_{SS} = t_{d1} + t_{d2} + t_{d3} + t_{d4} \quad (11)$$

t_{d1} is about 1.36ms. t_{d3} is determined by the fixed 85µs plus the time to obtain valid ID voltage. If the ID is valid before the output reaches the 1.1V, the minimum time to validate the ID input is 500ns. Therefore the minimum t_{d3} is about 86µs.

During t_{d2} and t_{d4}, MP2932 digitally controls the DAC voltage change at 6.25mV per step. The time for each step is determined by the frequency of the soft-start oscillator which is defined by the resistor R_{SS} from SS pin to GND. The second soft-start ramp time t_{d2} and t_{d4} can be calculated based on Equations (12) and (13):

$$t_{d2} = \frac{2}{3} \times \frac{1.1 \times R_{SS}}{6.25 \times 25} (us) \quad (12)$$

$$t_{d4} = \frac{2}{3} \times \frac{(V_{VID} - 1.1) \times R_{SS}}{6.25 \times 25} (us) \quad (13)$$

For example, when ID is set to 1.5V and the R_{SS} is set at 100kΩ, the first soft-start ramp time t_{d2} will be 469µs and the second soft-start ramp time t_{d4} will be 171µs.

After the DAC voltage reaches the final ID setting, VR_RDY will be set to high with the fixed delay t_{d5}, it's about 85µs.

VR_RDY Signal

The VR_RDY pin is an open-drain logic output. It is pulled low during shutdown and releases high after a successful soft-start. VR_RDY will be pulled low when an under-voltage or over-voltage condition is detected, or the controller is disabled by a reset from EN_PWR, EN_VTT, POR, or ID OFF-code.

Under-voltage Detection

The under-voltage threshold is set at 50% of the ID code. When the output voltage at VSEN is below the under-voltage threshold, VR_RDY is pulled low.

Over-voltage Protection (OVP)

Regardless of the VR being enabled or not, the MP2932 OVP circuit will be active after its POR. The OVP thresholds are different at different operation conditions. When VR is not enabled and during the soft-start intervals t_{d1}, t_{d2} and t_{d3}, the OVP threshold is 1.275V. Once the controller detects valid ID input, the OVP trip point will be changed to DAC + 175mV.

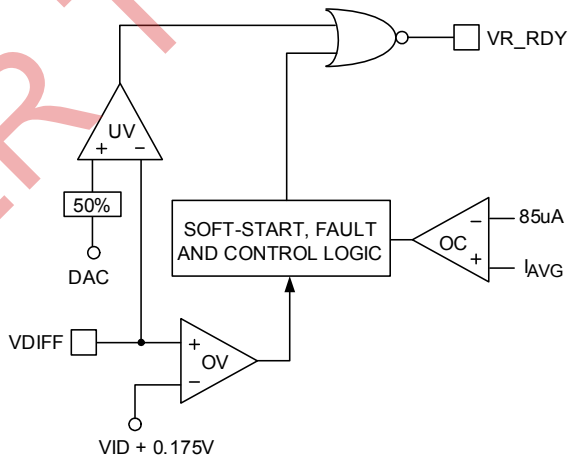


Figure 8—VR_RDY and Protection Circuitry

At the beginning of an over-voltage event, all PWM outputs are commanded low instantly (>20ns). The Intelli-phase LS-FET is turned on. When the VDIFF voltage falls below the DAC + 75mV, PWM signals enter a Hi-Z state, and the SD pin is pulled low to turn off the Intelli-phase. If the over-voltage condition reoccurs, the MP2932 will again command the LS-FET to turn on. The MP2932 will continue to protect the load in this way as long as the over-voltage condition occurs.

Once an over-voltage condition is detected, normal PWM operation ceases until the MP2932 is reset. Cycling the voltage on EN_PWR, EN_VTT or VCC below the POR-falling threshold will reset the controller. Cycling the ID codes will not reset the controller.

Over-current Protection (OCP)

MP2932 has two levels of over-current protection. Each phase is protected from a sustained over-current condition by limiting its peak current, while the combined phase currents are protected on an instantaneous basis.

In instantaneous protection mode, the MP2932 adopts the sensed average current I_{AVG} to detect an over-current condition. The I_{AVG} is compared with a constant 85μA reference current, as shown in Figure 8. Once I_{AVG} exceeds 85μA, a comparator triggers the converter to shutdown. At the beginning of over-current shutdown, the controller places all PWM signals in a Hi-Z state within 20ns to turn off the Intelli-phase. The system remains in this state about 12ms. If the controller is still enabled at the end of this wait period, it will attempt a soft-start. If the fault remains, the hiccup mode will continue indefinitely until either controller is disabled or the fault is cleared.

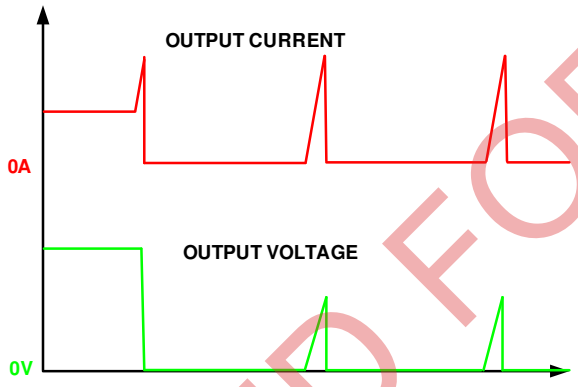


Figure 9—Over-current Behavior in HICCUP Mode. Fsw = 600kHz

For the individual channel over-current protection, the MP2932 continuously compares the sensed current signal of each channel with the 120μA reference current. If one channel current exceeds the reference current, MP2932 will pull PWM signal of this channel to low for the rest of the switching cycle. This PWM signal can be turned on next cycle if the sensed channel current is less than the 120μA reference current. The peak current limit of individual channel will not trigger the converter to shutdown.

Thermal Monitoring (VR_HOT/VR_FAN)

There are two thermal signals to indicate the temperature status of the voltage regulator: VR_HOT and VR_FAN. Both VR_FAN and VR_HOT pins are open-drain outputs, and external pull-up resistors are required. Those signals are valid only after the controller is enabled.

The VR_FAN signal indicates that the temperature of the voltage regulator is high and more cooling airflow is needed. The VR_HOT signal can be used to inform the system that the temperature of the voltage regulator is too high and the CPU should reduce its power consumption.

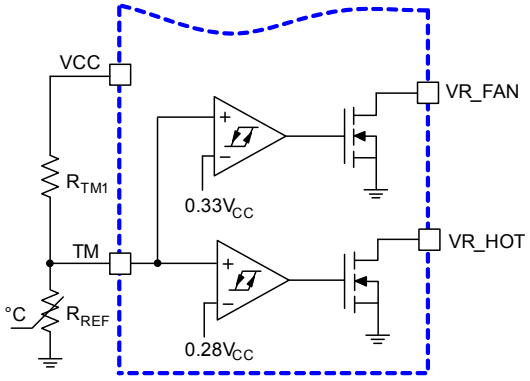


Figure 10—Block Diagram of Thermal Monitoring Function

Figure 10 shows the diagram of thermal monitoring function block. One NTC resistor should be placed close to the power stage of the voltage regulator to sense the temperature, and one pull-up resistor is needed to form the voltage divider for the TM pin. As the temperature of the power stage increases, the resistance of the NTC will reduce, resulting in the reduced voltage at the TM pin.

There are two comparators with hysteresis to compare the TM pin voltage to the fixed thresholds for VR_FAN and VR_HOT signals respectively. The VR_FAN signal is set to high when the TM voltage is lower than 33% of VCC voltage, and is pulled to GND when the TM voltage increases to above 39% of VCC voltage. The VR_FAN signal is set to high when the TM voltage goes below 28% of VCC voltage, and is pulled to GND when the TM voltage goes back to above 33% of VCC voltage. Figure 11 shows the operation of those signals.

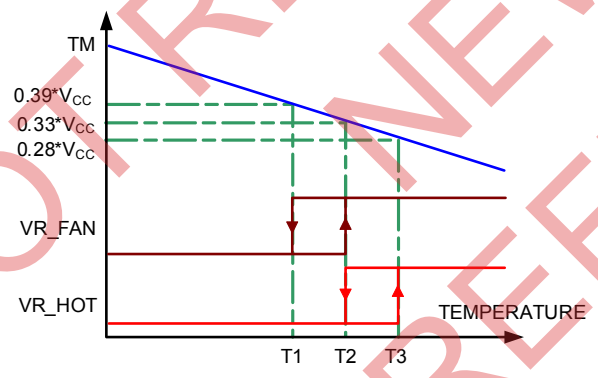


Figure 11—VR_HOT and VR_FAN Signal vs. TM Voltage

Current Sense Output

The MP2932 has 2 current sense output pins IDROOP and IOUT, they are identical. In typical application, IDROOP pin is connected to FB pin for the application where load line is required. IOUT pin was designed for load current measurement.

The current from the IDROOP pin is the sensed average current. In typical application, the IDROOP pin is connected to the FB pin for the application where load line is required. Load current information can be obtained by measuring the voltage at IOUT pin with a resistor connecting IOUT pin to the ground.

When load line function is not needed, the IDROOP pin can be used to obtain the load current information: with one resistor from the IDROOP pin to GND, the voltage at the IDROOP pin will be proportional to the load current in Equation (14):

$$V_{IDROOP} = \frac{R_{IDROOP}}{N} \frac{R_X}{R_{ISEN}} I_{LOAD} \quad (14)$$

Where V_{IDROOP} is the voltage at the IDROOP pin, R_{IDROOP} is the resistor between the IDROOP pin and GND, I_{LOAD} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the ISEN+ pin, N is the active channel number, and R_X is the resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method.

The resistor from the IDROOP pin to GND should be chosen to ensure that the voltage at the IDROOP pin is less than 2V under the maximum load current.

If the IDROOP pin is not used, tie it to GND.

APPLICATION INFORMATION

Current Sensing Resistor

The resistors connected to the ISEN+ pins determine the gains in the load-line regulation loop and the channel-current balance loop as well as setting the overcurrent trip point. Select values for these resistors by using Equation (15):

$$R_{ISEN} = \frac{R_X}{85 \times 10^{-6}} \frac{I_{OCP}}{N} \quad (15)$$

Where R_{ISEN} is the sense resistor connected to the ISEN+ pin, N is the active channel number, R_X is the resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method, and I_{OCP} is the desired overcurrent trip point. Typically, I_{OCP} can be chosen to be 1.3x the maximum load current of the specific application.

Load-Line Regulation Resistor

The load-line regulation resistor is labeled R_{FB} in Figure 4. Its value depends on the desired load-line requirement of the application.

The desired load-line can be calculated by using Equation (16):

$$R_{LL} = \frac{V_{DROOP}}{I_{FL}} \quad (16)$$

Where I_{FL} is the full load current of the specific application, and V_{RDROOP} is the desired voltage droop under the full load condition.

Based on the desired load-line R_{LL}, the load-line regulation resistor can be calculated by using Equation (17):

$$R_{FB} = \frac{NR_{ISEN}R_{LL}}{R_X} \quad (17)$$

Where N is the active channel number, R_{ISEN} is the sense resistor connected to the ISEN+ pin, and R_X is the resistance of the current sense, either the DCR of the inductor or R_{SENSE} depending on the sensing method.

Compensation

There are two distinct methods for achieving the compensation.

Compensating Load-Line Regulated Converter

The load-line regulated converter behaves in a similar manner to a peak-current mode controller because the two poles at the output-filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_C and C_C.

Treating the system as though it were a voltage-mode regulator by compensating the L-C poles and the ESR zero of the voltage-mode.

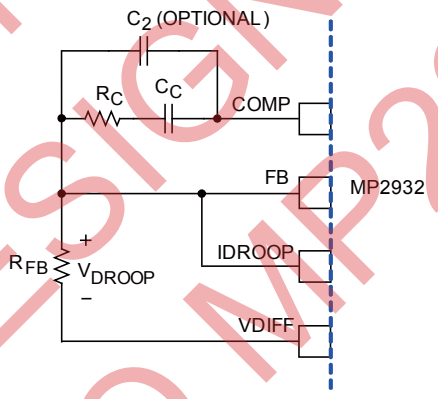


Figure 12— Compensation Circuit for MP2932 with Load-line Regulation

The feedback resistor, R_{FB}, has already been chosen as outlined in “Load-Line Regulation Resistor”. Select a target bandwidth for the compensated system, f_0. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of f_0 to the L-C pole frequency and the ESR zero frequency.

The optional capacitor C_2, (22pF to 150pF) is sometimes needed to bypass noise away from the PWM comparator (see Figure 12).

Compensation without Load-Line Regulation

The non load-line regulated converter is accurately modeled as a voltage-mode regulator with two poles at the L-C resonant frequency and a zero at the ESR frequency. A type-III controller, as shown in Figure 13, provides the necessary compensation.

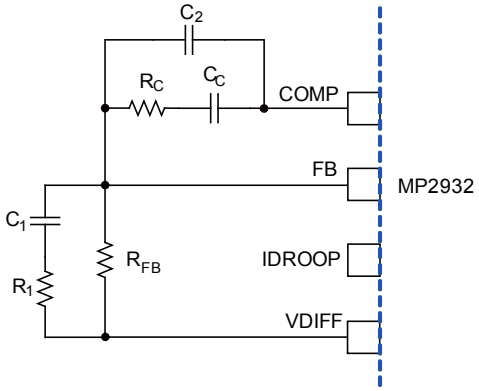


Figure 13—Compensation Circuit for MP2932 without Load-line Regulation

The first step is to choose the desired bandwidth, f_0, of the compensated system. Choose a frequency high enough to assure adequate transient performance but not higher than 1/3 of the switching frequency. The type-III compensator has an extra high-frequency pole, f_{HF}. A good general rule is to choose $f_{HF}=10f_0$, but it can be higher if desired. Choosing f_{HF} to be lower than $10f_0$ can cause problems with too much phase shift below the system bandwidth.

Output Inductor

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI; the load-current slew rate, di/dt; and the maximum allowable output voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount in Equation (18):

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \quad (18)$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

The ESR of the bulk capacitors also creates the majority of the output voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current, a voltage develops across the bulk-capacitor ESR. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{P-P(MAX)}$ determines the lower limit on the inductance.

$$L \geq (ESR)\frac{(V_{IN} - NV_{OUT})V_{OUT}}{f_s V_{IN} V_{P-P(MAX)}} \quad (19)$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Input Capacitor

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

Low capacitance, high-frequency ceramic capacitors are needed in addition to the bulk capacitors to suppress leading and falling edge voltage spikes. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitic impedances and maximize suppression.

PC Board Layout

For best performance of the MP2932, the following guidelines should be strictly followed:

Within the allotted implementation area, place the switching components first. Switching component placement should take into account power dissipation. Align the output inductors and MOSFETs such that space between the components is minimized while creating the PHASE plane. If possible, duplicate the same placement of these components for each phase.

Next, place the input and output capacitors. Position one high frequency ceramic input capacitor next to each upper MOSFET drain. Place the input capacitors as close to the upper MOSFET drains as dictated by the component size and dimensions. Locate the output capacitors between the inductors and the load, while keeping them in close proximity to the microprocessor socket.

Table 2—VR10 ID Table (with 6.25mV Extension)

ID4 400mV	ID3 200mV	ID2 100mV	ID1 50mV	ID0 25mV	ID5 12.5mV	ID6 6.25mV	VOLTAGE (V)
0	1	0	1	0	1	1	1.60000
0	1	0	1	0	1	0	1.59375
0	1	0	1	1	0	1	1.58750
0	1	0	1	1	0	0	1.58125
0	1	0	1	1	1	1	1.57500
0	1	0	1	1	1	0	1.56875
0	1	1	0	0	0	1	1.56250
0	1	1	0	0	0	0	1.55625
0	1	1	0	0	1	1	1.55000
0	1	1	0	0	1	0	1.54375
0	1	1	0	1	0	1	1.53750
0	1	1	0	1	0	0	1.53125
0	1	1	0	1	1	1	1.52500
0	1	1	0	1	1	0	1.51875
0	1	1	1	0	0	1	1.51250
0	1	1	1	0	0	0	1.50625
0	1	1	1	0	1	1	1.50000
0	1	1	1	0	1	0	1.49375
0	1	1	1	1	0	1	1.4875
0	1	1	1	1	0	0	1.48125
0	1	1	1	1	1	1	1.47500
0	1	1	1	1	1	0	1.46875
1	0	0	0	0	0	1	1.46250
1	0	0	0	0	0	0	1.45625
1	0	0	0	0	1	1	1.45000
1	0	0	0	0	1	0	1.44375
1	0	0	0	1	0	1	1.43750
1	0	0	0	1	0	0	1.43125
1	0	0	0	1	1	1	1.42500
1	0	0	0	1	1	0	1.41875
1	0	0	1	0	0	1	1.41250
1	0	0	1	0	0	0	1.40625
1	0	0	1	0	1	1	1.40000
1	0	0	1	0	1	0	1.39375
1	0	0	1	1	0	1	1.38750
1	0	0	1	1	0	0	1.38125
1	0	0	1	1	1	1	1.37500
1	0	0	1	1	1	0	1.36875
1	0	1	0	0	0	1	1.36250

Table 2—VR10 ID Table (with 6.25mV Extension) *continued*

ID4 400mV	ID3 200mV	ID2 100mV	ID1 50mV	ID0 25mV	ID5 12.5mV	ID6 6.25mV	VOLTAGE (V)
1	0	1	0	0	0	0	1.35625
1	0	1	0	0	1	1	1.35000
1	0	1	0	0	1	0	1.34375
1	0	1	0	1	0	1	1.33750
1	0	1	0	1	0	0	1.33125
1	0	1	0	1	1	1	1.32500
1	0	1	0	1	1	0	1.31875
1	0	1	1	0	0	1	1.31250
1	0	1	1	0	0	0	1.30625
1	0	1	1	0	1	1	1.30000
1	0	1	1	0	1	0	1.29375
1	0	1	1	1	0	1	1.28750
1	0	1	1	1	0	0	1.28125
1	0	1	1	1	1	1	1.27500
1	0	1	1	1	1	0	1.26875
1	1	0	0	0	0	1	1.26250
1	1	0	0	0	0	0	1.25625
1	1	0	0	0	1	1	1.25000
1	1	0	0	0	1	0	1.24375
1	1	0	0	1	0	1	1.23750
1	1	0	0	1	0	0	1.23125
1	1	0	0	1	1	1	1.22500
1	1	0	0	1	1	0	1.21875
1	1	0	1	0	0	1	1.21250
1	1	0	1	0	0	0	1.20625
1	1	0	1	0	1	1	1.20000
1	1	0	1	0	1	0	1.19375
1	1	0	1	1	0	1	1.18750
1	1	0	1	1	0	0	1.18125
1	1	0	1	1	1	1	1.17500
1	1	0	1	1	1	0	1.16875
1	1	1	0	0	0	1	1.16250
1	1	1	0	0	0	0	1.15625
1	1	1	0	0	1	1	1.15000
1	1	1	0	0	1	0	1.14375
1	1	1	0	1	0	1	1.13750
1	1	1	0	1	0	0	1.13125
1	1	1	0	1	1	1	1.12500
1	1	1	0	1	1	0	1.11875

Table 2—VR10 ID Table (with 6.25mV Extension) *continued*

ID4 400mV	ID3 200mV	ID2 100mV	ID1 50mV	ID0 25mV	ID5 12.5mV	ID6 6.25mV	VOLTAGE (V)
1	1	1	1	0	0	1	1.11250
1	1	1	1	0	0	0	1.10625
1	1	1	1	0	1	1	1.10000
1	1	1	1	0	1	0	1.09375
1	1	1	1	1	0	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	1	1	OFF
1	1	1	1	1	1	0	OFF
0	0	0	0	0	0	1	1.08750
0	0	0	0	0	0	0	1.08125
0	0	0	0	0	1	1	1.07500
0	0	0	0	0	1	0	1.06875
0	0	0	0	1	0	1	1.06250
0	0	0	0	1	0	0	1.05625
0	0	0	0	1	1	1	1.05000
0	0	0	0	1	1	0	1.04375
0	0	0	1	0	0	1	1.03750
0	0	0	1	0	0	0	1.03125
0	0	0	1	0	1	1	1.02500
0	0	0	1	0	1	0	1.01875
0	0	0	1	1	0	1	1.01250
0	0	0	1	1	0	0	1.00625
0	0	0	1	1	1	1	1.00000
0	0	0	1	1	1	0	0.99375
0	0	1	0	0	0	1	0.9875
0	0	1	0	0	0	0	0.98125
0	0	1	0	0	1	1	0.97500
0	0	1	0	0	1	0	0.96875
0	0	1	0	1	0	1	0.9625
0	0	1	0	1	0	0	0.95625
0	0	1	0	1	1	1	0.95000
0	0	1	0	1	1	0	0.94375
0	0	1	1	0	0	1	0.93750
0	0	1	1	0	0	0	0.93125
0	0	1	1	0	1	1	0.92500
0	0	1	1	0	1	0	0.91875
0	0	1	1	1	0	1	0.91250
0	0	1	1	1	0	0	0.90625
0	0	1	1	1	1	1	0.90000

Table 2—VR10 ID Table (with 6.25mV Extension) *continued*

ID4 400mV	ID3 200mV	ID2 100mV	ID1 50mV	ID0 25mV	ID5 12.5mV	ID6 6.25mV	VOLTAGE (V)
0	0	1	1	1	1	0	0.89375
0	1	0	0	0	0	1	0.88750
0	1	0	0	0	0	0	0.88125
0	1	0	0	0	1	1	0.87500
0	1	0	0	0	1	0	0.86875
0	1	0	0	1	0	1	0.86250
0	1	0	0	1	0	0	0.85625
0	1	0	0	1	1	1	0.85000
0	1	0	0	1	1	0	0.84375
0	1	0	1	0	0	1	0.83750
0	1	0	1	0	0	0	0.83125

Table 3—VR11 ID 8-BIT

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	VOLTAGE
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500

Table 3—VR11 ID 8-BIT *continued*

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	VOLTAGE
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500

Table 3—VR11 ID 8-BIT *continued*

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	VOLTAGE
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125

Table 3—VR11 ID 8-BIT *continued*

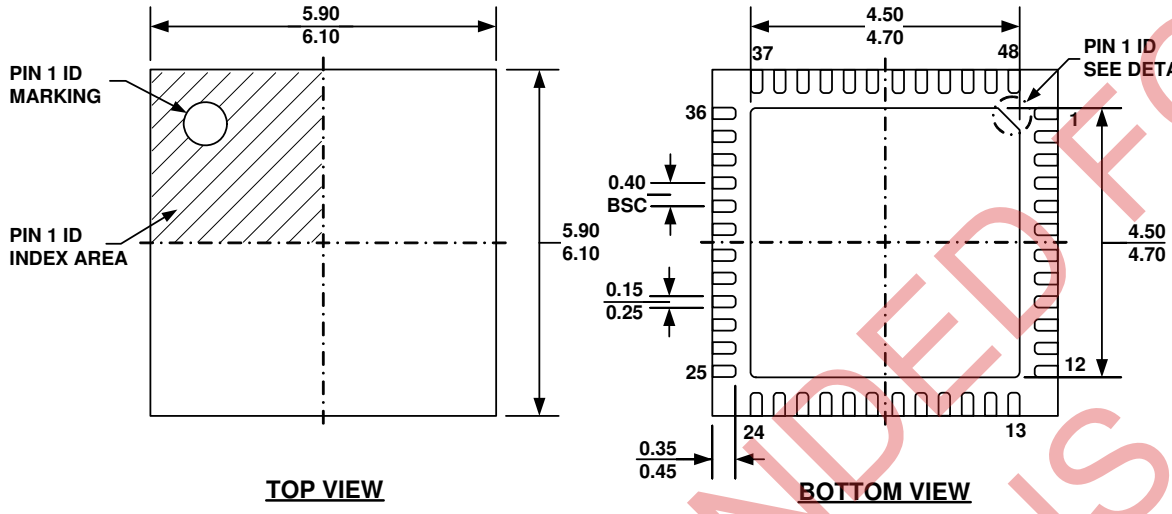
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	VOLTAGE
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125

Table 3—VR11 ID 8-BIT *continued*

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	VOLTAGE
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

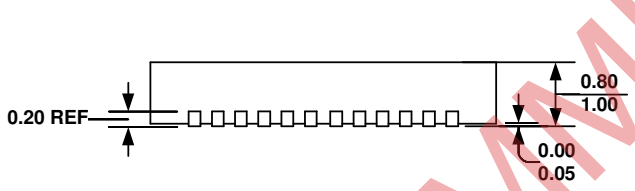
PACKAGE INFORMATION

QFN48 (6 x 6mm)

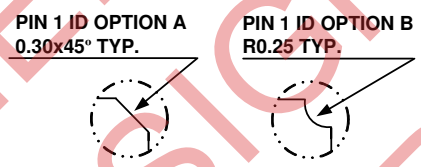


TOP VIEW

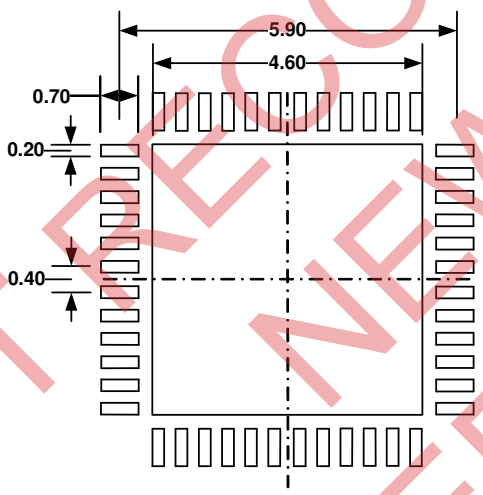
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VJJE-1.
5) DRAWING IS NOT TO SCALE.