ESD and Surge Protection Device, Bidirectional, 15 V

Micro−Packaged Diodes for ESD Protection

ESDL4151

The ESDL4151 is designed to protect voltage sensitive components that require low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, the part is well suited for use in high frequency designs such as USB 2.0/3.0 high speed applications.

X3DFN2
1.0 X 0.6
CASE 514AG

MARKING DIAGRAM

PIN 1

R5 = Specific Device Code
M = Date Code

Features

- Low Capacitance 0.8 pF (Typ)
- Low Clamping Voltage
- Small Body Outline Dimensions: 1.00 mm x 0.60 mm
- Low Body Height: 0.23 mm
- Stand−off Voltage: 15 V
- Protection for the following IEC Standards:
  IEC61000−4−2 Level 4: ±30 kV Contact Discharge
  IEC61000−4−5 (Lightning): 53 V Input (8/20 μs)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- USB 2.0/3.0
- MHL 2.0
- eSATA

ORDERING INFORMATION

Device	Package	Shipping†
ESDL4151MX4T5G	X3DFN2 (Pb−Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
IEC 61000−4−2 (ESD)	Contact Air		±30 ±30	kV
Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

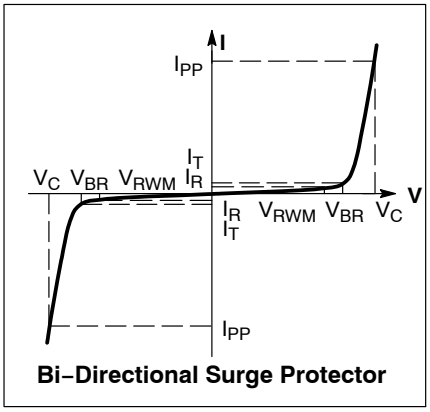
See Application Note AND8308/D for further description of survivability specs.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional Surge Protector

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			15	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	15.5	16.6	19.5	V
Reverse Leakage Current	I_R	@ 3.3 V, I/O Pin to GND @ 15 V, I/O Pin to GND			0.1 1.0	μA
Clamping Voltage	V_C	Per IEC61000−4−2, ±8 kV Contact	See Figures 1 & 2			V
Clamping Voltage TLP (Note 1)	V_C	I_{PP} = 8 A IEC61000−4−2 Level 2 Equivalent (±4 kV Contact, ±8 kV Air)		21.3		V
		I_{PP} = 16 A IEC61000−4−2 Level 4 Equivalent (±8 kV Contact, ±16 kV Air)		22.9		V
Reverse Peak Pulse Current	I_{PP}	IEC61000−4−5 (8x20 μs) Input Voltage	53			V
		IEC61000−4−5 (8x20 μs) per Figure 11	11			A
Clamping Voltage 8x20 μs Waveform per Figure A (Note 2)	V_C	IEC61000−4−5 (8x20 μs) Input Voltage = 53 V		23	26	V
Dynamic Resistance	R_{DYN}	I/O Pin to GND (8x20 μs)		0.43		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz		0.80	1.0	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z0 = 50, tp = 100 ns, tr = 1 ns, averaging window; t1 = 70 ns to t2 = 90 ns.
2. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−5 waveform.

TYPICAL CHARACTERISTICS

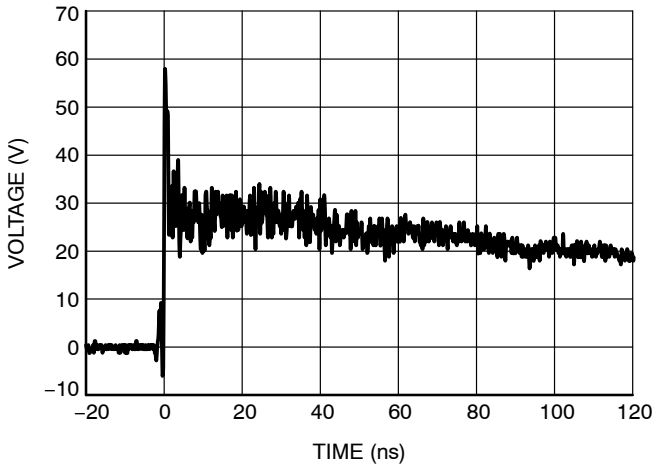


Figure 1. ESD Clamping Voltage Pin 1 to Pin 2 8 kV Contact per IEC61000−4−2

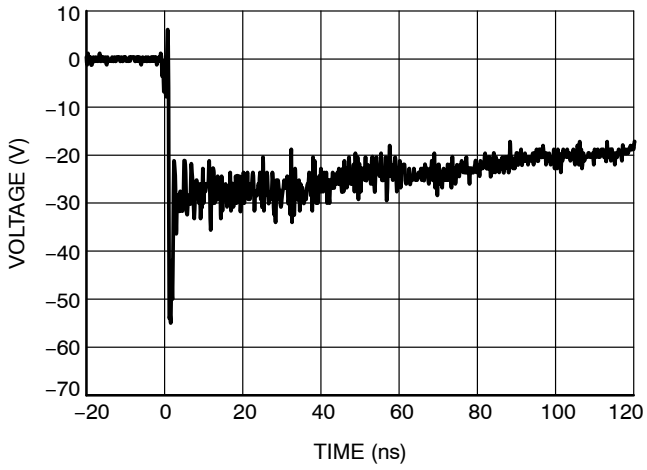


Figure 2. ESD Clamping Voltage Pin 2 to Pin 1 8 kV Contact per IEC61000−4−2

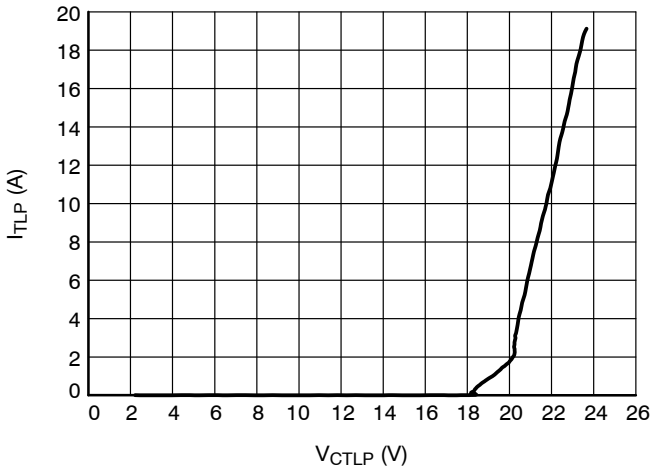


Figure 3. Pin 1 to Pin 2 100 ns TLP I−V Curve

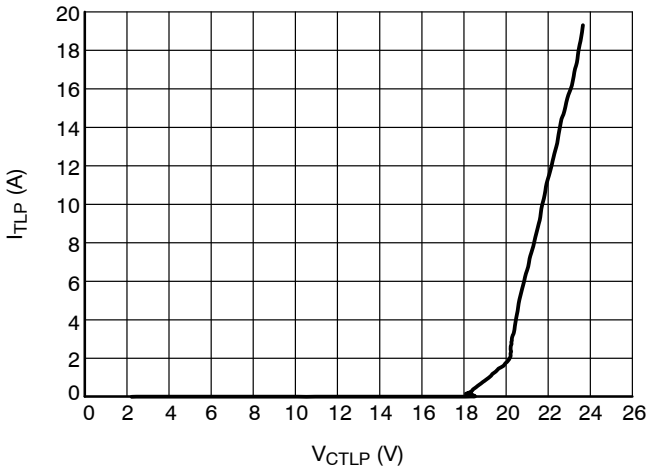


Figure 4. Pin 2 to Pin 1 TLP I−V Curve

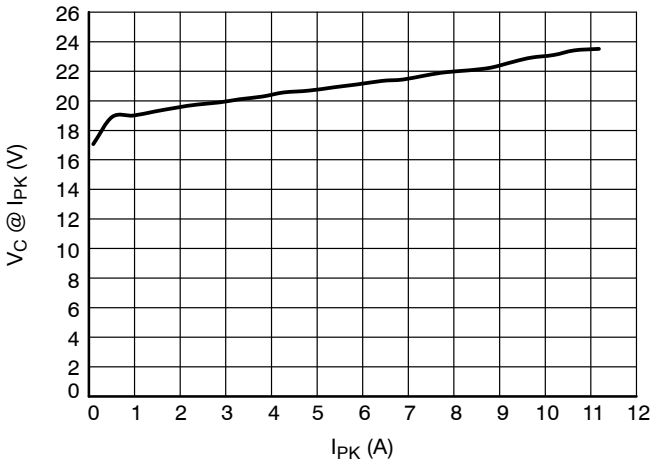


Figure 5. Pin 1 to Pin 2 Clamping Voltage vs. Peak Pulse Current (tp = 8/20 μs)

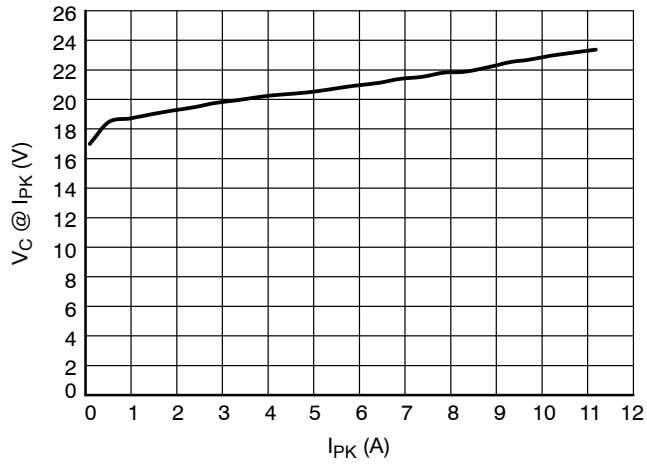


Figure 6. Pin 2 to Pin 1 Clamping Voltage vs. Peak Pulse Current (tp = 8/20 μs)

TYPICAL CHARACTERISTICS

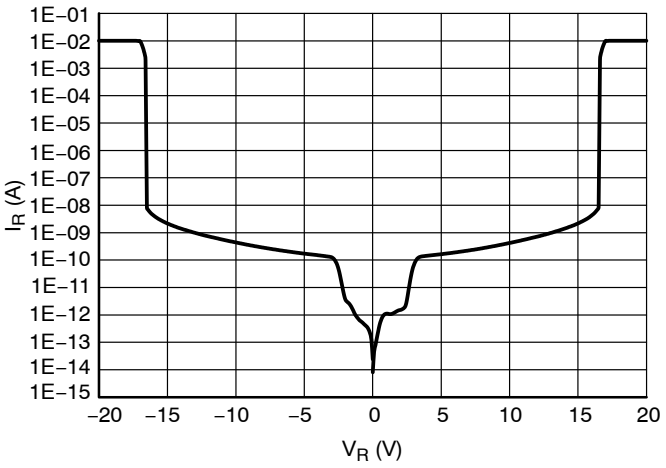


Figure 7. Reverse Leakage Current

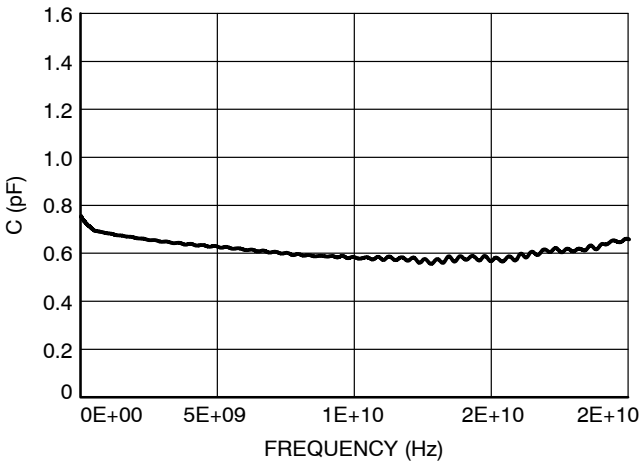


Figure 8. Capacitance Over Frequency

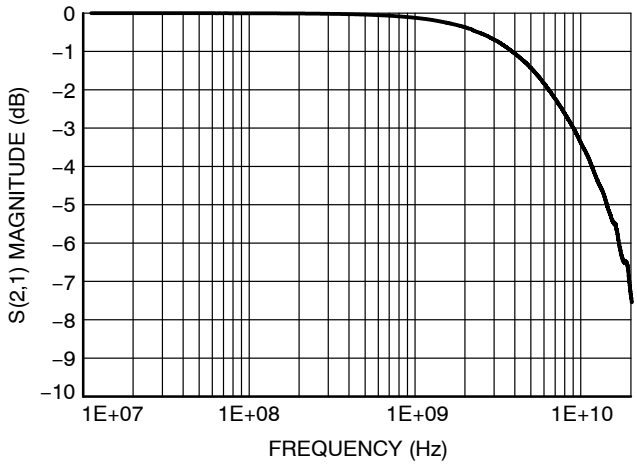


Figure 9. Insertion Loss

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

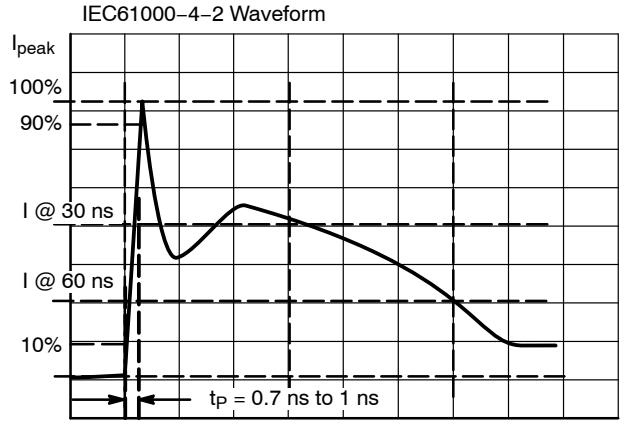


Figure 10. IEC61000−4−2 Spec

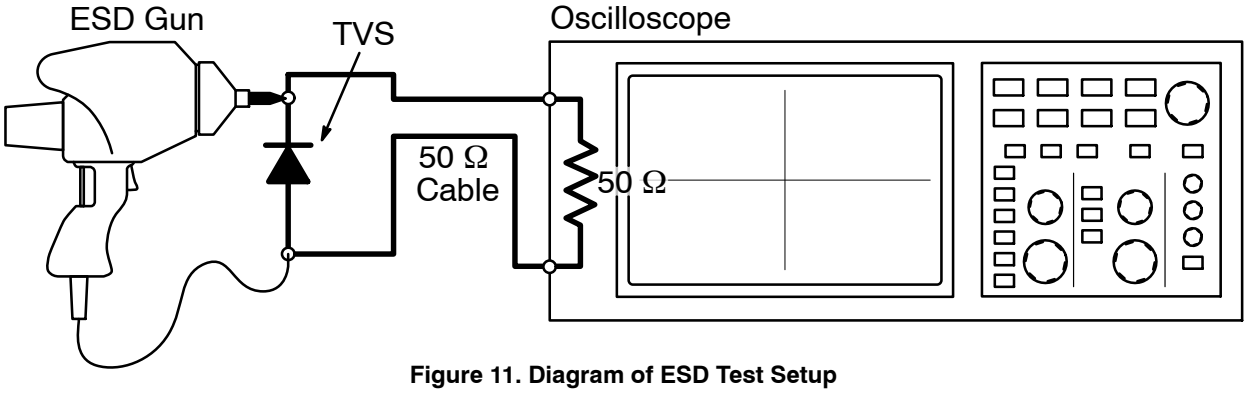


Figure 11. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

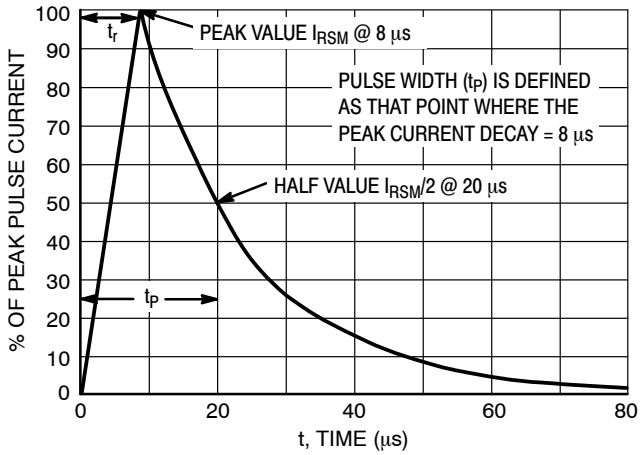


Figure 12. 8 X 20 μs Pulse Waveform

X3DFN2 1.0x0.6, 0.65P
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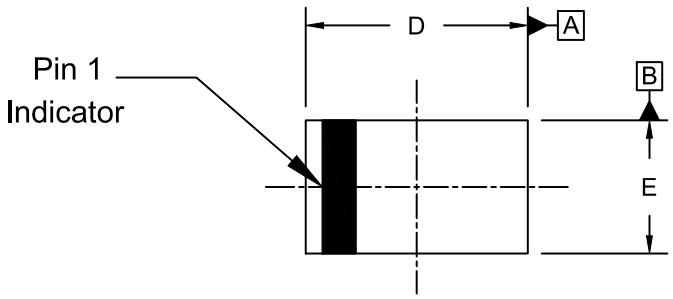
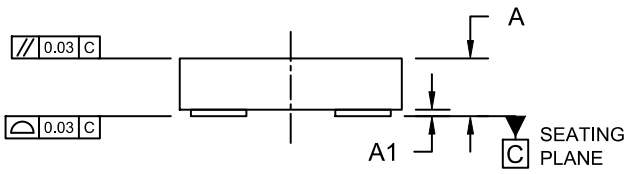
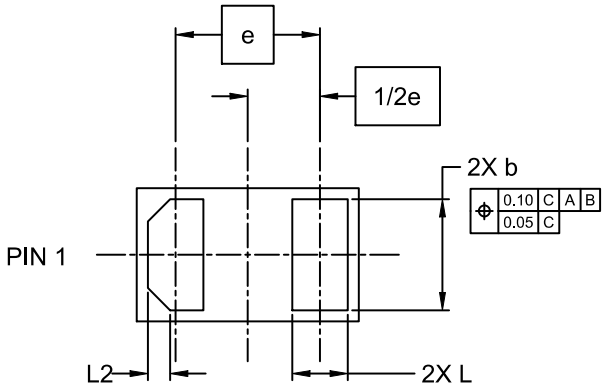


TOP VIEW



SIDE VIEW

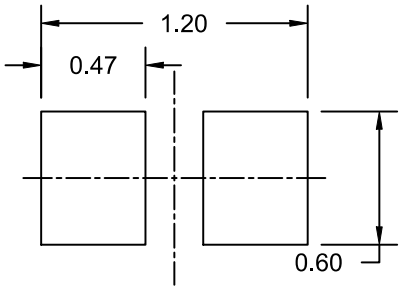


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS

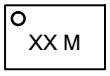
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.20	0.23	0.26
A1	0.00	---	0.03
b	0.45	0.50	0.55
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.65 BSC		
L	0.20	0.25	0.30
L2	0.10 REF		



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**X3DFN2 1.0x0.6, 0.65P**		**PAGE 1 OF 1**

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