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# FQP11P06

## P-Channel QFET<sup>®</sup> MOSFET

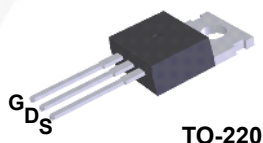
-60 V, -11.4 A, 175 mΩ

### Description

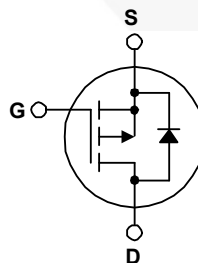
These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand a high energy pulse in the avalanche and commutation modes. These devices are well suited for low voltage applications such as automotive, DC/DC converters, and high efficiency switching for power management in portable and battery operated products.

### Features

- -11.4 A, -60 V,  $R_{DS(on)} = 175 \text{ m}\Omega$  (Max.) @  $V_{GS} = -10 \text{ V}$ ,  $I_D = -5.7 \text{ A}$
- Low Gate Charge (Typ. 13 nC)
- Low  $C_{rss}$  (Typ. 45 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



TO-220



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQP11P06	Unit
$V_{DSS}$	Drain-Source Voltage	-60	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	-11.4	A
		-8.05	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	-45.6	A
$V_{GSS}$	Gate-Source Voltage	$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	160	mJ
$I_{AR}$	Avalanche Current (Note 1)	-11.4	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	5.3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-7.0	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	53	W
		0.35	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQP11P06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.85	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP11P06	FQP11P06	TO-220	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-60	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	-0.07	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
		$V_{DS} = -48\text{ V}, T_C = 150^\circ\text{C}$	--	--	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -5.7\text{ A}$	--	0.14	0.175	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -30\text{ V}, I_D = -5.7\text{ A}$	--	5.1	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	420	550	pF
$C_{oss}$	Output Capacitance		--	195	250	pF
$C_{rfs}$	Reverse Transfer Capacitance		--	45	60	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -30\text{ V}, I_D = -5.7\text{ A},$ $R_G = 25\ \Omega$	--	6.5	25	ns	
$t_r$	Turn-On Rise Time		--	40	90	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	--	15	40	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	45	100	ns
$Q_g$	Total Gate Charge	$V_{DS} = -48\text{ V}, I_D = -11.4\text{ A},$ $V_{GS} = -10\text{ V}$	--	13	17	nC	
$Q_{gs}$	Gate-Source Charge		(Note 4)	--	2.0	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	6.3	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	-11.4	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-45.6	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -11.4\text{ A}$	--	--	-4.0	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -11.4\text{ A},$ $dI_F / dt = 100\text{ A}/\mu\text{s}$	--	83	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	0.26	--	$\mu\text{C}$

#### Notes:

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $L = 1.44\text{ mH}, I_{AS} = -11.4\text{ A}, V_{DD} = -25\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq -11.4\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Characteristics

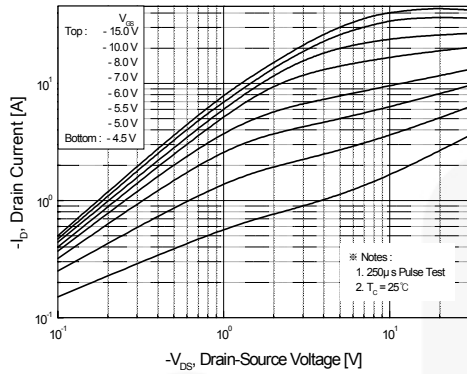


Figure 1. On-Region Characteristics

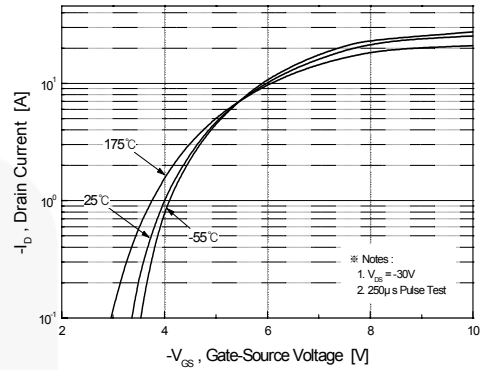


Figure 2. Transfer Characteristics

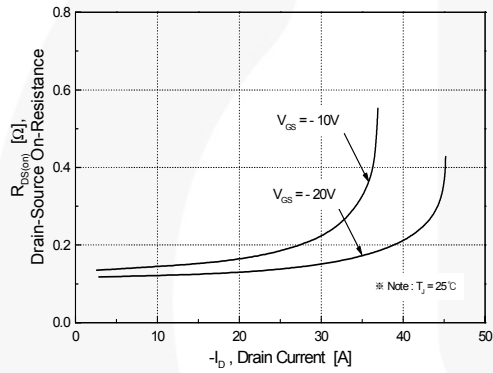


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

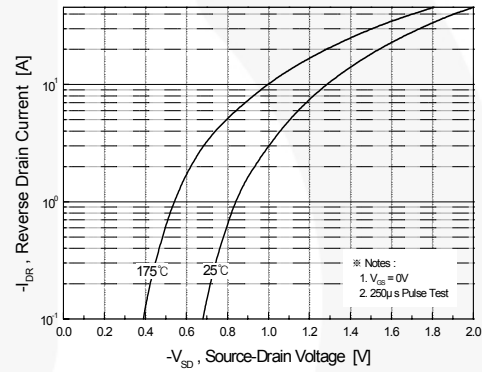


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

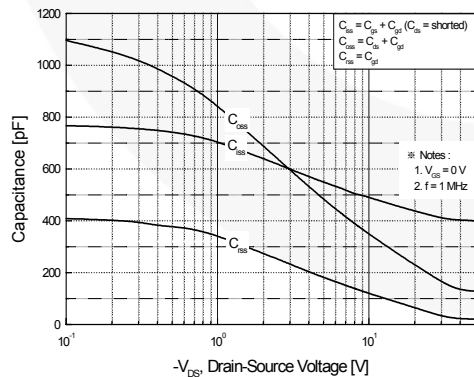


Figure 5. Capacitance Characteristics

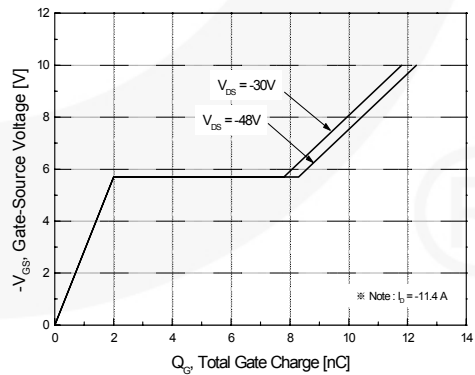
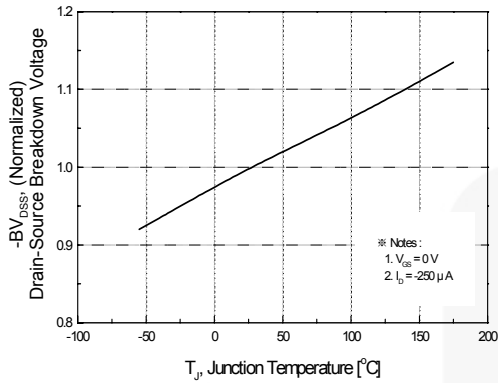
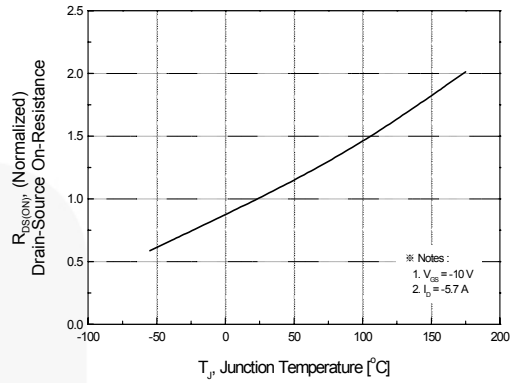


Figure 6. Gate Charge Characteristics

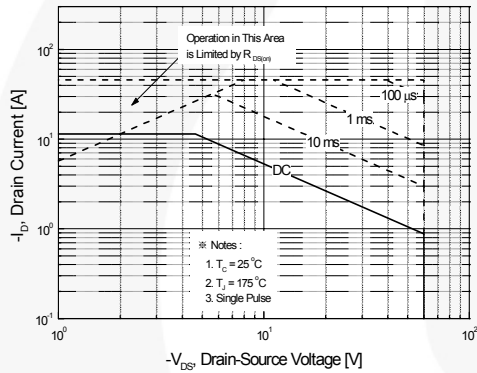
**Typical Characteristics** (Continued)



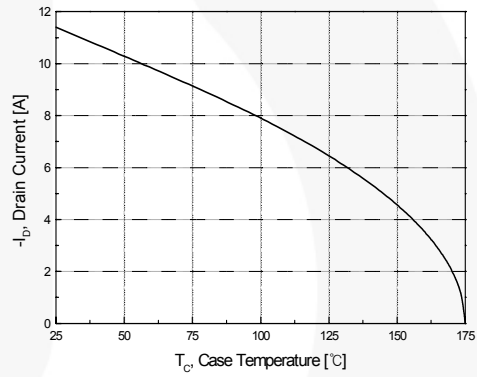
**Figure 7. Breakdown Voltage Variation vs. Temperature**



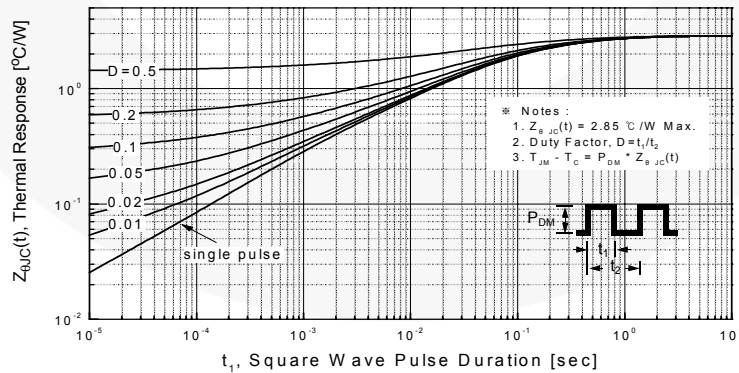
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

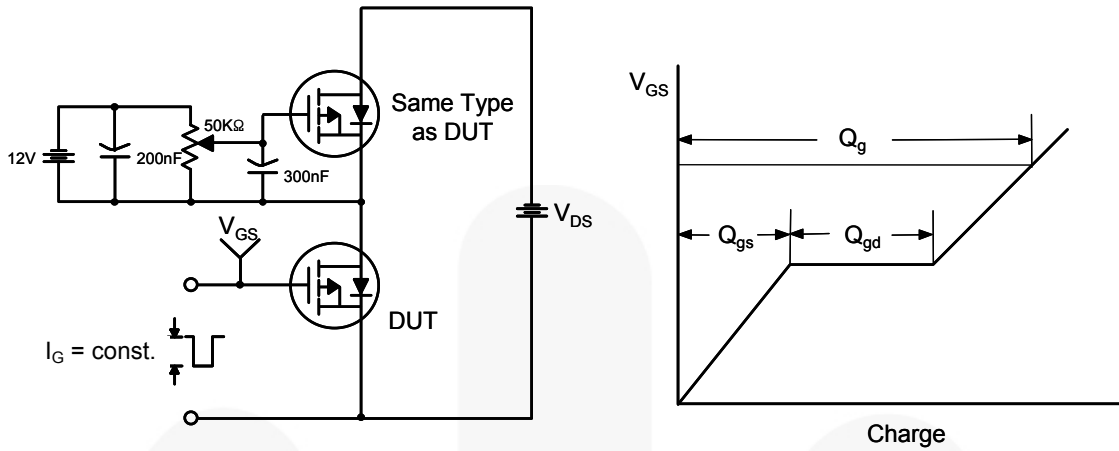


Figure 12. Gate Charge Test Circuit & Waveform

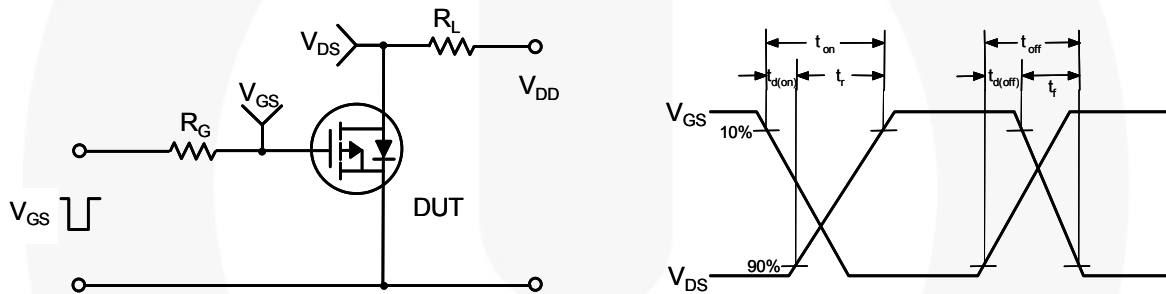


Figure 13. Resistive Switching Test Circuit & Waveforms

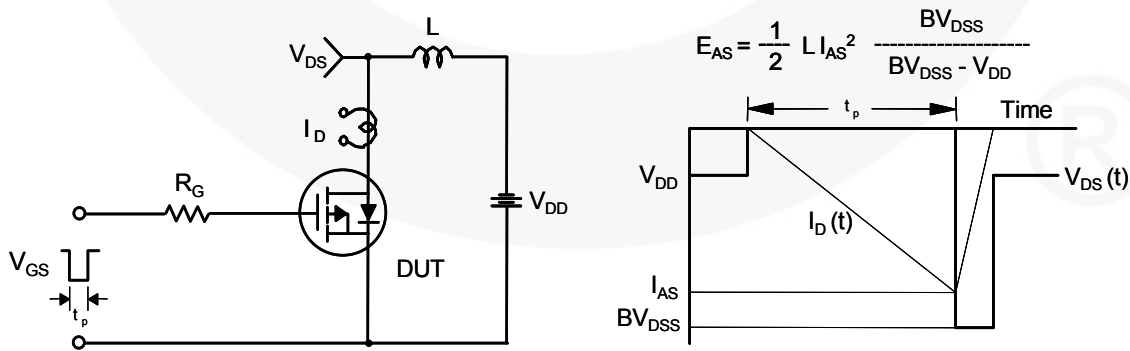


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

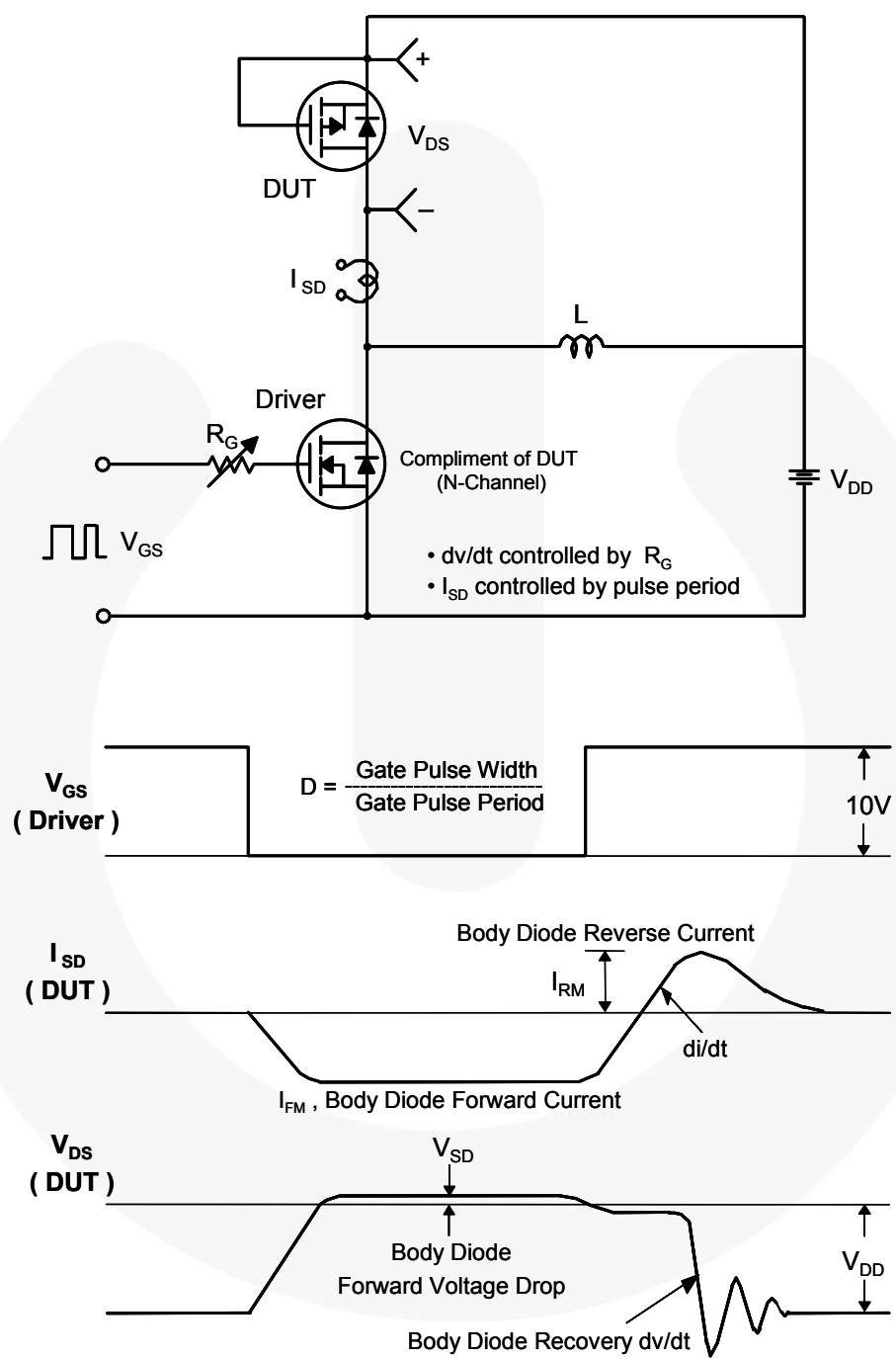
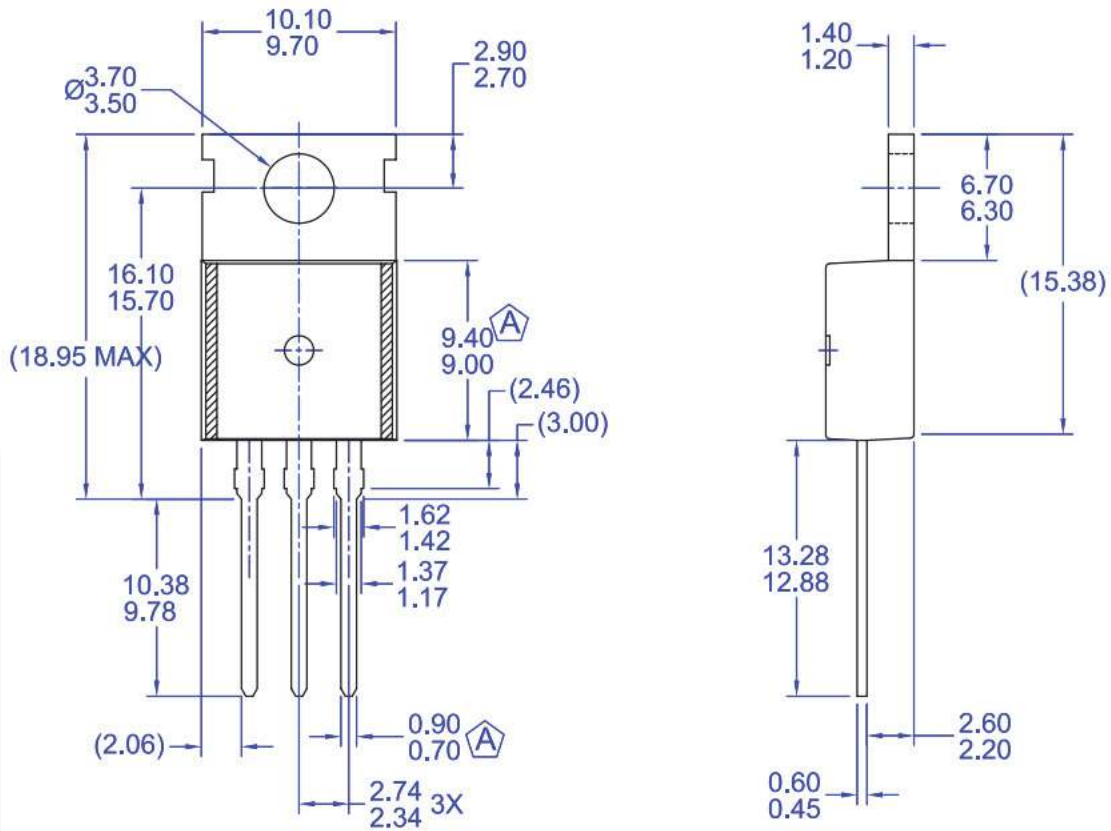


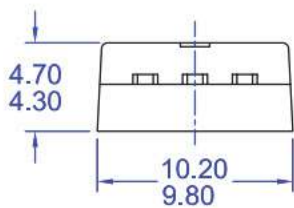
Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



### NOTES:

- A) CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DRAWING FILE/REVISION: MKT-TO220Y03REV1



**Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB**

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