# System Clock Chip for ATI RS480

**Recommended Application:**
ATI RS480 systems using AMD K8 processors

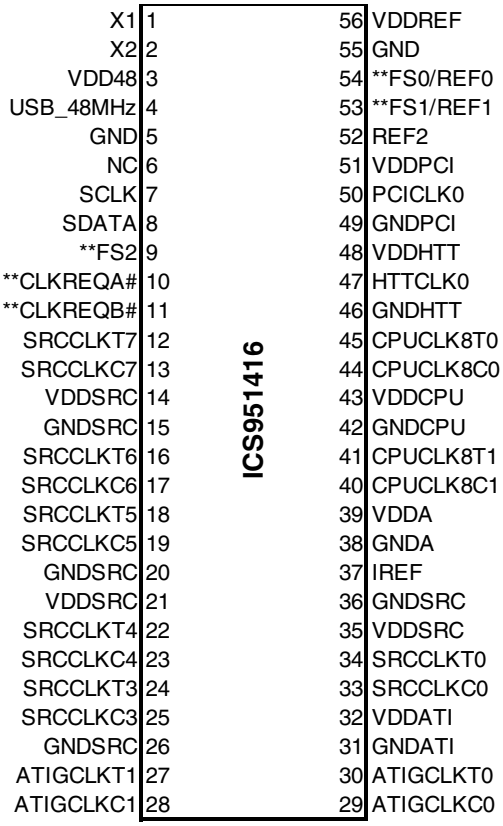
**Output Features:**

- 3 - 14.318 MHz REF clocks
- 1 - USB_48MHz USB clock
- 1 - HyperTransport 66 MHz clock seed
- 1 - PCI 33 MHz clock seed
- 2 - Pairs of AMD K8 clocks
- 6 - Pairs of SRC/PCI Express* clocks
- 2 - Pairs of ATIG (SRC/PCI Express) clocks

**Features:**

- 2 - Programmable Clock Request pins for SRC clocks
- ATIGCLKS are programmable for frequency
- Spread Spectrum for EMI reduction
- Outputs may be disabled via SMBus
- External crystal lead capacitors for maximum frequency accuracy

## Pin Configuration




**Note:** Pins preceeded by '**' have a 120 Kohm Internal Pull Down resistor

**56 Pin SSOP/TSSOP**

## Power Groups

| Pin Number | | Description |
|---|---|---|
| VDD | GND | |
| 56 | 55 | Xtal, REF |
| 51 | 49 | PCICLK output |
| 48 | 46 | HTTCLK output |
| 43 | 42 | CPU Outputs |
| 14, 21, 32,35 | 15, 20, 26,31,36 | SRC outputs |
| 39 | 38 | Analog, CPU PLL |
| 3 | 5 | USB_48MHz output |

## Functionality

| FS2 | FS1 | FS0 | CPU | HTT | PCI |
|---|---|---|---|---|---|
| | | | MHz | MHz | MHz |
| 0 | 0 | 0 | Hi-Z | Hi-Z | Hi-Z |
| 0 | 0 | 1 | X | X/3 | X/6 |
| 0 | 1 | 0 | 180.00 | 60.00 | 30.00 |
| 0 | 1 | 1 | 220.00 | 73.12 | 36.56 |
| 1 | 0 | 0 | 100.00 | 66.66 | 33.33 |
| 1 | 0 | 1 | 133.33 | 66.66 | 33.33 |
| 1 | 1 | 1 | 200.00 | 66.66 | 33.33 |



*Other names and brands may be claimed as the property of others.

## Pin Descriptions

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 2 | X2 | OUT | Crystal output, Nominally 14.318MHz |
| 3 | VDD48 | PWR | Power pin for the 48MHz output.3.3V |
| 4 | USB_48MHz | OUT | 48.00MHz USB clock |
| 5 | GND | PWR | Ground pin. |
| 6 | NC | N/A | No Connection. |
| 7 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 8 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 9 | **FS2 | IN | Frequency select pin. |
| 10 | **CLKREQA# | IN | Output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled.<br>0 = enabled, 1 = tri-stated |
| 11 | **CLKREQB# | IN | Output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled.<br>0 = enabled, 1 = tri-stated |
| 12 | SRCCLKT7 | OUT | True clock of differential SRC clock pair. |
| 13 | SRCCLKC7 | OUT | Complement clock of differential SRC clock pair. |
| 14 | VDDSRC | PWR | Supply for SRC clocks, 3.3V nominal |
| 15 | GNDSRC | PWR | Ground pin for the SRC outputs |
| 16 | SRCCLKT6 | OUT | True clock of differential SRC clock pair. |
| 17 | SRCCLKC6 | OUT | Complement clock of differential SRC clock pair. |
| 18 | SRCCLKT5 | OUT | True clock of differential SRC clock pair. |
| 19 | SRCCLKC5 | OUT | Complement clock of differential SRC clock pair. |
| 20 | GNDSRC | PWR | Ground pin for the SRC outputs |
| 21 | VDDSRC | PWR | Supply for SRC clocks, 3.3V nominal |
| 22 | SRCCLKT4 | OUT | True clock of differential SRC clock pair. |
| 23 | SRCCLKC4 | OUT | Complement clock of differential SRC clock pair. |
| 24 | SRCCLKT3 | OUT | True clock of differential SRC clock pair. |
| 25 | SRCCLKC3 | OUT | Complement clock of differential SRC clock pair. |
| 26 | GNDSRC | PWR | Ground pin for the SRC outputs |
| 27 | ATIGCLKT1 | OUT | True clock of differential SRC clock pair. |
| 28 | ATIGCLKC1 | OUT | Complementary clock of differential SRC clock pair. |

## Pin Descriptions (Continued)

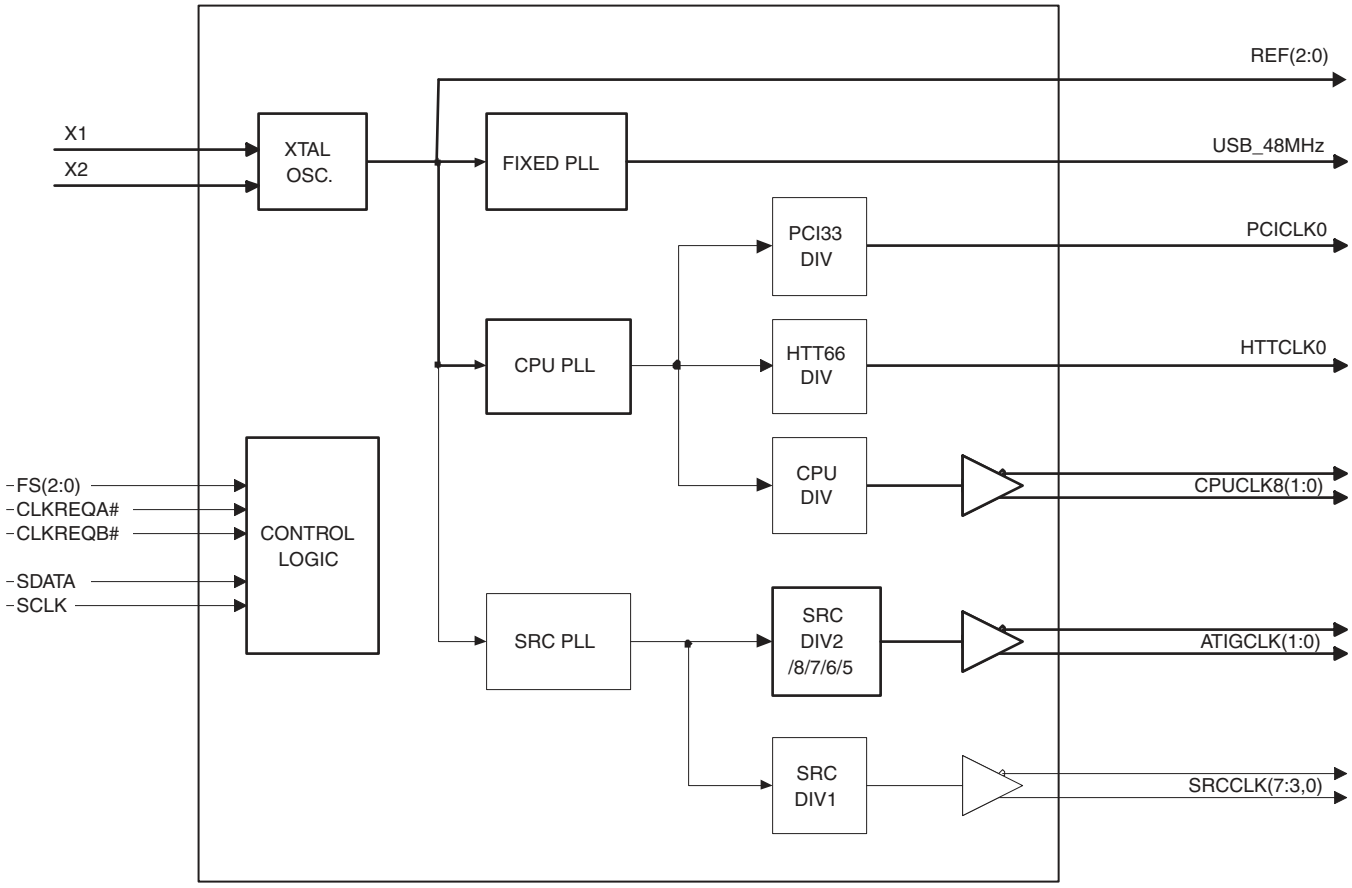
| PIN # | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 29 | ATIGCLKC0 | OUT | Complementary clock of differential SRC clock pair. |
| 30 | ATIGCLKT0 | OUT | True clock of differential SRC clock pair. |
| 31 | GNDATI | PWR | Ground for ATI Gclocks, nominal 3.3V |
| 32 | VDDATI | PWR | Power supply ATI Gclocks, nominal 3.3V |
| 33 | SRCCLKC0 | OUT | Complement clock of differential SRC clock pair. |
| 34 | SRCCLKT0 | OUT | True clock of differential SRC clock pair. |
| 35 | VDDSRC | PWR | Supply for SRC clocks, 3.3V nominal |
| 36 | GNDSRC | PWR | Ground pin for the SRC outputs |
| 37 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 38 | GNDA | PWR | Ground pin for the PLL core. |
| 39 | VDDA | PWR | 3.3V power for the PLL core. |
| 40 | CPUCLK8C1 | OUT | Complementary clock of differential 3.3V push-pull K8 pair. |
| 41 | CPUCLK8T1 | OUT | True clock of differential 3.3V push-pull K8 pair. |
| 42 | GNDCPU | PWR | Ground pin for the CPU outputs |
| 43 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 44 | CPUCLK8C0 | OUT | Complementary clock of differential 3.3V push-pull K8 pair. |
| 45 | CPUCLK8T0 | OUT | True clock of differential 3.3V push-pull K8 pair. |
| 46 | GNDHTT | PWR | Ground pin for the HTT outputs |
| 47 | HTTCLK0 | OUT | 3.3V Hyper Transport output |
| 48 | VDDHTT | PWR | Supply for HTT clocks, nominal 3.3V. |
| 49 | GNDPCI | PWR | Ground pin for the PCI outputs |
| 50 | PCICLK0 | OUT | PCI clock output. |
| 51 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 52 | REF2 | OUT | 14.318 MHz reference clock. |
| 53 | **FS1/REF1 | I/O | Frequency select latch input pin / 14.318 MHz reference clock. |
| 54 | **FS0/REF0 | I/O | Frequency select latch input pin / 14.318 MHz reference clock. |
| 55 | GND | PWR | Ground pin. |
| 56 | VDDREF | PWR | Ref, XTAL power supply, nominal 3.3V |

## General Description

The **ICS951416** is a main clock synthesizer chip that provides all clocks required for ATI RS480-based systems.

An SMBus interface allows full control of the device.

## Block Diagram



# General SMBus serial interface information

## How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

## How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 $_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X $_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

**Index Block Write Operation**

| Controller (Host) | | | ICS (Slave/Receiver) |
|---|---|---|---|
| T | starT bit | | |
| Slave Address D2$_{(H)}$ | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| | ○ | | |
| | ○ | | ○ |
| | ○ | | ○ |
| | | | ○ |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

**Index Block Read Operation**

| Controller (Host) | | | ICS (Slave/Receiver) |
|---|---|---|---|
| T | starT bit | | |
| Slave Address D2$_{(H)}$ | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address D3$_{(H)}$ | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count = X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | ○ |
| | ○ | | ○ |
| | ○ | | ○ |
| | ○ | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

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**Table1: CPU Frequency Selection Table**

| CPU FS4 (B0:b4) | CPU FS3 (B0:b3) | Bit2 FS2 | Bit1 FS1 | Bit0 FS0 | CPU (MHz) | HTT66 (MHz) | PCI33 (MHz) | Spread % |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Hi-Z | Hi-Z | Hi-Z | None |
| 0 | 0 | 0 | 0 | 1 | X/6 | X/12 | X/24 | None |
| 0 | 0 | 0 | 1 | 0 | 180.00 | 60.00 | 30.00 | None |
| 0 | 0 | 0 | 1 | 1 | 220.00 | 73.33 | 36.67 | None |
| 0 | 0 | 1 | 0 | 0 | 100.00 | 66.67 | 33.33 | None |
| 0 | 0 | 1 | 0 | 1 | 133.33 | 66.67 | 33.33 | None |
| 0 | 0 | 1 | 1 | 0 | 166.67 | 66.67 | 33.33 | None |
| 0 | 0 | 1 | 1 | 1 | 200.00 | 66.67 | 33.33 | None |
| 0 | 1 | 0 | 0 | 0 | 186.00 | 62.00 | 31.00 | None |
| 0 | 1 | 0 | 0 | 1 | 214.00 | 71.33 | 35.67 | None |
| 0 | 1 | 0 | 1 | 0 | 190.00 | 63.33 | 31.67 | None |
| 0 | 1 | 0 | 1 | 1 | 210.00 | 70.00 | 35.00 | None |
| 0 | 1 | 1 | 0 | 0 | 102.00 | 68.00 | 34.00 | None |
| 0 | 1 | 1 | 0 | 1 | 136.00 | 68.00 | 34.00 | None |
| 0 | 1 | 1 | 1 | 0 | 170.00 | 68.00 | 34.00 | None |
| 0 | 1 | 1 | 1 | 1 | 204.00 | 68.00 | 34.00 | None |
| 1 | 0 | 0 | 0 | 0 | 169.58 | 56.53 | 28.26 | -0.5% |
| 1 | 0 | 0 | 0 | 1 | 229.43 | 76.48 | 38.24 | -0.5% |
| 1 | 0 | 0 | 1 | 0 | 179.55 | 59.85 | 29.93 | -0.5% |
| 1 | 0 | 0 | 1 | 1 | 219.45 | 73.15 | 36.58 | -0.5% |
| 1 | 0 | 1 | 0 | 0 | 99.75 | 66.50 | 33.25 | -0.5% |
| 1 | 0 | 1 | 0 | 1 | 133.00 | 66.50 | 33.25 | -0.5% |
| 1 | 0 | 1 | 1 | 0 | 166.25 | 66.50 | 33.25 | -0.5% |
| 1 | 0 | 1 | 1 | 1 | 199.50 | 66.50 | 33.25 | -0.5% |
| 1 | 1 | 0 | 0 | 0 | 185.54 | 61.85 | 30.92 | -0.5% |
| 1 | 1 | 0 | 0 | 1 | 106.73 | 71.16 | 35.58 | -0.5% |
| 1 | 1 | 0 | 1 | 0 | 189.53 | 63.18 | 31.59 | -0.5% |
| 1 | 1 | 0 | 1 | 1 | 209.48 | 69.83 | 34.91 | -0.5% |
| 1 | 1 | 1 | 0 | 0 | 101.75 | 67.83 | 33.92 | -0.5% |
| 1 | 1 | 1 | 0 | 1 | 135.66 | 67.83 | 33.91 | -0.5% |
| 1 | 1 | 1 | 1 | 0 | 169.58 | 67.83 | 33.92 | -0.5% |
| 1 | 1 | 1 | 1 | 1 | 203.49 | 67.83 | 33.92 | -0.5% |

**Table2: SRC & ATIG Frequency Selection Table**

| Byte 5 | | | | | SRC(7:3,0), ATIG(1:0) (MHz) | Spread % | SRC OverClock |
|---|---|---|---|---|---|---|---|
| Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | | |
| SRC FS4 Spread Enable | SRC FS3 | SRC FS2 | SRC FS1 | SRC FS0 | | | |
| 0 | 0 | 0 | 0 | 0 | 100.00 | 0 | 1.00 |
| 0 | 0 | 0 | 0 | 1 | 100.00 | 0 | 1.00 |
| 0 | 0 | 0 | 1 | 0 | 100.00 | 0 | 1.00 |
| 0 | 0 | 0 | 1 | 1 | 100.00 | 0 | 1.00 |
| 0 | 0 | 1 | 0 | 0 | 101.00 | 0 | 1.01 |
| 0 | 0 | 1 | 0 | 1 | 101.00 | 0 | 1.01 |
| 0 | 0 | 1 | 1 | 0 | 101.00 | 0 | 1.01 |
| 0 | 0 | 1 | 1 | 1 | 101.00 | 0 | 1.01 |
| 0 | 1 | 0 | 0 | 0 | 102.00 | 0 | 1.02 |
| 0 | 1 | 0 | 0 | 1 | 102.00 | 0 | 1.02 |
| 0 | 1 | 0 | 1 | 0 | 102.00 | 0 | 1.02 |
| 0 | 1 | 0 | 1 | 1 | 102.00 | 0 | 1.02 |
| 0 | 1 | 1 | 0 | 0 | 104.00 | 0 | 1.04 |
| 0 | 1 | 1 | 0 | 1 | 104.00 | 0 | 1.04 |
| 0 | 1 | 1 | 1 | 0 | 104.00 | 0 | 1.04 |
| 0 | 1 | 1 | 1 | 1 | 104.00 | 0 | 1.04 |
| 1 | 0 | 0 | 0 | 0 | 99.75 | -0.5% | 1.00 |
| 1 | 0 | 0 | 0 | 1 | 99.75 | -0.5% | 1.00 |
| 1 | 0 | 0 | 1 | 0 | 99.75 | -0.5% | 1.00 |
| 1 | 0 | 0 | 1 | 1 | 99.75 | -0.5% | 1.00 |
| 1 | 0 | 1 | 0 | 0 | 100.74 | -0.5% | 1.01 |
| 1 | 0 | 1 | 0 | 1 | 100.74 | -0.5% | 1.01 |
| 1 | 0 | 1 | 1 | 0 | 100.74 | -0.5% | 1.01 |
| 1 | 0 | 1 | 1 | 1 | 100.74 | -0.5% | 1.01 |
| 1 | 1 | 0 | 0 | 0 | 101.74 | -0.5% | 1.02 |
| 1 | 1 | 0 | 0 | 1 | 101.74 | -0.5% | 1.02 |
| 1 | 1 | 0 | 1 | 0 | 101.74 | -0.5% | 1.02 |
| 1 | 1 | 0 | 1 | 1 | 101.74 | -0.5% | 1.02 |
| 1 | 1 | 1 | 0 | 0 | 103.74 | -0.5% | 1.04 |
| 1 | 1 | 1 | 0 | 1 | 103.74 | -0.5% | 1.04 |
| 1 | 1 | 1 | 1 | 0 | 103.74 | -0.5% | 1.04 |
| 1 | 1 | 1 | 1 | 1 | 103.74 | -0.5% | 1.04 |

**Table 3: CPU Divider Ratios**

| | Divider (3:2) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Divider (1:0) | **Bit** | **00** | | **01** | | **10** | | **11** | **MSB** |
| | **00** | 0000 | **2** | 0100 | **4** | 1000 | **8** | 1100 | **16** |
| | **01** | 0001 | **3** | 0101 | **6** | 1001 | **12** | 1101 | **24** |
| | **10** | 0010 | **5** | 0110 | **10** | 1010 | **20** | 1110 | **40** |
| | **11** | 0011 | **15** | 0111 | **30** | 1011 | **60** | 1111 | **120** |
| | **LSB** | Address | Div | Address | Div | Address | Div | Address | Div |

**Table 4: HTT Divider Ratios**

| | Divider (3:2) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Divider (1:0) | **Bit** | **00** | | **01** | | **10** | | **11** | **MSB** |
| | **00** | 0000 | **4** | 0100 | **8** | 1000 | **16** | 1100 | **32** |
| | **01** | 0001 | **3** | 0101 | **6** | 1001 | **12** | 1101 | **24** |
| | **10** | 0010 | **5** | 0110 | **10** | 1010 | **20** | 1110 | **40** |
| | **11** | 0011 | **15** | 0111 | **30** | 1011 | **60** | 1111 | **120** |
| | **LSB** | Address | Div | Address | Div | Address | Div | Address | Div |

**Table 5: SRC, ATIG Divider Ratios**

| | Divider (3:2) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Divider (1:0) | **Bit** | **00** | | **01** | | **10** | | **11** | **MSB** |
| | **00** | 0000 | **2** | 0100 | **4** | 1000 | **8** | 1100 | **16** |
| | **01** | 0001 | **3** | 0101 | **6** | 1001 | **12** | 1101 | **24** |
| | **10** | 0010 | **5** | 0110 | **10** | 1010 | **20** | 1110 | **40** |
| | **11** | 0011 | **7** | 0111 | **14** | 1011 | **28** | 1111 | **56** |
| | **LSB** | Address | Div | Address | Div | Address | Div | Address | Div |

**Table 6: Group Skews**

| | Parameter | Description | Test Conditions | Skew Window | Unit |
|---|---|---|---|---|---|
| Time Independent | Tsk_CPU_CPU | CPU to CPU Skew | Measured at crossing points of CPUCLKT rising edges | 250 | ps |
| | Tsk_CPU_PCI | CPU to PCI skew | Meastured at crossing point for CPUCLKT and 1.5V for PCI clock | 2000 | ps |
| | Tsk_PCI33-HT66 | PCI33 to HT66 skew | Measured between rising edges at 1.5V | 500 | ps |
| | Tsk_CPU_HT66 | CPU to HT66 skew | Meastured at crossing point for CPUCLKT and 1.5V for HT66 clock | 2000 | ps |
| Time Variant | Tsk_CPU_CPU | CPU to CPU Skew | Measured at crossing points of CPUCLKT rising edges | 200 | ps |
| | Tsk_CPU_PCI | CPU to PCI skew | Meastured at crossing point for CPUCLKT and 1.5V for PCI clock | 200 | ps |
| | Tsk_PCI33-HT66 | PCI33 to HT66 skew | Measured between rising edges at 1.5V | 200 | ps |
| | Tsk_CPU_HT66 | CPU to HT66 skew | Meastured at crossing point for CPUCLKT and 1.5V for HT66 clock | 200 | ps |
| | Tsk_SRC_SRC | SRC to SRC skew | Meastured at crossing point for SRCCLKT | N/A | ps |

**SMBus Table: Frequency Select Register**

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | - | FS Source | Latched Input or SMBus Frequency Select | RW | Latched Inputs | SMBus | 0 |
| **Bit 6** | - | SS_EN | PLL Spread Enable | RW | OFF | ON | 0 |
| **Bit 5** | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| **Bit 4** | - | FS4 | Freq Select Bit 4 | RW | See Table 1: CPU Frequency Selection | | 0 |
| **Bit 3** | - | FS3 | Freq Select Bit 3 | RW | | | 0 |
| **Bit 2** | - | FS2 | Freq Select Bit 2 | RW | | | Latched |
| **Bit 1** | - | FS1 | Freq Select Bit 1 | RW | | | Latched |
| **Bit 0** | - | FS0 | Freq Select Bit 0 | RW | | | Latched |

**Note: Byte 0 Bit 6, Byte 0 Bit 4 and Byte 5 Bit 4 must be set to '1' to fully enable spread.**

**SMBus Table: Output Control Register**

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 50 | PCICLK0 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 6** | 47 | HTTCLK0 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 5** | 4 | USB_48MHz | Output Enable | RW | Disable | Enable | 1 |
| **Bit 4** | 54 | REF0 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 3** | 53 | REF1 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 2** | 52 | REF2 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 1** | 45,44 | CPUCLK8(0) | Output Enable | RW | Disable | Enable | 1 |
| **Bit 0** | 41,40 | CPUCLK8(1) | Output Enable | RW | Disable | Enable | 1 |

**SMBus Table: CLKREQB# Output Control Register**

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 12,13 | REQBSRC7 | CLKREQB# Controls SRC7 | RW | Does not control | Controls | 0 |
| **Bit 6** | 16,17 | REQBSRC6 | CLKREQB# Controls SRC6 | RW | Does not control | Controls | 0 |
| **Bit 5** | 18,19 | REQBSRC5 | CLKREQB# Controls SRC5 | RW | Does not control | Controls | 0 |
| **Bit 4** | 22,23 | REQBSRC4 | CLKREQB# Controls SRC4 | RW | Does not control | Controls | 0 |
| **Bit 3** | 24,25 | REQBSRC3 | CLKREQB# Controls SRC3 | RW | Does not control | Controls | 0 |
| **Bit 2** | - | Reserved | Reserved | RW | Reserved | Reserved | X |
| **Bit 1** | - | Reserved | Reserved | RW | Reserved | Reserved | X |
| **Bit 0** | 34,33 | REQBSRC0 | CLKREQB# Controls SRC0 | RW | Does not control | Controls | 0 |

**SMBus Table: SRCCLK(7:3,0), CLKREQA# Output Control Register**

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 12,13 | SRCCLK7 | Master Output control. Enables or disables output, regardless of CLKREQ# inputs. | RW | Disable | Enable | 1 |
| **Bit 6** | 16,17 | SRCCLK6 | | RW | Disable | Enable | 1 |
| **Bit 5** | 18,19 | SRCCLK5 | | RW | Disable | Enable | 1 |
| **Bit 4** | 22,23 | SRCCLK4 | | RW | Disable | Enable | 1 |
| **Bit 3** | 24,25 | SRCCLK3 | | RW | Disable | Enable | 1 |
| **Bit 2** | 34,33 | SRCCLK0 | | RW | Disable | Enable | 1 |
| **Bit 1** | 24,25 | REQASRC3 | CLKREQA# Controls SRC3 | RW | Does not control | Controls | 0 |
| **Bit 0** | 34,33 | REQASRC0 | CLKREQA# Controls SRC0 | RW | Does not control | Controls | 0 |

**SMBus Table: SRCCLK(3,0), ATIGCLK Output Control Register**

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 12,13 | REQASRC7 | CLKREQA# Controls SRC7 | RW | Does not control | Controls | 0 |
| **Bit 6** | 16,17 | REQASRC6 | CLKREQA# Controls SRC6 | RW | Does not control | Controls | 0 |
| **Bit 5** | 18,19 | REQASRC5 | CLKREQA# Controls SRC5 | RW | Does not control | Controls | 0 |
| **Bit 4** | 22,23 | REQASRC4 | CLKREQA# Controls SRC4 | RW | Does not control | Controls | 0 |
| **Bit 3** | 27,28 | ATIGCLK1 | Output Enable These outputs cannot be controlled by CLKREQ# pins. | RW | Disabled | Enabled | 1 |
| **Bit 2** | 30,29 | ATIGCLK0 | | RW | Disabled | Enabled | 1 |
| **Bit 1** | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| **Bit 0** | 4 | USB_48Str | 48MHz Strength Control | RW | 1X | 2X | 0 |

**Note: Do NOT simultaneously select CLKREQA# and CLKREQB# to control an SRC output. Behavior of the device is undefined under these conditions.**

**SMBus Table: Output Drive and ATIG Frequency Control Register**

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 52 | REF2Str | REF2 Strength Control | RW | 1X | 2X | 0 |
| **Bit 6** | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| **Bit 5** | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| **Bit 4** | - | SRCFS4 SSEN | Freq Select Bit 4 Spread Enable | RW | See Table 2: SRC Frequency Selection | | 0 |
| **Bit 3** | - | SRCFS3 | Freq Select Bit 3 | RW | | | 0 |
| **Bit 2** | - | SRCFS2 | Freq Select Bit 2 | RW | | | 0 |
| **Bit 1** | - | SRCFS1 | Freq Select Bit 1 | RW | | | 0 |
| **Bit 0** | - | SRCFS0 | Freq Select Bit 0 | RW | | | 0 |

**SMBus Table: Device ID Register**

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | DevID 7 | Device ID MSB | R | - | - | 0 |
| Bit 6 | - | DevID 6 | Device ID 6 | R | - | - | 0 |
| Bit 5 | - | DevID 5 | Device ID 5 | R | - | - | 0 |
| Bit 4 | - | DevID 4 | Device ID4 | R | - | - | 1 |
| Bit 3 | - | DevID 3 | Device ID3 | R | - | - | 0 |
| Bit 2 | - | DevID 2 | Device ID2 | R | - | - | 1 |
| Bit 1 | - | DevID 1 | Device ID1 | R | - | - | 1 |
| Bit 0 | - | DevID 0 | Device ID LSB | R | - | - | 0 |

**SMBus Table: Vendor ID Register**

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | RID3 | Revision ID | R | - | - | X |
| Bit 6 | - | RID2 | | R | - | - | X |
| Bit 5 | - | RID1 | | R | - | - | X |
| Bit 4 | - | RID0 | | R | - | - | X |
| Bit 3 | - | VID3 | VENDOR ID (0001 = ICS) | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

**SMBus Table: Byte Count Register**

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | BC7 | Byte Count Programming b(7:0) | RW | Writing to this register will configure how many bytes will be read back, default is 9 bytes. | | 0 |
| Bit 6 | - | BC6 | | RW | | | 0 |
| Bit 5 | - | BC5 | | RW | | | 0 |
| Bit 4 | - | BC4 | | RW | | | 0 |
| Bit 3 | - | BC3 | | RW | | | 1 |
| Bit 2 | - | BC2 | | RW | | | 0 |
| Bit 1 | - | BC1 | | RW | | | 0 |
| Bit 0 | - | BC0 | | RW | | | 1 |

**SMBus Table: WD TimeR Control Register**

| Byte 9 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | WDH_EN | Watchdog Hard Alarm Enable | RW | Disable | Enable | 0 |
| Bit 6 | - | WDS_EN | Watchdog Soft Alarm Enable | RW | Disable | Enable | 0 |
| Bit 5 | - | WD Hard Status | WD Hard Alarm Status | R | Normal | Alarm | X |
| Bit 4 | - | WD Soft Status | WD Soft Alarm Status | R | Normal | Alarm | X |
| Bit 3 | - | WDTCtrl | Watch Dog Time base Control | RW | 290ms Base | 1160ms Base | 0 |
| Bit 2 | - | WD2 | WD Timer Bit 2 | RW | These bits represent X*290ms (or 1.16S) the watchdog timer waits | | 1 |
| Bit 1 | - | WD1 | WD Timer Bit 1 | RW | | | 1 |
| Bit 0 | - | WD0 | WD Timer Bit 0 | RW | | | 1 |

**SMBus Table: M/N Programming & WD Safe Frequency Control Register**

| Byte 10 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | M/N_EN | CPU/SRC M/N Programming Enable | RW | Disable | Enable | 0 |
| Bit 6 | - | Reserved | Reserved | RW | - | - | 0 |
| Bit 5 | - | WD Safe Freq Source | WD Safe Freq Source | RW | B10b(4:0) | Latch Inputs | 0 |
| Bit 4 | - | WD SF4 | Watch Dog Safe Freq Programming bits | RW | Writing to these bit will configure the safe frequency as Byte0 bit (4:0). | | 0 |
| Bit 3 | - | WD SF3 | | RW | | | 0 |
| Bit 2 | - | WD SF2 | | RW | | | 0 |
| Bit 1 | - | WD SF1 | | RW | | | 0 |
| Bit 0 | - | WD SF0 | | RW | | | 0 |

**SMBus Table: CPU Frequency Control Register**

| Byte 11 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divier in Byte 11 and 12 will configure the CPU VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = | | X |
| Bit 6 | - | N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | M Div5 | M Divider Programming bit (5:0) | RW | | | X |
| Bit 4 | - | M Div4 | | RW | | | X |
| Bit 3 | - | M Div3 | | RW | | | X |
| Bit 2 | - | M Div2 | | RW | | | X |
| Bit 1 | - | M Div1 | | RW | | | X |
| Bit 0 | - | M Div0 | | RW | | | X |

**SMBus Table: CPU Frequency Control Register**

| Byte 12 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | N Div7 | N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6) | RW | The decimal representation of M and N Divier in Byte 11 and 12 will configure the CPU VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = | | X |
| Bit 6 | - | N Div6 | | RW | | | X |
| Bit 5 | - | N Div5 | | RW | | | X |
| Bit 4 | - | N Div4 | | RW | | | X |
| Bit 3 | - | N Div3 | | RW | | | X |
| Bit 2 | - | N Div2 | | RW | | | X |
| Bit 1 | - | N Div1 | | RW | | | X |
| Bit 0 | - | N Div0 | | RW | | | X |

**SMBus Table: CPU Spread Spectrum Control Register**

| Byte 13 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | SSP7 | Spread Spectrum Programming bit(7:0) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of CPU | | X |
| Bit 6 | - | SSP6 | | RW | | | X |
| Bit 5 | - | SSP5 | | RW | | | X |
| Bit 4 | - | SSP4 | | RW | | | X |
| Bit 3 | - | SSP3 | | RW | | | X |
| Bit 2 | - | SSP2 | | RW | | | X |
| Bit 1 | - | SSP1 | | RW | | | X |
| Bit 0 | - | SSP0 | | RW | | | X |

**SMBus Table: CPU Spread Spectrum Control Register**

| Byte 14 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 6 | - | SSP14 | Spread Spectrum Programming bit(14:8) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of CPU | | X |
| Bit 5 | - | SSP13 | | RW | | | X |
| Bit 4 | - | SSP12 | | RW | | | X |
| Bit 3 | - | SSP11 | | RW | | | X |
| Bit 2 | - | SSP10 | | RW | | | X |
| Bit 1 | - | SSP9 | | RW | | | X |
| Bit 0 | - | SSP8 | | RW | | | X |

**SMBus Table: SRC Frequency Control Register**

| Byte 15 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divier in Byte 15 and 16 will configure the SRC VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency | | X |
| Bit 6 | - | N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | M Div5 | M Divider Programming bits | RW | | | X |
| Bit 4 | - | M Div4 | | RW | | | X |
| Bit 3 | - | M Div3 | | RW | | | X |
| Bit 2 | - | M Div2 | | RW | | | X |
| Bit 1 | - | M Div1 | | RW | | | X |
| Bit 0 | - | M Div0 | | RW | | | X |

**SMBus Table: SRC Frequency Control Register**

| Byte 16 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | N Div7 | N Divider Programming b(7:0) | RW | The decimal representation of M and N Divier in Byte 15 and 16 will configure the SRC VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = | | X |
| Bit 6 | - | N Div6 | | RW | | | X |
| Bit 5 | - | N Div5 | | RW | | | X |
| Bit 4 | - | N Div4 | | RW | | | X |
| Bit 3 | - | N Div3 | | RW | | | X |
| Bit 2 | - | N Div2 | | RW | | | X |
| Bit 1 | - | N Div1 | | RW | | | X |
| Bit 0 | - | N Div0 | | RW | | | X |

**SMBus Table: SRC Spread Spectrum Control Register**

| Byte 17 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | SSP7 | Spread Spectrum Programming b(7:0) | RW | These Spread Spectrum bits in Byte 17 and 18 will program the spread pecentage of SRC | | X |
| Bit 6 | - | SSP6 | | RW | | | X |
| Bit 5 | - | SSP5 | | RW | | | X |
| Bit 4 | - | SSP4 | | RW | | | X |
| Bit 3 | - | SSP3 | | RW | | | X |
| Bit 2 | - | SSP2 | | RW | | | X |
| Bit 1 | - | SSP1 | | RW | | | X |
| Bit 0 | - | SSP0 | | RW | | | X |

**SMBus Table: SRC Spread Spectrum Control Register**

| Byte 18 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 6 | - | SSP14 | Spread Spectrum Programming b(14:8) | RW | These Spread Spectrum bits in Byte 17 and 18 will program the spread pecentage of SRC | | X |
| Bit 5 | - | SSP13 | | RW | | | X |
| Bit 4 | - | SSP12 | | RW | | | X |
| Bit 3 | - | SSP11 | | RW | | | X |
| Bit 2 | - | SSP10 | | RW | | | X |
| Bit 1 | - | SSP9 | | RW | | | X |
| Bit 0 | - | SSP8 | | RW | | | X |

**SMBus Table: Programmable Output Divider Register**

| Byte 19 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | CPUDiv3 | CPU Divider Ratio Programming Bits | RW | See Table 3: CPU Divider Ratios | | X |
| Bit 6 | - | CPUDiv2 | | RW | | | X |
| Bit 5 | - | CPUDiv1 | | RW | | | X |
| Bit 4 | - | CPUDiv0 | | RW | | | X |
| Bit 3 | - | HTTDiv3 | HTT Divider Ratio Programming Bits (PCI divider is always 2x the HTT divider or 1/2 freq.) | RW | See Table 4: HTT Divider Ratios | | X |
| Bit 2 | - | HTTDiv2 | | RW | | | X |
| Bit 1 | - | HTTDiv1 | | RW | | | X |
| Bit 0 | - | HTTDiv0 | | RW | | | X |

**SMBus Table: Programmable Output Divider Register**

| Byte 20 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | SRC_Div3 | SRC_ Divider Ratio Programming Bits | RW | See Table 5: SRC and ATIG Divider Ratios | | X |
| Bit 6 | - | SRC_Div2 | | RW | | | X |
| Bit 5 | - | SRC_Div1 | | RW | | | X |
| Bit 4 | - | SRC_Div0 | | RW | | | X |
| Bit 3 | - | ATIG_Div3 | ATIG_ Divider Ratio Programming Bits | RW | | | X |
| Bit 2 | - | ATIG_Div2 | | RW | | | X |
| Bit 1 | - | ATIG_Div1 | | RW | | | X |
| Bit 0 | - | ATIG_Div0 | | RW | | | X |

## Absolute Maximum Ratings

Supply Voltage . . . . . 3.8V
Logic Inputs . . . . . GND –0.5 V to $V_{DD}$ +3.8 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C
ESD Protection . . . . . Input ESD protection usung human body model > 1KV

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A$ = 0 - 70°C; Supply Voltage $V_{DD}$ = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | 3.3 V +/-5% | 2 | | $V_{DD}$ + 0.3 | V | 1 |
| Input Low Voltage | $V_{IL}$ | 3.3 V +/-5% | $V_{SS}$ - 0.3 | | 0.8 | V | 1 |
| Input High Current | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ | -5 | | 5 | uA | 1 |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0 V; Inputs with no pull-up resistors | -5 | | | uA | 1 |
| | $I_{IL2}$ | $V_{IN}$ = 0 V; Inputs with pull-up resistors | -200 | | | uA | 1 |
| Operating Current | $I_{DD3.3OP}$ | all outputs driven | | | 300 | mA | |
| Input Frequency[3] | $F_i$ | $V_{DD}$ = 3.3 V | | 14.31818 | | MHz | 3 |
| Pin Inductance[1] | $L_{pin}$ | | | | 7 | nH | 1 |
| Input Capacitance[1] | $C_{IN}$ | Logic Inputs | | | 5 | pF | 1 |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF | 1 |
| | $C_{INX}$ | X1 & X2 pins | | | 5 | pF | 1 |
| Clk Stabilization[1,2] | $T_{STAB}$ | From $V_{DD}$ Power-Up or de-assertion of PD# to 1st clock | | | 3 | ms | 1,2 |
| Modulation Frequency | | Triangular Modulation | 30 | | 33 | kHz | 1 |
| SMBus Voltage | $V_{DD}$ | | 2.7 | | 5.5 | V | 1 |
| Low-level Output Voltage | $V_{OL}$ | @ $I_{PULLUP}$ | | | 0.4 | V | 1 |
| Current sinking at $V_{OL}$ = 0.4 V | $I_{PULLUP}$ | | 4 | | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time[3] | $T_{RI2C}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time[3] | $T_{FI2C}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3] Input frequency should be measured at the REFOUT pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

## Electrical Characteristics - K8 Push Pull Differential Pair

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ =AMD64 Processor Test Load

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Rising Edge Rate | $\delta V/\delta t$ | Measured at the AMD64 processor's test load. 0 V +/- 400 mV (differential measurement) | 2 | | 10 | V/ns | 1 |
| Falling Edge Rate | $\delta V/\delta t$ | | 2 | | 10 | V/ns | 1 |
| Differential Voltage | $V_{DIFF}$ | Measured at the AMD64 processor's test load. (single-ended measurement) | 0.4 | 1.25 | 2.3 | V | 1 |
| Change in $V_{DIFF\_DC}$ Magnitude | $\Delta V_{DIFF}$ | | -150 | | 150 | mV | 1 |
| Common Mode Voltage | $V_{CM}$ | | 1.05 | 1.25 | 1.45 | V | 1 |
| Change in Common Mode Voltage | $\Delta V_{CM}$ | | -200 | | 200 | mV | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | Measurement from differential wavefrom. Maximum difference of cycle time between 2 adjacent cycles. | 0 | 100 | 200 | ps | 1 |
| Jitter, Accumulated | $t_{ja}$ | Measured using the JIT2 software package with a Tek 7404 scope. TIE (Time Interval Error) measurement technique: Sample resolution = 50 ps, Sample Duration = 10 us | -1000 | | 1000 | | 1,2,3 |
| Duty Cycle | $d_{t3}$ | Measurement from differential wavefrom | 45 | | 53 | % | 1 |
| Output Impedance | $R_{ON}$ | Average value during switching transition. Used for determining series termination value. | 15 | 35 | 55 | Ω | 1 |
| Group Skew | $t_{src-skew}$ | Measurement from differential wavefrom | | | 250 | ps | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All accumulated jitter specifications are guaranteed assuming that REF is at 14.31818MHz

[3] Spread Spectrum is off

## Electrical Characteristics - SRC 0.7V Current Mode Differential Pair

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ =2pF, $R_S$=33.2Ω, $R_P$=49.9Ω, $I_{REF}$ = 475Ω

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Current Source Output Impedance | Zo | $V_O = V_x$ | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal using oscilloscope math function. | 660 | | 850 | mV | 1,3 |
| Voltage Low | VLow | | -150 | | 150 | | 1,3 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | | | | 1 |
| Crossing Voltage (abs) | Vcross(abs) | | 250 | 350 | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vcross | Variation of crossing over all edges | | 12 | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Average period | Tperiod | 75.00 MHz nominal | 8.5684 | 8.5714 | 8.5744 | ns | 2 |
| | | 75.00 MHz spread | 8.5684 | | 8.6244 | ns | 2 |
| | | 100.00 MHz nominal | 9.9970 | 10.0000 | 10.0030 | ns | 2 |
| | | 100.00 MHz spread | 9.9970 | | 10.0530 | ns | 2 |
| | | 116.67 MHz nominal | 13.3303 | 13.3333 | 13.3363 | ns | 2 |
| | | 116.67 MHz spread | 13.3303 | | 13.3863 | ns | 2 |
| | | 133.33 MHz nominal | 7.4972 | 7.5002 | 7.5032 | ns | 2 |
| | | 133.33 MHz spread | 7.4972 | | 7.5532 | ns | 2 |
| Absolute min period | Tabsmin | @100.00MHz nominal/spread | 9.8720 | | | ns | 1,2 |
| Rise Time | $t_r$ | $V_{OL}$ = 0.175V, $V_{OH}$ = 0.525V | 175 | | 700 | ps | 1 |
| Fall Time | $t_f$ | $V_{OH}$ = 0.525V $V_{OL}$ = 0.175V | 175 | | 700 | ps | 1 |
| Rise Time Variation | d-$t_r$ | | | 30 | 125 | ps | 1 |
| Fall Time Variation | d-$t_f$ | | | 30 | 125 | ps | 1 |
| Duty Cycle | $d_{t3}$ | Measurement from differential wavefrom | 45 | | 55 | % | 1 |
| Group Skew | $t_{src-skew}$ | Measurement from differential wavefrom | | | 250 | ps | |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | Measurement from differential wavefrom | | | 100 | ps | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For $R_R$ = 475Ω (1%), $I_{REF}$ = 2.32mA. $I_{OH}$ = 6 x $I_{REF}$ and $V_{OH}$ = 0.7V @ $Z_O$=50Ω.

## Electrical Characteristics - PCI33, HTT66 Clocks

$T_A$ = 0 - 70°C; VDD=3.3V +/-5%; $C_L$ = 30 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| PCI33 Clock period | $T_{period}$ | 33.33MHz output nominal | 29.9910 | | 30.0090 | ns | 2 |
| | | 33.33MHz output spread | 29.9910 | | 30.1598 | ns | 2 |
| HTT66 Clock period | $T_{period}$ | 66.67MHz output nominal | 14.9955 | | 15.0045 | ns | 2 |
| | | 66.67MHz output spread | 14.9955 | | 15.0799 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.55 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$ @MIN = 1.0 V | -33 | | -46 | mA | 1 |
| | | $V_{OH}$@ MAX = 3.135 V | -50 | | -80 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @ MIN = 1.95 V | 47 | | 64 | mA | 1 |
| | | $V_{OL}$ @ MAX = 0.4 V | 58 | | 91 | mA | 1 |
| Edge Rate | δV/δt | Rising edge rate | 1 | | 4 | V/ns | 1 |
| Edge Rate | δV/δt | Falling edge rate | 1 | | 4 | V/ns | 1 |
| Rise Time | $t_{r1}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | | 2 | ns | 1 |
| Fall Time | $t_{f1}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | | 2 | ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | | 55 | % | 1 |
| Skew | $t_{sk1}$ | $V_T$ = 1.5 V | | | 500 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | | 180 | ps | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that REF is at 14.31818MHz

## Electrical Characteristics - 48MHz, USB

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ = 10-20 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -200 | | 200 | ppm | 1,2 |
| Clock period | $T_{period}$ | 48.00MHz output nominal | 20.8257 | | 20.8340 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.55 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$ @ MIN = 1.0 V | -33 | | -46 | mA | 1 |
| | | $V_{OH}$@ MAX = 3.135 V | -50 | | -80 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @MIN = 1.95 V | 47 | | 64 | mA | 1 |
| | | $V_{OL}$ @ MAX = 0.4 V | 58 | | 91 | mA | 1 |
| Edge Rate | δV/δt | Rising edge rate | 1 | | 2 | V/ns | 1 |
| Edge Rate | δV/δt | Falling edge rate | 1 | | 2 | V/ns | 1 |
| Rise Time | $t_{r1}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | 1.43 | 2 | ns | 1 |
| Fall Time | $t_{f1}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | 1.33 | 2 | ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | 48 | 55 | % | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | | 180 | ps | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that REF is at 14.31818MHz

## Electrical Characteristics - REF-14.318MHz

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ = 10-20 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1 |
| Clock period | $T_{period}$ | 14.318MHz output nominal | 69.8270 | | 69.8550 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.4 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$ @MIN = 1.0 V | -29 | | -41 | mA | 1 |
| | | V OH@MAX = 3.135 V | -45 | | -71 | | |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @MIN = 1.95 V | 39 | | 54 | mA | 1 |
| | | VOL @MAX = 0.4 V | 49 | | 77 | | |
| Edge Rate | δV/δt | Rising edge rate | 1 | | 4 | V/ns | 1 |
| Edge Rate | δV/δt | Falling edge rate | 1 | | 4 | V/ns | 1 |
| Rise Time | $t_{r1}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | | 2 | ns | 1 |
| Fall Time | $t_{f1}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | | 2 | ns | 1 |
| Skew | $t_{sk1}$ | $V_T$ = 1.5 V | | | 500 | ps | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | | 55 | % | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | | 700 | ps | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that REF is at 14.31818MHz

| SRC Reference Clock | | | |
|---|---|---|---|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, Route as non -coupled 50 ohm trace. | 0.5 max | inch | 2, 3 |
| L2 length, Route as non -coupled 50 ohm trace. | 0.2 max | inch | 2, 3 |
| L3 length, Route as non -coupled 50 ohm trace. | 0.2 max | inch | 2, 3 |
| Rs | 33 | ohm | 2, 3 |
| Rt | 49.9 | ohm | 2, 3 |

| Down Device Differential Routing | Dimension or Value | Unit | Figure |
|---|---|---|---|
| L4 length, Route as coupled **microstrip** 100 ohm differential trace. | 2 min to 16 max | inch | 2 |
| L4 length, Route as coup led **stripline** 100 ohm differential trace. | 1.8 min to 14.4 max | inch | 2 |

| Differential Routing to PCI Express Connector | Dimension or Value | Unit | Figure |
|---|---|---|---|
| L4 length, Route as coupled **microstrip** 100 ohm differential trace. | 0.25 to 14 max | inch | 3 |
| L4 length, Rout e as coupled **stripline** 100 ohm differential trace. | 0.225 min to 12.6 max | inch | 3 |

Fig.1

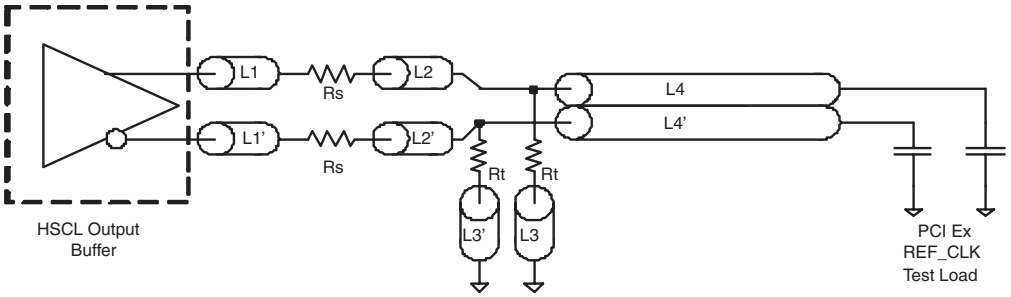



Fig.2

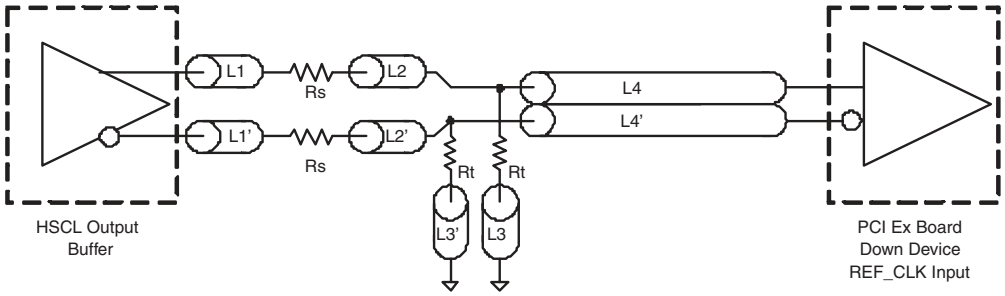
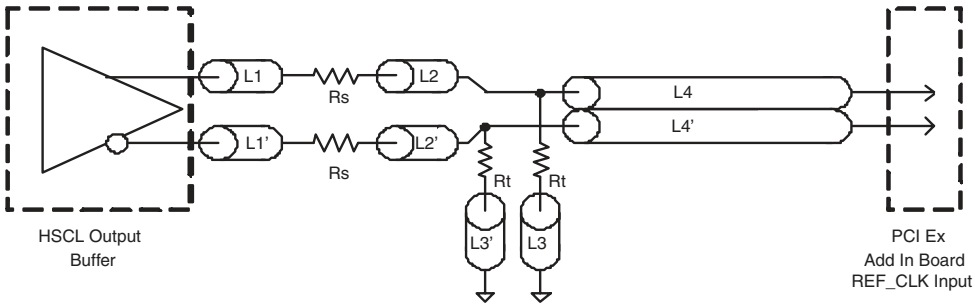



Fig.3



## Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the **ICS951416** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

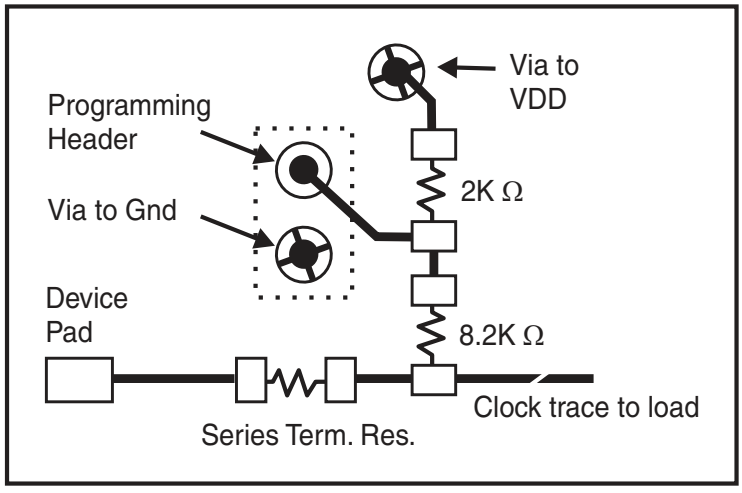
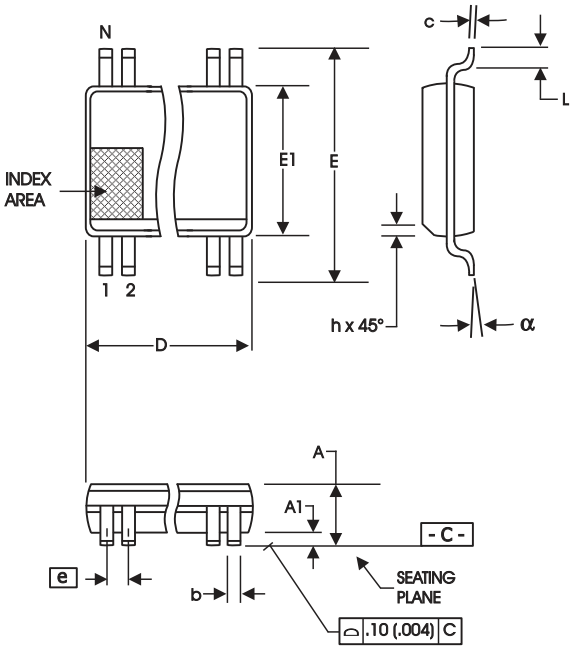



**Fig. 1**




**56-Lead, 300 mil Body, 25 mil, SSOP**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 56 | 18.31 | 18.55 | .720 | .730 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

## Ordering Information

**ICS951416yFLFT**

Example:

**ICS XXXX y F - LF T**

**Designation for tape and reel packaging**
**RoHS Compliant (Optional)**
**Package Type**
F = SSOP
**Revision Designator** (will not correlate with datasheet revision)
**Device Type (consists of 3 to 7 digit numbers)**
**Prefix**
ICS, AV = Standard Device

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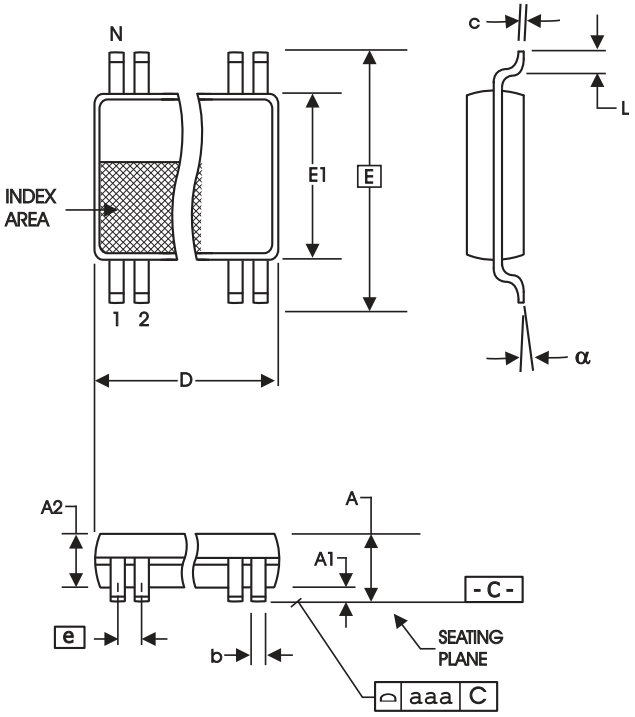


**56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP**
**(240 mil) (20 mil)**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 56 | 13.90 | 14.10 | .547 | .555 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

## Ordering Information

### ICS951416yGLFT

Example:

**ICS XXXX y G - LF T**

**Designation for tape and reel packaging**
**RoHS Compliant (Optional)**
**Package Type**
G = TSSOP
**Revision Designator** (will not correlate with datasheet revision)
**Device Type (consists of 3 to 7 digit numbers)**
**Prefix**
ICS, AV = Standard Device

0937H—05/26/05

## Revision History

| Rev. | Issue Date | Description | Page # |
|---|---|---|---|
| D | 11/11/2004 | Changes Pull Down Symbol from ~ to ** | 1,2,3 |
| E | 12/8/2004 | Update CPU and SRC frequency selection table. | 6,7 |
| F | 4/22/2005 | 1. Updated the Electrical Characteristics for HTT.<br>2. Updated Ordering Information from "Lead Free" to "Annealed Lead Free". | 18,23-24 |
| G | 4/29/2005 | Updated the Electrical Characteristics for REF and USB. | 19, 20 |
| H | 5/26/2005 | 1. Changed Byte 10 bit 7 to "CPU/SRC M/N Programming Bit.<br>2. Updated LF Ordering Information to "RoHS Compliant" | 12, 23-24 |

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