DC to 18 GHz, Ultra Wideband, Dual Rank, 4 GSPS Track-and-Hold Amplifier

Data Sheet **HMC1061LC5**

FEATURES

- 18 GHz input sampling bandwidth (1 V p-p full-scale)
- 4 GSPS maximum sampling rate
- 67 dB SFDR at 4 GHz and 0.5 V p-p input and CLK = 1 GSPS)
- 56 dB SFDR at 4 GHz and 1 V p-p input and CLK = 1 GSPS)
- Direct coupled input/output
- Ultra clean output waveforms, minimal glitching
- ≥65 dB hold mode feedthrough rejection
- 1.45 per specs mV rms hold mode output noise
- 32-terminal ceramic leadless chip carrier, 5 mm × 5 mm

APPLICATIONS

- RF ATE applications
- Digital sampling oscilloscopes
- RF demodulation systems
- Digital receiver systems
- High speed peak detectors
- Software defined radio
- Radar, electronic counter measures (ECM), and electronic intelligence systems
- High speed digital-to-analog converter (DAC) deglitching

FUNCTIONAL BLOCK DIAGRAM

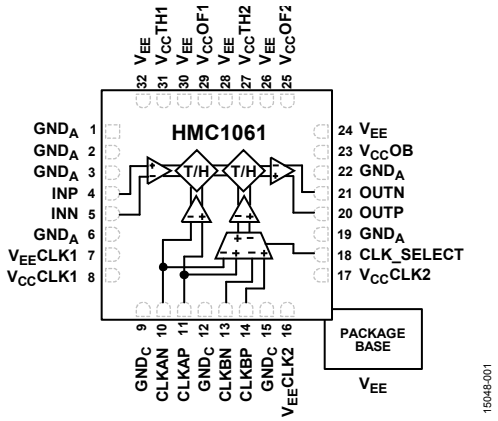

Figure 1.

GENERAL DESCRIPTION

The HMC1061LC5 is a silicon germanium (SiGe), monolithic, fully differential, dual rank, track-and-hold amplifier that provides unprecedented bandwidth and dynamic range performance to wideband sampled signal systems. The track-and-hold amplifier offers precision signal sampling over an 18 GHz bandwidth, with 9-bit to 10-bit linearity from dc to beyond 5 GHz input frequency, 1.45 mV noise, and <70 fs random aperture jitter.

The HMC1061LC5 can be clocked to 4 GSPS with minimal dynamic range loss. The track-and-hold amplifier can be used to expand the bandwidth and/or high frequency linearity of high speed analog to digital conversion and signal acquisition systems. Wideband data acquisition systems with multi GHz required bandwidth for a variety of applications, such as software defined radio, radar systems, electronic warfare (EW), electronic intelligence (ELINT), and automated test equipment (ATE).

Rev. B Document Feedback

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REVISION HISTORY

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

2/2018—Rev. 03.0816 to Rev. B

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C.

Table 1.

Parameter	Test Conditions/Comments	Test Level[1]	Min	Typ	Max	Unit
ANALOG INPUTS (INP, INN)						
Differential Full-Scale Range	Full-scale input for linearity test	I		1		V p-p
Input Resistance	Each lead to ground	III		50		Ω
Return Loss	0 GHz to 12 GHz	III		12.5		dB
	12 GHz to 18 GHz	III		6		dB
Input Common-Mode Voltage		III	−0.1	0	+0.1	V
CLOCK INPUTS (CLKAP, CLKAN, CLKBP, CLKBN)						
DC Differential Clock Voltage						
High		III	20	40	2000	mV
Low		III	−2000	−40	−20	mV
Amplitude (Sinusoidal Input)	Per port	II	−6	0	+10	dBm
Input Common-Mode Voltage		III	−0.5	0	+0.5	V
Clock Slew Rate	Recommended for best linearity	III		2 to 4		V/ns
Return Loss	0 GHz to 3 GHz	III		18		dB
	3 GHz to 6 GHz	III		11		dB
Input Resistance	Each lead to ground	III		50		Ω
ANALOG OUTPUTS (OUTP, OUTN)						
Differential Full-Scale Range		IV		1		V p-p
Common-Mode Output Voltage		IV		0		V
Differential Output Voltage		I	−50	0	+50	mV
Output Impedance	Per port	III		50		Ω
Return Loss	0 GHz to 5 GHz	III		14		dB
TRACK MODE DYNAMICS						
Baseband Gain		I	−2.5	0	+1	dB
Track Mode Bandwidth	At 1 V p-p input	IV		5.1		GHz
HOLD MODE DYNAMICS						
Sampling Bandwidth	At −3 dB gain, 1 V p-p input level	III		18		GHz
Differential Droop Rate (Linear Component)		I		−1.4		%/ns
Differential Droop Rate Magnitude (Fixed Component)		I		4		mV/ns
Feedthrough Rejection	At 3 GHz	III		≥65		dB
Integrated Noise[2]	500 MHz clock frequency	III		1.45		mV rms
Maximum Hold Time						
First Rank		III		2		ns
Second Rank		III		2		ns
Total Maximum Effective Hold Time		III		4		ns
Single Tone at 0.995 GHz	Full-scale input (1 V p-p)[3]	III				
Total Harmonic Distortion (THD)				−54		dB
Spurious-Free Dynamic Range (SFDR)				54		dB
Single Tone at 1.995 GHz	Full-scale input (1 V p-p)[3]	III				
THD				−55		dB
SFDR				55		dB
Single Tone at 2.995 GHz	Full-scale input (1 V p-p)[3]	III				
THD				−54		dB
SFDR				54		dB
Single Tone at 3.995 GHz	Full-scale input (1 V p-p)[3]	I				
THD				−55		dB
SFDR				56		dB

Parameter	Test Conditions/Comments	Test Level[1]	Min	Typ	Max	Unit
Single Tone at 4.995 GHz	Full-scale input (1 V p-p)[3]	III				
THD				−57		dB
SFDR				58		dB
Single Tone at 5.995 GHz	Full-scale input (1 V p-p)[3]	III				
THD				−54		dB
SFDR				55		dB
Single Tone at 7.995 GHz	Full-scale input (1 V p-p)[3]	III				
THD				−43		dB
SFDR				46		dB
Single Tone at 9.995 GHz	Full-scale input (1 V p-p)[3]	III				
THD				−34		dB
SFDR				37		dB
Single Tone at 11.995 GHz	Full-scale input (1 V p-p)[3]	III				
THD				−31		dB
SFDR				32		dB
Single Tone at 13.995 GHz	Full-scale input (1 V p-p)[3]	III				
THD				−26		dB
SFDR				28		dB
Single Tone at 15.995 GHz	Full-scale input (1 V p-p)[3]	III				
THD				−27		dB
SFDR				27		dB
Single Tone at 17.995 GHz	Full-scale input (1 V p-p)[3]	III				
THD				−27		dB
SFDR				28		dB
Single Tone at 0.995 GHz	Half full-scale input (0.5 V p-p)[3]	III				
THD				−66		dB
SFDR				66		dB
Single Tone at 1.995 GHz	Half full-scale input (0.5 V p-p)[3]	III				
THD				−66		dB
SFDR				66		dB
Single Tone at 2.995 GHz	Half full-scale input (0.5 V p-p)[3]	III				
THD				−65		dB
SFDR				66		dB
Single Tone at 3.995 GHz	Half full-scale input (0.5 V p-p)[3]	III				
THD				−65		dB
SFDR				67		dB
Single Tone at 4.995 GHz	Half full-scale input (0.5 V p-p)[3]	III				
THD				−66		dB
SFDR				67		dB
Single Tone at 5.995 GHz	Half full-scale input (0.5 V p-p)[3]	III				
THD				−61		dB
SFDR				61		dB
Single Tone at 7.995 GHz	Half full-scale input (0.5 V p-p)[3]	III				
THD				−51		dB
SFDR				53		dB
Single Tone at 9.995 GHz	Half full-scale input (0.5 V p-p)[3]	III				
THD				−43		dB
SFDR				44		dB
Single Tone at 11.995 GHz	Half full-scale input (0.5 V p-p)[3]	III				
THD				−41		dB
SFDR				44		dB

Parameter	Test Conditions/Comments	Test Level[1]	Min	Typ	Max	Unit
Single Tone at 13.995 GHz	Half full-scale input (0.5 V p-p)[3]	III				
THD				−33		dB
SFDR				34		dB
Single Tone at 15.995 GHz	Half full-scale input (0.5 V p-p)[3]	III				
THD				−36		dB
SFDR				38		dB
Single Tone at 17.995 GHz	Half full-scale input (0.5 V p-p)[3]	III				
THD				−36		dB
SFDR				37		dB
TRACK TO HOLD AND HOLD TO TRACK SWITCHING						
Aperture Delay	Simulated value			−6		ps
Random Aperture Jitter	Full-scale input at 1 GHz[3]	III		<70		fs
Differential Pedestal (Linear Component)						
First Rank	1 GHz clock frequency, 6 dBm clock power	III		−1.0		%
Second Rank	1 GHz clock frequency, 6 dBm clock power	III		0.15		%
Differential Pedestal Magnitude (Fixed Component)						
First Rank		III		2.8		mV
Second Rank		III		1.6		mV
Clock Frequency	At 50% duty cycle	III	250		4000	MHz
Clock Buffer Pipeline Delay	Simulated value			35		ps
Acquisition Time to 1 mV	Simulated value			132		ps
Settling Time to 1 mV	Simulated value			135		ps
Output Buffer Delay (from Second Rank Hold Node to Output)	Simulated value			43		ps
POWER SUPPLY REQUIREMENTS						
V_{CC}TH Voltage (V_{CC}TH1 and V_{CC}TH2)			1.9	2	2.1	V
V_{CC}TH Current (Sum of V_{CC}TH1 and VccTH2)		I		140		mA
V_{CC}OF Voltage (V_{CC}OF1 and V_{CC} OF2)			1.9	2	2.1	V
V_{CC}OF Current (Sum of V_{CC}OF1 and V_{CC}OF2)		I		47		mA
V_{CC}OB Voltage			1.9	2	2.1	V
V_{CC}OB Current		I		74		mA
V_{CC}CLK Voltage (V_{CC}CLK1 and V_{CC}CLK2)			1.9	2	2.1	V
V_{CC}CLK Current (Sum of V_{CC}CLK1 and V_{CC}CLK2)		I		64		mA
V_{EE} Voltage (V_{EE}CLK1, V_{EE}CLK2, V_{EE})			−5	−4.75	−4.5	V
(V_{EE} + V_{EE}CLK) Current		I		−357		mA
Power Consumption		I		2.34		W

[1] See Table 3.
[2] The noise bandwidth is limited by an output amplifier bandwidth of ~7 GHz.
[3] 1 GSPS clock, clock power = 6 dBm per input terminal.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{CC}THx, V_{CC}OFx, and V_{CC}CLKx	2.1 V_{DC}
V_{CC}OB	3 V_{DC}
V_{EE} and V_{EE}CLK	−5.25 V_{DC}
Input Power	
CLKAP, CLKAN, CLKBP, and CLKBN	10 dBm
INP and INN	10 dBm
Junction Temperature	125°C
Continuous Power Dissipation, P_{DISS} (T = 85 °C)	2.5 W
Maximum Peak Reflow Temperature (MSL3)	260°C
Thermal Resistance (Junction to Package Bottom)	16.0°C/W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Electrostatic Discharge (ESD) Sensitivity, Human Body Model (HBM)	Class 1B

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 3. Explanation of Test Levels

Test Level	Description
I	100% production tested at T_A = 25°C.
II	Guaranteed by design and/or characterization testing.
III	Characterization sample tested.
IV	Typical value only.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

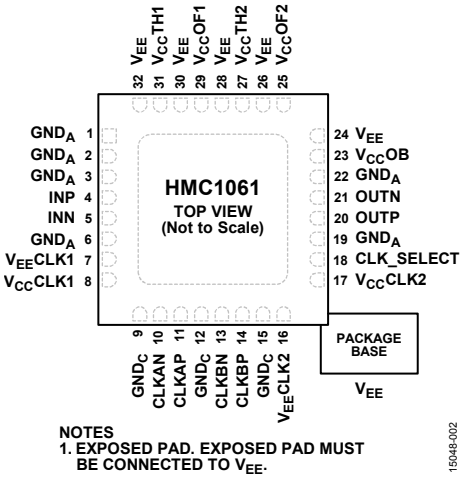

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3, 6, 19, 22	GND_A	Analog Ground. This ground and clock ground must be connected to the same dc potential, but they can be radio frequency (RF) isolated from each other if desired. See Figure 3 for the interface schematic.
4	INP	Positive Differential Signal Input. This input is a dc-coupled, ground referenced input with a nominal common-mode voltage level of 0 V. Input impedance = 50 Ω, full-scale differential voltage = 1 V p-p, and a maximum input level = 10 dBm. See Figure 4 for the interface schematic.
5	INN	Negative Differential Signal Input. This input is a dc-coupled, ground referenced input with a nominal common-mode voltage level = 0 V. Input impedance = 50 Ω, full-scale differential voltage = 1 V p-p, and maximum input level = 10 dBm. See Figure 4 for the interface schematic.
7, 16	$V_{EE}CLK1$, $V_{EE}CLK2$	Negative Clock Buffer V_{EE} Supplies. Nominal voltage = −4.75 V (V_{EE} + V_{EE} CLK1+ V_{EE} CLK2) Current = −357 mA nominal. See Figure 5 for the interface schematic.
8, 17	$V_{CC}CLK1$, $V_{CC}CLK2$	Positive Clock Buffer V_{CC} Supplies. Nominal voltage = 2 V (V_{cc}CLK1 + V_{cc}CLK2). See Figure 5 for the interface schematic.
9, 12, 15	GND_C	Clock Ground. Clock ground and analog ground must be connected to the same dc potential but they can be RF isolated from each other. See Figure 6 for the interface schematic.
10, 11	CLKAN, CLKAP	Differential Clock A Input (Negative and Positive). These pins provide the clock to first rank device. These pins also provide a properly timed clock to the second rank device when CLK_SELECT = 0 V. These inputs are dc-coupled, ground referenced inputs with nominal common mode level of 0 V. Input impedance = 50 Ω. First rank track mode: differential clock positive. First rank hold mode: differential clock negative. Maximum input level = 10 dBm. See Figure 7 for the interface schematic.
13, 14	CLKBN, CLKBP	Differential Clock B Input (Negative And Positive). These pins provide the clock to the second rank device if CLK_SELECT = −4.75 V. These pins are dc-coupled, ground referenced inputs with a nominal common-mode voltage level of 0 V. Input impedance = 50 Ω. Terminated if unused. Second rank track mode: differential clock negative. Second rank hold mode: differential clock positive. Maximum input level = 10 dBm. See Figure 7 for the interface schematic.
18	CLK_SELECT	Clock Mode Select Terminal. Nominal 0 V for Internal Clock B mode, current = 230 µA (nominal). Nominal −4.75 V for external clock B mode, current = −230 µA (nominal). See Figure 8 for the interface schematic.
20, 21	OUTP, OUTN	Differential Output (Positive And Negative). These outputs are dc-coupled, ground referenced outputs with a nominal common-mode voltage level of 0 V. Output impedance = 50 Ω. Intended to be dc or ac coupled to 50 Ω load impedance. See Figure 9 for the interface schematic.
23	$V_{CC}OB$	Positive V_{CC} Supply for the 50 Ω Output Buffer. Nominal voltage = 2 V, current = 74 mA (nominal). This pin can be biased with 1 < $V_{CC}OB$ < 3 V to adjust the output common-mode voltage to an exact desired value between −0.5 V and +0.5 V. Output common-mode voltage adjustment has a sensitivity of approximately V_{OCM} (V) ~ 0.5 ($V_{CC}OB$ − 2). See Figure 11 for the interface schematic.
24, 26, 28, 30, 32	V_{EE}	Negative V_{EE} Supply. Nominal voltage = −4.75 V (V_{EE} + V_{EE}CLK1+ V_{EE}CLK2), current = −357 mA (nominal). See Figure 10 for the interface schematic.

Pin No.	Mnemonic	Description
25, 29	$V_{CC}OF2$, $V_{CC}OF1$	Positive V_{CC} Supplies for the Front End of the Output Buffer Circuitry. $V_{CC}OF2$ is for the output of the IC, while $V_{CC}OF1$ is for the interstage buffer between the first and second rank track-and-hold amplifiers. Nominal voltage = 2 V ($V_{CC}OF1 + V_{CC}OF2$), current = 47 mA (nominal). See Figure 11 for the interface schematic.
27, 31	$V_{CC}TH2$, $V_{CC}TH1$	Positive Power Supplies for the Track-and-Hold Amplifier Portions of the HMC1061LC5. $V_{CC}TH2$ is the supply for second rank track-and-hold core circuitry and $V_{CC}TH1$ is the supply for the first rank track-and-hold core circuitry. Nominal voltage = 2 V ($V_{CC}TH1 + V_{CC}TH2$), current = 140 mA (nominal). See Figure 12 for the interface schematic.
EPAD		Exposed Pad. The exposed pad must be connected to V_{EE}.

INTERFACE SCHEMATICS

Figure 3. GND_A Interface Schematic

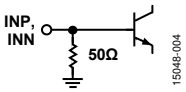

Figure 4. INP and INN Interface Schematic

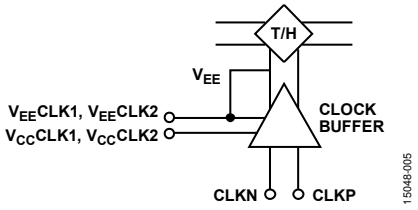

Figure 5. $V_{EE}CLKx$ and $V_{CC}CLKx$ Interface Schematic

Figure 6. GND_C Interface Schematic

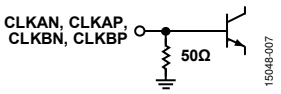

Figure 7. CLKxN and CLKxP Interface Schematic

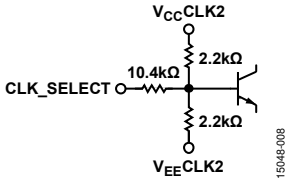

Figure 8. CLK_SELECT Interface Schematic

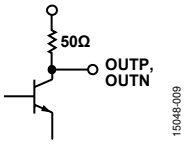

Figure 9. OUTP and OUTN Interface Schematic

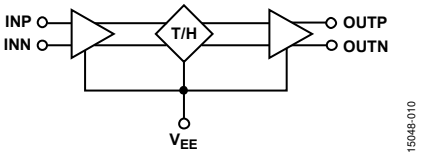

Figure 10. V_{EE} Interface Schematic

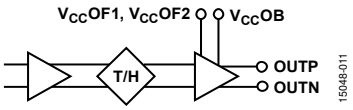

Figure 11. $V_{CC}OF1$, $V_{CC}OF2$, and $V_{CC}OB$ Interface Schematic

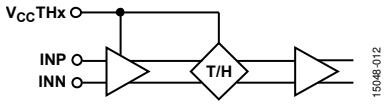

Figure 12. $V_{CC}TH1$ and $V_{CC}TH2$ Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

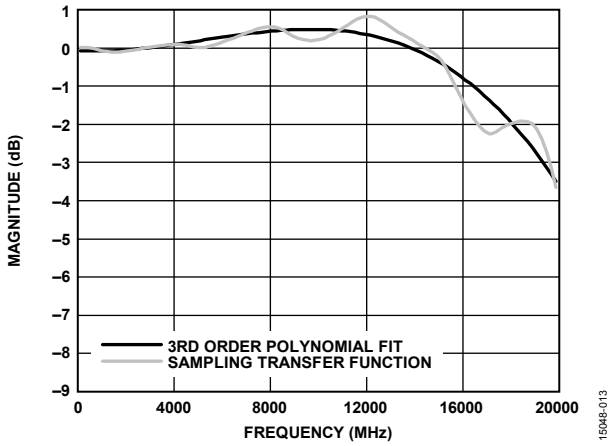

Figure 13. Sampling Transfer Function

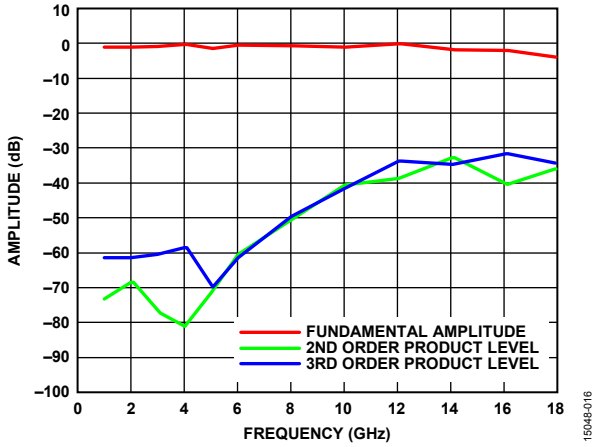

Figure 16. Sampling Transfer Function and Linearity of High Speed Track-and-Hold Analog-to-Digital Converter (ADC) Assembly

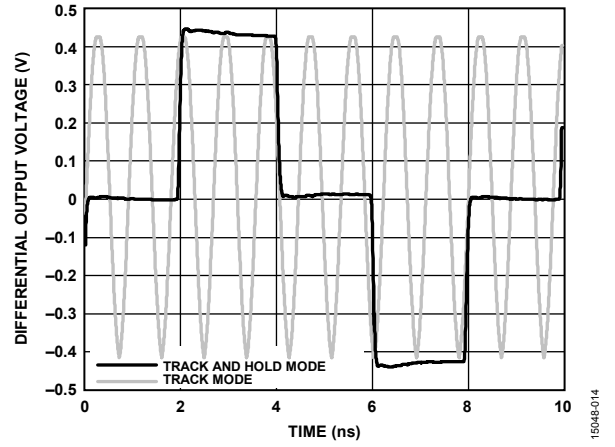

Figure 14. Time Domain Output Waveform at f_{CLK} = 500 MHz, f_{IN} = 1.125 GHz

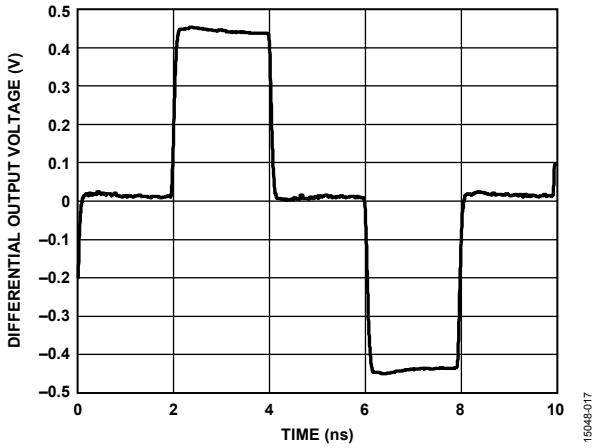

Figure 17. Time Domain Output Waveform at f_{CLK} = 500 MHz, f_{IN} = 10.125 GHz

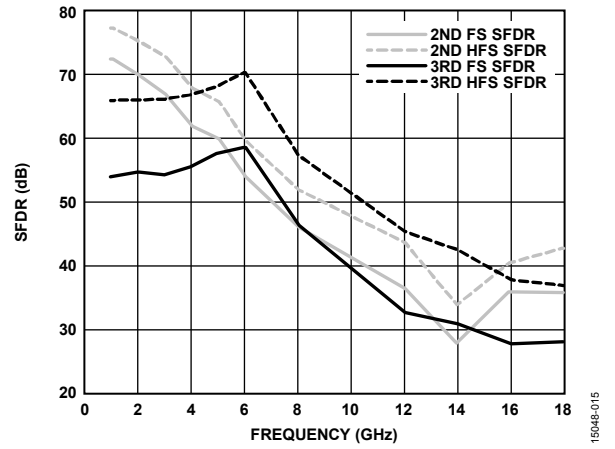

Figure 15. Hold Mode SFDR vs. Frequency and Input Power at f_{CLK} = 500 MHz at 10 dBm, FS = Full-Scale Input Level, HFS = Half-Full-Scale Input Level (Measurement dynamic range for half full-scale and full-scale inputs is about 68 dB and 74 dB, respectively. Due to measurement noise floor limitations; measured spurious products tend to limit at these levels.)

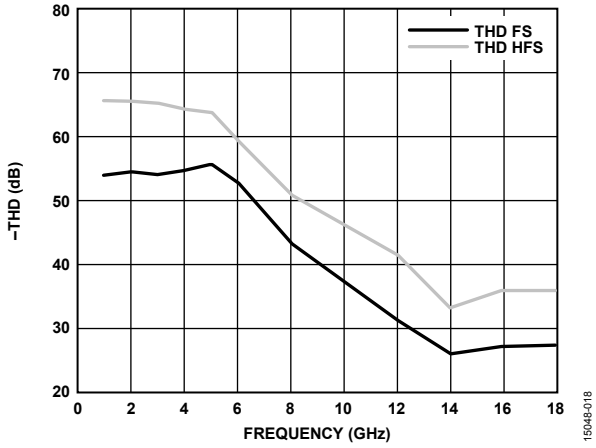

Figure 18. Hold Mode –THD vs. Frequency and Input Power at f_{CLK} = 500 MHz at 10 dBm

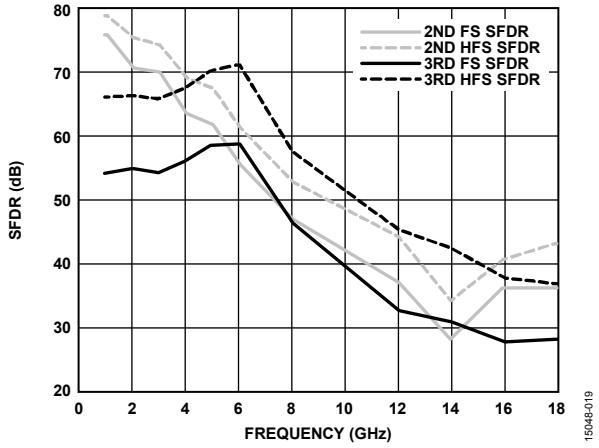

Figure 19. Hold Mode SFDR vs. Frequency and Input Power at f_{CLK} = 1 GHz at 6 dBm

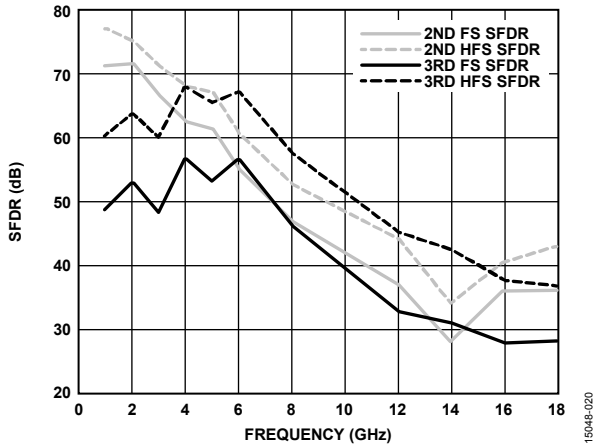

Figure 20. Hold Mode SFDR vs. Frequency and Input Power at f_{CLK} = 2 GHz at 0 dBm

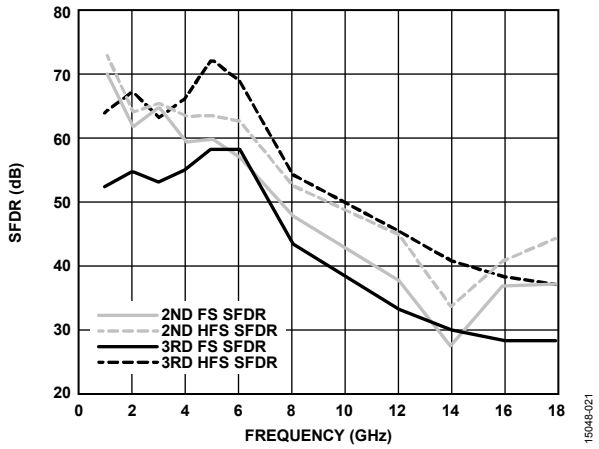

Figure 21. Hold Mode SFDR vs. Frequency and Input Power at f_{CLK} = 3 GHz at 0 dBm

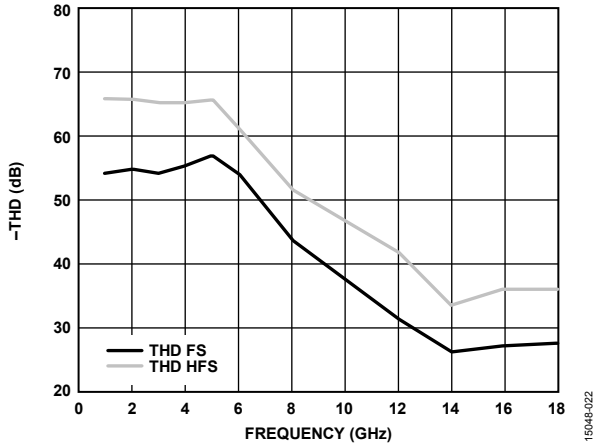

Figure 22. Hold Mode –THD vs. Frequency and Input Power at f_{CLK} = 1 GHz at 6 dBm

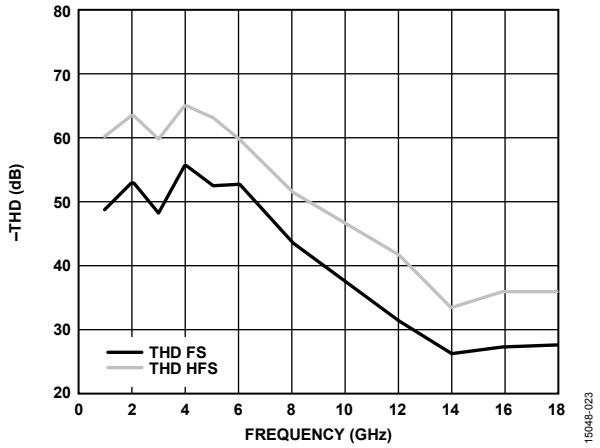

Figure 23. Hold Mode –THD vs. Frequency and Input Power at f_{CLK} = 2 GHz at 0 dBm

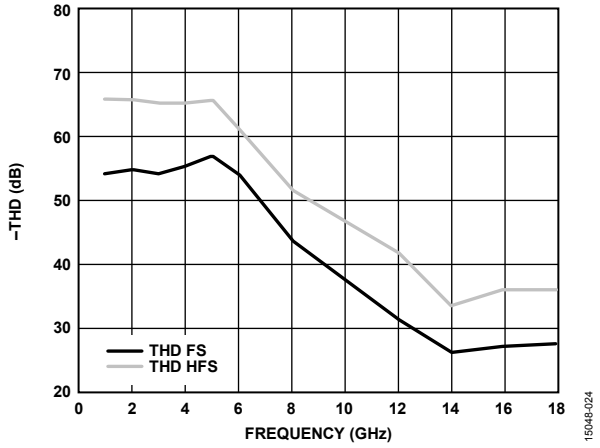

Figure 24. Hold Mode –THD vs. Frequency and Input Power at f_{CLK} = 3 GHz at 0 dBm

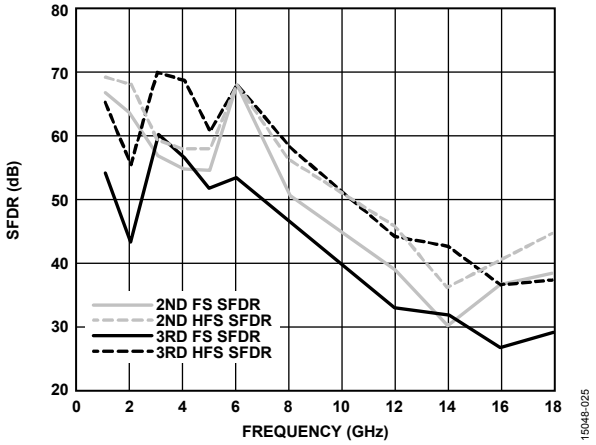

Figure 25. Hold Mode SFDR vs. Frequency and Input Power at f_{CLK} = 4 GHz at 0 dBm

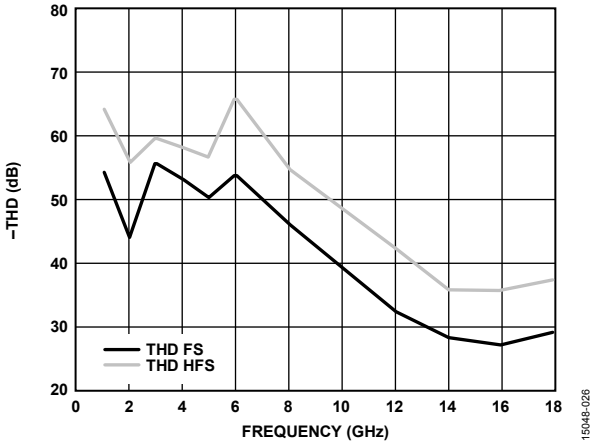

Figure 26. Hold Mode –THD vs. Frequency and Input Power at f_{CLK} = 4 GHz at 0 dBm

TERMINOLOGY

Aperture Delay
Aperture delay is the exact sample time relative to the time that the hold command is applied to the device. Aperture delay is the difference between the delay of the clock switching transition to the hold node and the input signal group delay to the hold node. If the input signal group delay to the hold node exceeds the clock delay, this value is negative.

Aperture Jitter
Aperture jitter is the standard deviation of the sample instant in time.

Acquisition Time
Acquisition time is the interval between the internal hold-to-track transition and the time at which the hold node signal is tracking the input signal within a specified accuracy. Acquisition time does not include the pipeline delay of the clock buffer.

Differential Pedestal
Differential pedestal is a component in the sample value caused by charge redistribution in the track-and-hold switch during the sampling transition. In general, the pedestal can consist of three components: a fixed offset, a component that is linearly related to input signal amplitude, and a component that is nonlinearly related to input signal amplitude. The majority of the pedestal is usually linear. The value of the pedestal (P) can be approximated by

$$P = P_O + P_{LIN} \times V_{IN}$$

where:
P_O is the fixed pedestal component.
P_{LIN} is the linear pedestal component.
V_{IN} is the sampled signal level.

Differential Droop Rate
Differential droop rate is the slow drift in the differential output voltage of a held sample while the track-and-hold amplifier is in hold mode. Differential droop rate is typically caused by current leakage on the hold capacitors and corresponds to a decay in the held voltage with increasing time. The droop can be approximated as the sum of a fixed component and a component that is linearly related to the held sample voltage. The total droop (D) can be approximated by

$$D = D_O + D_{LIN} \times V_{IN}$$

where:
D_O is the fixed component.
D_{LIN} is the linear droop constant.
V_{IN} is the sampled signal level.

The sign of D_O tends to be random so that only the magnitude is specified. Because the droop is mostly linear, it causes little nonlinearity.

Feedthrough Rejection
Feedthrough rejection is the measure of the off state (hold mode) isolation of the track-and-hold internal switch. Feedthrough rejection is defined as the ratio of the amplitude of the output signal (for a sinusoidal input) feeding through during the hold mode to the amplitude of the output signal during track mode. Normalization by the track mode signal gives the true switch isolation without the effects of the output amplifier bandwidth limiting.

Full-Scale Range
Full-scale range is the voltage range between the minimum and maximum signal levels that can be handled by the track-and-hold amplifier while still meeting the device specifications.

Sampling Bandwidth
Sampling bandwidth is the −3 dB bandwidth of the sampled signal levels and is represented by the held sample amplitudes. It includes both the bandwidth of the transfer function from the signal input to the hold node and any band limiting effects associated with the finite time duration of the sampling aperture.

Settling Time
Settling time is the interval between the internal track hold transition and the time at which the held output signal is settled to within a specified accuracy. It does not include the pipeline delay of the clock buffer and does include the group delay of the output amplifier.

Spurious Free Dynamic Range (SFDR)
SFDR is the ratio (usually expressed in dB) between the sinusoidal output signal amplitude and the amplitude of the largest non-linearity product falling within one Nyquist bandwidth. It may be specified for both full-scale input and some fraction(s) of full-scale input. A SFDR based only on second-order nonlinear products is referred to as the second-order SFDR (SFDR2). A SFDR based only on third-order products is referred to as the third-order SFDR (SFDR3).

Total Harmonic Distortion (THD)
THD is the ratio of the total power in the nonlinearity generated harmonics and harmonic (measured in one Nyquist band) to the output signal power.

THEORY OF OPERATION

The HMC1061LC5 ultra wideband, dual rank, track-and-hold amplifier is optimized for use in microwave data conversion applications requiring maximum sampling bandwidth, high linearity over a wide bandwidth, and low noise. A key application of this device is front-end sampling for high speed ADCs to enhance their input bandwidth and/or high frequency linearity. Although several high speed ADCs offer enhanced sample rates, few of them offer input bandwidth beyond a few GHz. In addition, maintenance of good sampling linearity at frequencies beyond the ultrahigh frequency (UHF) band is technologically challenging and most ADC converters suffer rapidly degraded linearity above a 1 GHz or 2 GHz signal frequency. The HMC1061LC5 addresses these limitations with a 18 GHz input bandwidth and excellent broadband linearity. After sampling takes place within the track-and-hold amplifier, the low bandwidth held output waveform can be processed by an ADC with substantially reduced bandwidth. In addition, ADC converter linearity performance limitations at high input frequencies are also mitigated because the settled waveform is processed with the optimal baseband linearity of the ADC converter.

The dual rank track-and-hold amplifier is formed from two cascaded, single rank track-and-hold amplifier that are clocked 180 degrees out of phase such that, while the master Track-and-Hold 1 device (TH1) is holding, the slave Track-and-Hold 2 device (TH2) is tracking, and vice versa. The resulting output waveform consists of two time segments. The first segment consists of the TH1 hold mode as seen through TH2 track mode transfer function. At the beginning of the second time segment, TH2 samples the held TH1 waveform and then continues to hold that value while TH1 switches back to track mode and reacquires and tracks the input waveform. The resulting output waveform provides a held sample value of nearly one complete clock cycle, presenting the downstream ADC with a constant, settled waveform with minimal high frequency spectral content.

The device can be clocked in one of two ways, depending on the voltage applied to the CLK_SELECT terminal. The device can be configured such that the slave track-and-hold amplifier uses an internal clock derived and buffered from the master clock (Clock A). In this case, the CLK_SELECT terminal must be grounded, the user provides Clock A, and the internal clock driving the slave always operates at the same frequency as the master, Clock A. Alternatively, the CLK_SELECT terminal can be connected to the V_{EE} supply, enabling external Clock B control of the slave. In this mode, users must supply both Clock A and Clock B, but have the option of operating the slave at the same frequency or even a different frequency than the master. This mode is useful for decimation operations (where Clock B is a submultiple of the master clock) or other more complex clocking schemes. In all cases, the maximum hold time limits shown in Table 1 must be followed.

ESD

On-chip ESD protection networks are incorporated on the terminals, but the RF or microwave compatible interfaces provide minimal protection and ESD precautions must be used.

POWER SUPPLY SEQUENCING

The recommended power supply start-up sequence is V_{CC}OB, V_{CC}OFx, V_{CC}TH, V_{CC}CLK, and V_{EE}/V_{EE} CLKx if biased from independent supplies. V_{CC}OB, V_{CC}OFx, V_{CC}THx, and V_{CC}CLKx can be connected to one 2 V supply if desired.

INPUT SIGNAL DRIVE

For best results, the inputs must be driven differentially. The input can be driven single-ended, but the linearity of the device degrades. The unused input must be terminated in 50 Ω when driving the device single-ended.

CLOCK INPUT

The first rank device is in track mode when CLKAP – CLKAN is high and it is in hold mode when CLKAP – CLKAN is low. The second rank device has an opposite polarity clock. It is in track mode when CLKBP – CLKBN is low. The clock inputs must be driven differentially if possible. The clock inputs can be driven single-ended if desired, but the single-ended amplitude and slew rate must be similar to the full differential amplitude and slew rate recommended for differential drive. The unused input must be terminated to 50 Ω.

The track-and-hold mode linearity of the device varies somewhat with clock power at lower clock frequencies; this results from a weak dependence of the linearity on clock zero crossing slew rate for slew rates beneath a critical value. For optimal linearity, a clock zero-crossing slew rate of roughly 2 V/ns to 4 V/ns (per clock input) or more is recommended. For sinusoidal clock inputs, 4 V/ns corresponds to a sinusoidal clock power per differential half circuit input of –6 dBm at 4 GHz, 0 dBm at 2 GHz, and 6 dBm at 1 GHz. Regardless of the clock frequency, a minimum clock amplitude of –6 dBm is recommended (per differential half circuit input).

OUTPUTS

The outputs must be sensed differentially for the cleanest output waveforms. The output impedance is 50 Ω resistive returned to the V_{CC}OB supply. The output stage is designed to drive 50 Ω terminated to ground on each differential half circuit output. The HMC1061LC5 offers a true ground referenced common-mode output that is typically within ±50 mV of ground; however, it is possible to adjust the V_{CC}OB power supply slightly to fine tune the output common-mode voltage level to precisely 0 V if desired.

Additionally, the common-mode output level may be adjusted within the range of approximately ±0.5 V by adjusting the $V_{CC}OB$ power supply according to the approximate relation $V_{OCM} = (V_{CC}OB-2) \div 2$ where V_{OCM} is the output common mode voltage and $V_{CC}OB$ can be varied in the range of +1 V < $V_{CC}OB$ < +3 V.

The bandwidth of the output amplifier that buffers the track-and-hold amplifier signal between the hold node and the 50 Ω outputs is approximately 7 GHz. The broad output buffer bandwidth is maintained to support the fast settling times required for users operating at high clock rates. However, because of the broad bandwidth, the output amplifier noise contribution to the total output noise is significant. Users operating at lower clock rates (such as < 1 GHz) may optimize their signal-to-noise ratio (SNR) by filtering the output to a lower bandwidth than the output amplifier bandwidth of 7 GHz. Such an output filter does not reduce the sampled front-end noise (which is frozen into the signal samples and represents the majority of the track-and-hold amplifier noise because of the wide front-end bandwidth) but it can reduce the output amplifier noise contribution. The user can filter the output to the lowest bandwidth that still retains the maximum settling time required to support the chosen clock rate. Typically this optimal bandwidth is of the order of 2 to 3 times the clock rate and it can be realized with a simple single-pole resistor circuit (RC) filter if desired (for example, a shunt capacitance on the outputs). A user operating at a clock rate of 350 MHz with a 1 GHz noise bandwidth output filter can achieve approximately 1 dB lower noise relative to the unfiltered output condition.

The output has very sharp transitions at the clock edges due to the broad output amplifier bandwidth. The user must be aware that any significant length of cable between the chip output and the load causes frequency response roll off and dispersion that can produce low amplitude tails with relatively long time constants in the settling of the output waveform into the load. This effect is most noticeable when operating in a lab setting with output cables of a few feet length, even with high quality cable. Output cables between the track-and-hold amplifier and the load must be of very high quality and 2 feet or less in length.

Reflections between the load and the part degrades the hold mode response. The output cable length can be adjusted to minimize the reflection perturbations to some extent. In general, the round trip transit time of the cable must be an integer number of clock periods to obtain the minimal reflection perturbation in the hold mode portion of the waveform. The optimal performance is obtained when the track-and-hold amplifier is within 50 ps or less of the load since this gives a reflection duration equal to the approximate settling time of the device. In ADC applications, the track-and-hold amplifier must be placed as close as possible to the ADC to minimize reflection effects on the path between the track-and-hold output and the input of the ADC.

LINEARITY MEASUREMENT

When characterizing the linearity of a track-and-hold amplifier, the transfer function linearity of the held samples (referred to as track-and-hold mode linearity) is usually the quantity of most interest to the user. These samples contain the signal information that is ultimately digitized by the downstream ADC. A linearity measurement issue unique to the track-and-hold device is the need for output waveform frequency response correction. In the case of a dual rank track-and-hold amplifier, the output waveform resembles a square wave with duration equal to the clock period. Mathematically, the output can be viewed as the convolution of an ideal delta function sample train with a single square pulse of duration equal to one clock period. This weights the output spectral content with a sin(πf/fs)/(πf/fs)(Sinc) function frequency response envelope which has nulls at harmonics of the clock frequency, fs, and substantial response reduction beyond half the clock frequency. This spectral content and envelope function are observed during spectrum analyzer measurement because the analyzer simply reproduces the entire spectrum of the incoming waveform. However, the spectral content of the held samples without the envelope weighting is required for proper measurement of the linearity, as measured by a downstream ADC converter that samples a time instant in the held waveform. Either the impact of the response envelope must be corrected in the data, or a measurement method must be used that heterodynes the relevant nonlinear harmonic products to low frequencies to avoid significant envelope response weighting. This latter method is referred to as the low frequency beat product technique.

The low frequency beat product technique is commonly used for high speed track-and-hold amplifier linearity measurements, although the measurement does impose restrictions on the specific input signal and clock frequencies that can be used. For example, with a clock frequency of 512.5 MHz, a single-tone input at 995 MHz beats with the second harmonic of the sampling frequency (through the sampling process) to produce a first-order beat product at 30 MHz. Likewise, the second and third harmonics of the input signal (generated via distortion in the track-and-hold amplifier) beat with the fourth and sixth harmonics of the sampling frequency, respectively, to produce second and third-order beat products at 60 MHz and 90 MHz. In this manner, the track-and-hold nonlinearity in the vicinity of 1 GHz can be measured even though the 995 MHz fundamental and the 1.99 GHz and 2.985 GHz nonlinear harmonics are well beyond the 256 MHz 4 dB bandwidth of the sinx/x response envelope.

The possible input frequency choices are overly limited when the low frequency beat product technique is used at high clock rates. A related high frequency beat product measurement using correction for the sinx/x envelope weighting must be employed to measure linearity over a wide range of input frequencies.

Analog Devices, Inc., uses both low frequency and high frequency beat product methods to measure linearity for a wide range of clock and signal frequencies. High frequency beat

product measurement avoids excessive envelope correction error by maintaining all beat products within the 4 dB bandwidth of the sinc function, where the envelope response is stable and easily modeled.

Independent and accurate measurement of linearity in a track-and-hold amplifier waveform (without a downstream ADC to sample a single point on the held waveform) is challenging at these low nonlinearity levels. This challenge is due to the waveform transitions and/or small glitches that can impact the measured spectrum during direct spectrum analyzer measurements of the output waveform (without sampling). These measurement artifacts are worst case at high clock frequencies where a significant fraction of the waveform duration is consumed by transients. It is believed that these measurement artifacts at high clock frequencies contribute to the linearity ripple, which is seen in the plots at higher clock rates. The true linearity is likely represented by the average through these curve variations.

For the same reasons described previously, the linearity characterization of the track-and-hold amplifier waveform via direct spectrum analysis tends to represent a worst case scenario relative to the true linearity obtained by sampling one point on the held waveform as would be obtained during track-and-hold amplifier ADC measurements. This is supported by our track-and-hold amplifier ADC combination measurements documented in this data sheet and in the AN-1472 Application Note, the AN-1474 Application Note, and the AnalogDialogue article, *Radically Extending Bandwidth to Crush the X-Band Frequencies Using a Track-and-Hold Sampling Amplifier and RF ADC*, which discuss substantially better linearity, particularly at low signal frequencies. The measured linearity presented from direct spectrum analysis of the entire track-and-hold amplifier waveform is believed to represent a worst case indication of the true track-and-hold linearity. The AN-1472 Application Note is for the single rank version of the track-and-hold amplifier, the HMC661, upon which the HMC1061LC5 dual rank design is based.

This effect is shown by the track-and-hold amplifier ADC assembly performance data in Figure 16. Figure 16 shows the typical sampling transfer function and linearity obtained by using the HMC1061LC5 as a front-end sampler for a high speed, 12-bit ADC as derived from a breadboard setup using the HMC1061LC5 evaluation board and the ADC reference board operating at 1 GSPS sample rate.

The track-and-hold amplifier is driven with a differentially leveled input signal from 1 GHz to 18 GHz at −1.5 dB full-scale referenced to the track-and-hold amplifier full-scale level of 1 V p-p differential, as shown in Figure 16. The track-and-hold amplifier baseband gain of ~−0.5 dB, combined with the signal loss in the input traces of the ADC evaluation board (1 dB), results in a −1 dBFS input level to the converter, relative to its 0.8 V p-p differential full-scale level. As the data shows in Figure 16, the −3 dB bandwidth of the composite sampling process is 18 GHz as established by the front-end track-and-hold amplifier sampler. Inspection of the second and third-order product levels show that the linearity performance of the composite track-and-hold amplifier ADC assembly is actually better than the performance measured for the track-and-hold amplifier alone with direct spectrum analyzer measurement of the track-and-hold amplifier waveform. This is particularly true at low frequencies where the SFDR is 61 dB to 62 dB vs. the 57 dB that is expected by third-order product limitations at −1.5 dBFS track-and-hold amplifier levels. These differences are due to the additional measurement artifacts introduced by the track-and-hold waveform transitions in direct spectrum analyzer measurement. For this reason, the linearity performance of the track-and-hold amplifier ADC assembly tends to be a better indicator of the true track-and-hold linearity as long as the ADC has a low frequency baseband SFDR several dB higher than the track-and-hold amplifier, such that the track-and-hold amplifier nonlinearity dominates. Due to the relatively high track-and-hold amplifier linearity, typically the condition of track-and-hold amplifier nonlinearity domination can only be met by ADCs with 12 bits or more of resolution.

APPLICATIONS INFORMATION

EVALUATION PRINTED CIRCUIT BOARD (PCB)

The evaluation PCB of the HMC1061LC5 uses RF circuit design techniques. Signal lines must have 50 Ω impedance where as the package ground leads must connect directly to the ground plane similar to that shown in Figure 27.

The package base is internally connected to the V_{EE} and V_{EE}CLKx supply and must be connected to a V_{EE} supply plane for heat sinking. A sufficient number of via holes must be used to connect the top and bottom ground planes to provide good RF grounding. The evaluation circuit board shown in Figure 27 is available from Analog Devices upon request.

Table 5. Bill of Materials for Evaluation PCB EVAL01-HMC1061LC5[1]

Item	Description
J1, J2, J7, J8	SRI K connectors
J3 to J6	SRI SMA connectors
J9	Header, 0.9 inch, 9 pin, through hole
J10	DC pin
C1 to C6, C14	0.01 µF capacitors, 0402 package
C7 to C12	4.7 µF capacitors, tantalum
L1 to L4	Ferrite, 0402, Steward LI0402E300R-10
L5	Ferrite, 1206, Steward HI1206T500R-10
L6	Ferrite, 0603, Steward LI0603E470R-10
R16	0 Ω resistor, 0402 package
U1	HMC1061LC5 track-and-hold amplifier
PCB[2]	600-00176-00 evaluation board
Heatsink	Modified Wakefield 658-35AB (Digi-Key Part Number 345-1066-ND) 1.1 inch (length) × 0.825 inch (width) × 0.35 inch (height)

[1] Reference this number when ordering complete evaluation PCB.
[2] Use the Arlon 25FR or Rogers 4350 for circuit board material.

APPLICATION CIRCUIT FOR THE EVALUATION PCB

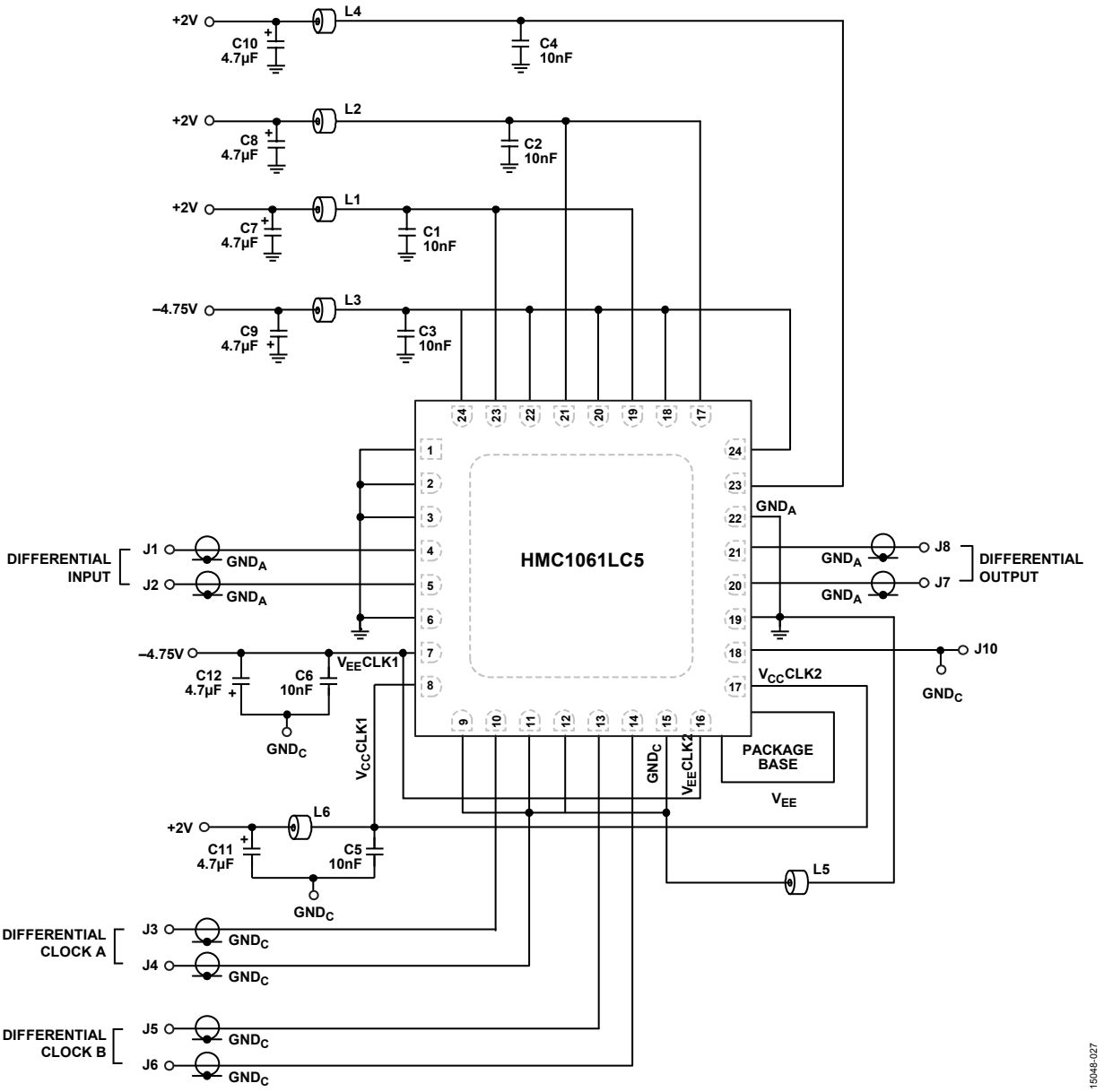

Figure 27. Evaluation Board PCB Application Circuit

OUTLINE DIMENSIONS

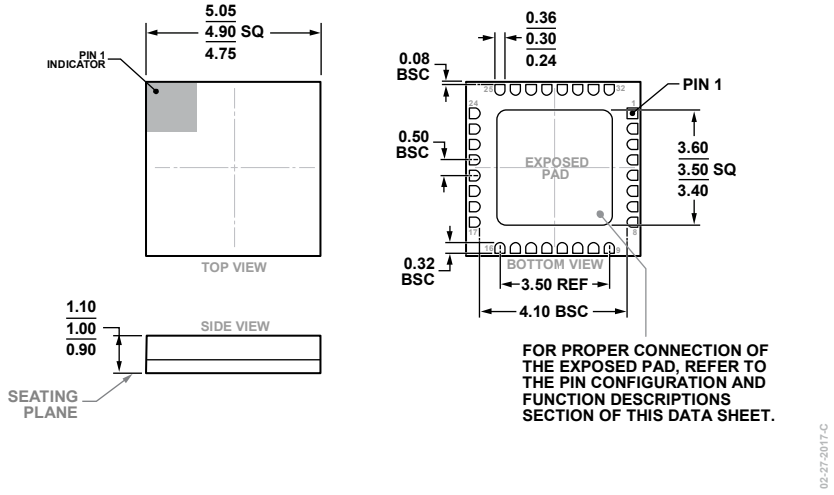

Figure 28. 32-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-32-1)
Dimensions shown in millimeters.

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
HMC1061LC5	−40°C to +85°C	MSL3	32-Terminal Ceramic Leadless Chip Carrier [LCC]	E-32-1
HMC1061LC5TR	−40°C to +85°C	MSL3	32-Terminal Ceramic Leadless Chip Carrier [LCC]	E-32-1
HMC1061LC5TR-R5	−40°C to +85°C	MSL3	32-Terminal Ceramic Leadless Chip Carrier [LCC]	E-32-1
EVAL01-HMC1061LC5			Evaluation Board	

[1] The HMC1061LC5, HMC1061LC5TR, and HMC1061LC5TR-R5 are RoHS Compliant Parts.
[2] See the Absolute Maximum Ratings section.