19-4215; Rev 2; 4/11

EVALUATION KIT AVAILABLE

Programmable, High-Speed, Multiple Input/Output LVDS Crossbar Switches

General Description

The MAX9132/MAX9134/MAX9135 high-speed, multiple-port, low-voltage differential signaling (LVDS) crossbar switches are specially designed for digital video and camera signal transmission. These switches have a wide bandwidth, supporting data rates up to 840Mbps. The MAX9132 has three input ports and two output ports, the MAX9134 has three input ports and four output ports, and the MAX9135 has four input ports and three output ports. The digital video or camera signal can go through the switches from an input port to one or multiple output ports.

The MAX9132/MAX9134/MAX9135 switch routing is programmable through either an I²C interface or a Local Interconnect Network (LIN) serial interface. In addition, the MAX9134/MAX9135 provide pins to set switch routing. These pins also set the initial conditions for the I²C mode. To generate more input or output ports, these switches can be connected in parallel or in cascade.

The MAX9132/MAX9134/MAX9135 operate from a +3.3V supply and are specified over the -40°C to +105°C temperature range. The MAX9134/MAX9135 are available in a 32-pin (5mm x 5mm) TQFP package, while the MAX9132 is available in a 20-pin (6.5mm x 4.4mm) TSSOP package. The input/output port pins are rated up to ±25kV ESD for the ISO Air-Gap Discharge Model, ±15kV ESD for the IEC Air-Gap Discharge Model, and ±10kV for the ESD Contact Discharge Model. All other pins support up to ±3kV ESD for the Human Body Model.

Applications

Digital Video in Automotive

Video/Audio Distribution Systems

Camera Surveillance Systems

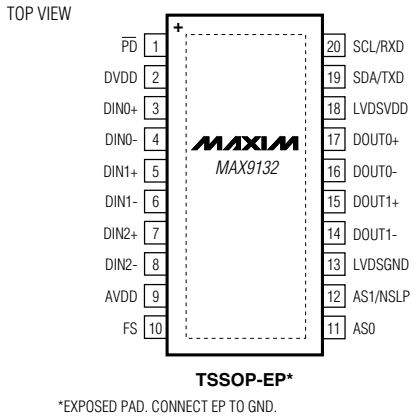
High-Speed Digital Media Routing

Navigation System Displays

Features

- **Supports Up to 840Mbps Data Rate at Each Port**
- **Nonactivated Ports are in High-Impedance State for Easy Port Expansion**
- **Programmable Preemphasis on LVDS Outputs**
- **Self Common-Mode Biasing on LVDS Inputs**
- **Three Selectable Approaches for Switch Routing:**
  - **I²C Interface**
  - **LIN Interface**
  - **Programmable Pins (MAX9134/MAX9135)**
- **±25kV ESD Protection**
- **+3.3V Supply Voltage**
- **-40°C to +105°C Operating Temperature Range**

Pin Configurations



TSSOP-EP*

*EXPOSED PAD. CONNECT EP TO GND.

Pin Configurations continued at end of data sheet.

Ordering Information

PART	PIN-PACKAGE	INPUTS	OUTPUTS	ROUTE CONTROL
MAX9132GUP+	20 TSSOP-EP*	3	2	I²C, LIN
MAX9132GUP/V+	20 TSSOP-EP*	3	2	I²C, LIN
MAX9134GHJ+	32 TQFP-EP*	3	4	I²C, LIN, Pins
MAX9135GHJ+	32 TQFP-EP*	4	3	I²C, LIN, Pins

Note: *Devices are specified over the -40°C to +105°C temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
/V denotes an automotive qualified part.

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +4.0V
All Pins to GND .....-0.3V to V_{DD} + 0.3V
Short-Circuit Duration (all outputs).....Continuous
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFP (derate 27.8mW/°C above +70°C).....2222mW
20-Pin TSSOP (derate 26.5mW/°C above +70°C) 2122mW
Operating Temperature Range .....-40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
All Other Pins Including SCL, SDA to GND .....±2kV
IEC 61000-4-2 (R_D = 330Ω, C_S = 150pF)
Contact Discharge
(DIN_, DOUT_) to GND .....±10kV
Air-Gap Discharge
(DIN_, DOUT_) to GND .....±15kV
ISO 10605 (R_D = 2kΩ, C_S = 330pF)
Contact Discharge
(DIN_, DOUT_) to GND .....±10kV
Air-Gap Discharge
(DIN_, DOUT_) to GND .....±25kV
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

20 TSSOP-EP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....37.7°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....2°C/W
32 TQFP-EP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....36°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....4°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

DC ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = $V_{LVDSVDD}$ = +3.0V to +3.6V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = $V_{LVDSVDD}$ = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}			3.0		3.6	V
Supply Current	I_{AVDD}, I_{DVDD}, $I_{LVDSVDD}$	Outputs switching at 20MHz	MAX9132		60	80	mA
			MAX9134/MAX9135		86	100	
SINGLE-ENDED CMOS INPUTS ($\overline{PD}$, FS, RXD)							
Input High Level	V_{IH1}			2.0			V
Input Low Level	V_{IL1}					0.8	V
Input High Current	I_{IN1}	V_{IN} = 0 to V_{DD}		-20		+20	µA
SINGLE-ENDED OUTPUTS (TXD, AS1/NSLP)							
Output High Level	V_{OH}			V_{DD} - 0.4			V
Output Low Level	V_{OL}	I_{OL} = 4mA				0.4	V
3-LEVEL INPUTS (S5–S0, AS0, AS1)							
Input High Level	V_{IH3}			2.5			V
Input Low Level	V_{IL3}					0.8	V
Input Open Level	V_{IO3}	Measured at the input pins		1.2	1.45	1.9	V
Input Current	I_{L3}, I_{H3}	V_{IL3} = 0V or V_{IH3} = V_{DD}		-20		+20	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = $V_{LVDSVDD}$ = +3.0V to +3.6V, T_A = -40°C to +105°C unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = $V_{LVDSVDD}$ = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL INPUTS (DIN_)						
Differential Input High Threshold	V_{IDH}	V_{ID} = V_{IN+} - V_{IN-}			100	mV
Differential Input Low Threshold	V_{IDL}	V_{ID} = V_{IN+} - V_{IN-}	-100			mV
Common Input Voltage	V_{COM}	V_{COM} = (V_{IN+} - V_{IN-})/2	1.00	1.29	1.60	V
Input Current	I_{IN+}, I_{IN-}		-50		+50	µA
DIFFERENTIAL OUTPUTS (DOUT_)						
Differential Output Voltage	V_{OD}	50Ω load, no preemphasis	250	3.65	450	mV
Change in V_{OD} Between Complementary Output States	$\lvert\Delta V_{OD}\rvert$		0	1	35	mV
Output Common-Mode Voltage	V_{COM}		1.125	1.29	1.475	V
Change in V_{COM} Between Complementary Output States	$\lvert\Delta V_{COM}\rvert$[4]		0	1	35	mV
Output Short-Circuit Current	I_{OS}	Two output pins connected to GND	-15	-7		mA
SERIAL-INTERFACE INPUT, OUTPUT (SCL, SDA)						
Input High Level	V_{IH}		0.7 x V_{DD}			V
Input Low Level	V_{IL}				0.3 x V_{DD}	V
High-Level Output Leakage Current	I_{LEAKH}	Open drain with 1kΩ pullup to V_{DD}			1	µA
Low-Level Output	V_{OL}	I_{OL} = 3mA			0.4	V
Input Capacitance	C_I			10		pF

AC ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = $V_{LVDSVDD}$ = +3.0V to +3.6V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = $V_{LVDSVDD}$ = +3.3V, T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL SIGNALS (DOUT_)						
Output-to-Output Skew	t_{SK}	R_L = 100Ω differential		50	250	ps
Rise Time	t_R	20% to 80% of the signal swing; R_L = 50Ω differential (R_L = 100Ω double termination), C_L = 5pF		0.3	0.4	ns
Fall Time	t_F	20% to 80% of the signal swing; R_L = 50Ω differential (R_L = 100Ω double termination), C_L = 5pF		0.3	0.4	ns
Duty Cycle	D	Input duty cycle 50%; 840Mbps clock pattern	45		55	%

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AC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = $V_{LVDSVDD}$ = +3.0V to +3.6V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = $V_{LVDSVDD}$ = +3.3V, T_A = +25°C.) (Notes 3, 4)

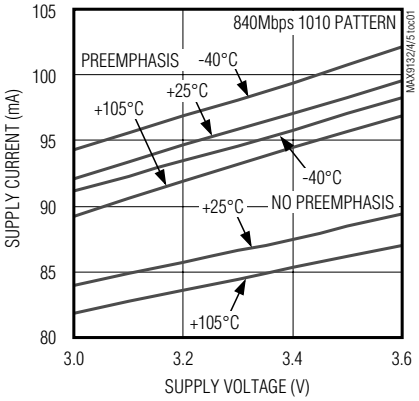
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Peak-to-Peak Jitter (Preemphasis On)	t_J	V_{ID} = 200mV, V_{COM} = 1.2V, 840Mbps clock pattern; input transition time (20% to 80%) = 200ps		10	30	ps
		V_{ID} = 200mV, V_{COM} = 1.2V, 840Mbps 2^{23} - 1 PRBS pattern; input transition time (20% to 80%) = 200ps		85	180	ps
Propagation Delay	t_D			2		ns
LVDS Switchover Time	t_{LON}	Switchover time from one channel to another			100	ns
LVDS with Preemphasis Amplitude	$\lvert V_{ODPE} \rvert$	50Ω differential (100Ω double termination) load, 840Mbps	335	530	680	mV
I^2C TIMING						
CLK Frequency	f_{SCL}				400	kHz
Start Condition Hold Time	$t_{HD:STA}$	(Figure 1)	0.6			µs
Low Period of SCL Clock	t_{LOW}	(Figure 1)	1.3			µs
High Period of SCL Clock	t_{HIGH}	(Figure 1)	0.6			µs
Repeated START Condition Setup Time	$t_{SU:STA}$	(Figure 1)	0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Figure 1)	0		0.9	µs
Data Setup Time	$t_{SU:STA}$	(Figure 1)	100			ns
Setup Time for STOP Condition	$t_{SU:STO}$	(Figure 1)	0.6			µs
Bus Free Time	t_{BUF}	(Figure 1)	1.3			µs

Note 2: Parameters are 100% production tested at T_A = +25°C, unless otherwise noted.
Note 3: I^2C timing parameters are specified for fast-mode I^2C. Maximum data rate = 400kbps.
Note 4: Parameters are guaranteed by design.

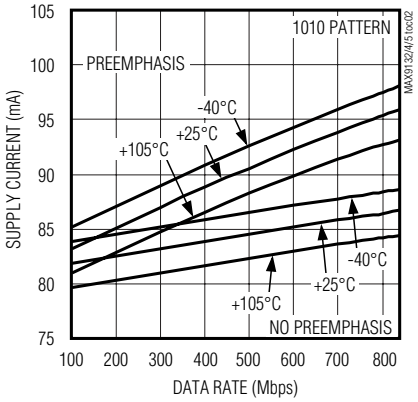
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = $V_{LVDSVDD}$ = +3.3V, T_A = +25°C, unless otherwise noted.)

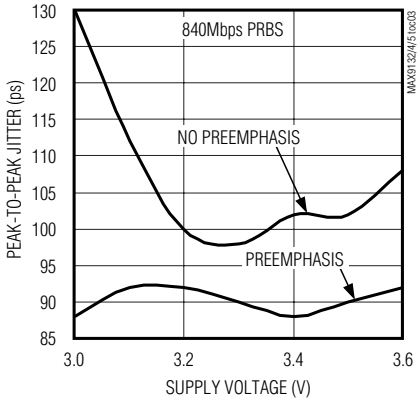
SUPPLY CURRENT vs. SUPPLY VOLTAGE



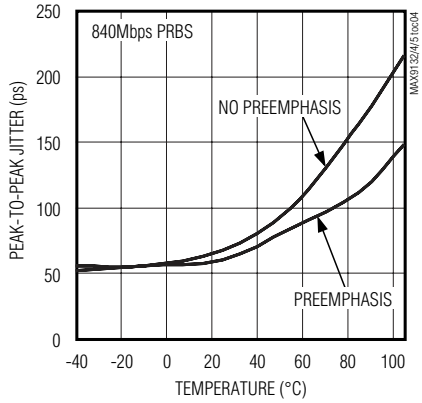
SUPPLY CURRENT vs. DATA RATE



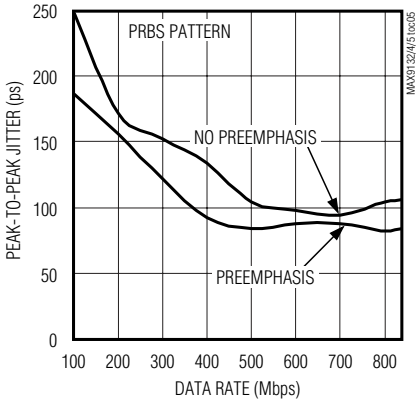
PEAK-TO-PEAK JITTER vs. SUPPLY VOLTAGE



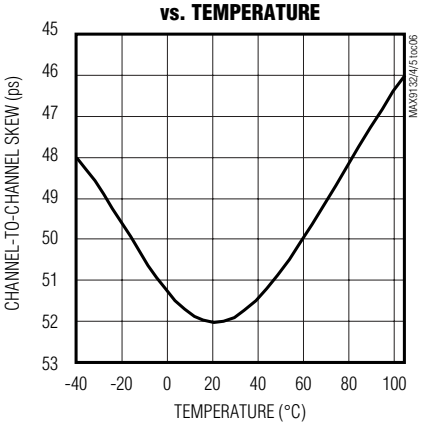
PEAK-TO-PEAK JITTER vs. TEMPERATURE



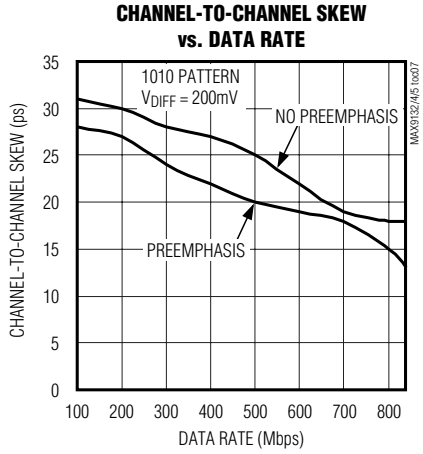
PEAK-TO-PEAK JITTER vs. DATA RATE



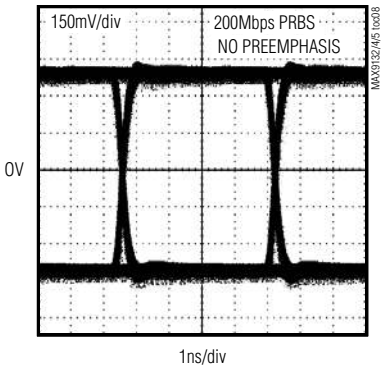
CHANNEL-TO-CHANNEL SKEW vs. TEMPERATURE



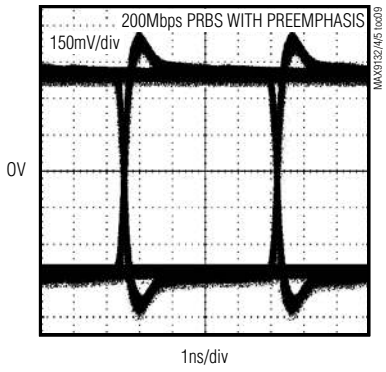
CHANNEL-TO-CHANNEL SKEW vs. DATA RATE



EYE DIAGRAM



EYE DIAGRAM

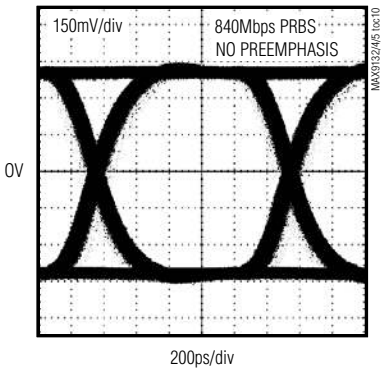


Programmable, High-Speed, Multiple Input/Output LVDS Crossbar Switches

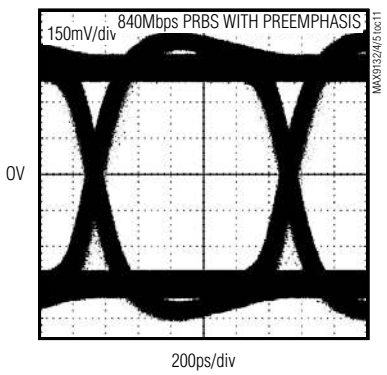
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = $V_{LVDSVDD}$ = +3.3V, T_A = +25°C, unless otherwise noted.)

EYE DIAGRAM



EYE DIAGRAM



Pin Description

PIN			NAME	FUNCTION
MAX9132 TSSOP	MAX9134 TQFP	MAX9135 TQFP		
1	31	30	$\overline{PD}$	Power-Down Input. $\overline{PD}$ = low for power-down. $\overline{PD}$ = high for power-up without preemphasis. Leave $\overline{PD}$ open for power-up with preemphasis on all outputs.
2	32	31	DVDD	Digital Power Supply. Bypass DVDD to DGND with 0.1µF and 0.01µF capacitors as close as possible to the device.
3	1	1	DIN0+	Port 0 Positive Input
4	2	2	DIN0-	Port 0 Negative Input
5	3	3	DIN1+	Port 1 Positive Input
6	4	4	DIN1-	Port 1 Negative Input
—	5	—	AGND	Analog Ground
7	6	5	DIN2+	Port 2 Positive Input
8	7	6	DIN2-	Port 2 Negative Input
—	—	7	DIN3+	Port 3 Positive Input
—	—	8	DIN3-	Port 3 Negative Input
9	8	9	AVDD	Analog Power Supply. Bypass AVDD to AGND with 0.1µF and 0.01µF capacitors as close as possible to the device.
10	—	—	FS	I^2C and LIN Interface Selection Input. FS = low for LIN, FS = high for I^2C.
—	9	10	S0	Routing Selection 0 Input. See Tables 6a and 6b.
—	10	11	S1	Routing Selection 1 Input. See Tables 6a and 6b.
—	11	12	S2	Routing Selection 2 Input. See Tables 6a and 6b.
—	12	13	S3	Routing Selection 3 Input. See Tables 6a and 6b.
11	13	14	AS0	3-Level I^2C Address Selection 0 Input (Table 3) or LIN Identifier Selection 0 Input (Table 4)

Pin Description (continued)

PIN			NAME	FUNCTION
MAX9132 TSSOP	MAX9134 TQFP	MAX9135 TQFP		
12	14	15	AS1/NSLP	3-Level I^2C Address Selection 1 Input (in I^2C Mode, Table 3). In LIN bus mode, it becomes an NSLP output, the sleep mode activation pin (active low) to the LIN bus driver.
13	16, 25	19, 24	LVDSGND	LVDS Ground
—	17	—	DOUT3-	Port 3 Negative Output
—	18	—	DOUT3+	Port 3 Positive Output
—	19	17	DOUT2-	Port 2 Negative Output
—	20	18	DOUT2+	Port 2 Positive Output
14	21	20	DOUT1-	Port 1 Negative Output
15	22	21	DOUT1+	Port 1 Positive Output
16	23	22	DOUT0-	Port 0 Negative Output
17	24	23	DOUT0+	Port 0 Positive Output
18	15, 26	16, 25	LVDSVDD	LVDS Supply Input. Bypass LVDSVDD to LVDSGND with 0.1µF and 0.01µF capacitors as close as possible to the device.
19	27	26	SDA/TXD	I^2C Data Link Input/LIN Tx Output. SDA/TXD becomes SDA when in I^2C mode and TXD when in LIN mode.
20	28	27	SCL/RXD	I^2C Clock/LIN Rx Input. SCL/RXD becomes SCL when in I^2C mode and RXD when in LIN mode.
—	29	28	S5	Routing Selection 5 Input. See Tables 6a and 6b.
—	30	29	S4	Routing Selection 4 Input. See Tables 6a and 6b.
—	—	32	DGND	Digital Ground
—	—	—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance.

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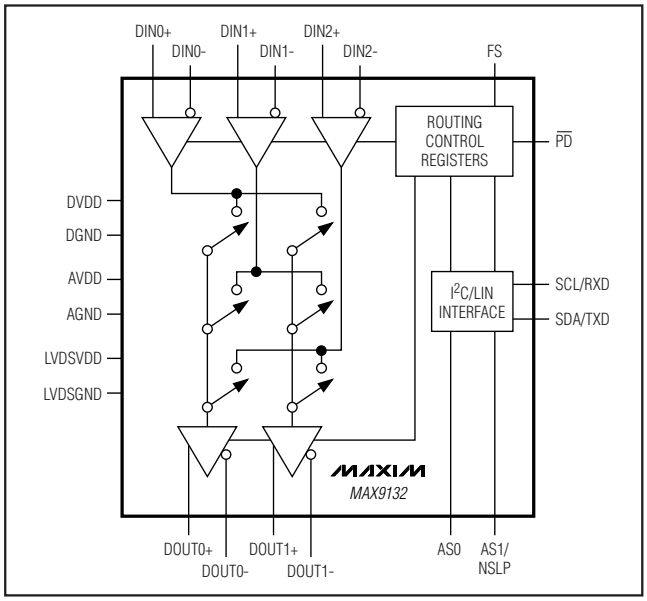
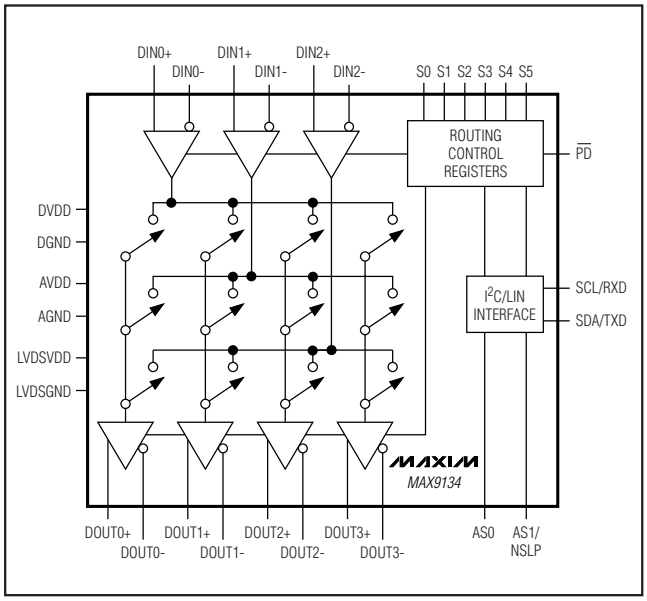
Functional Diagrams





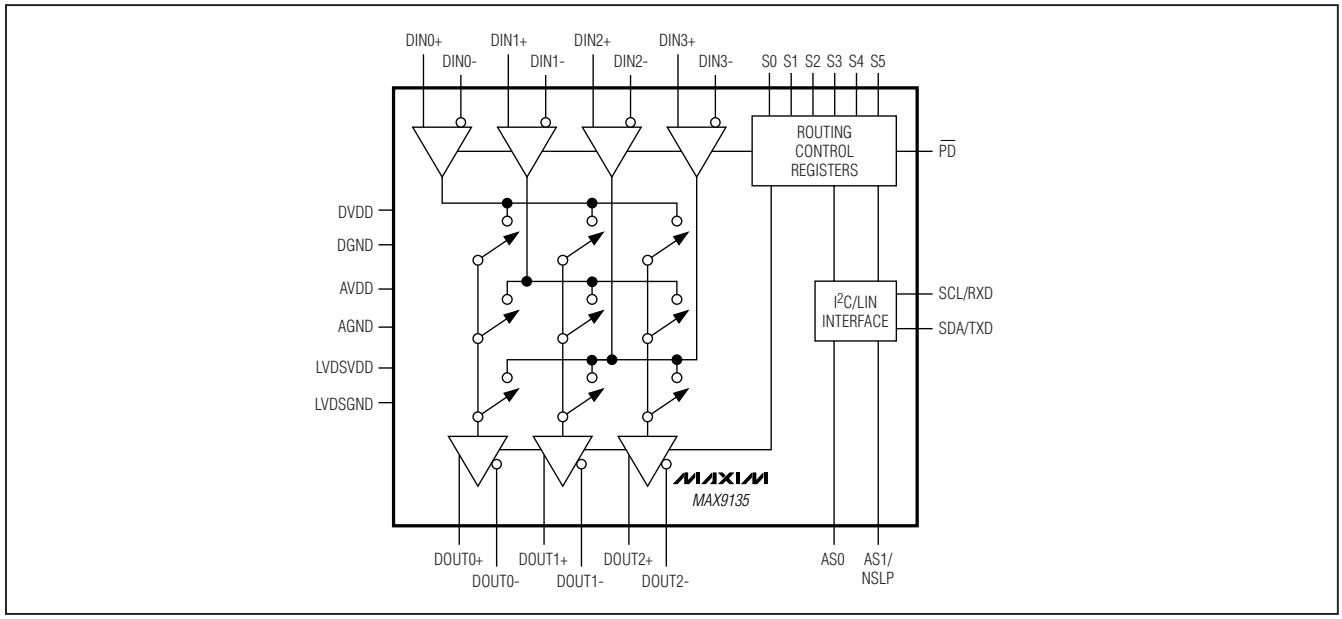


Table 1. Register Address Map

REGISTER ADDRESS (HEX)	READ/ WRITE	LIN INTERFACE DESCRIPTION	I²C DESCRIPTION
0x00	R	LIN Status Register	Reserved
0x01	R/W	Switch Control Register 1	Switch Control Register 1
0x02	R/W	Switch Control Register 2 (MAX9134/MAX9135 only)	Switch Control Register 2 (MAX9134/MAX9135 only)
0xFF	W	Reserved	Route Activation Register

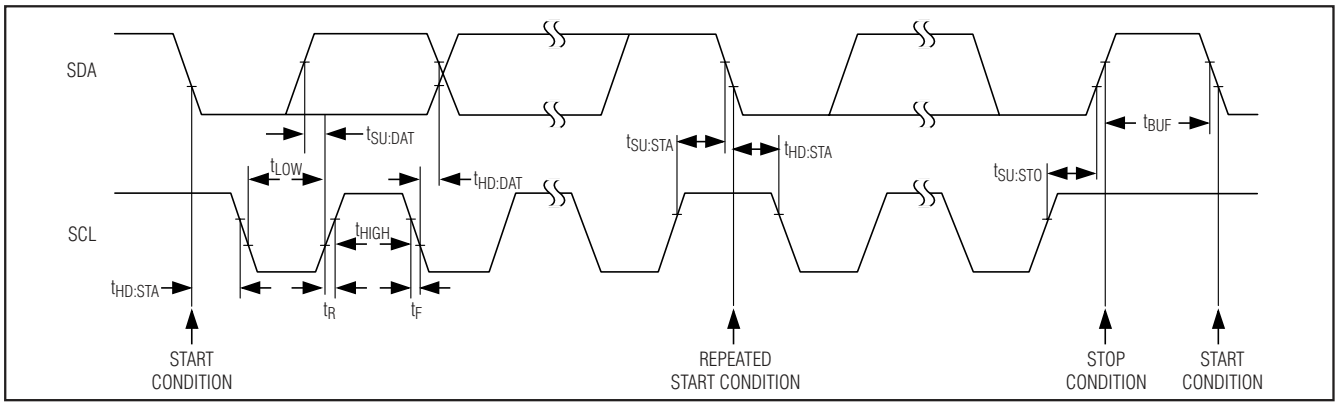


Figure 1. I²C Serial-Interface Timing Details

Detailed Description

The MAX9132/MAX9134/MAX9135 high-speed, multiple-port, low-voltage differential signaling (LVDS) crossbar switches are specially designed for digital video and camera signal transmission. These switches have a wide bandwidth, supporting data rates up to 840Mbps. This allows the use of MAX9132/MAX9134/MAX9135 with LVDS serializers/deserializers (SerDes) to create a complete video or camera network. The MAX9132 has three input ports and two output ports, the MAX9134 has three input ports and four output ports, and the MAX9135 has four input ports and three output ports. The video or camera signal can go through the switch from an input port to one or multiple output ports.

The MAX9132/MAX9134/MAX9135 switch routing is programmable through either an I²C interface or a Local Interconnect Network (LIN) serial interface. AS0 and AS1 set the slave addresses for either of these modes, allowing several devices on a bus simultaneously. In addition, the MAX9134/MAX9135 provide 3-level pins S[5:0] to set switch routing and the initial conditions for I²C mode. To improve the signal integrity, all the LVDS outputs feature selectable preemphasis.

Initial Power-Up

On power-up, all control registers have a value of 0x00. For the MAX9134/MAX9135, leaving S[5:0] unconnected, allows control through the LIN interface with all outputs deactivated. Otherwise, the switch runs in pin-control mode with S[5:0] controlling the switch routing. The I²C is also active while the device is in pin-control mode. Successful routing through I²C overrides the pin settings. For more details, see the *I²C Interface* section. For the MAX9132, the FS input determines which interface is active.

Register Description

There are four 1-byte control registers in the MAX9132/MAX9134/MAX9135. These registers control the routing of the switch. Table 1 describes the register map for both I²C and LIN. When the MAX9132/MAX9134/MAX9135 operate in LIN mode, register 0x00 acts as an error flag register. Its function is described in detail in Table 5. In either I²C or LIN mode, the control registers (0x01, 0x02) program the MAX9132/MAX9134/MAX9135 switch routing control. In addition, these registers can individually activate and deactivate preemphasis for each output port. Table 2a describes the routing for the MAX9132/MAX9134 and Table 2b for the MAX9135. For I²C programming, register 0xFF controls the activation of routing.

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Table 2a. I²C/LIN Switch Routing Control Registers for the MAX9132/MAX9134

REGISTER ADDRESS	REGISTER BIT(S)	DESCRIPTION	VALUE	FUNCTION
0x01	D7	DOUT1 Preemphasis	0	DOUT1 preemphasis off
			1	DOUT1 preemphasis on
	D[6:4]	DOUT1 Routing Connection	000	DOUT1 in high impedance
			001	DOUT1 connected to DIN1
			010	DOUT1 connected to DIN0
			011	DOUT1 connected to DIN2
	D3	DOUT0 Preemphasis	0	DOUT0 preemphasis off
			1	DOUT0 preemphasis on
	D[2:0]	DOUT0 Routing Connection	000	DOUT0 in high impedance
			001	DOUT0 connected to DIN1
			010	DOUT0 connected to DIN0
			011	DOUT0 connected to DIN2
0x02 (MAX9134 only)	D7	DOUT3 Preemphasis	0	DOUT3 preemphasis off
			1	DOUT3 preemphasis on
	D[6:4]	DOUT3 Routing Connection	000	DOUT3 in high impedance
			001	DOUT3 connected to DIN1
			010	DOUT3 connected to DIN0
			011	DOUT3 connected to DIN2
	D3	DOUT2 Preemphasis	0	DOUT2 preemphasis off
			1	DOUT2 preemphasis on
	D[2:0]	DOUT2 Routing Connection	000	DOUT2 in high impedance
			001	DOUT2 connected to DIN1
			010	DOUT2 connected to DIN0
			011	DOUT2 connected to DIN2

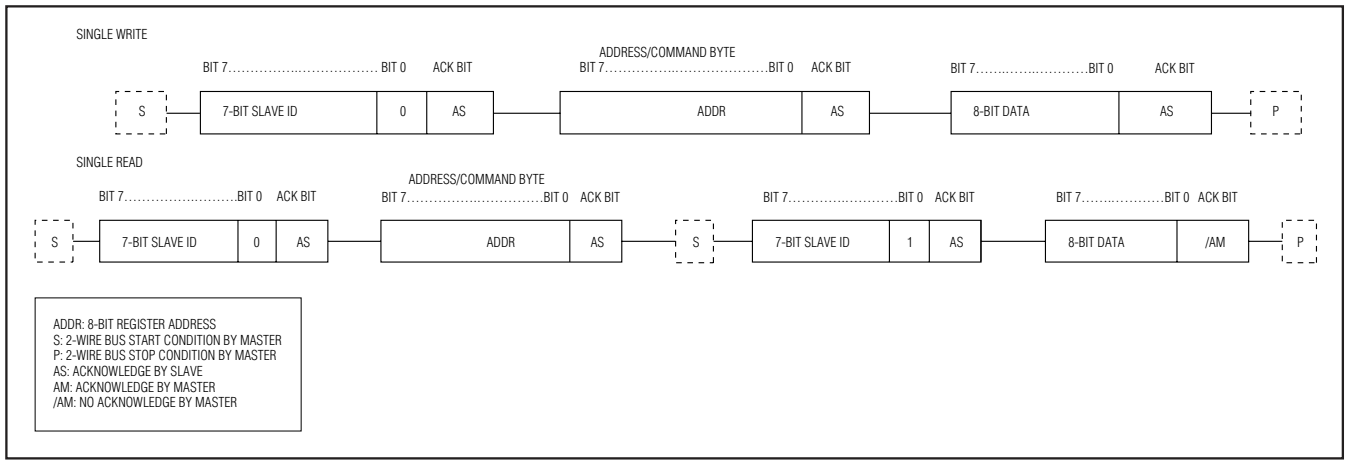

Figure 2. Single-Byte Write and Single-Byte Read

Table 2b. I²C Switch Routing Control Registers for the MAX9135

REGISTER ADDRESS	REGISTER BIT(S)	DESCRIPTION	VALUE	FUNCTION
0x01	D7	DOUT1 Preemphasis	0	DOUT1 preemphasis off
			1	DOUT1 preemphasis on
	D[6:4]	DOUT1 Routing Connection	000	DOUT1 not connected
			001	DOUT1 connected to DIN1
			010	DOUT1 connected to DIN0
			011	DOUT1 connected to DIN2
			100	DOUT1 connected to DIN3
	D3	DOUT0 Preemphasis	0	DOUT0 preemphasis off
			1	DOUT0 preemphasis on
	D[2:0]	DOUT0 Routing Connection	000	DOUT0 not connected
			001	DOUT0 connected to DIN1
			010	DOUT0 connected to DIN0
			011	DOUT0 connected to DIN2
			100	DOUT0 connected to DIN3
0x02	D[7:4]	Reserved	0000	Set these bits to 0000
	D3	DOUT2 Preemphasis	0	DOUT2 preemphasis off
			1	DOUT2 preemphasis on
	D[2:0]	DOUT2 Routing Connection	000	DOUT2 not connected
			001	DOUT2 connected to DIN1
			010	DOUT2 connected to DIN0
			011	DOUT2 connected to DIN2
			100	DOUT2 connected to DIN3

I²C Interface

The MAX9132/MAX9134/MAX9135 operate as slaves that send and receive data through I²C (see Figure 1). The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the slave and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the I²C interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START condition sent by a master, followed by the 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, a data byte, and finally a STOP condition. Table 3 shows the slave address selection by the AS0 and AS1 pins.

Data Format for Writing to the Slave

A write to the MAX9132/MAX9134/MAX9135 comprises the transmission of the slave address with the R/$\overline{W}$ bit set to 0, followed by at least 1 byte of information. The first byte of information is the command byte. The command byte determines which registers of the MAX9132/MAX9134/MAX9135 are to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, the MAX9132/MAX9134/MAX9135 take no further action beyond storing the command byte. Any bytes that are received after the command byte are data bytes. The first data byte goes into the internal register of the crossbar switch selected by the command byte (Figure 2). If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX9132/MAX9134/MAX9135 internal registers because the command byte address generally autoincrements (Table 1).

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Table 3. I²C Slave Addresses

PIN		ADDRESS						ADDRESS (HEX)
AS0	AS1	A[7:5]	A4	A3	A2	A1	A0	
Low	Low	101	0	0	0	0	R/$\overline{W}$	0xA0
Low	Open	101	0	0	0	1	R/$\overline{W}$	0xA2
Low	High	101	0	0	1	0	R/$\overline{W}$	0xA4
Open	Low	101	0	0	1	1	R/$\overline{W}$	0xA6
Open	Open	101	0	1	0	0	R/$\overline{W}$	0xA8
Open	High	101	0	1	0	1	R/$\overline{W}$	0xAA
High	Low	101	0	1	1	0	R/$\overline{W}$	0XAC
High	Open	101	0	1	1	1	R/$\overline{W}$	0xAE
High	High	101	1	0	0	0	R/$\overline{W}$	0xB0

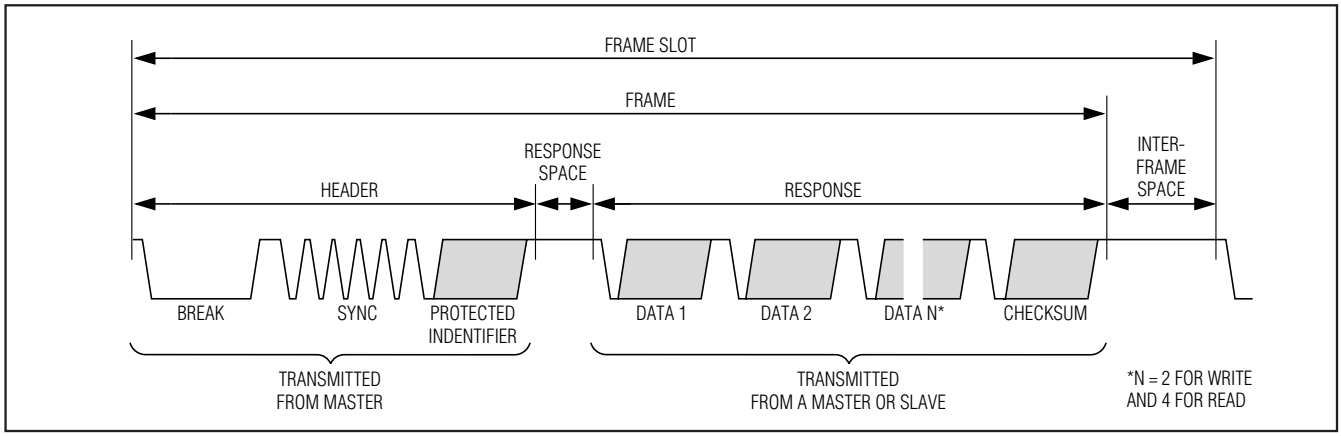

Figure 3. LIN Bus Signal Format

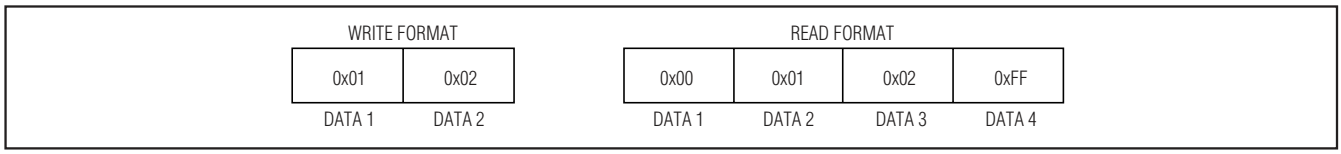

Figure 4. LIN Write and Read Data Frame

Data Format for Reading from the Slave

The MAX9132/MAX9134/MAX9135 are read using the devices' internally stored command bytes as an address pointer, the same way the stored command byte is used as an address pointer for a write. The pointer does not autoincrement after each data byte is read. Initiate a read by writing the command byte to the proper slave address (Figure 2), then send the device's slave address with the R/$\overline{W}$ bit set to 1. The slave now responds with the contents of the requested register (Figure 2).

LIN Interface

The LIN interface is a low-speed, low-cost interface used in slow control signal traffic in automotive applications. This device is the slave node in the LIN bus cluster and is designed based on the LIN Rev. 1.3 specification. The LIN master sends data to the MAX9132/MAX9134/MAX9135 LSB first, up to a maximum data rate of 20kbps. The LIN slave node waits for the synchronization pulse, then synchronizes itself to the pulse. The node must then read the identifier and send/receive data bytes to the master, setting the error flag register when necessary. The LIN interface uses the same routing function of the switch control registers (0x01, 0x02) as the I²C inter-

Table 4. LIN Identifiers for Write and Read Operations

AS0	WRITE ID		READ ID	
	ID[5:0]	PID FIELD	ID[5:0]	PID FIELD
Low	0x08	0x08	0x27	0xE7
Open	0x0A	0xCA	0x29	0xE9
High	0x1C	0x9C	0x2B	0x2B

Table 5. Register 0x00 Error Flag Mapping for LIN

REGISTER BIT(S)	DESCRIPTION	FUNCTION
D[7:5]	Reserved	Reserved
D4	Sync	Sync pulse widths outside the given tolerances detected
D3	Transmit	Value read on RXD different from value transmitted on TXD during a read
D2	Checksum	Checksum sent during a write does not match the expected checksum
D1	Parity	ID parity bit does not match expected parity
D0	Frame	Message frame did not complete within the maximum allowed time

face. The routing action takes place after correct checksum verification. The LIN status register (0x00) holds the error flags for the LIN transceiver. For a write, the master writes 2 bytes of data to the registers (0x01, 0x02). For a read, the slave outputs the contents of registers 0x00, 0x01, and 0x02, along with the stuffing byte at a constant value (0xFF). In either mode, the checksum follows at the end of the data bytes. Figure 3 shows the write and read signal frame format. Figure 4 shows the LIN write and read data frame.

LIN-Protected Identifier

The LIN bus uses the 8-bit protected identifier (PID) to address the slave nodes. Two parity bits (MSBs) along with 6 ID bits (LSBs) make up the PID field. Table 4 defines the sets of the identifiers for the write/read operations of the LIN slave node. AS0 selects the identifiers. AS1/NSLP becomes the NSLP output for activating the LIN driver chip (MAX13020).

LIN Error Handling

Register 0x00 contains the error flags found in the LIN signal by the slave note (Table 5). A successful LIN read resets register 0x00.

Pin Control by S[5:0] (MAX9134/MAX9135)

For the MAX9134/MAX9135, the routing can be controlled by the hardware pins (S[5:0]). If the I²C register 0xFF is not written by 0xFF, then chip routing is determined by S[5:0]. Also, these pins set the initial power-up routing condition of the chip. Table 6a gives the details of the routing control for the MAX9134. Table 6b gives the details of the routing control for the MAX9135. Once the I²C register 0xFF is written by 0xFF, the I²C registers 0x01 and 0x02 take over the routing and the pin (S[5:0]) setting is ignored. After the I²C routing takes place, the pin setting can be changed without affecting the routing. The new pin setting takes effect if the $\overline{PD}$ pin or the chip supply is toggled. Usually, once I²C controls the routing, there is no value in using the pin routing.

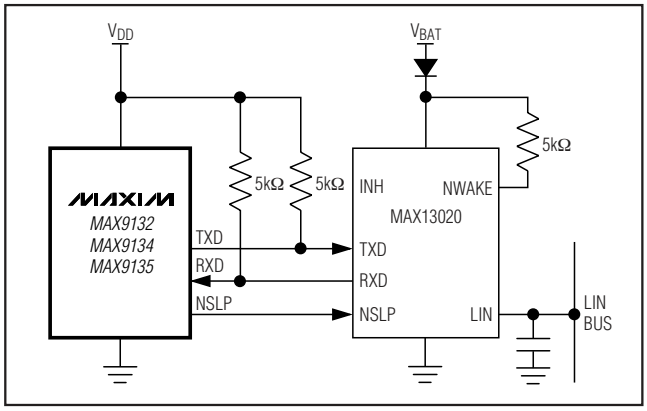

Figure 5. Connecting the MAX9132/MAX9134/MAX9135 to the MAX13020

Applications Information

3-Level Inputs

The MAX9132/MAX9134/MAX9135 use several 3-level inputs to control the device. Use three-state logic to realize the 3-level logic using digital control. Alternatively, if a high-impedance output is unavailable, apply a voltage of $V_{DD}/2$ to realize the midlevel high-impedance state.

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Table 6a. Switch Routing Control Pin Setting for the MAX9134

PORT	S5	S4	S3	S2	S1	S0	CONNECTION	DESCRIPTION
DOUT0, DOUT1	0	X	X	X	X	0	DOUT0 connected to DIN0	Both DOUT0 and DOUT1 outputs are on
						Open	DOUT0 connected to DIN1	
						1	DOUT0 connected to DIN2	
					0	X	DOUT1 connected to DIN0	
					Open		DOUT1 connected to DIN1	
					1		DOUT1 connected to DIN2	
	1	X	X	X	0	0	DOUT0 connected to DIN0	DOUT1 is not connected, DOUT0 is on
						Open	DOUT0 connected to DIN1	
						1	DOUT0 connected to DIN2	
		X	X	X	Open	0	DOUT1 connected to DIN0	DOUT0 is not connected, DOUT1 is on
						Open	DOUT1 connected to DIN1	
						1	DOUT1 connected to DIN2	
	1	X	X	X	1	X	DOUT0 and DOUT1 in high impedance	Both DOUT0 and DOUT1 are not connected
DOUT2, DOUT3	X	0	X	0	X	X	DOUT2 connected to DIN0	Both DOUT2 and DOUT3 outputs are on
				Open			DOUT2 connected to DIN1	
				1			DOUT2 connected to DIN2	
			0	X			DOUT3 connected to DIN0	
			Open				DOUT3 connected to DIN1	
			1				DOUT3 connected to DIN2	
	X	1	0	0	X	X	DOUT2 connected to DIN0	DOUT3 is not connected, DOUT2 is on
				Open			DOUT2 connected to DIN1	
				1			DOUT2 connected to DIN2	
			Open	0	X	X	DOUT3 connected to DIN0	DOUT2 is not connected, DOUT3 is on
				Open			DOUT3 connected to DIN1	
				1			DOUT3 connected to DIN2	
	X	1	1	X	X	X	DOUT2 and DOUT3 in high impedance	Both DOUT2 and DOUT3 are not connected

X = Don't care.

Interface Selection Using S[5:0] (MAX9134/MAX9135)

S[5:0] determine which interface controls the MAX9134/MAX9135. Leave S[5:0] unconnected or set to a midlevel state to enable the LIN interface. Other settings to S[5:0] set the switch routing according to Tables 6a (MAX9134) and 6b (MAX9135). The I²C interface is active when the MAX9132/MAX9134/MAX9135 are not in LIN interface mode. Writing to an I²C register overrides the S[5:0] settings.

Interface Selection Using FS (MAX9132 Only)

The FS input selects the interface for the MAX9132. Set FS low for LIN interface control and FS high for I²C interface. The MAX9132 powers up with all LVDS outputs unconnected for either mode.

Interfacing the MAX9132/MAX9134/MAX9135 to the LIN Bus

The MAX9132/MAX9134/MAX9135 interface to the LIN bus through the MAX13020 LIN transceivers. This device translates the +12V to +42V LIN bus signal down

Table 6b. Switch Routing Control Pin Setting for the MAX9135

PORT	S5	S4	S3	S2	S1	S0	CONNECTION	DESCRIPTION
DOUT0	0	X	X	X	X	0	DOUT0 connected to DIN0	S5 and S0 determine DOUT0 connection
	0					Open	DOUT0 connected to DIN1	
	0					1	DOUT0 connected to DIN2	
	1	X	X	X	X	0	DOUT0 connected to DIN3	
	1					Open	DOUT0 in high impedance	
DOUT1	X	0	X	X	0	X	DOUT1 connected to DIN0	S4 and S1 determine DOUT1 connection
		0			Open		DOUT1 connected to DIN1	
		0			1		DOUT1 connected to DIN2	
		1	X	X	0		DOUT1 connected to DIN3	
		1			Open		DOUT1 in high impedance	
DOUT2	X	X	0	0	X	X	DOUT2 connected to DIN0	S3 and S2 determine DOUT2 connection
			0	Open			DOUT2 connected to DIN1	
			0	1			DOUT2 connected to DIN2	
			1	0			DOUT2 connected to DIN3	
			1	Open			DOUT2 in high impedance	

X = Don't care.

to the +3.3V logic level. Figure 5 shows the circuit that interfaces the crossbar switches to the LIN bus.

Waking Up the LIN Bus Driver

At power-up, the MAX9132/MAX9134/MAX9135 leave NSLP low, keeping the LIN bus driver in sleep mode. When the LIN driver receives a wake-up signal (Figure 6) from the LIN bus, the driver pulls RXD low. When the MAX9132/MAX9134/MAX9135 detect a falling edge on RXD, the device pulls NSLP high waking up the LIN driver. The MAX9132/MAX9134/MAX9135 then enable the TXD pin.

Putting the LIN Bus Driver into Sleep Mode

There are two conditions under which the MAX9132/MAX9134/MAX9135 put the LIN driver to sleep: line activity timeout and receiving a sleep command. The first condition arises if there is inactivity on the LIN bus for more than 3s. The second condition requires sending the data 0x00 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF using the identifier 0x3C to the device. If any of the two conditions happen, the device disables TXD and drives NSLP low. This puts the LIN driver into sleep mode.

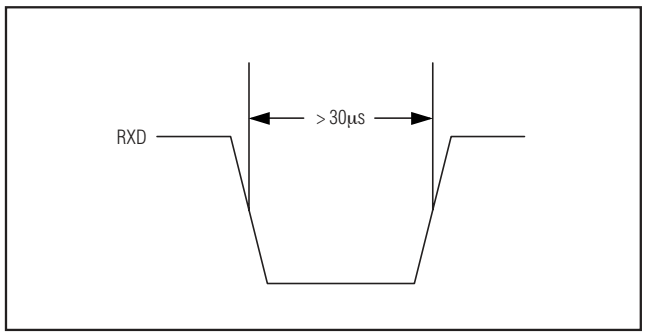

Figure 6. LIN Bus Wake-Up Signal

Multiple MAX9132/MAX9134/MAX9135 for Port Expansion

The MAX9132/MAX9134/MAX9135 high-impedance outputs allow the attachment of several parts in parallel. Figure 7 shows example connection schemes to realize larger crossbar connections.

LVDS Output Preemphasis

The MAX9132/MAX9134/MAX9135 feature a preemphasis mode where extra current is added to the output and causes the amplitude to increase by 50% at the transition point. Preemphasis helps to get a faster transition, better eye diagram, and improved signal integrity (see the *Typical Operating Characteristics*). During data transition, the switch injects additional current for a short period, typically 400ps. Leave $\overline{PD}$ open or apply a midlevel voltage ($V_{DD}/2$) to enable preemphasis on all LVDS outputs. Set $\overline{PD}$ high to set preemphasis through the I^2C or LIN interfaces. Preemphasis in this mode is initially not on.

Power-Down

Set $\overline{PD}$ low to enable power-down mode. The registers retain their values and the device resumes operation from the same mode upon power-up.

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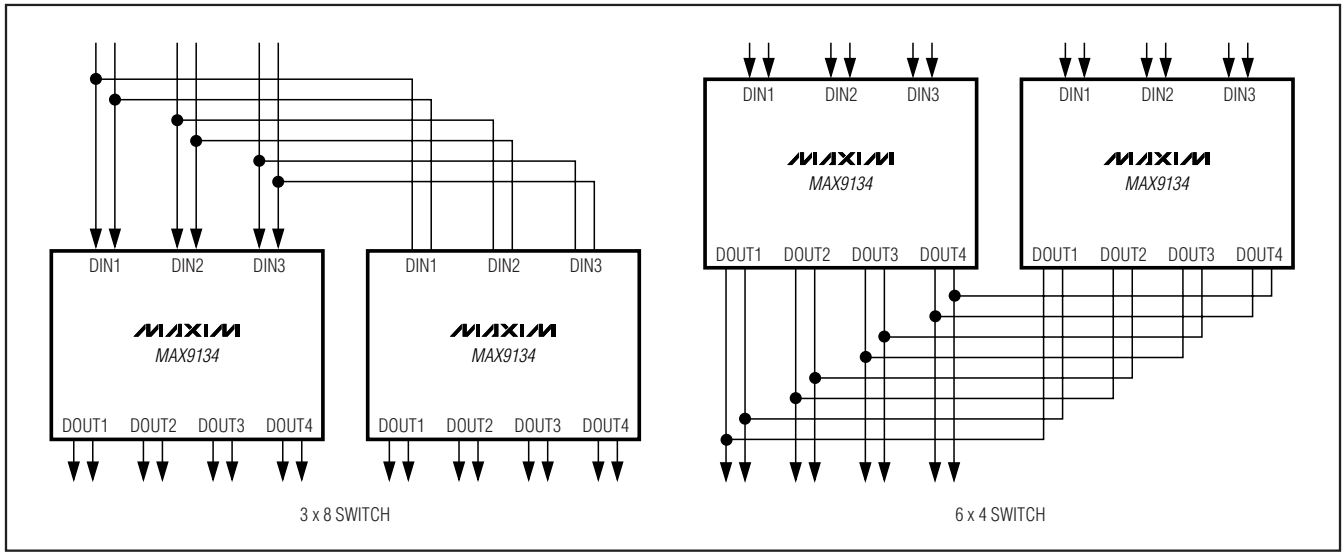

Figure 7. Topologies for Port Expansion

Input/Output Termination

Terminate LVDS inputs/outputs through 100Ω differential termination, or use an equivalent Thevenin termination. Terminate both inputs/outputs and use identical terminations on each for the lowest output-to-output skew.

Power-Supply Bypassing

Adequate power-supply bypassing is necessary to maximize the performance and noise immunity. Bypass each supply to their respective grounds with high-frequency surface-mount 0.01µF ceramic capacitors as close as possible to the device. Use multiple bypass vias for connection to minimize inductance.

Board Layout

Separate the I²C/LIN signals and LVDS signals to prevent crosstalk. When possible, use a four-layer PCB with separate layers for power, ground, LVDS, and digital signals. Layout PCB traces for 100Ω differential characteristic impedance. The trace dimensions depend on the type of trace used (microstrip or stripline).

Route the PCB traces for an LVDS channel (there are two conductors per LVDS channel) in parallel to maintain the differential characteristic impedance. Place the 100Ω (typ) termination resistor at both ends of the LVDS driver and receiver. Avoid vias. If vias must be used, use only one pair per LVDS channel and place the via for each line at the same point along the length of the PCB traces. This way, any reflections occur at the same time. Do not make vias into test points for automated test equipment. Make the PCB traces that make up a differential pair the same length to avoid skew within the differential pair.

Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic-field-canceling effects. Balanced cables pick up noise as common mode that is rejected by the LVDS receiver. Add a 0.1µF capacitor in series with each output for AC-coupling.

Choosing Pullup Resistors

I²C requires pullup resistors to provide a logic-high level to data and clock lines. There are tradeoffs between power dissipation and speed, and a compromise must be made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times to go from low to high (30% to 70%) for fast mode, which is defined for a data rate up to 400kbps (see the *I²C Interface* section for details). To meet the rise time requirement, choose the pullup resistors so that the rise time $t_R = 0.85R_{PULLUP} \times C_{BUS} < 300ns$. If the transition time becomes too slow, the setup and hold times may not be met and waveforms are not recognized.

Exposed Pad

The TQFP and TSSOP packages used for the MAX9132/MAX9134/MAX9135 have exposed pads on the bottom. The exposed pad is internally connected to ground. Connect the exposed pad to ground using a landing pad large enough to accommodate the entire exposed pad. Add vias from the exposed pad's land area to a copper polygon on the other side of the PCB to provide lower thermal impedance from the device to the ambient air.

ESD Protection

The MAX9132/MAX9134/MAX9135 ESD tolerance is rated for IEC 61000-4-2, Human Body Model, and ISO 10605 standards. IEC 61000-4-2 and ISO 10605 specify ESD tolerance for electronic systems. The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 8). For IEC 61000-4-2, the LVDS outputs are rated for ±10kV Contact Discharge and ±15kV Air-Gap Discharge. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 9). For the Human Body Model, all pins are rated for ±2kV Contact Discharge. The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 10). For ISO 10605, the LVDS outputs are rated for ±10kV Contact and ±25kV Air-Gap Discharge.

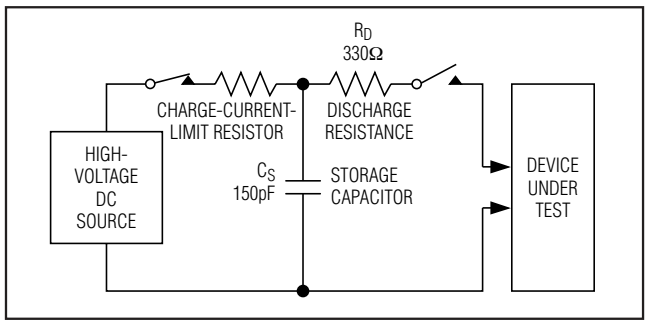

Figure 8. IEC 61000-4-2 Contact Discharge ESD Test Circuit

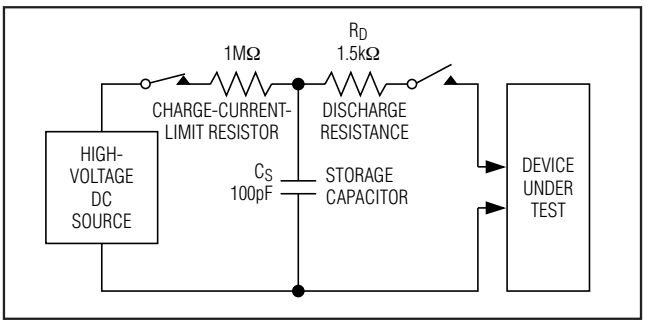

Figure 9. Human Body ESD Test Circuit

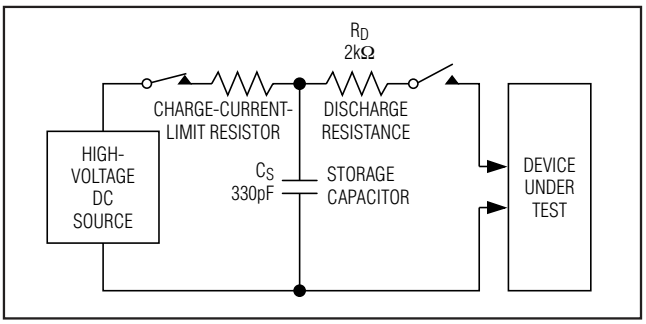

Figure 10. ISO 10605 Contact Discharge ESD Test Circuit

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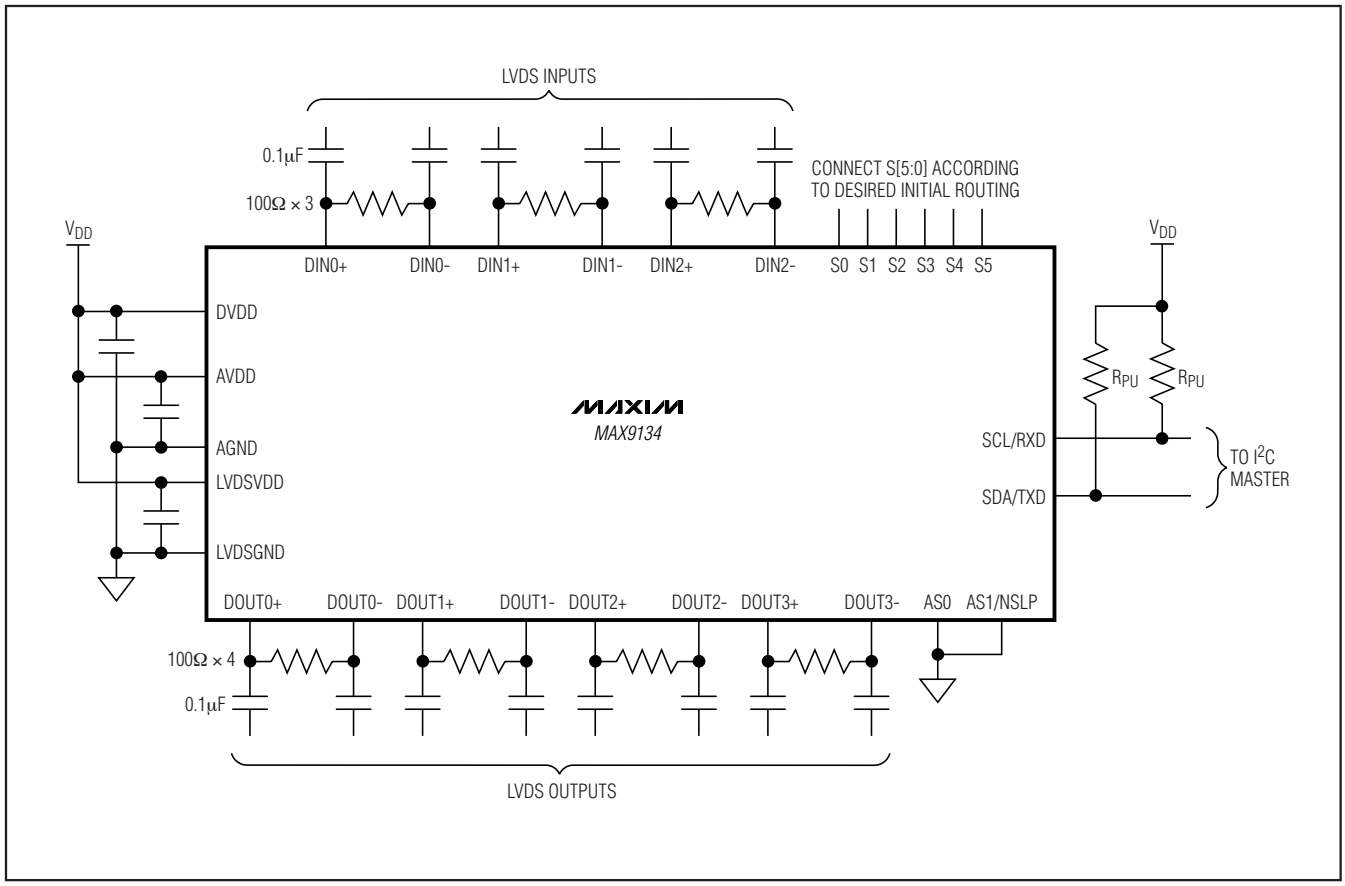
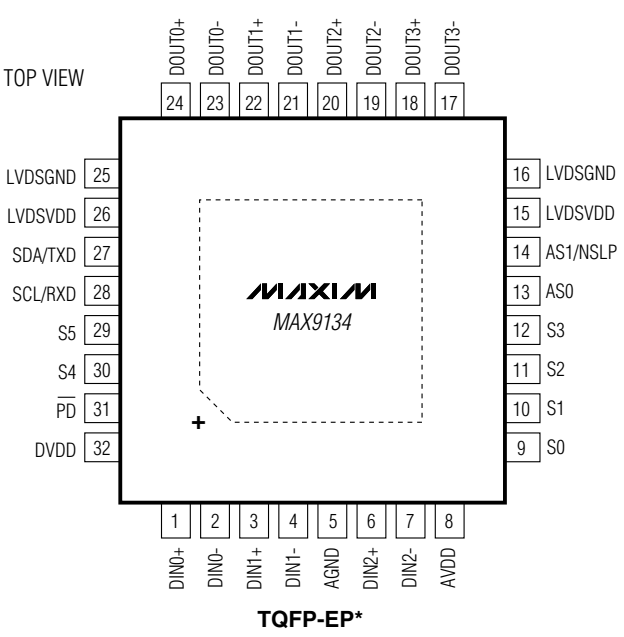
Typical Application Circuit



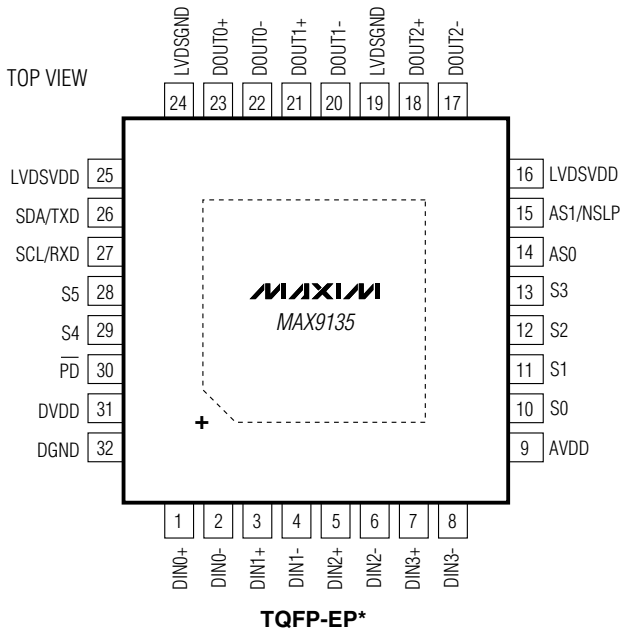
Programmable, High-Speed, Multiple Input/Output LVDS Crossbar Switches

Pin Configurations (continued)



TQFP-EP*

*EXPOSED PAD. CONNECT EP TO GND.



TQFP-EP*

*EXPOSED PAD. CONNECT EP TO GND.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TSSOP-EP	U20E+1	21-0108	90-0114
32 TQFP-EP	H32E+6	21-0079	90-0326

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/08	Initial release	—
1	2/11	Updated *Pin Control by S[5:0] (MAX9134/MAX9135)* and *Interface Selection Using FS (MAX9132 Only)* sections	13, 14
2	4/11	Added automotive part (MAX9132) to *Ordering Information*	1