

**IRLR3110ZPbF**  
**IRLU3110ZPbF**

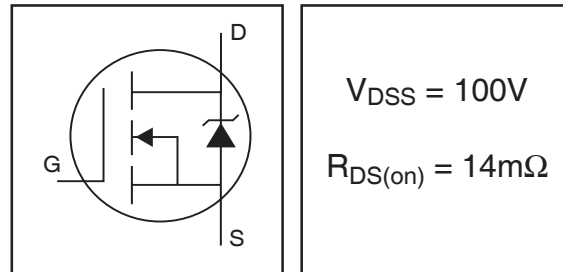
**Features**

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

**Description**

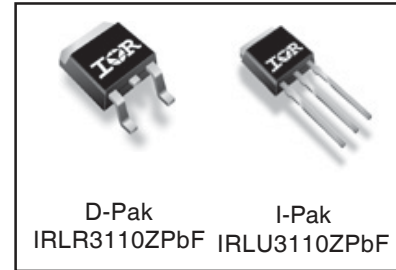
Specifically designed for Industrial applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Industrial applications and a wide variety of other applications.

HEXFET® Power MOSFET



$$V_{DSS} = 100V$$

$$R_{DS(on)} = 14m\Omega$$



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	63	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	45	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	42	
$I_{DM}$	Pulsed Drain Current ①	250	
$P_D @ T_C = 25^\circ C$	Power Dissipation	140	W
	Linear Derating Factor	0.95	W/°C
$V_{GS}$	Gate-to-Source Voltage	±16	V
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	110	mJ
$E_{AS}$ (Tested)	Single Pulse Avalanche Energy Tested Value ③	140	
$I_{AR}$	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy ⑤		mJ
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Reflow Soldering Temperature, for 10 seconds	300	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

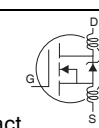
**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ③	—	1.05	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) ②③	—	40	
$R_{\theta JA}$	Junction-to-Ambient ④	—	110	

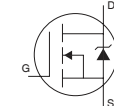
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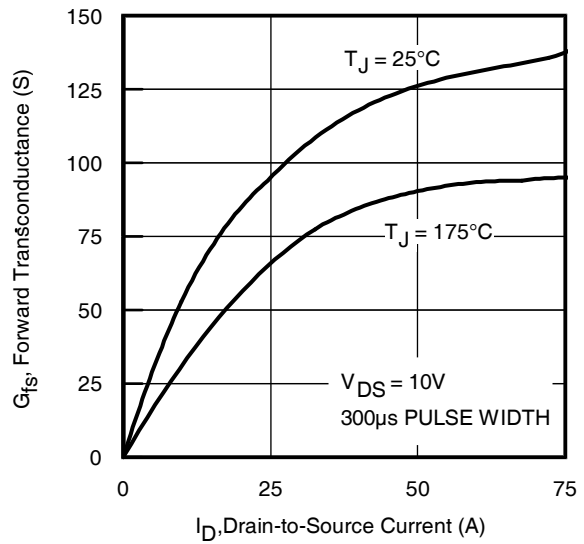
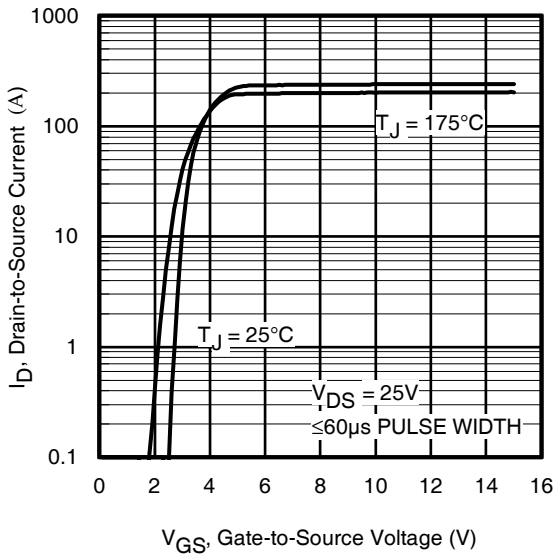
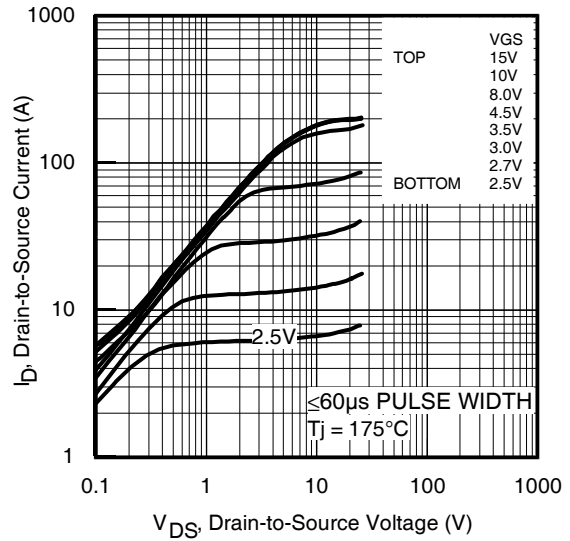
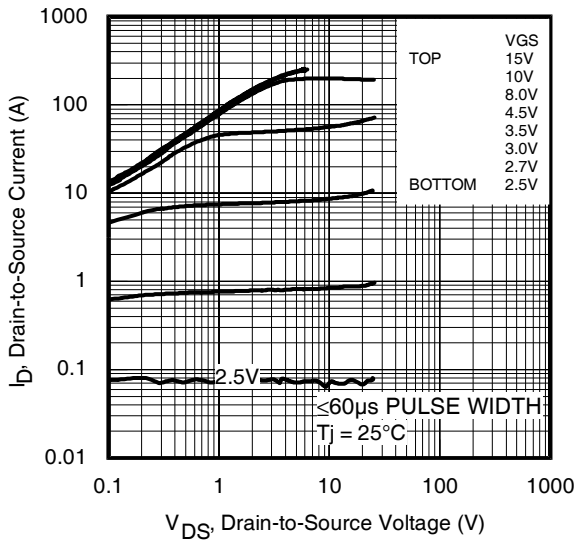
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### Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

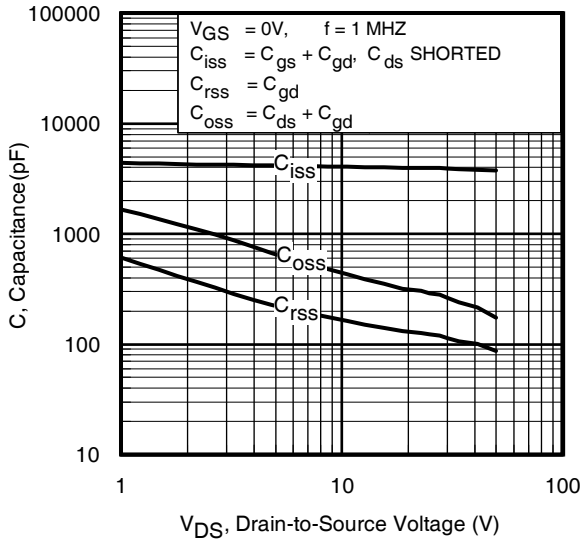
	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.077	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	11	14	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 38A ③
		—	12	16		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 32A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA
g <sub>fs</sub>	Forward Transconductance	52	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 38A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 16V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -16V
Q <sub>g</sub>	Total Gate Charge	—	34	48	nC	I <sub>D</sub> = 38A
Q <sub>gs</sub>	Gate-to-Source Charge	—	10	—		V <sub>DS</sub> = 50V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	15	—		V <sub>GS</sub> = 4.5V ③
t <sub>d(on)</sub>	Turn-On Delay Time	—	24	—	ns	V <sub>DD</sub> = 50V
t <sub>r</sub>	Rise Time	—	110	—		I <sub>D</sub> = 38A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	33	—		R <sub>G</sub> = 3.7Ω
t <sub>f</sub>	Fall Time	—	48	—		V <sub>GS</sub> = 4.5V ③
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	3980	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	310	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	130	—		f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	1820	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	170	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 80V, f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance	—	320	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V ④

### Source-Drain Ratings and Characteristics

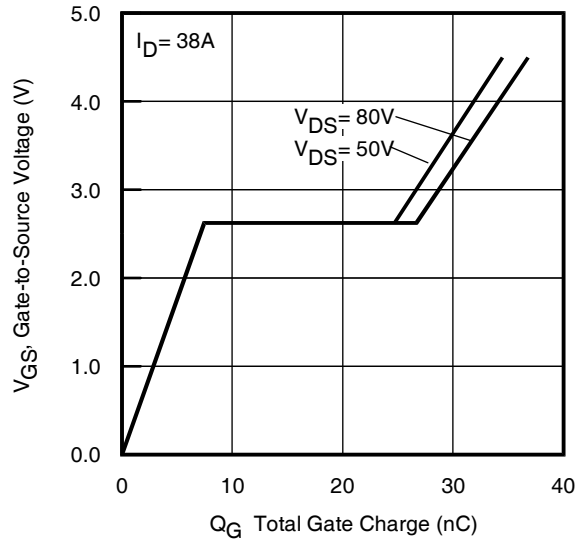
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	63	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	250		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 38A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	34	51	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 38A, V <sub>DD</sub> = 50V
Q <sub>rr</sub>	Reverse Recovery Charge	—	42	63	nC	di/dt = 100A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



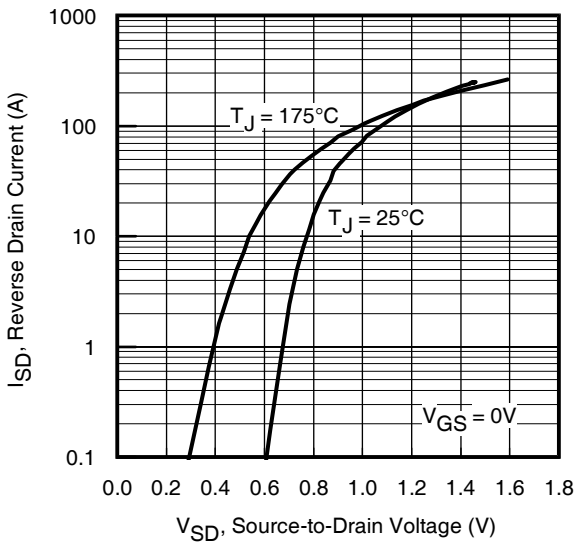
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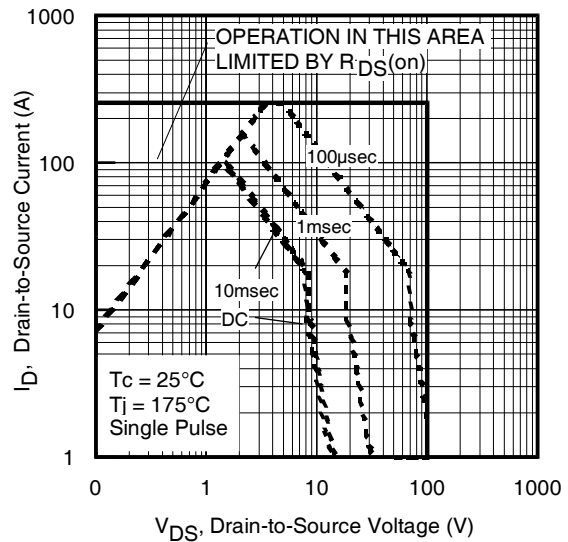
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



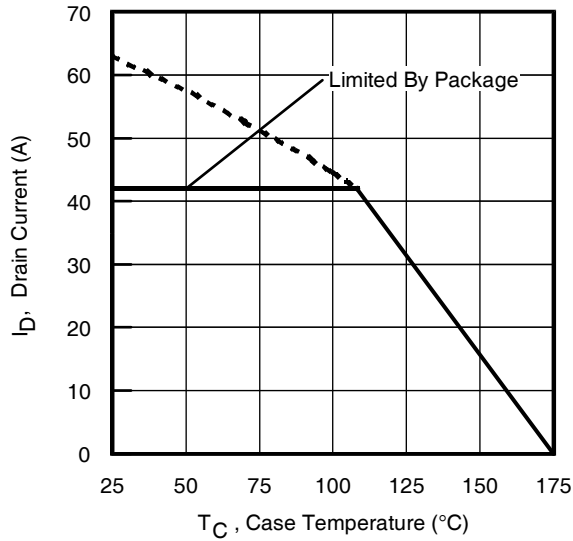
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



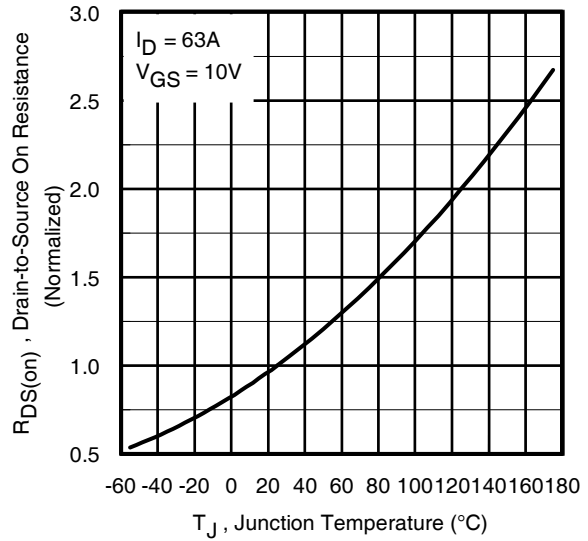
**Fig 7.** Typical Source-Drain Diode Forward Voltage



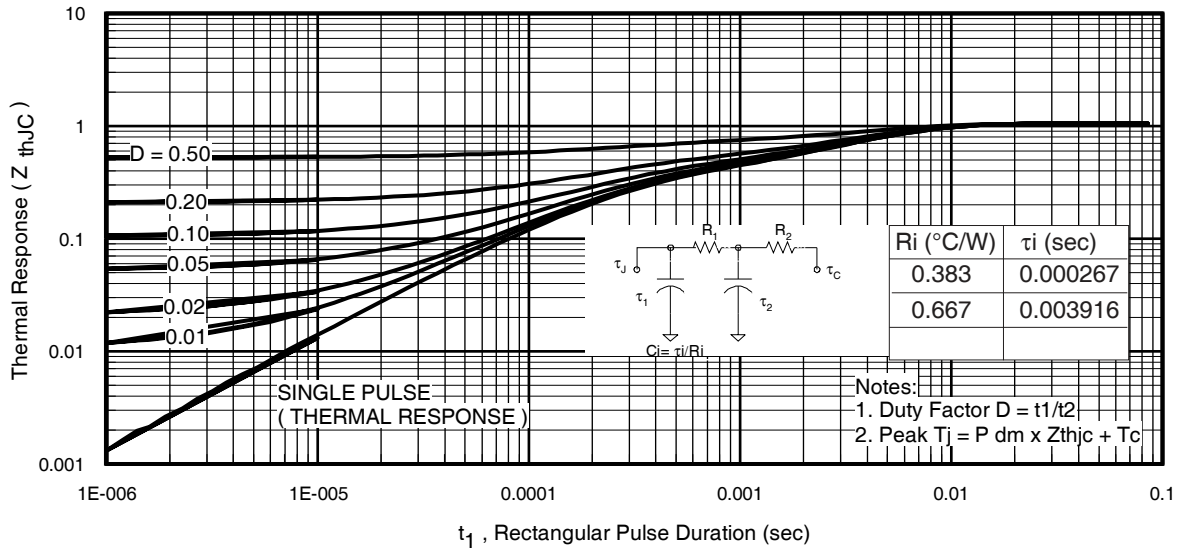
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current vs. Case Temperature

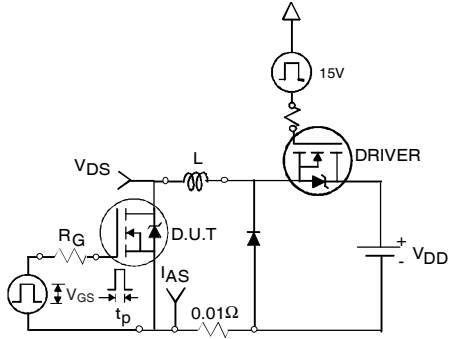


**Fig 10.** Normalized On-Resistance vs. Temperature

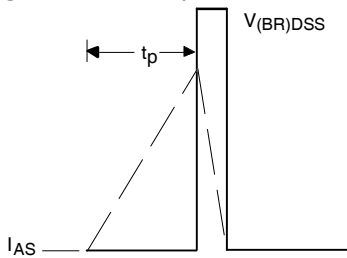


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

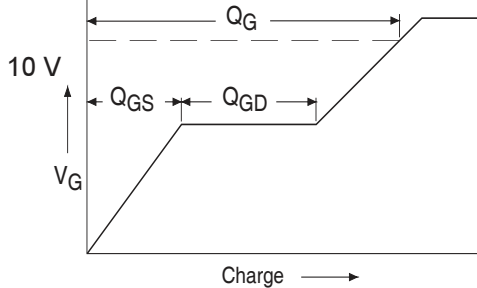
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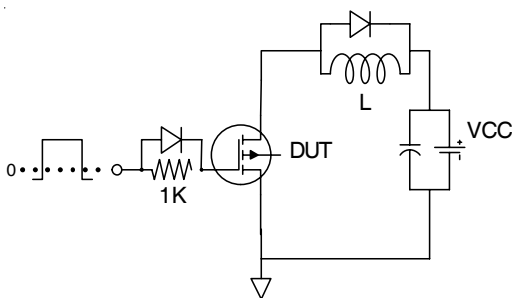
**Fig 12a.** Unclamped Inductive Test Circuit



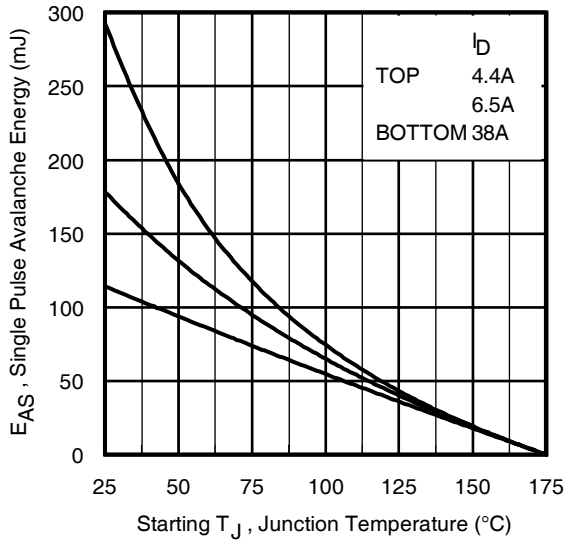
**Fig 12b.** Unclamped Inductive Waveforms



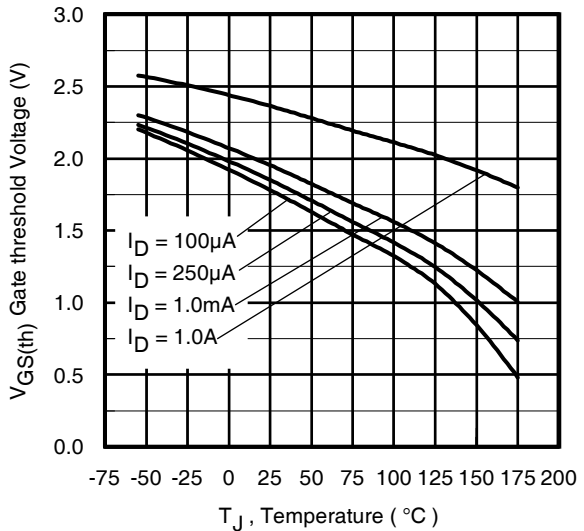
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



**Fig 14.** Threshold Voltage vs. Temperature

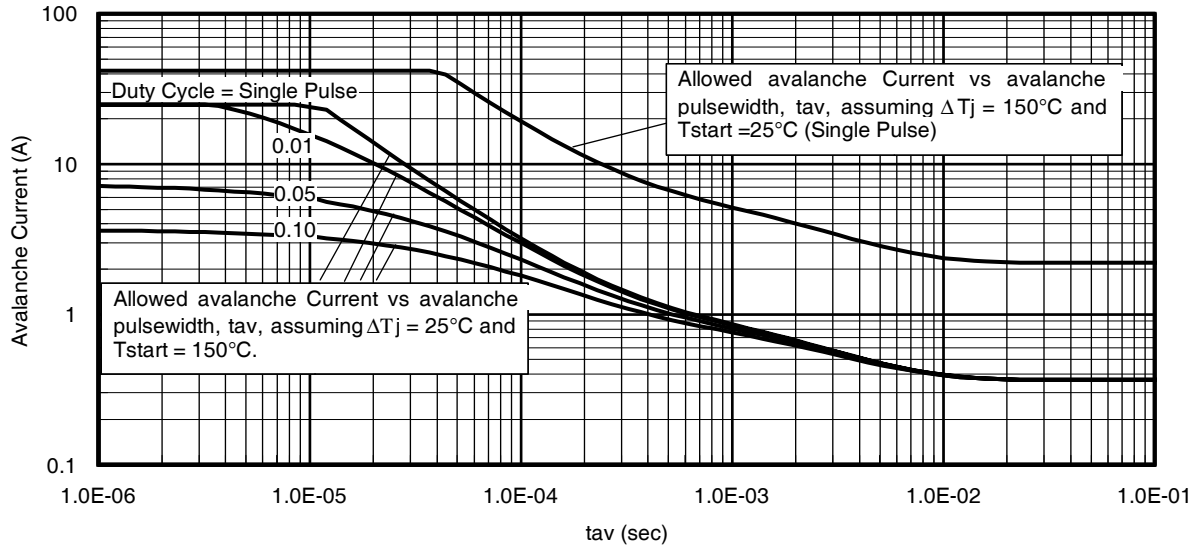


Fig 15. Typical Avalanche Current vs.Pulsewidth

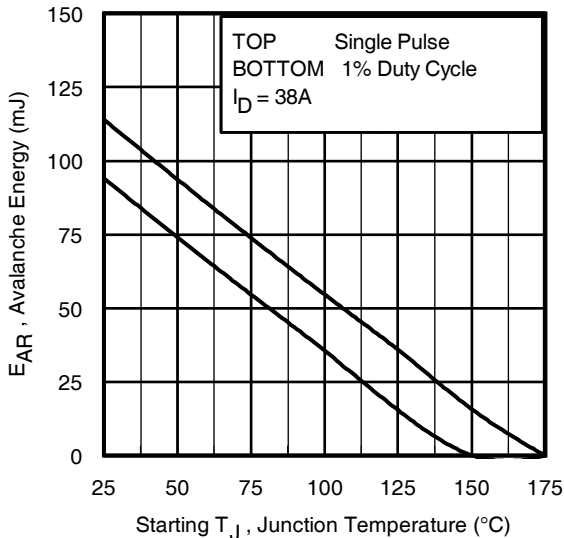


Fig 16. Maximum Avalanche Energy vs. Temperature

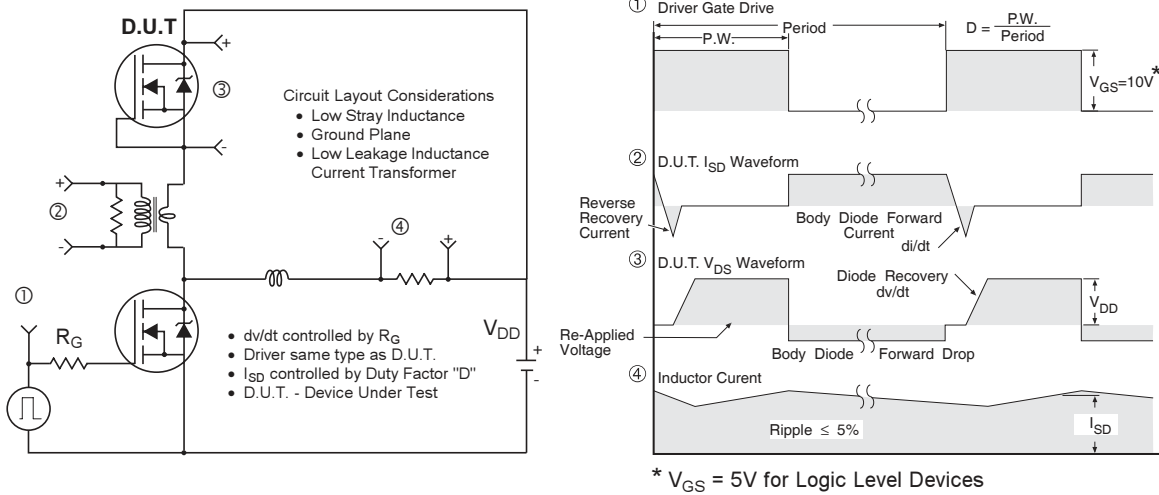
**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as neither  $T_{jmax}$  nor  $I_{av}$  (max) is exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

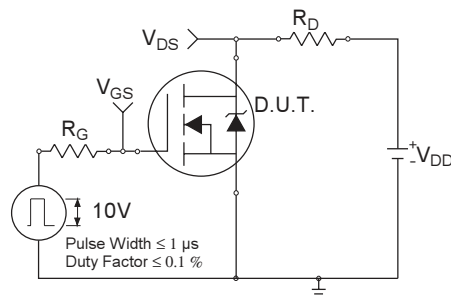
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

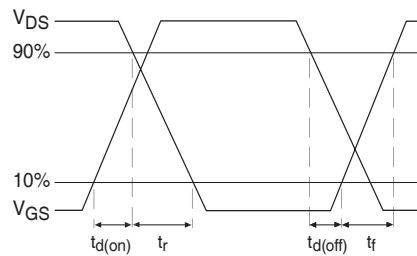
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



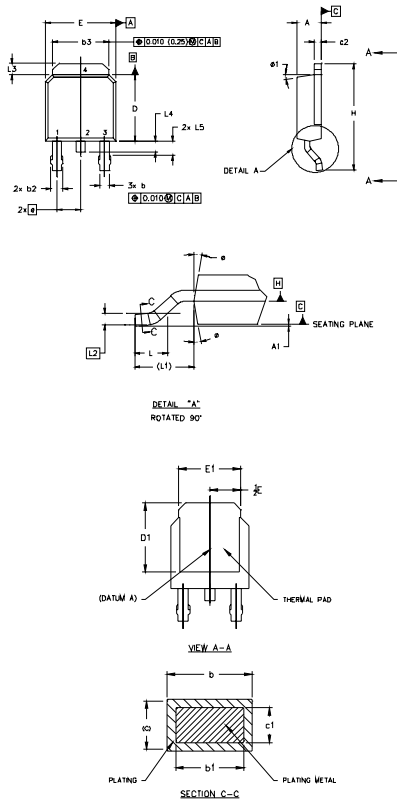
**Fig 18a. Switching Time Test Circuit**



**Fig 18b. Switching Time Waveforms**



## D-Pak (TO-252AA) Package Outline



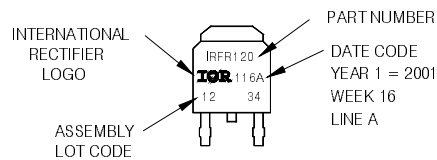
- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
  - 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
  - 3.0 LEAD DIMENSION UNCONTROLLED IN L5
  - 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
  - 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.254] FROM THE LEAD TIP.
  - 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	2.18	2.39	.086	.094		
A1		0.13		.005		
b	0.64	0.89	.025	.035	5	LEAD ASSIGNMENTS
b1	0.64	0.79	.025	0.031	5	
b2	0.76	1.14	.030	.045		HEXFEET
b3	4.95	5.46	.195	.215		1.- GATE
c	0.46	0.61	.018	.024	5	2.- DRAIN
c1	0.41	0.56	.016	.022	5	3.- SOURCE
c2	.046	0.89	.018	.036	5	4.- DRAIN
D	5.97	6.22	.235	.245	6	
D1	5.21	-	.205	-	4	
E	6.35	6.73	.250	.265	6	
E1	4.32	-	.170	-	4	IGBTs, CoPACK
e	2.29		.090 BSC			1.- GATE
H	9.40	10.41	.370	.410		2.- COLLECTOR
L	1.40	1.78	.055	.070		3.- EMITTER
L1	2.74 REF.		.108 REF.			4.- COLLECTOR
L2	0.051 BSC		.020 BSC			
L3	0.89	1.27	.035	.050		
L4		1.02		.040		
L5	1.14	1.52	.045	.060	3	
ø	0"	10"	0"	10"		
ø1	0"	15"	0"	15"		

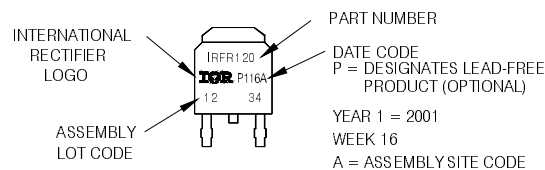
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 2001  
IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position  
indicates 'Lead-Free'



OR

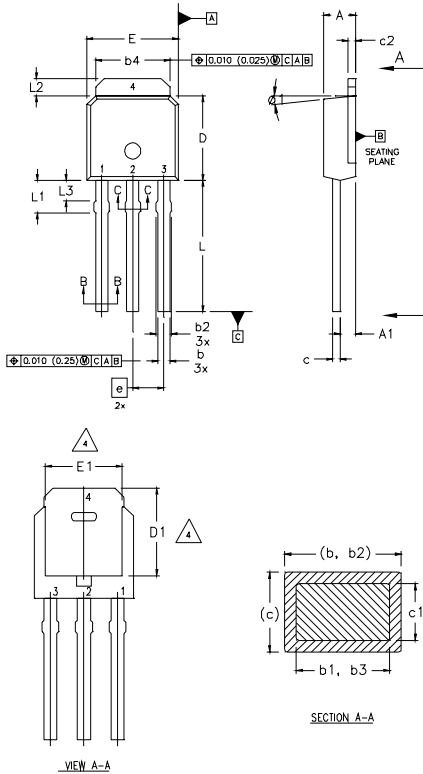


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

# IRLR/U3110ZPbF

International  
**IR** Rectifier

## I-Pak (TO-251AA) Package Outline



- NOTES:
- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
  - 2 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
  - 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
  - 5 LEAD DIMENSION UNCONTROLLED IN L3.
  - 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
  - 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
  - 8 CONTROLLING DIMENSION : INCHES.

### LEAD ASSIGNMENTS

#### HEXFEEET

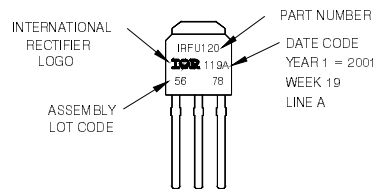
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0"	15"	0"	15"	

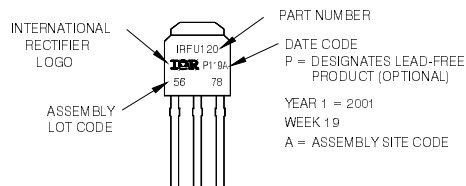
## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 2001  
IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position  
indicates Lead-Free'



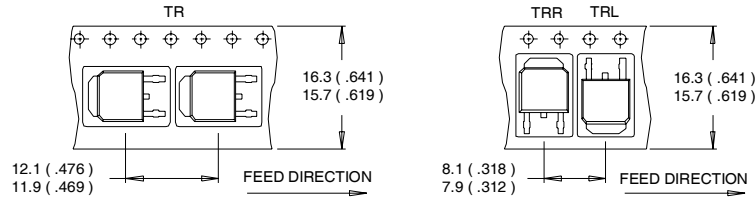
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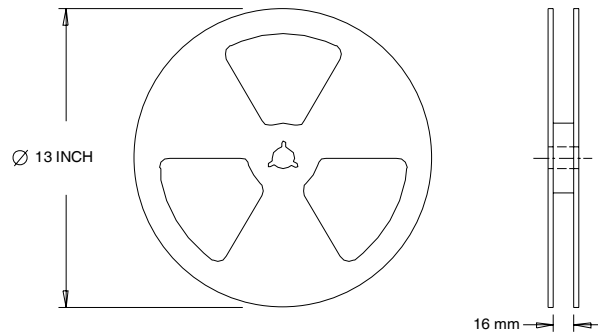
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.16\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 38\text{A}$ ,  $V_{GS} = 10\text{V}$ . Part not recommended for use above this value.
- ③ Pulse width  $\leq 1.0\text{ms}$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑤ Limited by  $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material).
- ⑧  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .

Data and specifications subject to change without notice.  
 This product has been designed for the Industrial market.  
 Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

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