ADS1259-Q1 Automotive, 14.4-kSPS, 24-Bit Analog-to-Digital Converter With Integrated Low-Drift Reference

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Temperature Grade 1: –40°C to 125°C
  - HBM ESD Classification 2
  - CDM ESD Classification C4B
- Programmable Data Rates: 10 SPS to 14.4 kSPS
- Single-Cycle Settling Digital Filter
- High Performance:
  - 21.3 ENOB at 1.2 kSPS
  - INL: 3 ppm
  - Offset Drift: 0.05 µV/°C
  - Gain Drift: 0.5 ppm/°C
- Internal Reference: 2.5 V, 10 ppm/°C Drift
- Internal 2% Accurate Oscillator
- Input Signal Out-of-Range Detection
- Optional Checksum and Redundant Data-Read Capability to Augment Data Integrity
- SPI™-Compatible Interface, Mode 1
- Analog Supply: 5 V or ±2.5 V
- Digital Supply: 2.7 V to 5 V

2 Applications

- Automotive Power Train
- Electrical Vehicles

3 Description

The ADS1259-Q1 is a precision, low-drift, 24-bit, analog-to-digital converter (ADC). The device can perform conversions at data rates up to 14.4 kSPS with high resolution and is therefore ideally suited to measure rapidly changing signals that have a wide dynamic range. An integrated low-noise, low-drift 2.5-V reference eliminates the need for an external voltage reference, thus reducing system cost and component count.

The converter uses a fourth-order, inherently stable, delta-sigma (ΔΣ) modulator that provides outstanding noise performance and linearity. The device can use the integrated oscillator, an external crystal, or an external clock as the ADC clock source.

A fast-responding input overrange detector flags the conversion data if an input overrange event occurs. To augment data integrity in noisy automotive environments the ADS1259-Q1 offers an optional checksum byte and a redundant conversion data-read capability.

The ADS1259-Q1 consumes 13 mW during operation and less than 25 µW when powered down. TI offers the ADS1259-Q1 device in a TSSOP-20 package with full specification from –40°C to 125°C.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
ADS1259QPWRQ1	TSSOP (20)	6,5 mm × 4,4 mm

ADS1259-Q1 Simplified Block Diagram

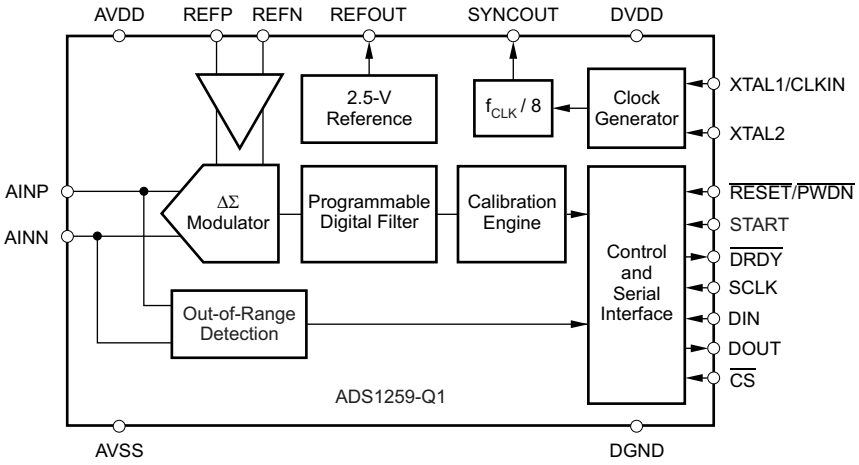


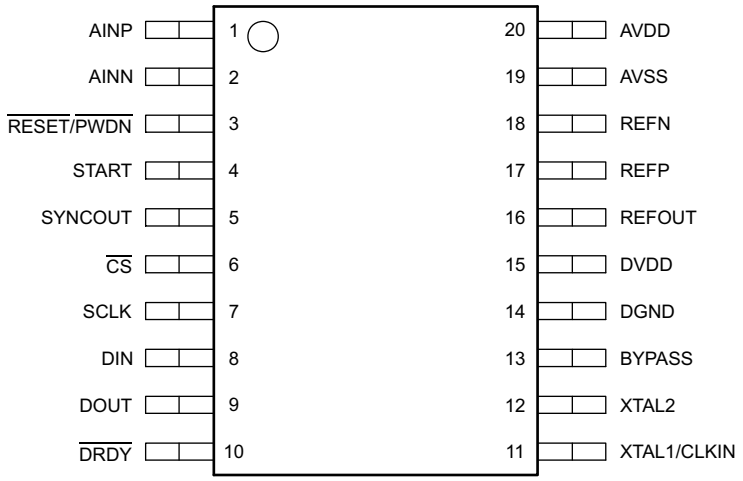
Table of Contents

4 Revision History

DATE	REVISION	NOTES
March 2014	*	Initial release

5 Terminal Configuration and Functions

20-Terminal TSSOP
PW Package
(Top View)



Terminal Functions

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
1	AINP	Analog input	Positive analog input
2	AINN	Analog input	Negative analog input
3	$\overline{\text{RESET}}/\overline{\text{PWDN}}$	Digital input	Reset or power down; reset is active-low; hold low for power down.
4	START	Digital input	Start conversions, active-high
5	SYNCOUT	Digital output	Sync clock output ($f_{(CLK)}$ / 8)
6	$\overline{\text{CS}}$	Digital input	SPI chip-select, active-low
7	SCLK	Digital input	SPI clock input
8	DIN	Digital input	SPI data input
9	DOUT	Digital output	SPI data output
10	$\overline{\text{DRDY}}$	Digital output	Data-ready output, active-low
11	XTAL1/CLKIN	Digital input	Internal oscillator: DGND External clock: clock input Crystal oscillator: external crystal1
12	XTAL2	Digital	External crystal2, otherwise no connection
13	BYPASS	Analog	Core voltage bypass. Connect a 1-µF capacitor to DGND.
14	DGND	Digital	Digital ground
15	DVDD	Digital	Digital power supply
16	REFOUT	Analog output	Positive internal reference output. Connect a 1-µF capacitor, C_{REFOUT}, to AVSS.
17	REFP	Analog input	Positive reference input. Connect a 1-µF capacitor, C_{REFIN}, to REFN.(1)
18	REFN	Analog input	Negative reference input(1)
19	AVSS	Analog	Negative analog power supply and negative internal reference output
20	AVDD	Analog	Positive analog power supply

(1) Leave unused reference inputs unconnected or tie to AVDD.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
AVDD to AVSS		–0.3	7	V
AVSS to DGND		–2.8	0.3	V
DVDD to DGND		–0.3	7	V
Analog input voltage	AINN, AINP, REFN, REFP	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	$\overline{CS}$, DIN, $\overline{RESET}$/$\overline{PDWN}$, SCLK, START, XTAL1/CLKIN	DGND – 0.3	DVDD + 0.3	V
Input current, continuous	Any terminal except supply terminals	–10	10	mA
Operating junction temperature, T_J		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–60	150	°C
$V_{(ESD)}$(1)	Human-body model (HBM) ESD stress voltage(2)	–2	2	kV
	Charged-device model (CDM) ESD stress voltage(2)	–1	1	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity or immunity to damage caused by assembly-line electrostatic discharges into the device.
(2) Meets or exceeds the passing level per AEC-Q100.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
POWER SUPPLY					
Analog power supply	AVDD to AVSS	4.75	5.0	5.25	V
	AVSS to DGND	–2.6	–2.5	0	V
Digital power supply	DVDD to DGND	2.7	3.3	5.25	V
ANALOG INPUTS					
Absolute input voltage	AINP or AINN	AVSS – 0.1		AVDD + 0.1	V
Differential input voltage(1)	$V_{(IN)} = (V_{(AINP)} - V_{(AINN)})$	$-V_{ref}$		V_{ref}	V
VOLTAGE REFERENCE INPUTS					
Reference input voltage	$V_{ref} = (V_{(REFP)} - V_{(REFN)})$	0.5	2.5	AVDD – AVSS + 0.2	V
Absolute negative reference voltage	REFN	AVSS – 0.1	AVSS	REFP – 0.5	V
Absolute positive reference voltage	REFP	REFN + 0.5	AVSS + 2.5	AVDD + 0.1	V
EXTERNAL CLOCK SOURCES ($f_{(CLK)}$)					
Crystal oscillator	Frequency	2	7.3728	8	MHz
External clock	Frequency	0.1	7.3728	8	MHz
	Duty cycle	40%		60%	
DIGITAL INPUTS					
High-level input voltage, V_{IH}		0.8 DVDD		DVDD	V
Low-level input voltage, V_{IL}		DGND		0.2 DVDD	V
TEMPERATURE RANGE					
Operating ambient temperature, T_A		–40		125	°C

(1) Excluding the effects of offset and gain error.

6.4 Thermal Information

THERMAL METRIC(1)		PW (20 TERMINALS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Minimum and maximum specifications are at T_A = –40°C to 125°C. Typical specifications are at T_A = 25°C, AVDD = 2.5 V, AVSS = –2.5 V, DVDD = 3.3 V, external $f_{(CLK)}$ = 7.3728 MHz, external V_{ref} = 2.5 V, and $f_{(DATA)}$ = 60 SPS (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS					
Differential input impedance			120		kΩ
Common-mode input impedance			500		kΩ
SYSTEM PERFORMANCE					
Resolution (no missing codes)		24			Bits
Data rate, $f_{(DATA)}$		10		14,400	SPS
Noise (input referred)	Shorted inputs, See SBAS424 for more information.		0.7		μV_{RMS}
Integral nonlinearity, INL	Best-fit method	–10	±3	10	ppm
Offset voltage (input referred)		–250	±40	250	µV
Offset voltage after calibration(1)			±1		µV
Offset drift	T_A = –40°C to 125°C		0.05	0.25	µV/°C
Gain error(2)		–0.5%	±0.05%	0.5%	
Gain error after calibration(1)			±0.0002%		
Gain drift	T_A = –40°C to 125°C		0.5	2.5	ppm/°C
Normal-mode rejection ratio, NMRR			See SBAS424.		
Common-mode rejection ratio, CMRR	60 Hz, ac(3)	100	120		dB
AVDD, AVSS power-supply rejection ratio, PSRR	60 Hz, ac(3)	85	95		dB
DVDD power supply-rejection ratio, PSRR	60 Hz, ac(3)	85	110		dB
OUT-OF-RANGE DETECTION					
Threshold level	AVSS + 150 mV ≤ $V_{(AINP)}$, $V_{(AINN)}$ ≤ AVDD – 150 mV		±105		%FSR
Threshold level accuracy	AVSS + 150 mV ≤ $V_{(AINP)}$, $V_{(AINN)}$ ≤ AVDD – 150 mV		±0.5		%FSR
VOLTAGE REFERENCE INPUTS					
Average reference input current	AVSS ≤ $V_{(REFP)}$, $V_{(REFN)}$ ≤ AVDD		350		nA
Average reference input current drift			0.2		nA/°C
INTERNAL VOLTAGE REFERENCE					
Reference output voltage	$V_{(REFOUT)}$ = (REFOUT – AVSS)		2.5		V
Accuracy	T_A = 25°C	–0.4%		0.4%	
Temperature drift	T_A = –40°C to 125°C		10	40	ppm/°C
Drive current (sink and source)		–10		10	mA
Load regulation			10		µV/mA
Turn-on settling time	±0.001% settling, C_{REFIN} = 1 µF, C_{REFOUT} = 1 µF		1		s
Long-term stability	0 to 1000 hours		70		ppm
Thermal hysteresis			30		ppm
CLOCK SOURCE ($f_{(CLK)}$)					
Internal oscillator frequency			7.3728		MHz
Internal oscillator accuracy		–2%	±0.2%	2%	
External crystal oscillator start-up time(4)	18-pF load capacitors		20		ms
DIGITAL INPUTS AND OUTPUTS (DVDD = 2.7 V to 5.25 V)					
High-level output voltage, V_{OH}	I_{OH} = 1 mA	0.8 DVDD			V
	I_{OH} = 8 mA		0.75 DVDD		
Low-level output voltage, V_{OL}	I_{OL} = 1 mA			0.2 DVDD	V
	I_{OL} = 8 mA		0.2 DVDD		
Input hysteresis			0.1		V
Input leakage	0 < $V_{(DIGITAL\ INPUT)}$ < DVDD	–10		10	µA

(1) Calibration accuracy is on the level of noise (signal and ADC), reduced by the effect of 16-reading averaging.
(2) Excludes internal reference error.
(3) $f_{(DATA)}$ = 14.4 kSPS. Placing a notch of the digital filter at 60 Hz (setting $f_{(DATA)}$ = 10 SPS or 60 SPS) further improves the common-mode rejection and power-supply rejection of this input frequency.
(4) External crystal start-up time can vary with crystal manufacturer and over temperature.

Electrical Characteristics (continued)

Minimum and maximum specifications are at T_A = –40°C to 125°C. Typical specifications are at T_A = 25°C, AVDD = 2.5 V, AVSS = –2.5 V, DVDD = 3.3 V, external $f_{(CLK)}$ = 7.3728 MHz, external V_{ref} = 2.5 V, and $f_{(DATA)}$ = 60 SPS (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY					
Absolute analog supply current (AVDD, AVSS)	Operating (internal reference enabled)		2.3	5	mA
	Standby mode (internal reference enabled)		200		µA
	Standby mode (internal reference disabled)		1		
	Power-down mode		1		
Digital supply current (DVDD)	Operating (internal oscillator(5))		500	700	µA
	Standby mode (internal oscillator)		160	300	
	Power-down mode (external CLKIN, SCLK stopped, digital inputs maintained at V_{IH} or V_{IL} voltage levels)		1	10	
Power dissipation	Operating (internal reference enabled, internal oscillator)		13	28	mW
	Standby mode (internal reference enabled, internal oscillator)		1.5		
	Standby mode (internal reference disabled, internal oscillator)		0.5		
	Power-down mode		10		µW

(5) Internal oscillator current: 40 µA (typ.)

7 Residue

See SBAS424 for any information on the ADS1259-Q1 device that is not covered in the foregoing sections.

8 Device Documentation and Support

8.1 Trademarks

SPI is a trademark of Motorola.
All other trademarks are the property of their respective owners.

8.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1259QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD1259Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ADS1259-Q1 :

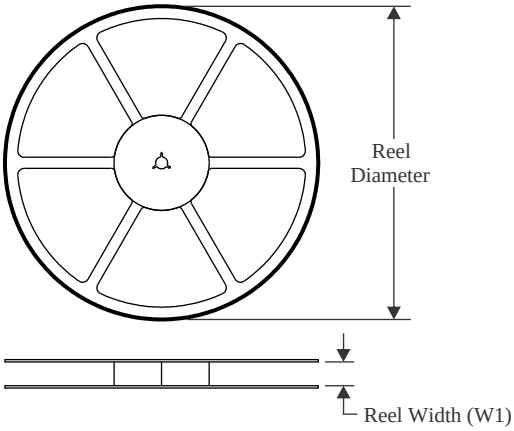
- Catalog: ADS1259

NOTE: Qualified Version Definitions:

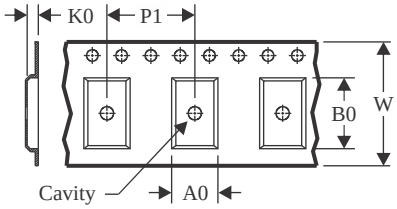
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

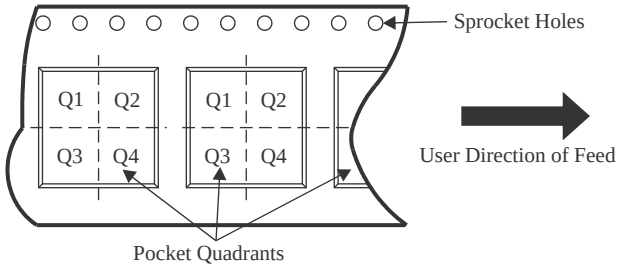


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

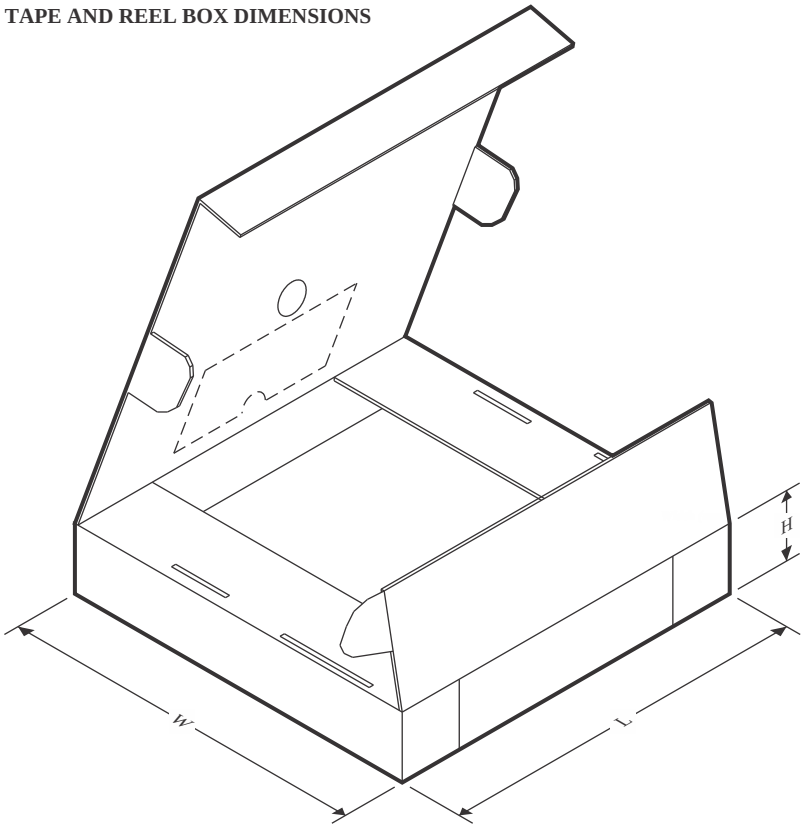
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1259QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

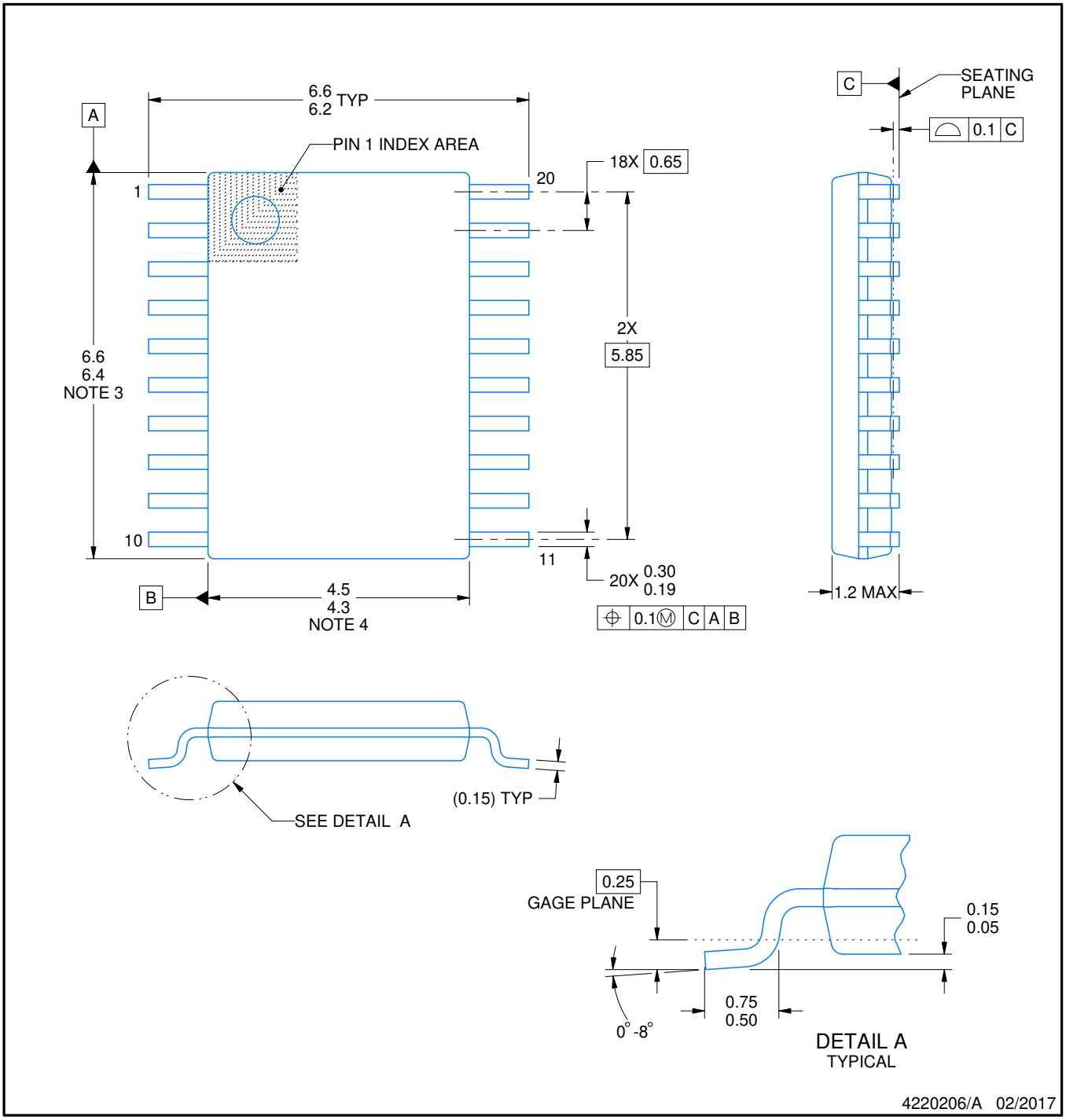
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1259QPWRQ1	TSSOP	PW	20	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0020A

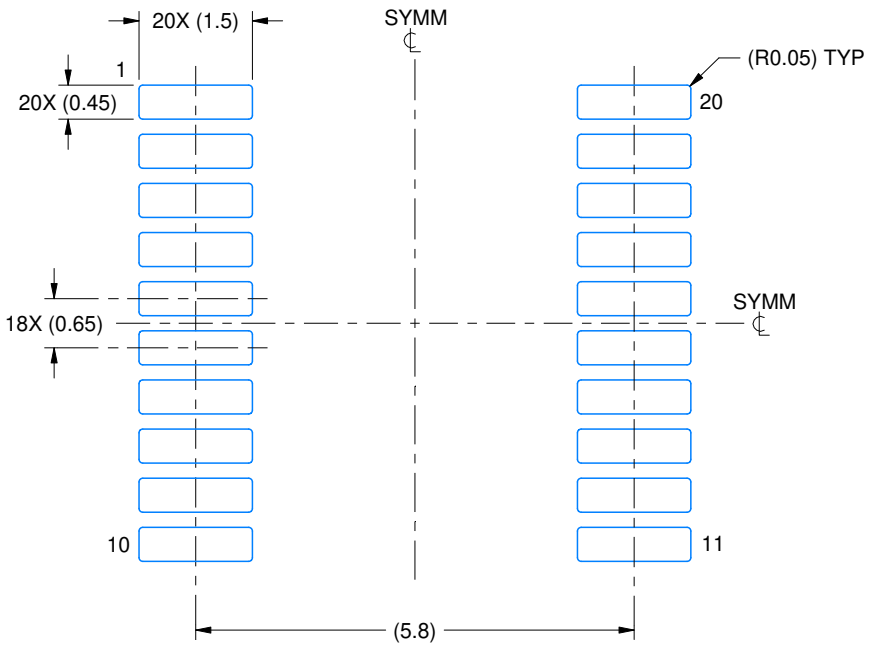
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



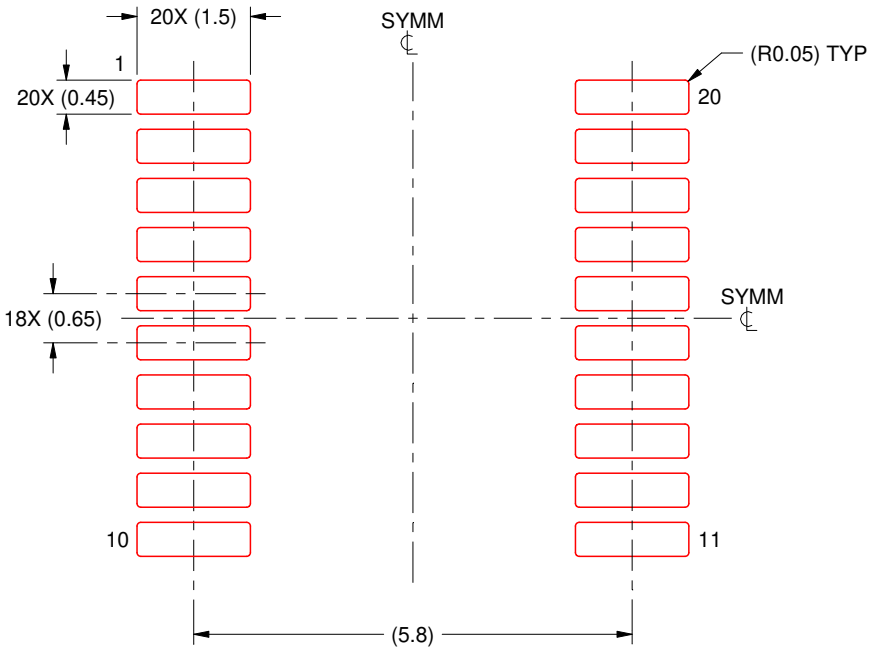
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



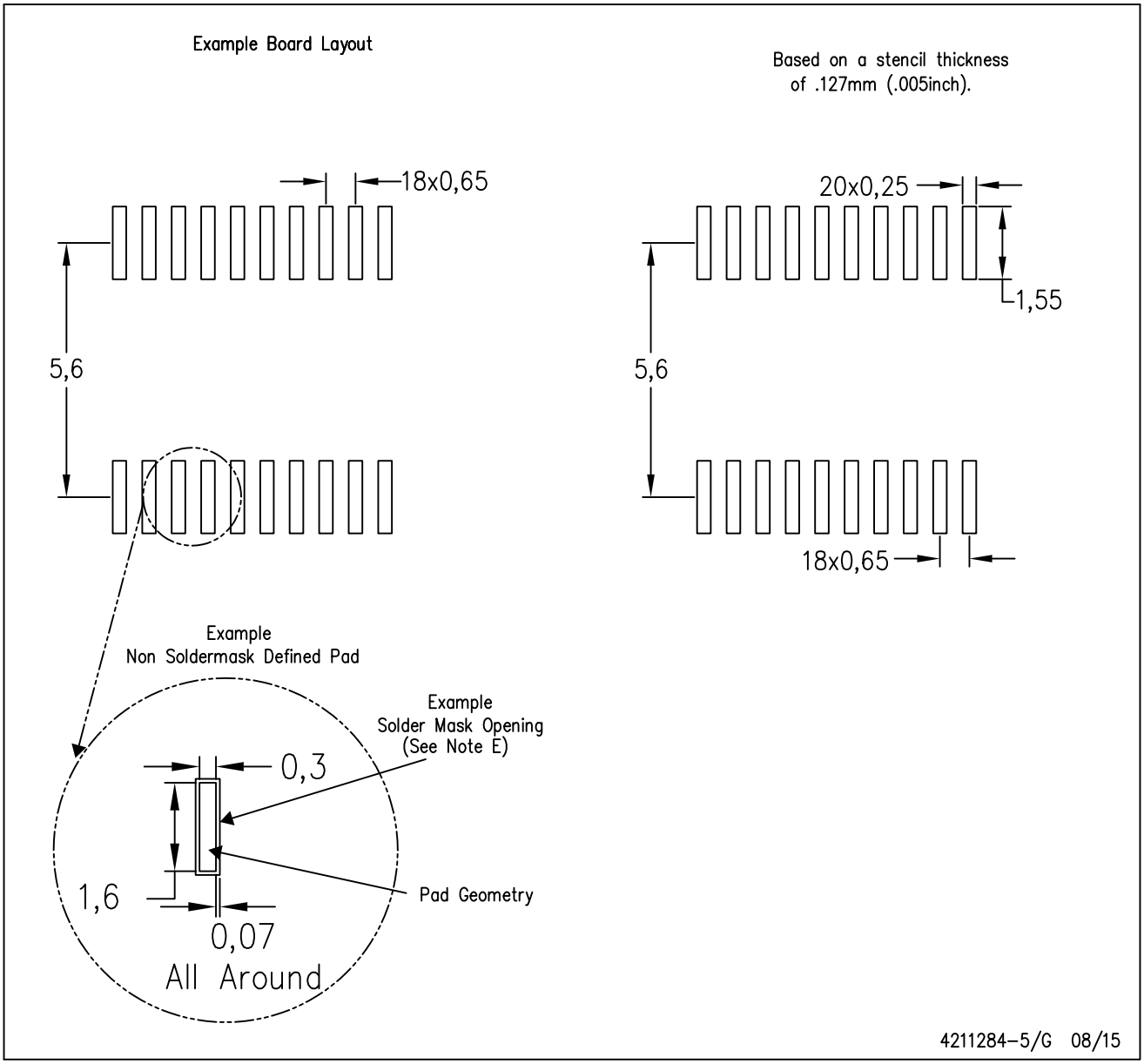
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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