19-1459; Rev 2; 3/02

EVALUATION KIT AVAILABLE

±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

General Description

The MAX104 PECL-compatible, 1Gsps, 8-bit analog-to-digital converter (ADC) allows accurate digitizing of analog signals with bandwidths to 2.2GHz. Fabricated on Maxim's proprietary advanced GST-2 bipolar process, the MAX104 integrates a high-performance track/hold (T/H) amplifier and a quantizer on a single monolithic die.

The innovative design of the internal T/H, which has an exceptionally wide 2.2GHz full-power input bandwidth, results in high performance (greater than 7.5 effective bits) at the Nyquist frequency. A fully differential comparator design and decoding circuitry reduce out-of-sequence code errors (thermometer bubbles or sparkle codes) and provide excellent metastable performance of one error per 10^{16} clock cycles. Unlike other ADCs that can have errors resulting in false full- or zero-scale outputs, the MAX104 limits the error magnitude to 1LSB.

The analog input is designed for either differential or single-ended use with a ±250mV input voltage range. Dual, differential, PECL-compatible output data paths ensure easy interfacing and include an 8:16 demultiplexer feature that reduces output data rates to one-half the sampling clock rate. The PECL outputs can be operated from any supply between +3V to +5V for compatibility with +3.3V or +5V referenced systems. Control inputs are provided for interleaving additional MAX104 devices to increase the effective system sampling rate.

The MAX104 is packaged in a 25mm x 25mm, 192-contact Enhanced Super-Ball Grid Array (ESBGA™) and is specified over the commercial (0°C to +70°C) temperature range.

Applications

Digital RF/IF Signal Processing
Direct RF Downconversion
High-Speed Data Acquisition
Digital Oscilloscopes
High-Energy Physics
Radar/Sonar/ECM Systems
ATE Systems

Typical Operating Circuit appears at end of data sheet.

ESBGA is a trademark of Amkor/Anam.

Features

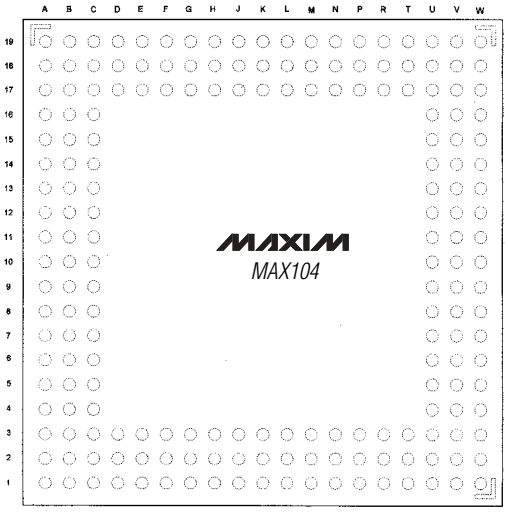
- **1Gsps Conversion Rate**
- **2.2GHz Full-Power Analog Input Bandwidth**
- **>7.5 Effective Bits at f_{IN} = 500MHz (Nyquist Frequency)**
- **±0.25LSB INL and DNL**
- **50Ω Differential Analog Inputs**
- **±250mV Input Signal Range**
- **On-Chip, +2.5V Precision Bandgap Voltage Reference**
- **Latched, Differential PECL Digital Outputs**
- **Low Error Rate: 10^{-16} Metastable States at 1Gsps**
- **Selectable 8:16 Demultiplexer**
- **Internal Demux Reset Input with Reset Output**
- **192-Contact ESBGA Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX104CHC	0°C to +70°C	192 ESBGA

192-Contact ESBGA Ball Assignment Matrix

TOP VIEW



ESBGA

±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

ABSOLUTE MAXIMUM RATINGS

$V_{CC}A$ to GNDA .....-0.3V to +6V
$V_{CC}D$ to GNDD.....-0.3V to +6V
$V_{CC}I$ to GNDI.....-0.3V to +6V
$V_{CC}O$ to GNDD.....-0.3V to ($V_{CC}D$ + 0.3V)
AUXEN1, AUXEN2 to GND .....-0.3V to ($V_{CC}D$ + 0.3V)
V_{EE} to GNDI.....-6V to +0.3V
Between GNDs.....-0.3V to +0.3V
$V_{CC}A$ to $V_{CC}D$ .....-0.3V to +0.3V
$V_{CC}A$ to $V_{CC}I$.....-0.3V to +0.3V
PECL Digital Output Current.....50mA
REFIN to GNDR .....-0.3V to ($V_{CC}I$ + 0.3V)
REFOUT Current .....+100µA to -5mA
ICONST, IPTAT to GNDI .....-0.3V to +1.0V
TTL/CMOS Control Inputs (DEMUXEN, DIVSELECT).....-0.3V to ($V_{CC}D$ + 0.3V)
RSTIN+, RSTIN- .....-0.3V to ($V_{CC}O$ + 0.3V)
VOSADJ Adjust Input .....-0.3V to ($V_{CC}I$ + 0.3V)
CLK+ to CLK- Voltage Difference.....±3V
CLK+, CLK-.....(V_{EE} - 0.3V) to (GNDD + 1V)
CLKCOM.....(V_{EE} - 0.3V) to (GNDD + 1V)
VIN+ to VIN- Voltage Difference .....±2V
VIN+, VIN- to GNDI.....±2V
Continuous Power Dissipation (T_A = +70°C)
192-Contact ESBGA (derate 61mW/°C above +70°C).....4.88W
(with heatsink and 200 LFM airflow, derate 106mW/°C above +70°C) 8.48W
Operating Temperature Range
MAX104CHC.....0°C to +70°C
Operating Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = +5.0V ±5%, V_{EE} = -5.0V ±5%, $V_{CC}O$ = +3.0V to $V_{CC}D$, REFIN connected to REFOUT, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	RES		8			Bits
Integral Nonlinearity (Note 1)	INL	T_A = +25°C	-0.5	±0.25	0.5	LSB
Differential Nonlinearity (Note 1)	DNL	T_A = +25°C	-0.5	±0.25	0.5	LSB
Missing Codes		No missing codes guaranteed			None	Codes
ANALOG INPUTS						
Full-Scale Input Range	V_{FSR}	Note 1	475	500	525	mVp-p
Common-Mode Input Range	V_{CM}	Signal + offset w.r.t. GNDI		±0.8		V
Input Resistance	R_{IN}	VIN+ and VIN- to GNDI, T_A = +25°C	49	50	51	Ω
Input Resistance Temperature Coefficient	TC_R			150		ppm/°C
VOS ADJUST CONTROL INPUT						
Input Resistance (Note 2)	R_{VOS}		14	25		kΩ
Input V_{OS} Adjust Range		VOSADJ = 0 to 2.5V	±4	±5.5		LSB
REFERENCE INPUT AND OUTPUT						
Reference Output Voltage	REFOUT	Driving REFIN input only	2.475	2.50	2.525	V
Reference Output Load Regulation	ΔREFOUT	0 < I_{SOURCE} < 2.5mA			5	mV
Reference Input Resistance	R_{REF}	Referenced to GNDR	4	5		kΩ

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = +5.0V ±5%, V_{EE} = -5.0V ±5%, $V_{CC}O$ = +3.0V to $V_{CC}D$, REFIN connected to REFOUT, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUTS (Note 3)						
Clock Input Resistance	R_{CLK}	CLK+ and CLK- to CLKCOM, T_A = +25°C	48	50	52	Ω
Input Resistance Temperature Coefficient	TC_R			150		ppm/°C
TTL/CMOS CONTROL INPUTS (DEMUXEN, DIVSELECT)						
High-Level Input Voltage	V_{IH}		2.0			V
Low-Level Input Voltage	V_{IL}				0.8	V
High-Level Input Current	I_{IH}	V_{IH} = 2.4V			50	µA
Low-Level Input Current	I_{IL}	V_{IL} = 0	-1		1	µA
DEMUX RESET INPUT (Note 4)						
Digital Input High Voltage	V_{IH}		-1.165			V
Digital Input Low Voltage	V_{IL}				-1.475	V
PECL DIGITAL OUTPUTS (Note 5)						
Digital Output High Voltage	V_{OH}		-1.025		-0.880	V
Digital Output Low Voltage	V_{OL}		-1.810		-1.620	V
POWER REQUIREMENTS						
Positive Analog Supply Current	$I_{CC}A$			480	780	mA
Positive Input Supply Current	$I_{CC}I$			108	150	mA
Negative Input Supply Current	I_{EE}		-290	-210		mA
Digital Supply Current	$I_{CC}D$			205	340	mA
Output Supply Current (Note 6)	$I_{CC}O$			75	115	mA
Power Dissipation (Note 6)	P_{DISS}			5.25		W
Common-Mode Rejection Ratio (Note 7)	CMRR	VIN+ = VIN- = ±0.1V	40	68		dB
Positive Power-Supply Rejection Ratio (Note 8)	PSRR+	(Note 9)	40	73		dB
Negative Power-Supply Rejection Ratio (Note 8)	PSRR-	(Note 10)	40	68		dB

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AC ELECTRICAL CHARACTERISTICS

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = 5.0V, V_{EE} = -5.0V, $V_{CC}O$ = 3.3V, REFIN connected to REFOUT, f_S = 1Gsps, f_{IN} at -1dBFS, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG INPUT							
Analog Input Full-Power Bandwidth	BW_{-3dB}				2.2		GHz
Analog Input VSWR	VSWR	f_{IN} = 500MHz			1.1:1		V/V
Transfer Curve Offset	V_{OS}	VOSADJ control input open		-2	0	+2	LSB
DYNAMIC SPECIFICATIONS							
Effective Number of Bits (Note 11)	$ENOB_{1000}$	f_{IN} = 1000MHz	Differential		7.52		Bits
			Single-ended		7.40		
	$ENOB_{500}$	f_{IN} = 500MHz	Differential	7.2	7.55		
			Single-ended		7.49		
	$ENOB_{125}$	f_{IN} = 125MHz	Differential	7.4	7.74		
			Single-ended		7.73		
Signal-to-Noise Ratio (No Harmonics)	SNR_{1000}	f_{IN} = 1000MHz	Differential		46.4		dB
			Single-ended		46.4		
	SNR_{500}	f_{IN} = 500MHz	Differential	44.2	47.0		
			Single-ended		47.1		
	SNR_{125}	f_{IN} = 125MHz	Differential	45.4	47.4		
			Single-ended		47.4		
Total Harmonic Distortion (Note 12)	THD_{1000}	f_{IN} = 1000MHz	Differential		-52.6		dB
			Single-ended		-49.6		
	THD_{500}	f_{IN} = 500MHz	Differential		-52.5	-50	
			Single-ended		-51.3		
	THD_{125}	f_{IN} = 125MHz	Differential		-66.2	-61	
			Single-ended		-67.4		
Spurious-Free Dynamic Range	$SFDR_{1000}$	f_{IN} = 1000MHz	Differential		52.8		dB
			Single-ended		52.5		
	$SFDR_{500}$	f_{IN} = 500MHz	Differential	50	52.3		
			Single-ended		52.3		
	$SFDR_{125}$	f_{IN} = 125MHz	Differential	62	68.9		
			Single-ended		69.5		
Signal-to-Noise Ratio and Distortion	$SINAD_{1000}$	f_{IN} = 1000MHz	Differential		46.0		dB
			Single-ended		46.3		
	$SINAD_{500}$	f_{IN} = 500MHz	Differential	44.1	46.2		
			Single-ended		45.9		
	$SINAD_{125}$	f_{IN} = 125MHz	Differential	45.3	47.3		
			Single-ended		47.3		
Two-Tone Intermodulation	IMD	f_{IN1} = 124MHz, f_{IN2} = 126MHz, at -7dB below full-scale			-57.7		dB

AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = +5.0V, V_{EE} = -5.0V, $V_{CC}O$ = +3.3V, REFIN connected to REFOUT, f_S = 1Gsps, f_{IN} at -1dBFS, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS							
Maximum Sample Rate	f_{MAX}			1			Gsps
Clock Pulse Width Low	t_{PWL}	Figure 17		0.45			ns
Clock Pulse Width High	t_{PWH}	Figure 17		0.45		5	ns
Aperture Delay	t_{AD}	Figure 4			100		ps
Aperture Jitter	t_{AJ}	Figure 4			<0.5		ps
Reset Input Data Setup Time (Note 13)	t_{SU}	Figure 15		0			ps
Reset Input Data Hold Time (Note 13)	t_{HD}	Figure 15		0			ps
CLK to DREADY Propagation Delay	t_{PD1}	Figure 17			2.2		ns
DREADY to DATA Propagation Delay (Note 14)	t_{PD2}	Figure 17		-50	150	350	ps
DATA Rise Time	t_{RDATA}	20% to 80%, C_L = 3pF			420		ps
DATA Fall Time	t_{FDATA}	20% to 80%, C_L = 3pF			360		ps
DREADY Rise Time	$t_{RDREADY}$	20% to 80%, C_L = 3pF			220		ps
DREADY Fall Time	$t_{FDREADY}$	20% to 80%, C_L = 3pF			180		ps
Primary Port Pipeline Delay	t_{PDP}	Figures 6, 7, 8	DIV1, DIV2 modes		7.5		Clock Cycles
			DIV4 mode		7.5		
Auxiliary Port Pipeline Delay	t_{PDA}	Figures 6, 7, 8	DIV1, DIV2 modes		8.5		Clock Cycles
			DIV4 mode		9.5		

Note 1: Static linearity parameters are computed from a "best-fit" straight line through the code transition points. The full-scale range (FSR) is defined as 256 x slope of the line.

Note 2: The offset control input is a self-biased voltage divider from the internal +2.5V reference voltage. The nominal open-circuit voltage is +1.25V. It may be driven from an external potentiometer connected between REFOUT and GNDI.

Note 3: The clock input's termination voltage can be operated between -2.0V and GNDI. Observe the absolute maximum ratings on the CLK+ and CLK- inputs.

Note 4: Input logic levels are measured with respect to the $V_{CC}O$ power-supply voltage.

Note 5: All PECL digital outputs are loaded with 50Ω to $V_{CC}O$ - 2.0V. Measurements are made with respect to the $V_{CC}O$ power-supply voltage.

Note 6: The current in the $V_{CC}O$ power supply does not include the current in the digital output's emitter followers, which is a function of the load resistance and the V_{TT} termination voltage.

Note 7: Common-Mode Rejection Ratio is defined as the ratio of the change in the transfer-curve offset voltage to the change in the common-mode voltage, expressed in dB.

Note 8: Power-Supply Rejection Ratio is defined as the ratio of the change in the transfer-curve offset voltage to the change in power-supply voltage, expressed in dB.

Note 9: Measured with the positive supplies tied to the same potential; $V_{CC}A$ = $V_{CC}D$ = $V_{CC}I$. V_{CC} varies from +4.75V to +5.25V.

Note 10: V_{EE} varies from -5.25V to -4.75V.

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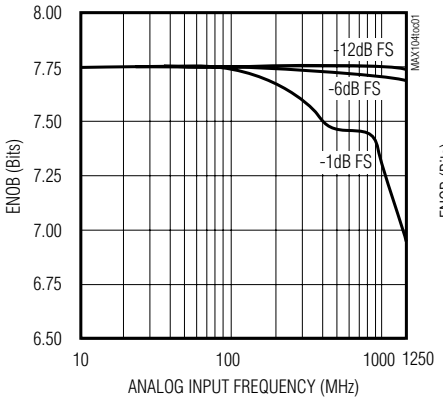
Note 11: Effective Number of Bits (ENOB) are computed from a curve fit referenced to the theoretical full-scale range.
Note 12: Total Harmonic Distortion (THD) is computed from the first five harmonics.
Note 13: Guaranteed by design with a reset pulse one clock period long or greater.
Note 14: Guaranteed by design. The DREADY to DATA propagation delay is measured from the 50% point on the rising edge of the DREADY signal (when the output data changes) to the 50% point on a data output bit. This places the falling edge of the DREADY signal in the middle of the data output valid window, within the differences between the DREADY and DATA rise and fall times, which gives maximum setup and hold time for latching external data latches.

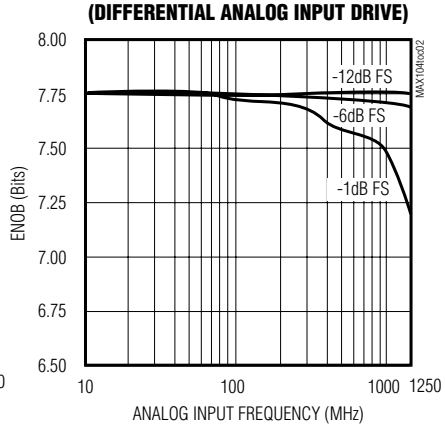
Typical Operating Characteristics

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = +5V, V_{EE} = -5V, $V_{CC}O$ = +3.3V, REFIN connected to REFOUT, f_S = 1Gsps, T_A = +25°C, unless otherwise noted.)

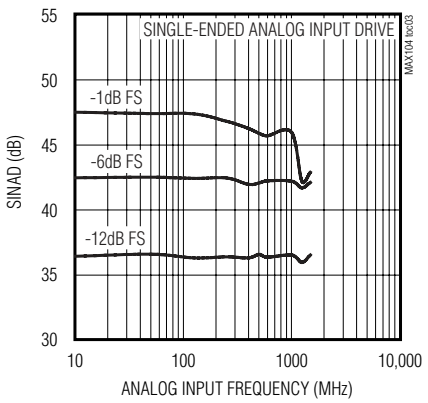
EFFECTIVE NUMBER OF BITS vs. ANALOG INPUT FREQUENCY (SINGLE-ENDED ANALOG INPUT DRIVE)



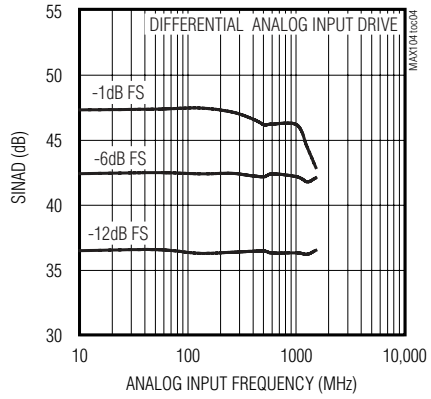
EFFECTIVE NUMBER OF BITS vs. ANALOG INPUT FREQUENCY (DIFFERENTIAL ANALOG INPUT DRIVE)



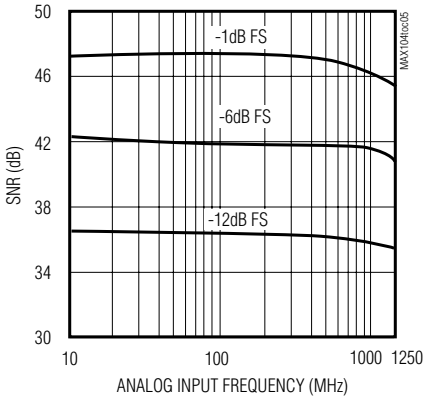
SIGNAL-TO-NOISE + DISTORTION vs. ANALOG INPUT FREQUENCY



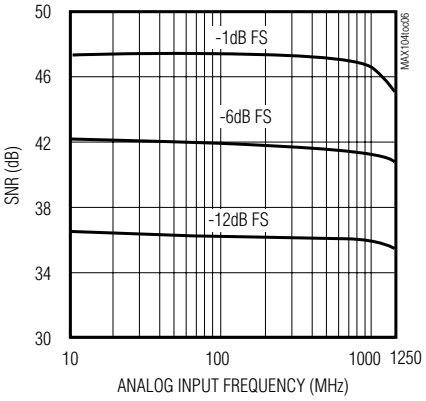
SIGNAL-TO-NOISE + DISTORTION vs. ANALOG INPUT FREQUENCY



SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY (SINGLE-ENDED ANALOG INPUT DRIVE)



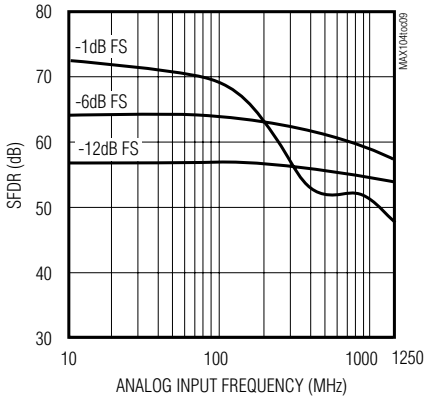
SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY (DIFFERENTIAL ANALOG INPUT DRIVE)



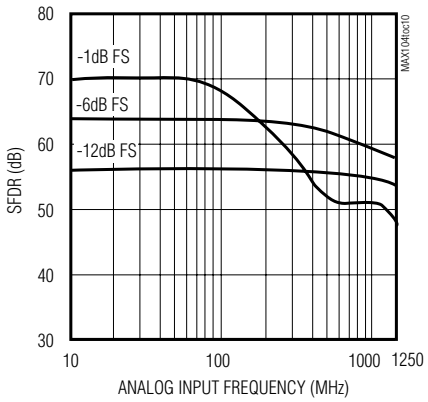
Typical Operating Characteristics (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = +5V, V_{EE} = -5V, $V_{CC}O$ = +3.3V, REFIN connected to REFOUT, f_S = 1Gsps, T_A = +25°C, unless otherwise noted.)

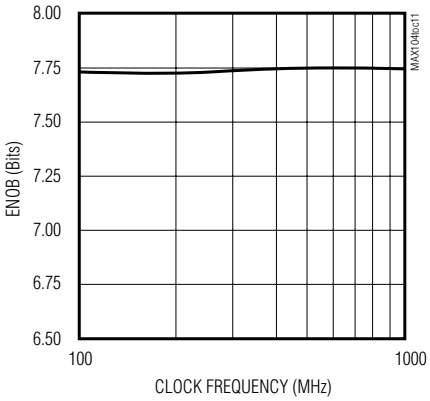
SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY (SINGLE-ENDED ANALOG INPUT DRIVE)



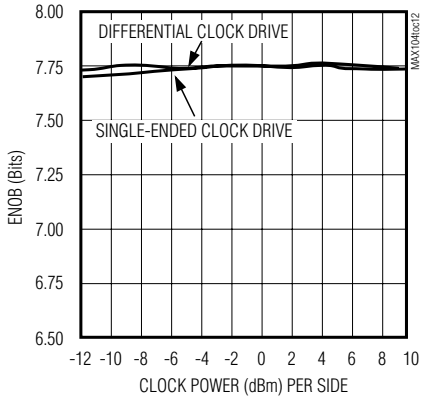
SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY (DIFFERENTIAL ANALOG INPUT DRIVE)



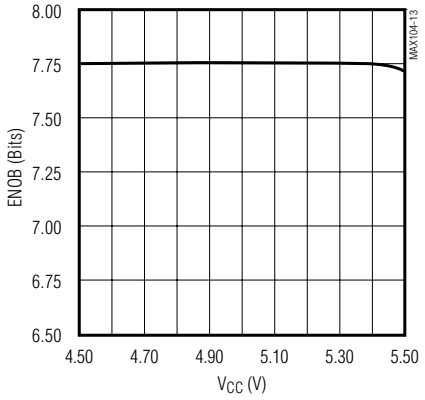
EFFECTIVE NUMBER OF BITS vs. CLOCK FREQUENCY (f_{IN} = 125MHz, -1dB FS)



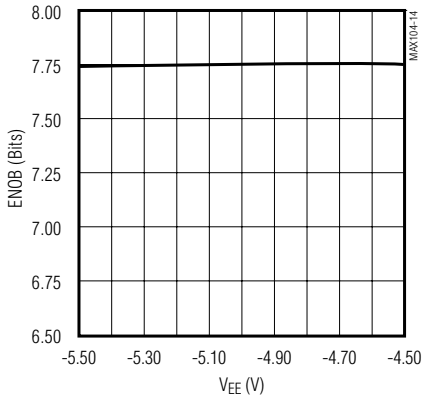
EFFECTIVE NUMBER OF BITS vs. CLOCK POWER (f_{IN} = 125MHz, -1dB FS)



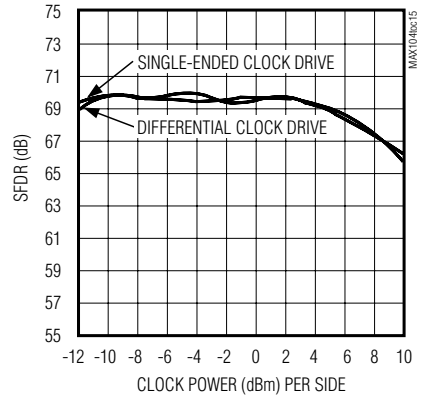
EFFECTIVE NUMBER OF BITS vs. $V_{CC}I$ = $V_{CC}A$ = $V_{CC}D$ (f_{IN} = 125MHz, -1dB FS)



EFFECTIVE NUMBER OF BITS vs. V_{EE} (f_{IN} = 125MHz, -1dB FS)



SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK POWER (f_{IN} = 125MHz, -1dB FS)

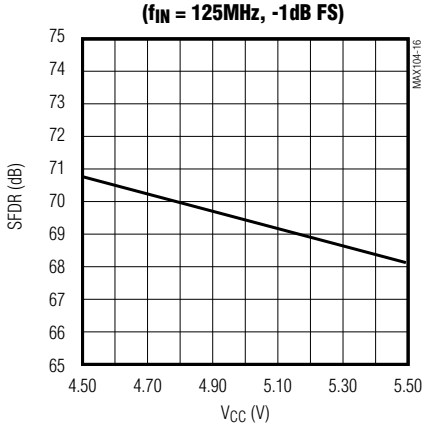


±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

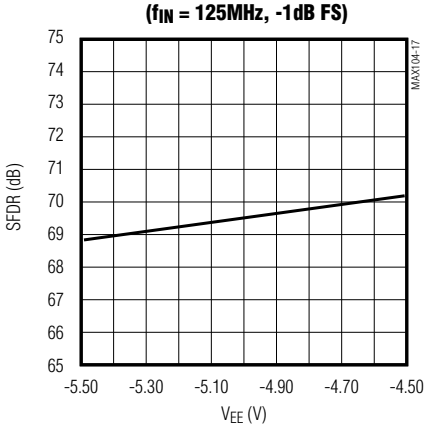
Typical Operating Characteristics (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = +5V, V_{EE} = -5V, $V_{CC}O$ = +3.3V, REFIN connected to REFOUT, f_S = 1Gsps, T_A = +25°C, unless otherwise noted.)

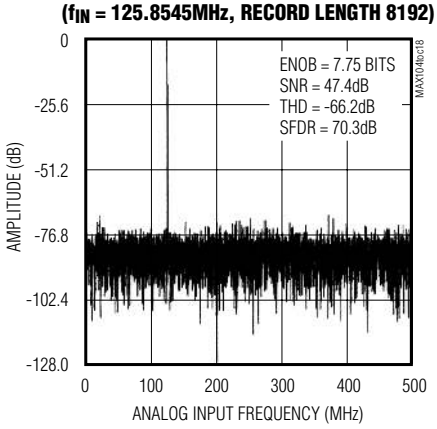
SPURIOUS-FREE DYNAMIC RANGE vs. $V_{CC}I$ = $V_{CC}A$ = $V_{CC}D$ (f_{IN} = 125MHz, -1dB FS)



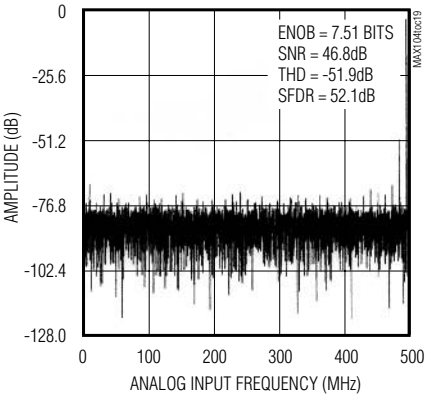
SPURIOUS-FREE DYNAMIC RANGE vs. V_{EE} (f_{IN} = 125MHz, -1dB FS)



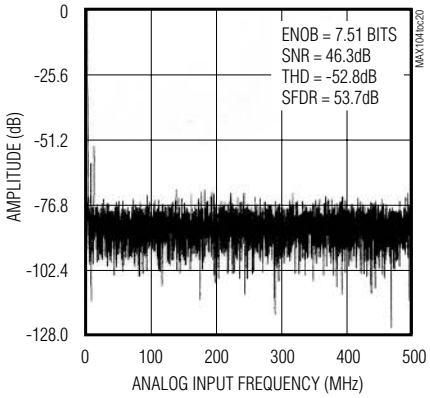
FFT PLOT (f_{IN} = 125.8545MHz, RECORD LENGTH 8192)



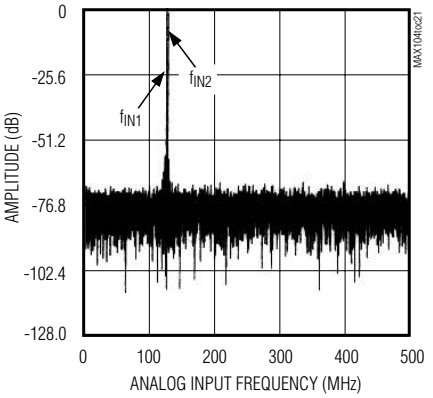
FFT PLOT (f_{IN} = 494.5068MHz, RECORD LENGTH 8192)



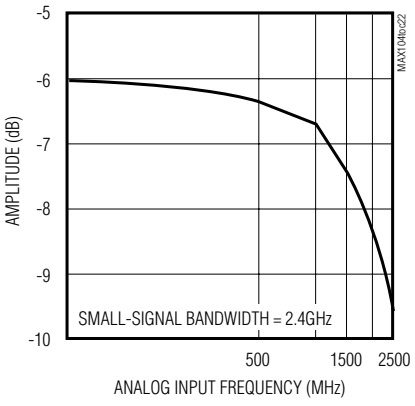
FFT PLOT (f_{IN} = 1005.0049MHz, RECORD LENGTH 8192)



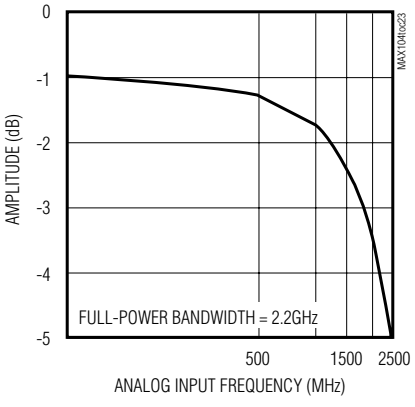
TWO-TONE INTERMODULATION FFT PLOT (f_{IN1} = 124MHz, f_{IN2} = 126MHz, 7dB BELOW FULL-SCALE, RECORD LENGTH 8192)



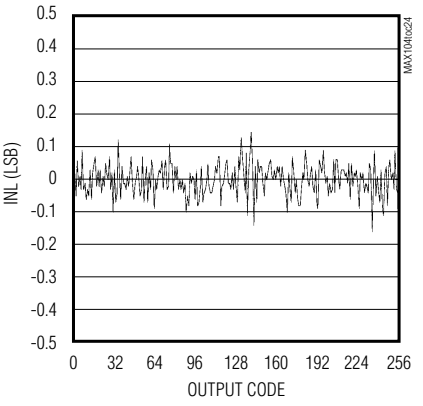
ANALOG INPUT BANDWIDTH -6dB BELOW FULL-SCALE



ANALOG INPUT BANDWIDTH FULL-POWER



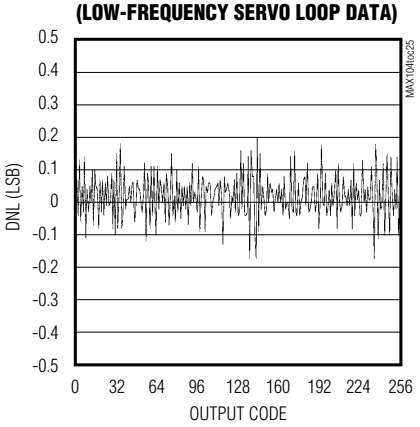
INTEGRAL NONLINEARITY vs. OUTPUT CODE (LOW-FREQUENCY SERVO LOOP DATA)



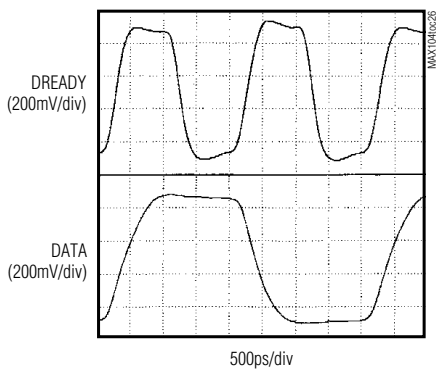
Typical Operating Characteristics (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = +5V, V_{EE} = -5V, $V_{CC}O$ = +3.3V, REFIN connected to REFOUT, f_S = 1Gsps, T_A = +25°C, unless otherwise noted.)

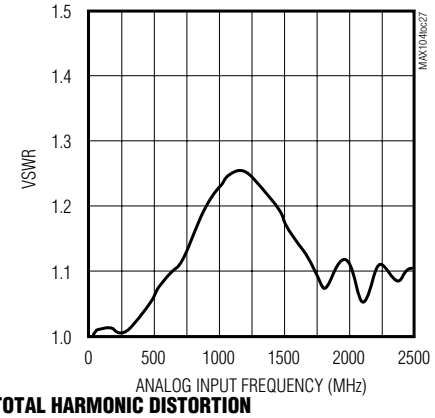
DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE (LOW-FREQUENCY SERVO LOOP DATA)



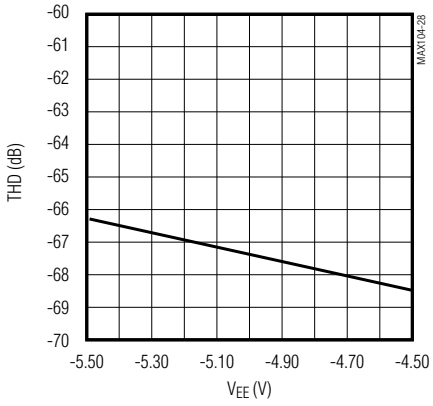
DREADY RISE/FALL TIME, DATA OUTPUT RISE/FALL TIME



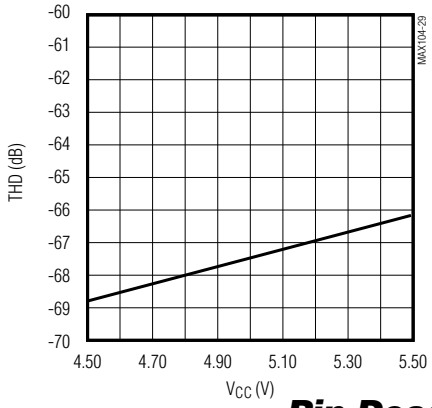
VSWR vs. ANALOG INPUT FREQUENCY



TOTAL HARMONIC DISTORTION vs. V_{EE} (f_{IN} = 125MHz, -1dB FS)



TOTAL HARMONIC DISTORTION vs. $V_{CC}I$ = $V_{CC}A$ = $V_{CC}D$ (f_{IN} = 125MHz, -1dB FS)



Pin Description

CONTACT	NAME	FUNCTION
A1–A4, A6, A7, B1, B2, C1, C2, D1, D2, D3, G1, H1, J2, J3, K1–K3, L2, L3, M1, N1, T2, T3, U1, V1, V2, W1–W4	GNDI	Analog Ground. For T/H amplifier, clock distribution, bandgap reference, and reference amplifier.
A5, B5, C5, H2, H3, M2, M3, U5, V5, W5	$V_{CC}I$	Analog Supply Voltage, +5V. Supplies T/H amplifier, clock distribution, bandgap reference, and reference amplifier.
A8, B8, C8, U6, V6, W6	GNDA	Analog Ground. For comparator array.
A9, B9, C9, U7, V7, W7	$V_{CC}A$	Analog Supply Voltage, +5V. Supplies analog comparator array.
A10, E17, F2, P3, R17, R18	TESTPOINT (T.P.)	Test Point. **Do not connect.**
A11, B11, B16, B17, C11, C16, U9, U17, V9, V17, V18, W9	GNDD	Digital Ground
A12–A19, B19, C19, D19, E19, F19, G19, H19, J19, K19, L19, M19, N19, P19, T19, U19, V19, W10-W19	$V_{CC}O$	PECL Supply Voltage, +3V to +5V

±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

Pin Description (continued)

CONTACT	NAME	FUNCTION
B3, B4, C3, C4, E3, F3, G2, G3, N2, N3, U2, U3, U4, V3, V4	V_{EE}	Analog Supply Voltage, -5V. Supplies T/H amplifier, clock distribution, bandgap reference, and reference amplifier.
B6, B7	GNDR	Reference Ground. **Must** be connected to GNDI.
B10, B18, C10, C17, C18, T17, T18, U8, U18, V8, W8	$V_{CC}D$	Digital Supply Voltage, +5V
B12	P0+	Primary Output Data Bit 0 (LSB)
B13	A0+	Auxiliary Output Data Bit 0 (LSB)
B14	P1+	Primary Output Data Bit 1
B15	A1+	Auxiliary Output Data Bit 1
C6	REFIN	Reference Input
C7	REFOUT	Reference Output
C12	P0-	Complementary Primary Output Data Bit 0 (LSB)
C13	A0-	Complementary Auxiliary Output Data Bit 0 (LSB)
C14	P1-	Complementary Primary Output Data Bit 1
C15	A1-	Complementary Auxiliary Output Data Bit 1
D17	DIVSELECT	TTL/CMOS Demux Divide Selection Input 1: Decimation DIV4 mode 0: Demultiplexed DIV2 mode
D18	AUXEN2	Tie to $V_{CC}O$ to power the auxiliary port. Tie to GNDD to power down.
E1	ICONST	Die Temperature Measurement Test Point. See *Die Temperature Measurement* section.
E2	IPTAT	Die Temperature Measurement Test Point. See *Die Temperature Measurement* section.
E18	DEMUXEN	TTL/CMOS Demux Enable Control 1: Enable Demux 0: Disable Demux
F1	VOSADJ	Offset Adjust Input
F17	P2-	Complementary Primary Output Data Bit 2
F18	P2+	Primary Output Data Bit 2
G17	A2-	Complementary Auxiliary Output Data Bit 2
G18	A2+	Auxiliary Output Data Bit 2
H17	P3-	Complementary Primary Output Data Bit 3
H18	P3+	Primary Output Data Bit 3

Pin Description (continued)

CONTACT	NAME	FUNCTION
J1	VIN-	Differential Input Voltage (-)
J17	A3-	Complementary Auxiliary Output Data Bit 3
J18	A3+	Auxiliary Output Data Bit 3
K17	DREADY-	Complementary Data-Ready Clock
K18	DREADY+	Data-Ready Clock
L1	VIN+	Differential Input Voltage (+)
L17	P4-	Complementary Primary Output Data Bit 4
L18	P4+	Primary Output Data Bit 4
M17	A4-	Complementary Auxiliary Output Data Bit 4
M18	A4+	Auxiliary Output Data Bit 4
N17	P5-	Complementary Primary Output Data Bit 5
N18	P5+	Primary Output Data Bit 5
P1	CLK-	Complementary Sampling-Clock Input
P2	TESTPOINT (T.P.)	This contact **must** be connected to GNDI.
P17	A5-	Complementary Auxiliary Output Data Bit 5
P18	A5+	Auxiliary Output Data Bit 5
R1, R2, R3	CLKCOM	50Ω Clock Termination Return
R19	AUXEN1	Tie to $V_{CC}O$ to power the auxiliary port. Tie to GNDD to power down.
T1	CLK+	Sampling Clock Input
U10	RSTIN-	Complementary PECL Demux Reset Input
U11	RSTOUT-	Complementary PECL Reset Output
U12	OR-	Complementary PECL Overrange Bit
U13	A7-	Complementary Auxiliary Output Data Bit 7 (MSB)
U14	P7-	Complementary Primary Output Data Bit 7 (MSB)
U15	A6-	Complementary Auxiliary Output Data Bit 6
U16	P6-	Complementary Primary Output Data Bit 6
V10	RSTIN+	PECL Demux Reset Input
V11	RSTOUT+	PECL Reset Output
V12	OR+	PECL Overrange Bit
V13	A7+	Auxiliary Output Data Bit 7 (MSB)
V14	P7+	Primary Output Data Bit 7 (MSB)
V15	A6+	Auxiliary Output Data Bit 6
V16	P6+	Primary Output Data Bit 6

±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

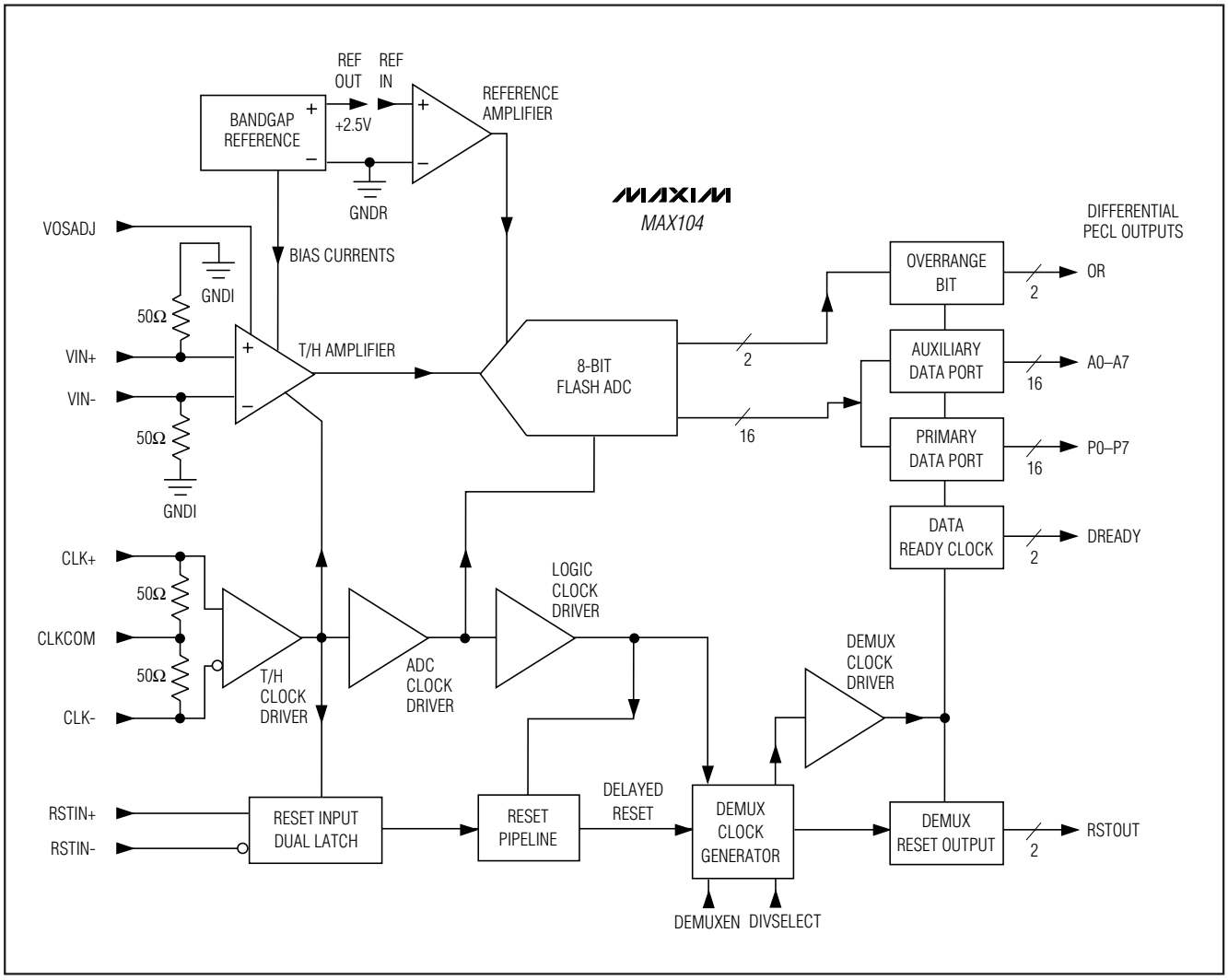


Figure 1. Simplified Functional Diagram

Detailed Description

The MAX104 is an 8-bit, 1Gsps flash analog-to-digital converter (ADC) with on-chip track/hold (T/H) amplifier and differential PECL-compatible outputs. The ADC (Figure 1) employs a fully differential 8-bit quantizer and a unique encoding scheme to limit metastable states to typically one error per 10^{16} clock cycles, with no error exceeding 1LSB max.

An integrated 8:16 output demultiplexer simplifies interfacing to the part by reducing the output data rate to one-half the sampling clock rate. This demultiplexer has internal reset capability that allows multiple MAX104s to be time-interleaved to achieve higher effective sampling rates.

When clocked at 1Gsps, the MAX104 provides a typical effective number of bits (ENOB) of >7.5 bits at an analog input frequency of 500MHz. The analog input of the MAX104 is designed for differential or single-ended use with a ±250mV full-scale input range. In addition, this ADC features an on-chip +2.5V precision bandgap reference. If desired, an external reference can also be used.

Principle of Operation

The MAX104's flash or parallel architecture provides the fastest multibit conversion of all common integrated ADC designs. The key to this high-speed flash architecture is the use of an innovative, high-performance comparator design. The flash converter and downstream logic translate the comparator outputs into a parallel 8-bit output code and pass this binary code on to the optional 8:16 demultiplexer, where primary and auxiliary ports output PECL-compatible data at up to 500Msps per port (depending on how the demultiplexer section is set on the MAX104).

The ideal transfer function appears in Figure 2.

On-Chip Track/Hold Amplifier

As with all ADCs, if the input waveform is changing rapidly during conversion, effective number of bits (ENOB) and signal-to-noise ratio (SNR) specifications will degrade. The MAX104's on-chip, wide-bandwidth (2.2GHz) T/H amplifier reduces this effect and increases the ENOB performance significantly, allowing precise capture of fast analog data at high conversion rates.

The T/H amplifier buffers the input signal and allows a full-scale signal input range of ±250mV. The T/H amplifier's differential 50Ω input termination simplifies interfacing to the MAX104 with controlled impedance lines. Figure 3 shows a simplified diagram of the T/H amplifier stage internal to the MAX104.

Aperture width, delay, and jitter (or uncertainty) are parameters that affect the dynamic performance of high-speed converters. Aperture jitter, in particular, directly influences SNR and limits the maximum slew rate (dV/dt) that can be digitized without contributing significant errors. The MAX104's innovative T/H amplifier design limits aperture jitter typically to less than 0.5ps.

Aperture Width

Aperture width (t_{AW}) is the time the T/H circuit requires (Figure 4) to disconnect the hold capacitor from the input circuit (for instance, to turn off the sampling bridge and put the T/H unit in hold mode).

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation (Figure 4) in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 4).

Internal Reference

The MAX104 features an on-chip +2.5V precision bandgap reference, which can be used by connecting

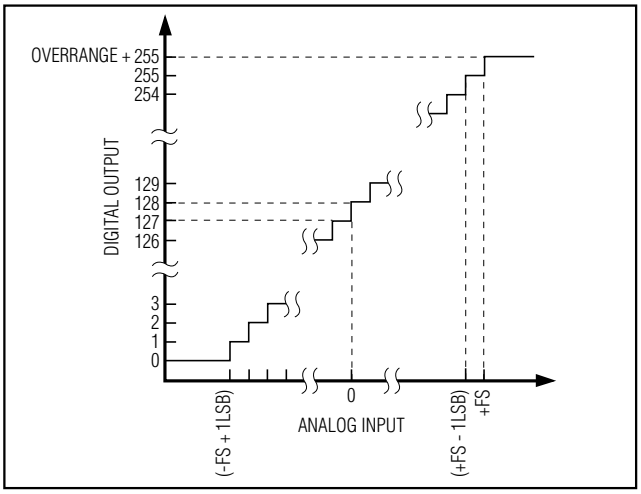


Figure 2. Transfer Function

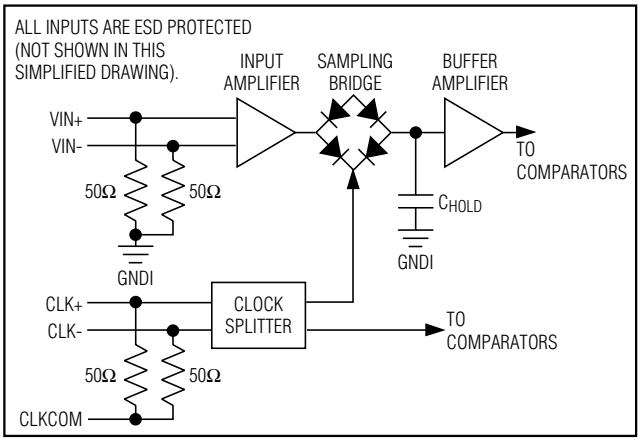


Figure 3. Internal Structure of the 2.2GHz T/H Amplifier

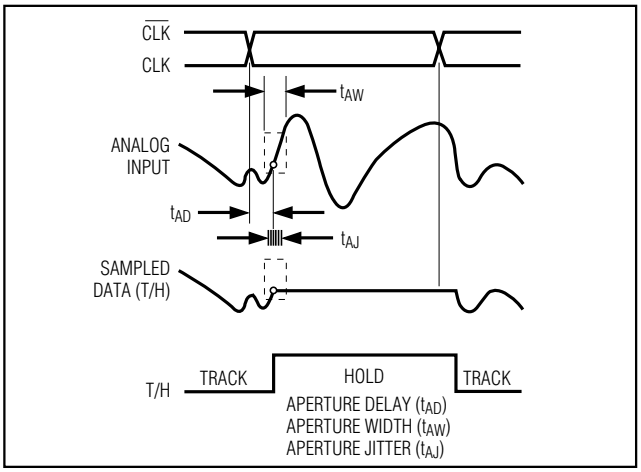


Figure 4. T/H Aperture Timing

±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

REFOUT to REFIN. This connects the reference output to the positive input of the reference buffer. The buffer's negative input is internally connected to GNDR. GNDR must be connected to GNDI on the user's application board. REFOUT can source up to 2.5mA to supply external devices if required.

An adjustable external reference can be used to adjust the ADC's full-scale range. To use an external reference supply, simply connect a high-precision reference to the REFIN pin and leave the REFOUT pin floating. In this configuration, REFOUT **must not** be simultaneously connected to avoid conflicts between the two references. REFIN has a typical input resistance of 5kΩ and accepts input voltages of +2.5V ±200mV. Using the MAX104's internal reference is recommended for best performance.

Digital Outputs

The MAX104 provides data in offset binary format to differential PECL outputs. A simplified circuit schematic of the PECL output cell is shown in Figure 5. All PECL outputs are powered from $V_{CC}O$, which may be operated from any voltage between +3.0V to $V_{CC}D$ for flexible interfacing with either +3.3V or +5V systems. The nominal $V_{CC}O$ supply voltage is +3.3V.

All PECL outputs on the MAX104 are open-emitter types and must be terminated at the far end of each transmission line with 50Ω to $V_{CC}O$ - 2V. Table 1 lists all MAX104 PECL outputs and their functions.

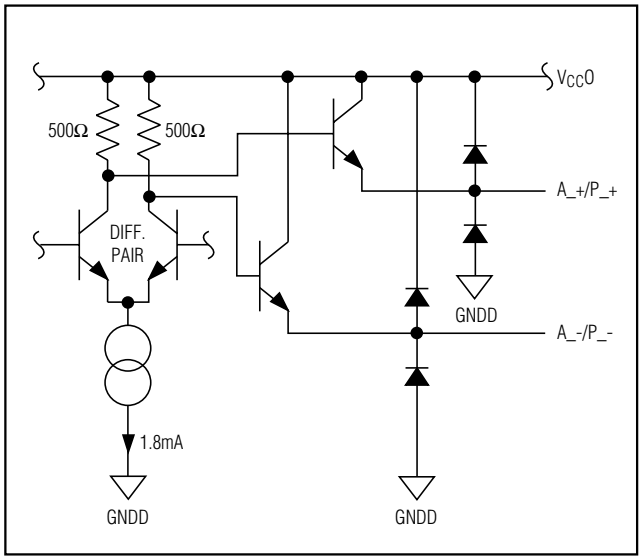


Figure 5. Simplified PECL Output Structure

Demultiplexer Operation

The MAX104 features an internal data demultiplexer that provides for three different modes of operation (see the following sections on *Demultiplexed DIV2 Mode, Non-Demultiplexed DIV1 Mode,* and *Decimation DIV4 Mode*) controlled by two TTL/CMOS-compatible inputs: DEMUXEN and DIVSELECT.

DEMUXEN enables or disables operation of the internal 1:2 demultiplexer. A logic high on DEMUXEN activates the internal demultiplexer, and a logic low deactivates it. With the internal demultiplexer enabled, DIVSELECT controls the selection of the operational mode. DIVSELECT low selects demultiplexed DIV2 mode, and DIVSELECT high selects decimation DIV4 mode (Table 2).

Table 1. PECL Output Functions

PECL OUTPUT SIGNALS	FUNCTIONAL DESCRIPTION
P0+, P0-, P1+, P1-, P2+, P2-, P3+, P3-, P4+, P4-, P5+, P5-, P6+, P6-, P7+, P7-	Primary-Port Differential Outputs from LSB to MSB. A "+" indicates the true outputs; a "-" denotes the complementary outputs.
A0+, A0-, A1+, A1-, A2+, A2-, A3+, A3-, A4+, A4-, A5+, A5-, A6+, A6-, A7+, A7-	Auxiliary-Port Differential Outputs from LSB to MSB. A "+" indicates the true outputs; a "-" denotes the complementary outputs.
DREADY+, DREADY-	Data-Ready Clock True and Complementary Outputs. These signal lines are used to latch the output data from the primary to the auxiliary output ports. Data changes on the rising edge of the DREADY clock.
OR+, OR-	Overrange True and Complementary Outputs
RSTOUT+, RSTOUT-	Reset Output True and Complementary Outputs

Non-Demultiplexed DIV1 Mode

The MAX104 may be operated at up to 500Msps in non-demultiplexed DIV1 mode (Table 2). In this mode, the internal demultiplexer is disabled, and sampled data is presented to the primary port only, with the data repeated at the auxiliary port but delayed by one clock cycle (Figure 6). Since the auxiliary output port contains the same data stream as the primary output port, the auxiliary port can be shut down to save power by connecting AUXEN1 and AUXEN2 to digital ground (GNDD). This powers down the internal bias cells and causes both outputs (true and complementary) of the auxiliary port to pull up to a logic-high level. To save additional power, the external 50Ω termination resistors connected to the PECL termination power supply ($V_{CC}O$ - 2V) may be removed from all auxiliary output ports.

Demultiplexed DIV2 Mode

The MAX104 features an internally selectable DIV2 mode (Table 2) that reduces the output data rate to one-half of the sample clock rate. The demultiplexed outputs are presented in dual 8-bit format with two consecutive samples appearing in the primary and auxiliary output ports on the rising edge of the data-ready clock (Figure 7). The auxiliary data port contains the previous sample, and the primary output contains the most recent data sample. AUXEN1 and AUXEN2 must be connected to $V_{CC}O$ to power-up the auxiliary port PECL output drivers.

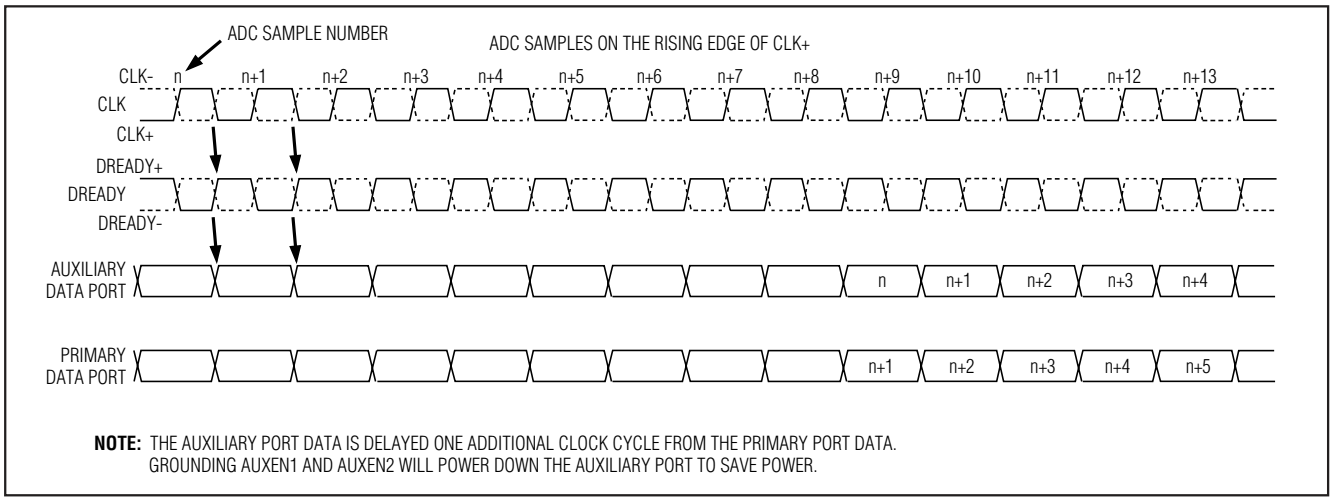


Figure 6. Non-Demuxed, DIV1-Mode Timing Diagram

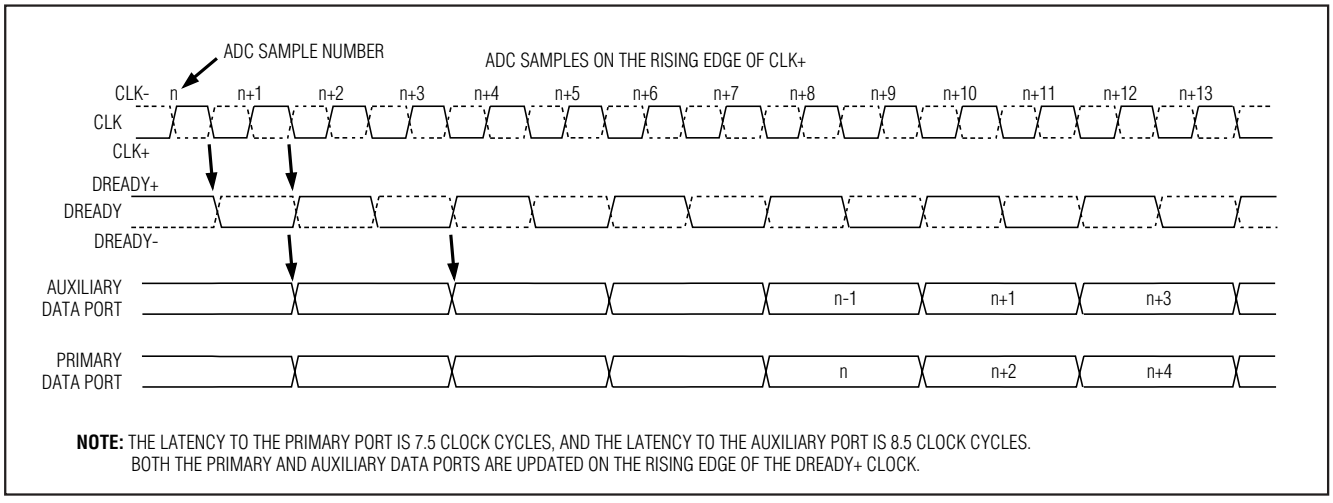


Figure 7. Demuxed DIV2-Mode Timing Diagram

±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

Decimation DIV4 Mode

The MAX104 also offers a special decimated, demultiplexed output (Figure 8) that discards every other input sample and outputs data at one-quarter the input sampling rate for system debugging at slower output data rates. With an input clock of 1GHz, the effective output data rate will be reduced to 250MHz per output port in the DIV4 mode (Table 2). Since every other sample is discarded, the effective sampling rate is 500Msps.

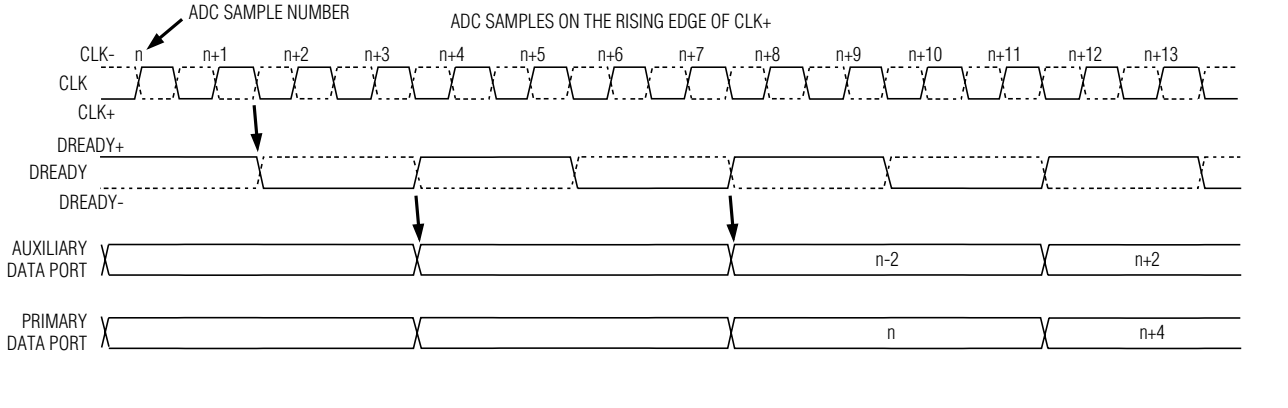
Overrange Operation

A single differential PECL overrange output bit (OR+, OR-) is provided for both primary and auxiliary demultiplexed outputs. The operation of the overrange bit depends on the status of the internal demultiplexer. In demultiplexed DIV2 mode and decimation DIV4 mode, the OR bit will flag an overrange condition if either the primary or auxiliary port contains an overranged sample (Table 2). In non-demultiplexed DIV1 mode, the OR port will flag an overrange condition only when the primary output port contains an overranged sample.

Applications Information

Single-Ended Analog Inputs

The MAX104 T/H amplifier is designed to work at full speed for both single-ended and differential analog inputs (Figure 9). Inputs VIN+ and VIN- feature on-chip, laser-trimmed 50Ω termination resistors to provide excellent voltage standing wave ratio (VSWR) performance.



NOTE: THE LATENCY TO THE PRIMARY PORT REMAINS 7.5 CLOCK CYCLES, WHILE THE LATENCY OF THE AUXILIARY PORT INCREASES TO 9.5 CLOCK CYCLES. THIS EFFECTIVELY DISCARDS EVERY OTHER SAMPLE AND REDUCES THE OUTPUT DATA RATE TO 1/4 THE SAMPLE CLOCK RATE.

Figure 8. Decimation DIV4-Mode Timing Diagram

Table 2. Demultiplexer Operation

DEMUXEN	DIVSELECT	DEMUX MODE	OVERRANGE BIT OPERATION
Low	X	DIV1 500Msps (max)	Flags overrange data appearing in primary port only.
High	Low	DIV2 500Msps/port	Flags overrange data appearing in either the primary or auxiliary port.
High	High	DIV4 250Msps/port	

X = Don't care

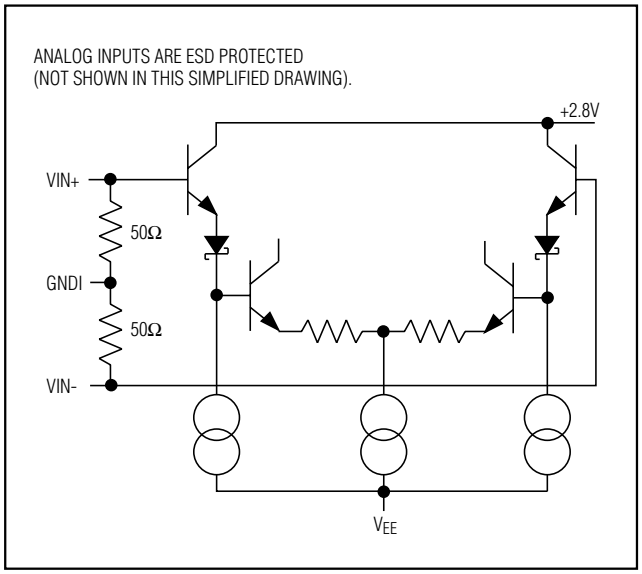


Figure 9. Simplified Analog Input Structure (Single-Ended/ Differential)

In a typical single-ended configuration, the analog input signal (Figure 10a) enters the T/H amplifier stage at the in-phase input (VIN+), while the inverted phase input (VIN-) is reverse-terminated to GNDI with an external 50Ω resistor. Single-ended operation allows for an input amplitude of ±250mV. Table 3 shows a selection of input voltages and their corresponding output codes for single-ended operation.

Differential Analog Inputs

To obtain a full-scale digital output with differential input drive (Figure 10b), 250mVp-p must be applied between VIN+ and VIN- (VIN+ = +125mV and VIN- = -125mV). Midscale digital output codes (01111111 or 10000000) occur when there is no voltage difference between VIN+ and VIN-. For a zero-scale digital output code, the

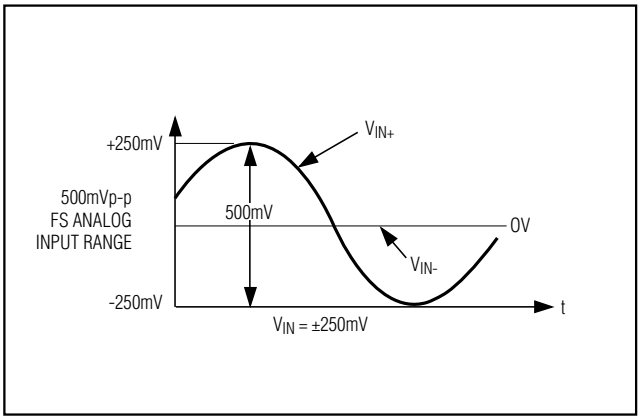


Figure 10a. Single-Ended Analog Input Signals

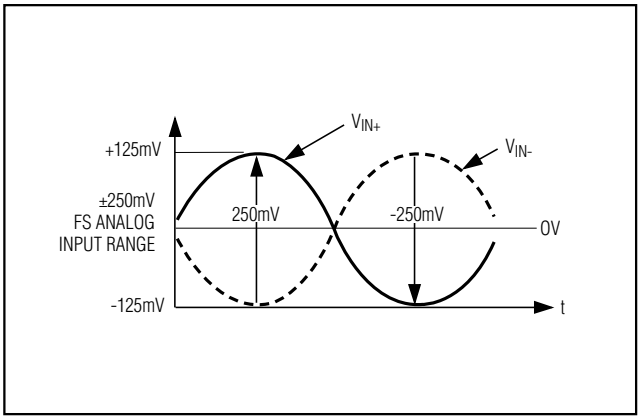


Figure 10b. Differential Analog Input Signals

in-phase (VIN+) input must see -125mV and the inverted input (VIN-) must see +125mV. A differential input drive is recommended for best performance. Table 4 represents a selection of differential input voltages and their corresponding output codes.

Table 3. Ideal Input Voltage and Output Code Results for Single-Ended Operation

VIN+	VIN-	OVERRANGE BIT	OUTPUT CODE
+250mV	0V	1	11111111 (full scale)
+250mV - 1LSB	0V	0	11111111
0V	0V	0	01111111 toggles 10000000
-250mV + 1LSB	0V	0	0000001
-250mV	0V	0	00000000 (zero scale)

±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

Table 4. Ideal Input Voltage and Output Code Results for Differential Operation

VIN+	VIN-	OVERRANGE BIT	OUTPUT CODE
+125mV	-125mV	1	11111111 (full scale)
+125mV - 0.5LSB	-125mV + 0.5LSB	0	11111111
0V	0V	0	01111111 toggles 10000000
-125mV + 0.5LSB	+125mV - 0.5LSB	0	00000001
-125mV	+125mV	0	00000000 (zero scale)

Offset Adjust

The MAX104 provides a control input (VOSADJ) to compensate for system offsets. The offset adjust input is a self-biased voltage divider from the internal +2.5V precision reference. The nominal open-circuit voltage is one-half the reference voltage. With an input resistance of typically 25kΩ, this pin may be driven by an external 10kΩ potentiometer (Figure 11) connected between REFOUT and GNDI to correct for offset errors. This control provides a typical ±5.5LSB offset adjustment range.

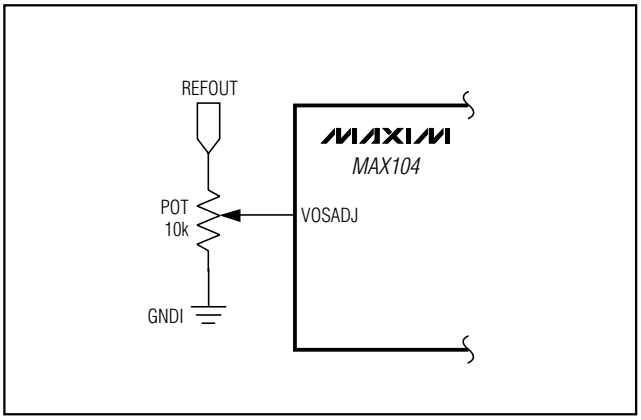


Figure 11. Offset Adjust with External 10kΩ Potentiometer

Clock Operation

The MAX104 clock inputs are designed for either single-ended or differential operation (Figure 12) with flexible input drive requirements. Each clock input is terminated with an on-chip, laser-trimmed 50Ω resistor to CLKCOM (clock-termination return). The CLKCOM termination voltage can be connected anywhere between ground and -2V for compatibility with standard ECL drive levels.

The clock inputs are internally buffered with a preamplifier to ensure proper operation of the data converter with even small-amplitude sine-wave sources. The MAX104 was designed for single-ended, low-phase-noise sine-wave clock signals with as little as 100mV amplitude (-10dBm). This eliminates the need for an external ECL clock buffer and its added jitter.

Single-Ended Clock Inputs (Sine-Wave Drive)

Excellent performance is obtained by AC- or DC-coupling a low-phase-noise sine-wave source into a single clock input (Figure 13a, Table 5). For proper DC balance, the undriven clock input should be externally 50Ω reverse-terminated to GNDI.

The dynamic performance of the data converter is essentially unaffected by clock-drive power levels from

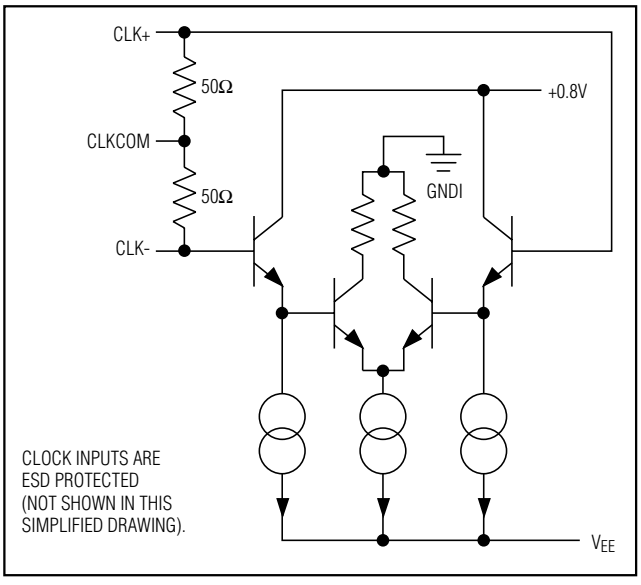


Figure 12. Simplified Clock Input Structure (Single-Ended/ Differential)

-10dBm (100mV clock signal amplitude) to +10dBm (1V clock signal amplitude). The MAX104 dynamic performance specifications are determined by a single-ended clock drive of +4dBm (500mV clock signal amplitude). To avoid saturation of the input amplifier stage, limit the clock power level to a maximum of +10dBm.

Differential Clock Inputs (Sine-Wave Drive)

The advantages of differential clock drive (Figure 13b, Table 5) can be obtained by using an appropriate balun or transformer to convert single-ended sine-wave sources into differential drives. The precision on-chip, laser-trimmed 50Ω clock-termination resistors ensure excellent amplitude matching. Refer to *Single-Ended Clock Inputs (Sine-Wave Drive)* for proper input amplitude requirements.

Single-Ended Clock Inputs (ECL Drive)

Configure the MAX104 for single-ended ECL clock drive by connecting the clock inputs as shown in Figure 13c (Table 5). A well bypassed V_{BB} supply (-1.3V) is essential to avoid coupling noise into the undriven clock input, which would degrade dynamic performance.

Differential Clock Inputs (ECL Drive)

The MAX104 may be driven from a standard differential (Figure 13d, Table 5) ECL clock source by setting the clock termination voltage at CLKCOM to -2V. Bypass the clock-termination return (CLKCOM) as close as possible to the ADC with a 0.01µF capacitor connected to GNDI.

AC-Coupling Clock Inputs

The clock inputs CLK+ and CLK- can also be driven with positive referenced ECL (PECL) logic if the clock

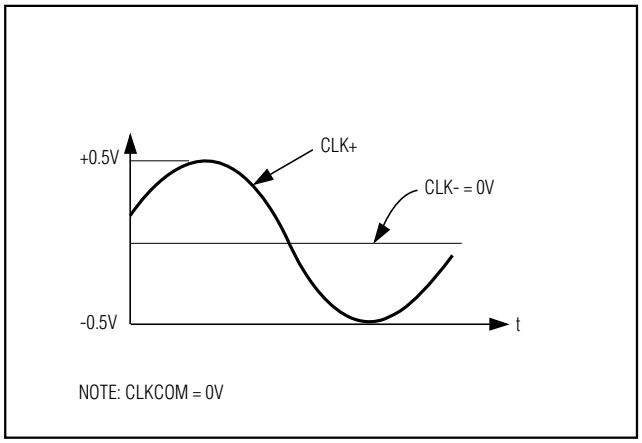


Figure 13a. Single-Ended Clock Input Signals

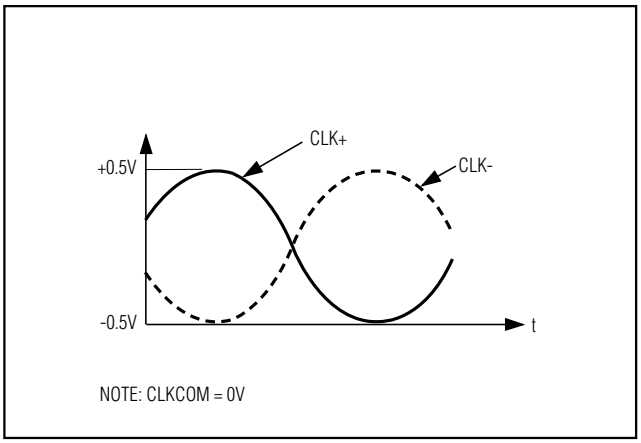


Figure 13b. Differential Clock Input Signals

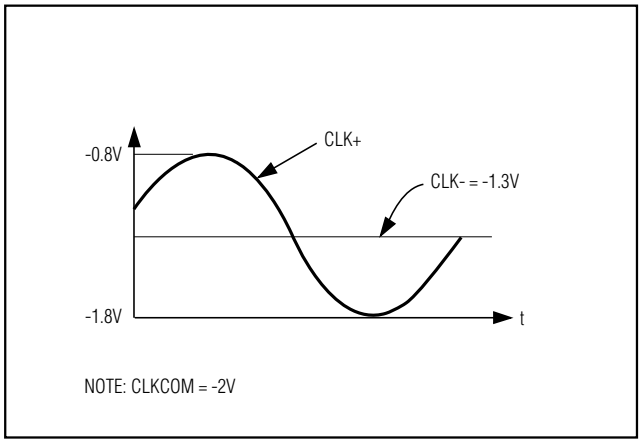


Figure 13c. Single-Ended ECL Clock Drive

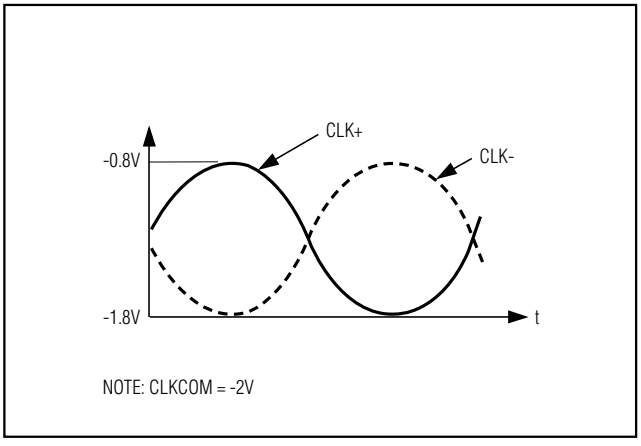


Figure 13d. Differential ECL Clock Drive

±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

Table 5. DC-Coupled Clock Drive Options

CLOCK DRIVE	CLK+	CLK-	CLKCOM	REFERENCE
Single-Ended Sine Wave	-10dBm to +4dBm	External 50Ω to GNDI	GNDI	Figure 13a
Differential Sine Wave	-10dBm to +4dBm	-10dBm to +4dBm	GNDI	Figure 13b
Single-Ended ECL	ECL Drive	-1.3V	-2V	Figure 13c
Differential ECL	ECL Drive	$\overline{\text{ECL}}$ Drive	-2V	Figure 13d

inputs are AC-coupled. Under this condition, connect CLKCOM to GNDI. Single-ended ECL/PECL/sine-wave drive is also possible if the undriven clock input is reverse-terminated to GNDI through a 50Ω resistor in series with a capacitor whose value is identical to that used to couple the driven input.

Demux Reset Operation

The MAX104 features an internal 1:2 demultiplexer that reduces the data rate of the output digital data to one-half the sample clock rate. Demux reset is necessary when interleaving multiple MAX104s and/or synchronizing external demultiplexers. The simplified block diagram of Figure 1 shows that the demux reset signal path consists of four main circuit blocks. From input to output, they are the reset input dual latch, the reset pipeline, the demux clock generator, and the reset output. The signals associated with the demux reset operation and the control of this section are listed in Table 6.

Reset Input Dual Latch

The reset input dual-latch circuit block accepts differential PECL reset inputs referenced to the same $V_{CC}O$ power supply that powers the MAX104 PECL outputs. For applications that do not require a synchronizing reset, the reset inputs can be left open. In this case, they will self-bias to a proper level with internal 50kΩ resistors and 20µA current source. This combination creates a -1V difference between RSTIN+ and RSTIN- to disable the internal reset circuitry. When driven with PECL logic levels terminated with 50Ω to ($V_{CC}O$ - 2V), the internal biasing network can easily be overdriven. Figure 14 shows a simplified schematic of the reset input structure.

To properly latch the reset input data, the setup time (t_{SU}) and the data hold time (t_{HD}) must be met with respect to the rising edge of the sample clock. The timing diagram of Figure 15 shows the timing relationship of the reset input and sampling clock.

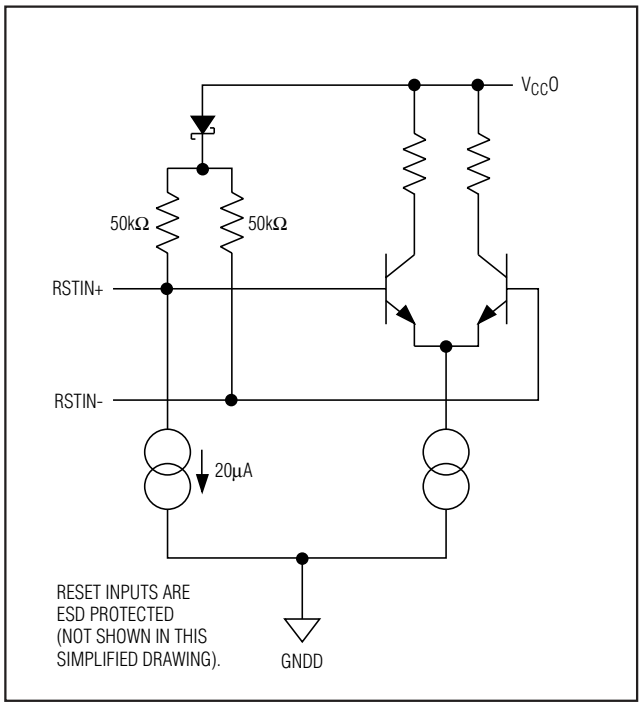


Figure 14. Simplified Reset Input Structure

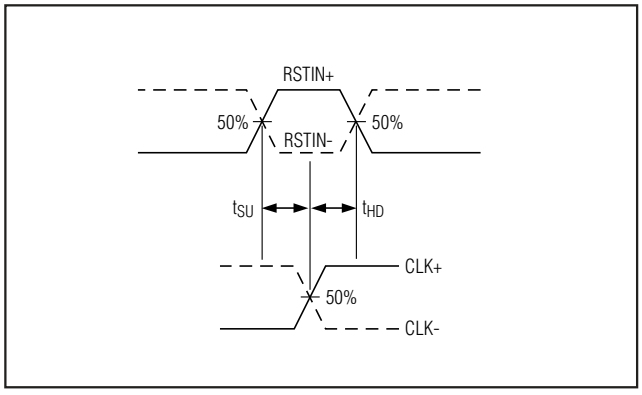


Figure 15. Reset Input Timing Definitions

Table 6. Demux Operating and Reset Control Signal

SIGNAL NAME	TYPE	FUNCTION
CLK+, CLK-	Sampling clock inputs	Master ADC timing signal. The ADC samples on the rising edge of CLK+.
DREADY+, DREADY-	Differential PECL outputs	Data-Ready PECL Output. Output data changes on the rising edge of DREADY+.
RSTIN+, RSTIN-	Differential PECL inputs	Demux reset input signals. Resets the internal demux when asserted.
RSTOUT+, RSTOUT-	Differential PECL outputs	Reset outputs for resetting additional external demux devices

Reset Pipeline

The next section in the reset signal path is the reset pipeline. The purpose of this block is to add clock cycles of latency to the reset signal, to match the latency of the converted analog data through the ADC. In this way, when reset data arrives at the RSTOUT+/RSTOUT- PECL output, it will be time-aligned with the analog data present in the primary and auxiliary ports at the time the reset input was deasserted at RSTIN+/RSTIN-.

Demux Clock Generator

The demux clock generator creates the DIV1, DIV2, or DIV4 clocks required for the different modes of demux and non-demux operation. The TTL/CMOS control inputs DEMUXEN and DIVSELECT control the demuxed mode selection, as described in Table 2. The timing diagrams in Figure 16 and Figure 17 show the output timing and data alignment in DIV1, DIV2, and DIV4 modes, respectively.

The phase relationship between the sampling clock at the CLK+/CLK- inputs and the data-ready clock at the DREADY+/DREADY- outputs will be random at device power-up. As with all divide-by-two circuits, two possible phase relationships exist between these clocks. The difference between the phases is simply the inversion of the DIV2-DREADY clock. The timing diagram in Figure 16 shows this relationship.

Reset all MAX104 devices to a known DREADY phase after initial power-up for applications such as interleaving, where two or more MAX104 devices are used to achieve higher effective sampling rates. This synchronization is necessary to set the order of output samples between the devices. Resetting the converters accomplishes this synchronization. The reset signal is used to force the internal counter in the demux clock-generator block to a known phase state.

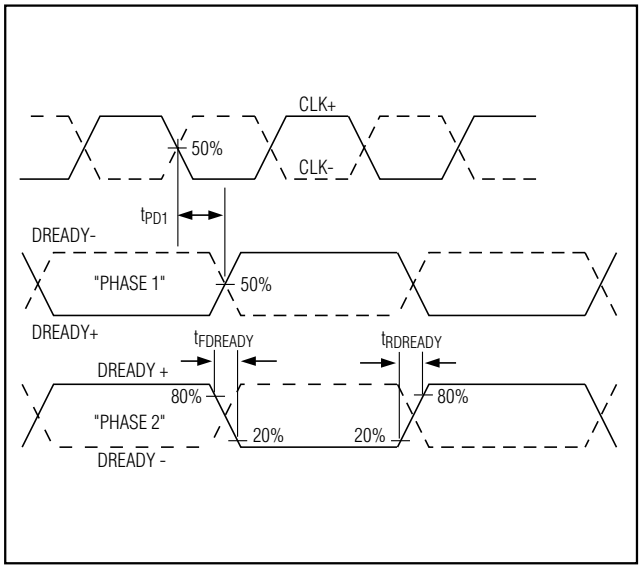


Figure 16. CLK and DREADY Timing in Demuxed DIV2 Mode Showing Two Possible DREADY Phases

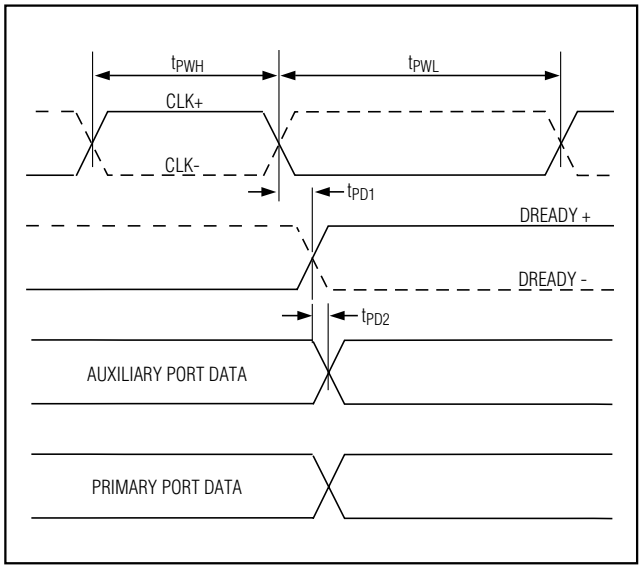


Figure 17. Output Timing for All Modes (DIV1, DIV2, DIV4)

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Reset Output

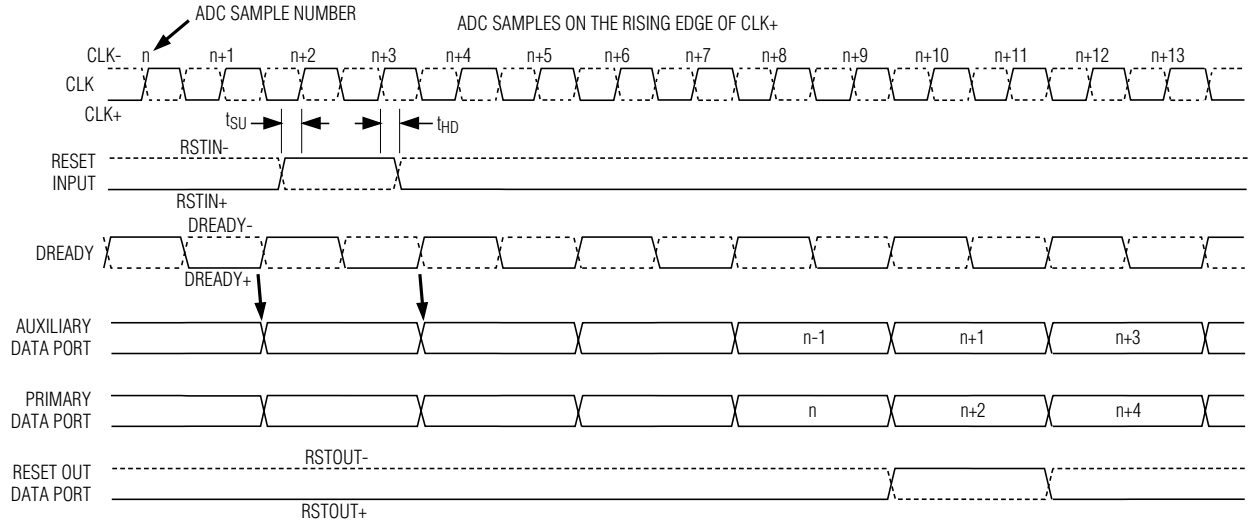
Finally, the reset signal is presented in differential PECL format to the last block of the reset signal path. RSTOUT+/RSTOUT- output the time-aligned reset signal used for resetting additional external demuxes in applications that need further output data rate reduction. Many demux devices require that their reset signal be asserted for several clock cycles while they are clocked. To accomplish this, the MAX104 DREADY clock will continue to toggle while RSTOUT is asserted.

When a single MAX104 device is used, no synchronizing reset is required, because the order of the samples in the output ports is unchanged regardless of the phase of the DREADY clock. In DIV2 mode, the data in the auxiliary port is delayed by 8.5 clock cycles, while the data in the primary port is delayed by 7.5 clock cycles. The older data is always in the auxiliary port, regardless of the phase of the DREADY clock.

The reset output signal, RSTOUT, is delayed by one less clock cycle (6.5 clock cycles) than the primary port. The reduced latency of RSTOUT serves to mark the start of synchronized data in the primary and auxiliary ports. When the RSTOUT signal returns to a zero, the DREADY clock phase is reset.

Since there are two possible phases of the DREADY clock with respect to the input clock, there are two possible timing diagrams to consider. The first timing diagram (Figure 18) shows the RSTOUT timing and data alignment of the auxiliary and primary output ports when the DREADY clock phase is already reset. For this example, the RSTIN pulse is two clock cycles long. Under this condition, the DREADY clock continues uninterrupted, as does the data stream in the auxiliary and primary ports.

The second timing diagram (Figure 19) shows the results when the DREADY phase is opposite from the reset phase. In this case, the DREADY clock “swallows” a clock cycle of the sample clock, resynchronizing to the reset phase. Note that the data stream in the auxiliary and primary ports has reversed. Before reset was



NOTE: THE LATENCY TO THE RESET OUTPUT IS 6.5 CLOCK CYCLES. THE LATENCY TO THE PRIMARY PORT IS 7.5 CLOCK CYCLES, AND THE LATENCY TO THE AUXILIARY PORT IS 8.5 CLOCK CYCLES. ALL DATA PORTS ARE UPDATED ON THE RISING EDGE OF THE DREADY+ CLOCK.

Figure 18. Reset Output Timing in Demuxed DIV2 Mode (DREADY Aligned)

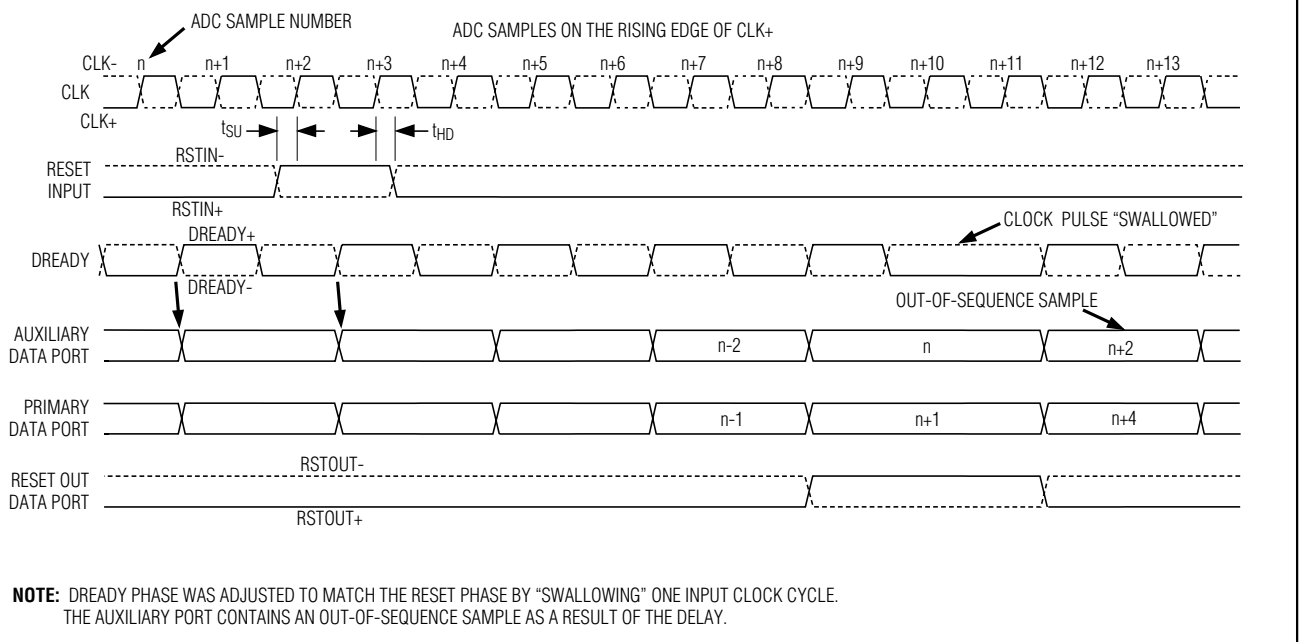


Figure 19. Reset Output Timing in Demuxed DIV2 Mode (DREADY Realigned)

asserted, the auxiliary port contained "even" samples while the primary port contained "odd" samples. After the RSTOUT is deasserted (which marks the start of the DREADY clock's reset phase), note that the order of the samples in the ports has been reversed. The auxiliary port also contains an out-of-sequence sample. This is a consequence of the "swallowed" clock cycle that was needed to resynchronize DREADY to the reset phase. Also note that the older sample data is always in the auxiliary port, regardless of the DREADY phase.

These examples illustrate the combinations that result with a reset input signal of two clock cycles. It is also possible to reset the internal MAX104 demux successfully with a reset pulse of only one clock cycle, provided that the setup-time and hold-time requirements are met with respect to the sample clock. However, this is not recommended when additional external demuxes are used.

Note that many external demuxes require that their reset signals be asserted while they are clocked, and may require more than one clock cycle of reset. More importantly, if the phase of the DREADY clock is such that a clock pulse will be "swallowed" to resynchronize, then no reset output will occur at all. In effect, the RSTOUT signal will be "swallowed" with the clock pulse. The best method to ensure complete system reset is to assert RSTIN for the appropriate number of DREADY clock cycles required to complete reset of the external demuxes.

Die Temperature Measurement

For applications that require monitoring of the die temperature, it is possible to determine the die temperature of the MAX104 under normal operating conditions by observing the currents I_{CONST} and I_{PTAT}, at contacts ICONST and IPTAT. I_{CONST} and I_{PTAT} are two 100µA (nominal) currents that are designed to be equal at +27°C. These currents are derived from the MAX104's internal precision +2.5V bandgap reference. I_{CONST} is designed to be temperature independent, while I_{PTAT} is directly proportional to the absolute temperature. These currents are derived from pnp current sources referenced from $V_{CC}I$ and driven into two series diodes connected to GNDI. The contacts ICONST and IPTAT may be left open, because internal catch diodes prevent saturation of the current sources. The simplest method

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of determining the die temperature is to measure each current with an ammeter (which shuts off the internal catch diodes) referenced to GNDI. The die temperature in °C is then calculated by the expression:

$$T_{DIE} = 300 \times \left[\frac{I_{PTAT}}{I_{CONST}} \right] - 273$$

Another method of determining the die temperature uses the operational amplifier circuit shown in Figure 20. The circuit produces a voltage that is proportional to the die temperature. A possible application for this signal is speed control for a cooling fan, to maintain constant MAX104 die temperature. The circuit operates by converting the I_{CONST} and I_{PTAT} currents to voltages V_{CONST} and V_{PTAT}, with appropriate scaling to account for their equal values at +27°C. This voltage difference is then amplified by two amplifiers in an instrumentation-amplifier configuration with adjustable gain. The nominal value of the circuit gain is 4.5092V/V. The gain of the instrumentation amplifier is given by the expression:

$$A_V = \frac{V_{TEMP}}{V_{CONST} - V_{PTAT}}$$

$$A_V = 1 + \frac{R1}{R2} + 2 \times \frac{R1}{R3}$$

To calibrate the circuit, first connect pins 2-3 on JU1 to zero the input of the PTAT path. With the MAX104 powered up, adjust potentiometer R3 until the voltage at the V_{TEMP} output is -2.728V. Connecting pins 1-2 on JU1 restores normal operation to the circuit after the calibration is complete. The voltage at the V_{TEMP} node will then be proportional to the actual MAX104 die temperature according to the equation:

$$T_{DIE}\ (°C) = 100 \times V_{TEMP}$$

The overall accuracy of the die temperature measurement using the operational-amplifier scaling circuitry is limited mainly by the accuracy and matching of the resistors in the circuit.

Thermal Management

Depending on the application environment for the ESBGA-packaged MAX104, the customer may have to apply an external heatsink to the package after board assembly. Existing open-tooled heatsinks are available from standard heatsink suppliers (see *Heatsink Manufacturers*). The heatsinks are available with pre-applied adhesive for easy package mounting.

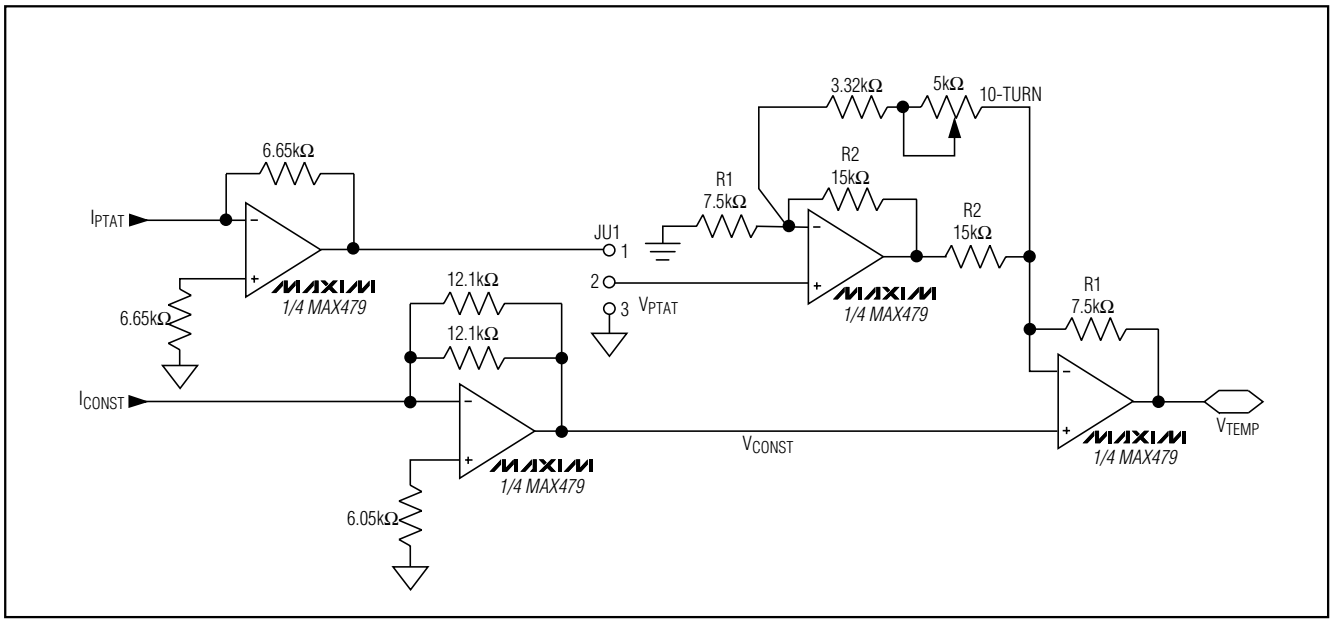

Figure 20. Die Temperature Acquisition Circuit with the MAX479

Table 7. Thermal Performance for MAX104 With or Without Heatsink

AIRFLOW (linear ft./min.)	MAX104 θ_{JA} (°C/W)	
	WITHOUT HEATSINK	WITH HEATSINK
0	16.5	12.5
200	14.3	9.4
400	13	8.3
800	12.5	7.4

Thermal Performance

The MAX104 has been modeled to determine the thermal resistance from junction to ambient. Table 7 lists the ADC's thermal performance parameters:

Ambient Temperature: T_A = +70°C

Heatsink Dimensions: 25mm x 25mm x 10mm

PC Board Size and Layout: 4" x 4"
2 Signal Layers
2 Power Layers

Heatsink Manufacturers

Aavid Engineering and IERC provide open-tool, low-profile heatsinks, fitting the 25mm x 25mm ESBGA package.

Aavid Engineering, Inc.
Phone: 714-556-2665
Heatsink Catalog #: 335224B00032
Heatsink Dimensions: 25mm x 25mm x 10mm

International Electronic Research Corporation (IERC)
Phone: 818-842-7277
Heatsink Catalog #: BDN09-3CB/A01
Heatsink Dimensions: 23.1mm x 23.1mm x 9mm

Bypassing/Layout/Power Supply

Grounding and power-supply decoupling strongly influence the MAX104's performance. At 1GHz clock frequency and 8-bit resolution, unwanted digital crosstalk may couple through the input, reference, power supply, and ground connections and adversely influence the dynamic performance of the ADC. Therefore, closely follow the grounding and power-supply decoupling guidelines (Figure 22).

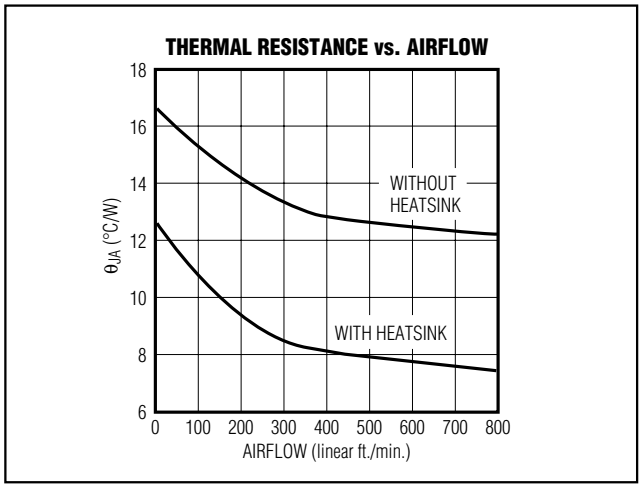

Figure 21. MAX104 Thermal Performance

Maxim strongly recommends using a multilayer printed circuit board (PCB) with separate ground and power-supply planes. Since the MAX104 has separate analog and digital ground connections (GNDA, GNDI, GNDR, and GNDD, respectively), the PCB should feature separate analog and digital ground sections connected at only one point (star ground at the power supply). Digital signals should run above the digital ground plane, and analog signals should run above the analog ground plane. Keep digital signals far away from the sensitive analog inputs, reference inputs, and clock inputs. High-speed signals, including clocks, analog inputs, and digital outputs, should be routed on 50Ω microstrip lines, such as those employed on the MAX104EVKIT.

The MAX104 has separate analog and digital power-supply inputs: V_{EE} (-5V analog and substrate supply) and $V_{CC}I$ (+5V) to power the T/H amplifier, clock distribution, bandgap reference, and reference amplifier; $V_{CC}A$ (+5V) to supply the ADC's comparator array; $V_{CC}O$ (+3V to $V_{CC}D$) to establish power for all PECL-based circuit sections; and $V_{CC}D$ (+5V) to supply all logic circuits of the data converter.

The MAX104 V_{EE} supply contacts **must not** be left open while the part is being powered up. To avoid this condition, add a high-speed Schottky diode (such as a Motorola 1N5817) between V_{EE} and GNDI. This diode prevents the device substrate from forward biasing, which could cause latchup.

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All supplies should be decoupled with large tantalum or electrolytic capacitors at the point where they enter the PCB. For best performance, bypass all power supplies to the appropriate ground with a 10µF tantalum capacitor, to filter power-supply noise, in parallel with a 0.01µF capacitor and a high-quality 47pF ceramic chip capacitor located very close to the MAX104 device, to filter very high-frequency noise.

Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX104 are measured using the best-straight-line fit method.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

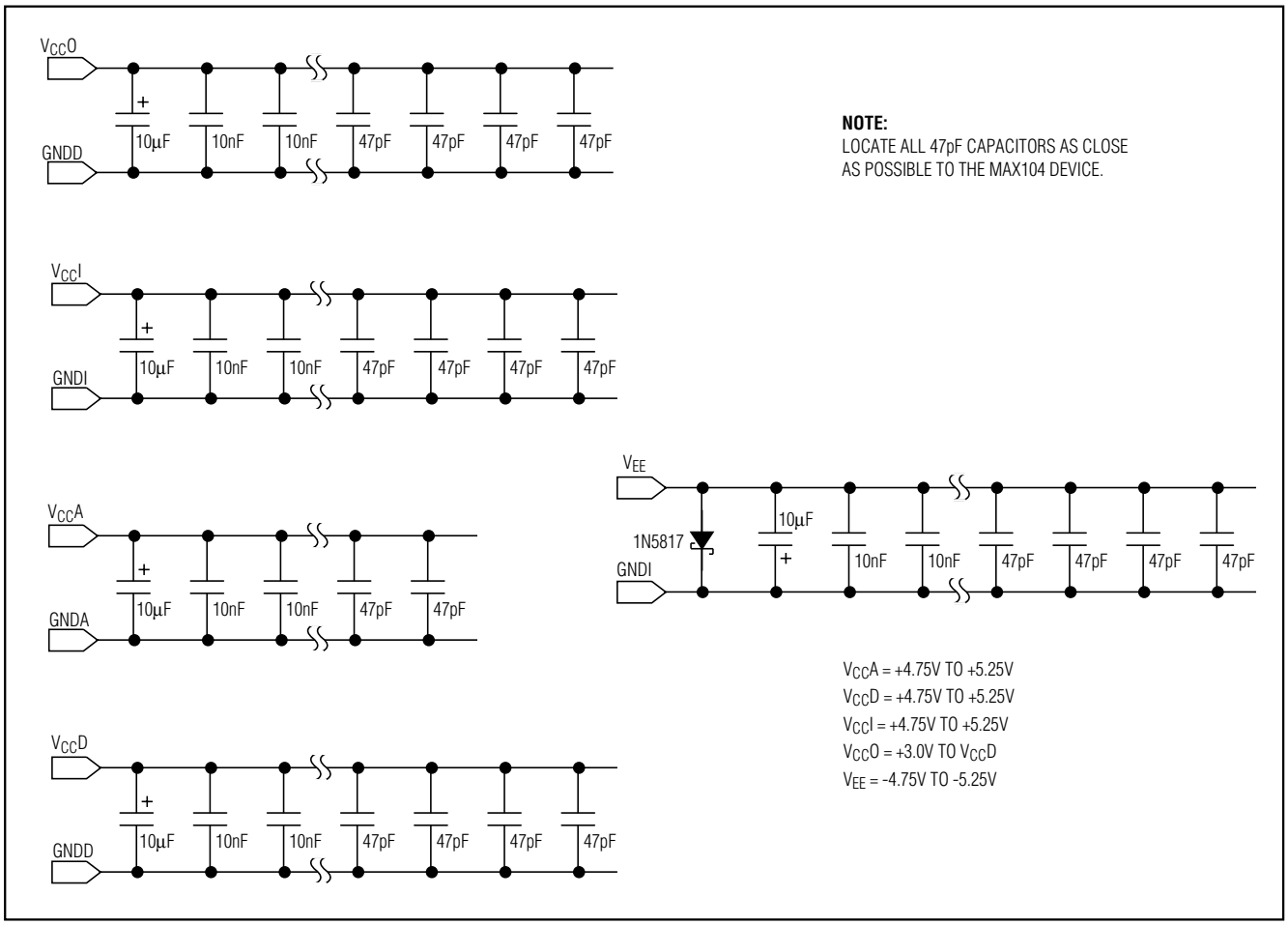


Figure 22. MAX104 Bypassing and Grounding

Bit Error Rates (BER)

Errors resulting from metastable states may occur when the analog input voltage (at the time the sample is taken) falls close to the decision point of any one of the input comparators. Here, the magnitude of the error depends on the location of the comparator in the comparator network. If it is the comparator for the MSB, the error will reach full scale. The MAX104's unique encoding scheme solves this problem by limiting the magnitude of these errors to 1LSB; it reduces the probability of these errors occurring to typically one in every 10^{16} clock cycles.

Dynamic Parameter Definitions

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{(MAX)} = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is calculated by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Effective Number of Bits (ENOB)

ENOB indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB is calculated from a curve fit referenced to the theoretical full-scale range.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is calculated from the effective number of bits (ENOB) as follows:

$$SINAD = (6.02 \times ENOB) + 1.76$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first four harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2 \right)} / V_1 \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio, expressed in decibels, of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

Intermodulation Distortion (IMD)

The two-tone IMD is the ratio, expressed in decibels, of either input tone to the worst 3rd-order (or higher) intermodulation products. The input tone levels are at -7dB full scale.

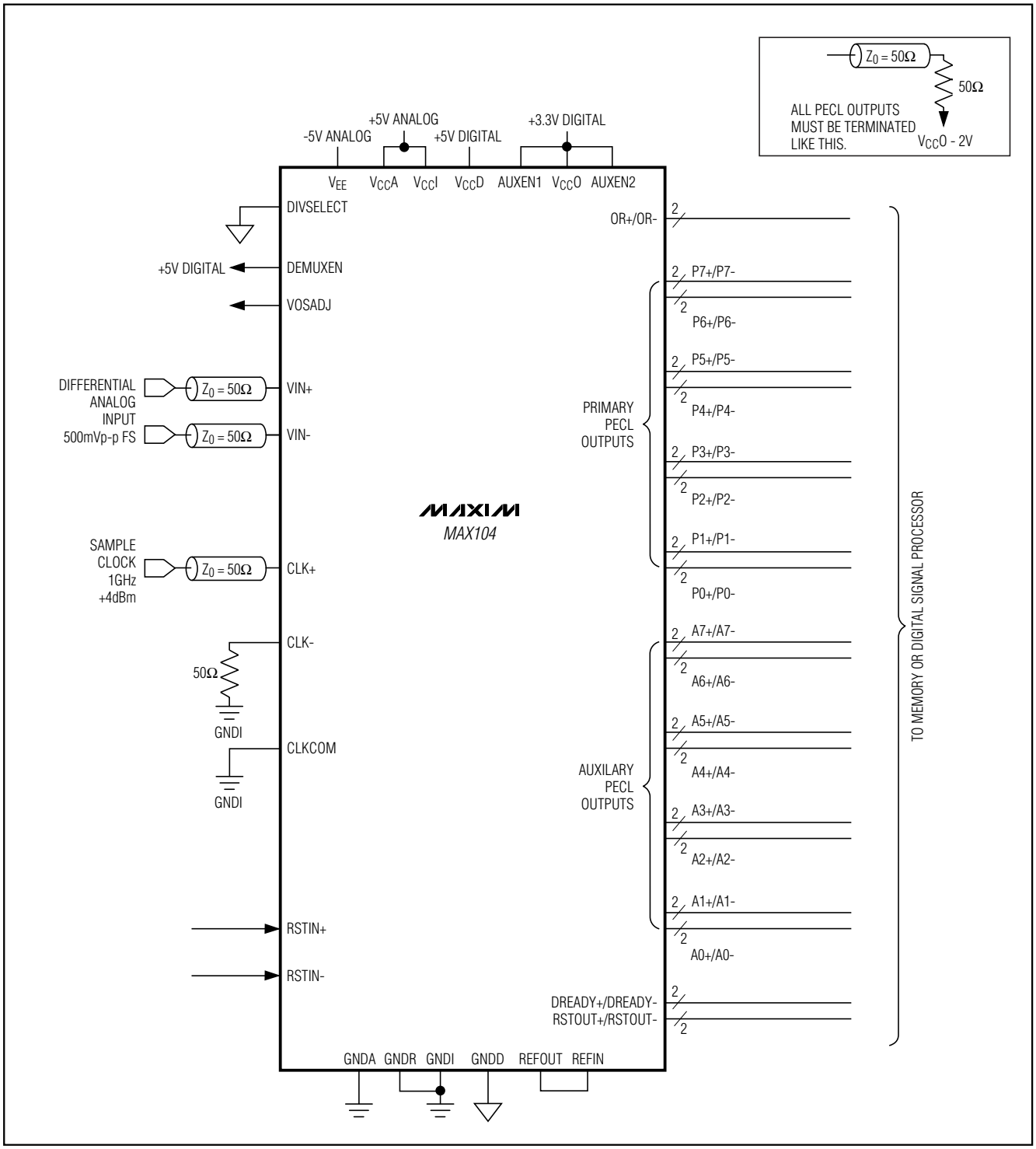
Chip Information

TRANSISTOR COUNT: 20,486

SUBSTRATE CONNECTED TO V_{EE}

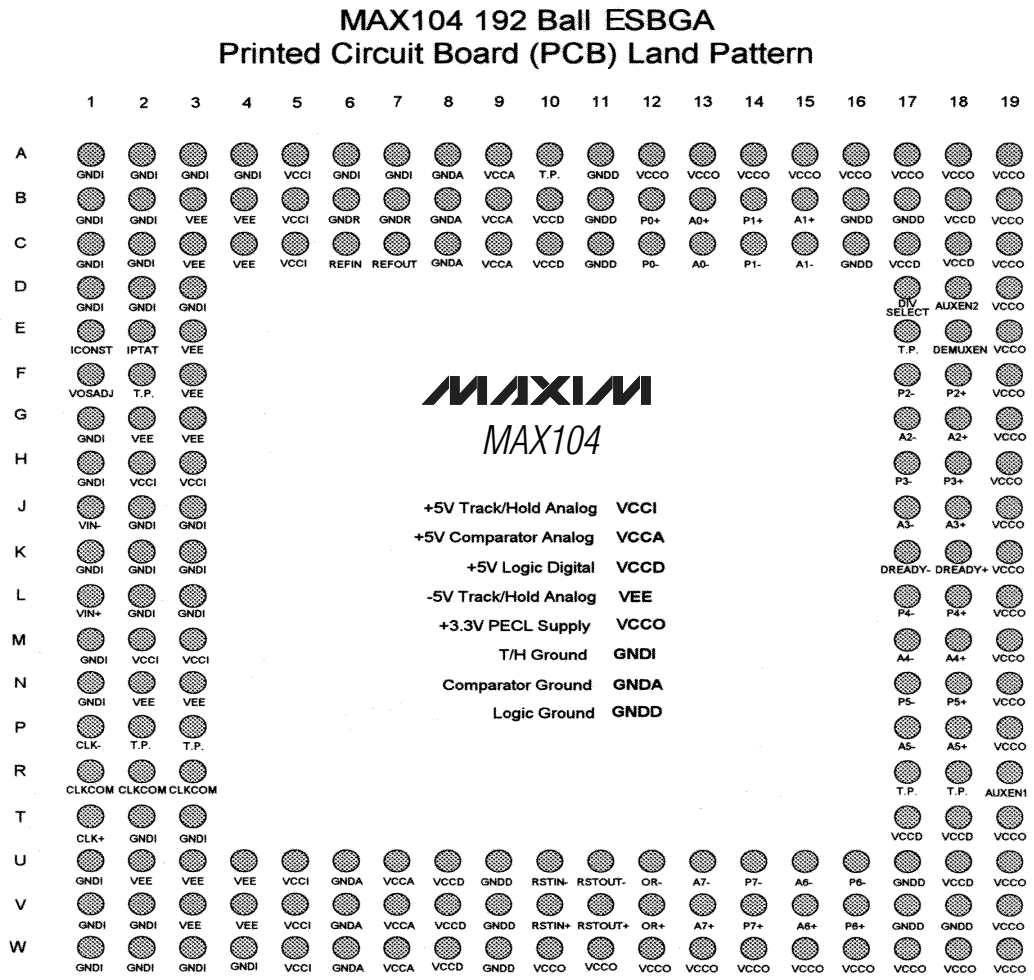
±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

Typical Operating Circuit



192-Contact ESBGA PCB Land Pattern

TOP VIEW

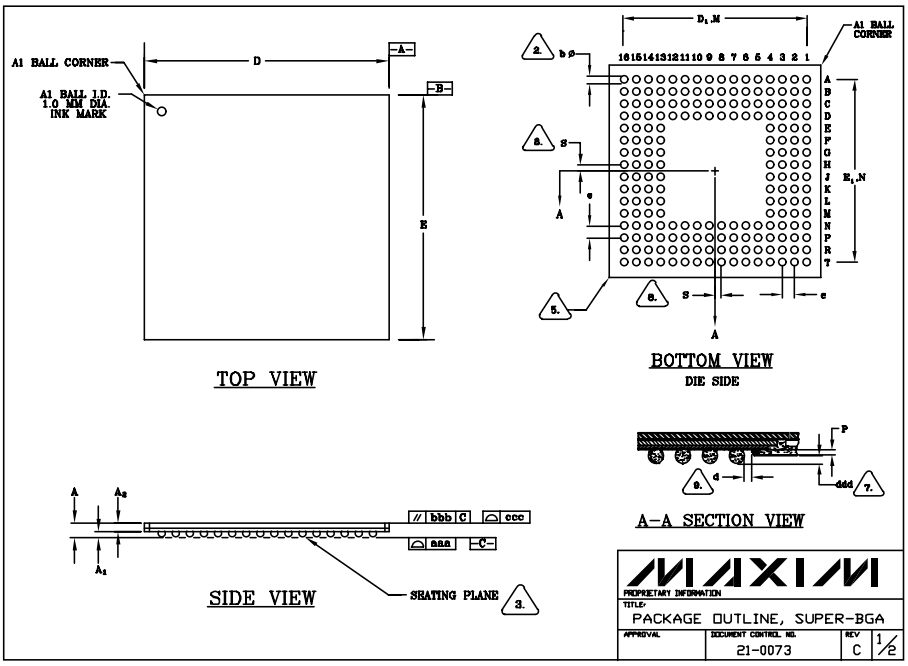


±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SUPER BGA.EPS



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C- .
3. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. THE 192 BALL 25 X 25 MM SBGA HAS 3 ROWS OF BALLS. THE 256 BALL 27 X 27 MM SBGA HAS 4 ROWS OF BALLS.
5. SHAPE AT CORNER.

6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. HEIGHT FROM BALL SEATING PLANE TO PLANE OF ENCAPSULANT.
8. "S" IS MEASURED WITH RESPECT TO -A- AND -B- AND DEFINES THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "S"=.000; WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW THE VALUE "S"=e/2. "S" MAY BE EITHER .000 OR e/2 FOR EACH VARIATION.
9. THE DIMENSION FROM THE OUTER EDGE OF THE RESIN DAM TO THE EDGE OF THE INNERMOST ROW OF SOLDER BALL PADS IS TO BE A MINIMUM OF 0.50mm.
10. "SUPER BGA" IS A REGISTERED TRADEMARK OF AMKOR TECHNOLOGIES.

STANDARD BODY SIZE DIMENSION TABLE

BODY SIZE	25.0 X 25.0MM PACKAGE			27.0 X 27.0MM PACKAGE			BODY SIZE
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	NOTE
A	1.41	1.54	1.67	1.41	1.54	1.67	OVERALL THICKNESS
A1	0.56	0.63	0.70	0.56	0.63	0.70	BALL HEIGHT
A2	0.85	0.91	0.97	0.85	0.91	0.97	BODY THICKNESS
D	24.90	25.00	25.10	26.90	27.00	27.10	BODY SIZE
D1	22.76	22.86	22.96	24.03	24.13	24.23	BALL FOOTPRINT
E	24.90	25.00	25.10	26.90	27.00	27.10	BODY SIZE
E1	22.76	22.86	22.96	24.03	24.13	24.23	BALL FOOTPRINT
M,N	19 x 19			20 x 20			BALL MATRIX
b	0.60	0.75	0.90	0.60	0.75	0.90	BALL DIAMETER
d	0.6			0.6			MIN DISTANCE ENCAP TO BALLS
e	1.27			1.27			BALL PITCH
aaa			0.15			0.15	COPLANARITY
bbb			0.15			0.15	PARALLEL
ccc			0.20			0.20	TOP FLATNESS
ddd/8	0.15	0.33	0.50	0.15	0.33	0.50	SEATING PLANE CLEARANCE
P	0.20	0.30	0.35	0.20	0.30	0.35	ENCAPSULATION HEIGHT
S	—	—	0.00	—	—	0.635	SOLDER BALL PLACEMENT

PROPRIETARY INFORMATION
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