OPA2325

Precision, 10-MHz, Low-Noise, Low-Power, RRIO, CMOS Operational Amplifier

1 Features

- Precision with Zero-Crossover Distortion:
  - Low Offset Voltage: 150 μV (maximum)
  - High CMRR: 114 dB
  - Rail-to-Rail I/O
- Wide Bandwidth: 10 MHz
- Quiescent Current: 650 μA/ch
- Single-Supply Voltage Range: 2.2 V to 5.5 V
- Low Input Bias Current: 0.2 pA
- Low Noise: 9 nV/√Hz at 10 kHz
- Slew Rate: 5 V/μs
- Unity-Gain Stable

2 Applications

- High-Z Sensor Signal Conditioning
- Transimpedance Amplifiers
- Test and Measurement Equipment
- Programmable Logic Controllers (PLCs)
- Motor Control Loops
- Communications
- Input, Output ADC, and DAC Buffers
- Active Filters

3 Description

The OPA2325 is a dual, precision, low-voltage complementary metal-oxide semiconductor (CMOS) operational amplifier optimized for very low noise and wide bandwidth while operating on a low quiescent current of only 650 μA.

The OPA2325 features a linear input stage with zero-crossover distortion that delivers excellent common-mode rejection ratio (CMRR) of typically 114 dB over the entire input range. The input common-mode range extends 100 mV beyond the negative and positive supply rails. The output voltage typically swings within 10 mV of the rails.

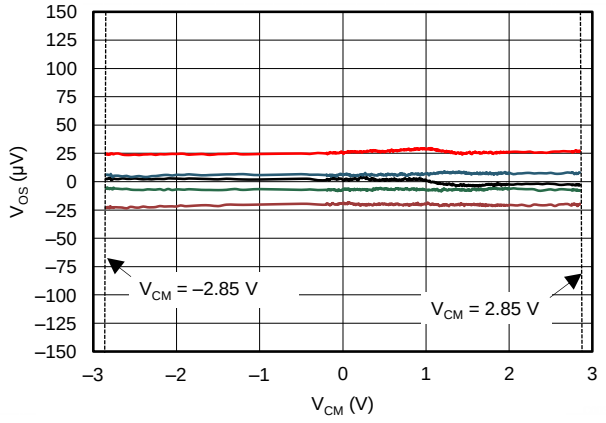
The zero-crossover distortion, combined with wide bandwidth (10 MHz), high slew rate (5 V/μs), and low noise (9 nV/√Hz), make the OPA2325 a very good successive-approximation register (SAR) analog-to-digital converter (ADC) input driver amplifier. In addition, the OPA2325 has a wide supply-voltage range from 2.2 V to 5.5 V with excellent power-supply rejection ratio (PSRR) over the entire supply range, making the device suitable for precision, low-power applications that run directly from batteries without regulation.

Device Information(1)

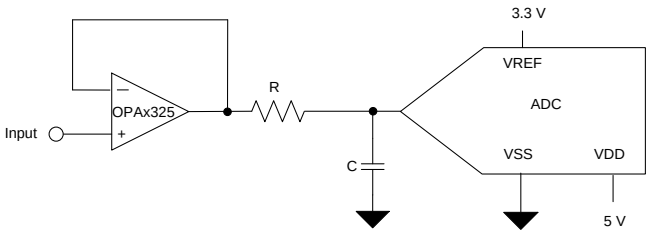
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2325	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Offset Voltage vs Input Common-Mode Voltage



The OPA2325 as an ADC Driver Amplifier



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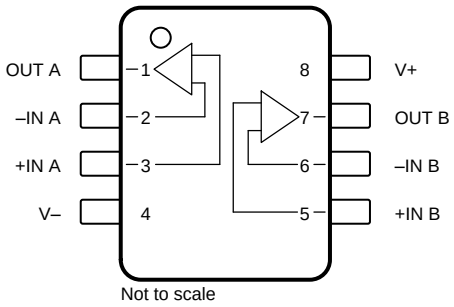
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2016) to Revision A	Page
• Added new VSSOP package option for dual-channel device	1
• Added top navigator icon for TI reference design	1

5 Pin Configuration and Functions

OPA2325: D and DGK Packages
8-Pin SOIC, 8-Pin VSSOP
Top View



Not to scale

Pin Functions: OPA2325

PIN		I/O	DESCRIPTION
NAME	D (SOIC), DGK (VSSOP)		
–IN A	2	I	Inverting input channel A
+IN A	3	I	Noninverting input channel A
–IN B	6	I	Inverting input channel B
+IN B	5	I	Noninverting input channel B
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
V–	4	—	Negative supply
V+	8	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_S = (V+) – (V–)		6	V
Signal input pins	Voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Current(2)	–10	10	mA
Output short-circuit(3)		Continuous		mA
Temperature	Specified, T_A	–40	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single supply	2.2		5.5	V
		Dual supply	±1.1		±2.75	
	Specified temperature range		–40		125	°C

6.4 Thermal Information: OPA2325

THERMAL METRIC(1)		OPA2325		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119	143	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60	47	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61	64	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	15.0	5.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	60.4	62.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: V_S = 2.2 V to 5.5 V or ±1.1 V to ±2.75 V

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			40	150	µV
dV_{OS}/dT	Input offset voltage drift	V_S = 5.5 V, T_A = –40°C to +125°C		2	7.5	µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.2 V to +5.5 V		6	20	µV/V
		V_S = 2.2 V to 5.5 V, T_A = –40°C to +125°C		15		
	Channel separation	At 1 kHz		130		dB
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	100	114		dB
		T_A = –40°C to +125°C	95			
INPUT BIAS CURRENT						
I_B	Input bias current			±0.2	±10	pA
		T_A = –40°C to +85°C			±500	
		T_A = –40°C to +125°C			±10	nA
I_{OS}	Input offset current			±0.2	±10	pA
		T_A = –40°C to +85°C			±500	
		T_A = –40°C to +125°C			±10	nA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		2.8		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz		10		$nV/\sqrt{Hz}$
		f = 10 kHz		9		
i_n	Input current noise density	f = 1 kHz		1.3		$fA/\sqrt{Hz}$
INPUT CAPACITANCE						
	Differential			5		pF
	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ	105	130		dB
		0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ, T_A = –40°C to +125°C	95	128		
		0.2 V < V_O < (V+) – 0.2 V, R_L = 2 kΩ	100	110		
PM	Phase margin	G = 1 V/V, V_S = 5 V, C_L = 15 pF		67		Degrees
FREQUENCY RESPONSE (V_S = 5.0 V, C_L = 50 pF)						
GBP	Gain bandwidth product	Unity gain		10		MHz
SR	Slew rate	G = +1		5		V/µs
t_S	Settling time	To 0.1%, 2-V step, G = +1		0.6		µs
		To 0.01%, 2-V step, G = +1		1		
	Overload recovery time	V_{IN} × G > V_S		200		ns
THD+N	Total harmonic distortion + noise(1)	V_O = 4 V_{PP}, G = +1, f = 10 kHz, R_L = 10 kΩ		0.0005%		
		V_O = 2 V_{PP}, G = +1, f = 10 kHz, R_L = 600 Ω		0.005%		

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

Electrical Characteristics: V_S = 2.2 V to 5.5 V or ±1.1 V to ±2.75 V (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from both rails	R_L = 10 kΩ		10	20	mV
		R_L = 10 kΩ, T_A = –40°C to +125°C			30	
		R_L = 2 kΩ		25	45	
		R_L = 2 kΩ, T_A = –40°C to +125°C			55	
I_{SC}	Short-circuit current	V_S = 5.5 V	See the *Typical Characteristics*			mA
C_L	Capacitive load drive		See the *Typical Characteristics*			
R_O	Open-loop output resistance	I_O = 0 mA, f = 1 MHz		180		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.2		5.5	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5 V		0.65	0.75	mA
		I_O = 0 mA, V_S = 5.5 V, T_A = –40°C to +125°C			0.8	
	Power-on time	V+ = 0 V to 5 V, to 90% I_Q level		28		µs
TEMPERATURE						
	Specified range		–40		125	°C
	Operating range		–40		150	°C

6.6 Typical Characteristics

at T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

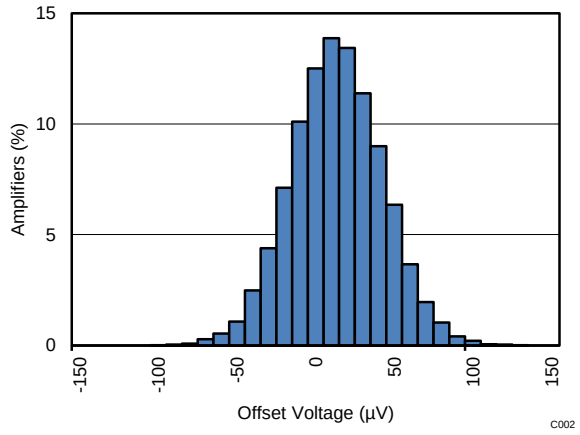


Figure 1. Offset Voltage Production Distribution Histogram

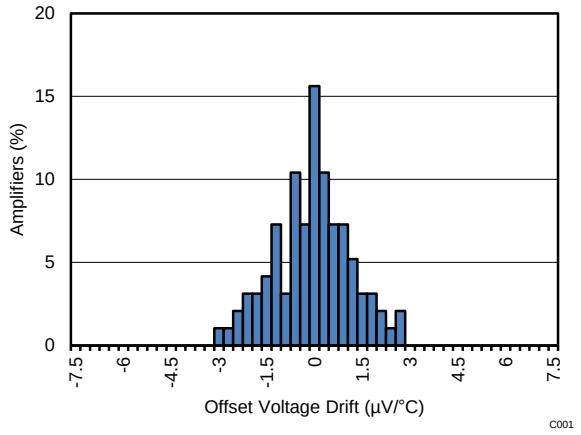


Figure 2. Offset Voltage Drift Distribution Histogram

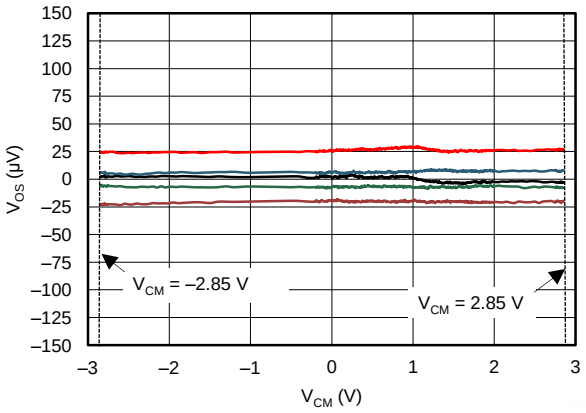


Figure 3. Offset Voltage vs Common-Mode Voltage

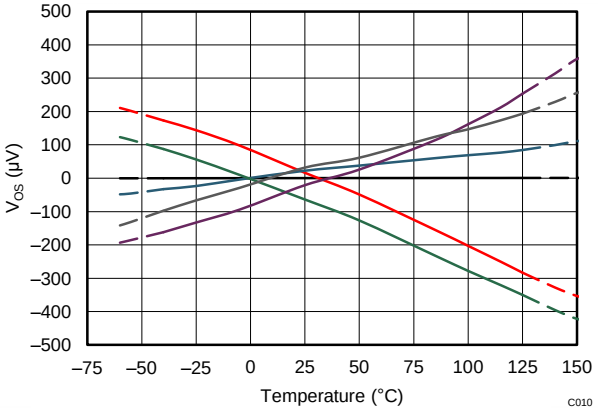


Figure 4. Offset Voltage vs Temperature

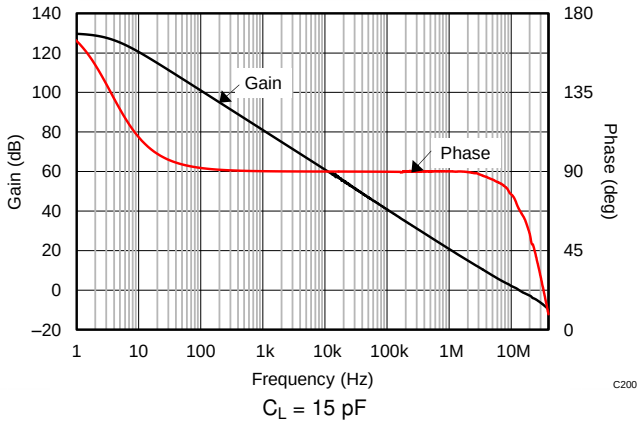


Figure 5. Open-Loop Gain and Phase vs Frequency

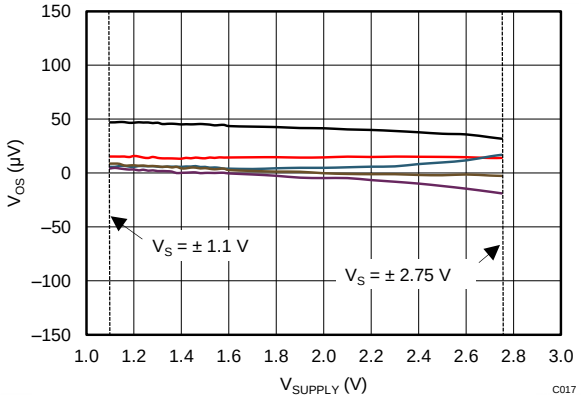


Figure 6. Offset Voltage vs Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

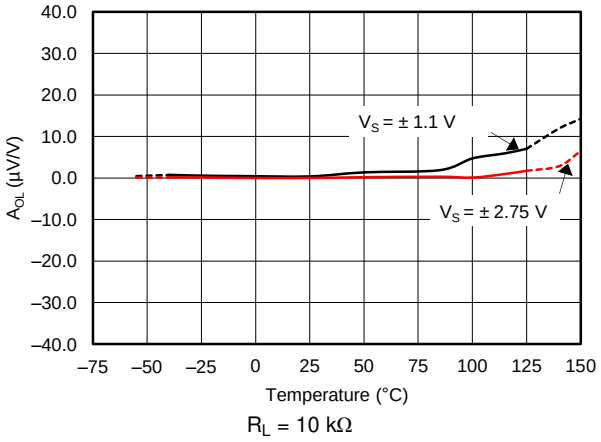


Figure 7. Open-Loop Gain vs Temperature

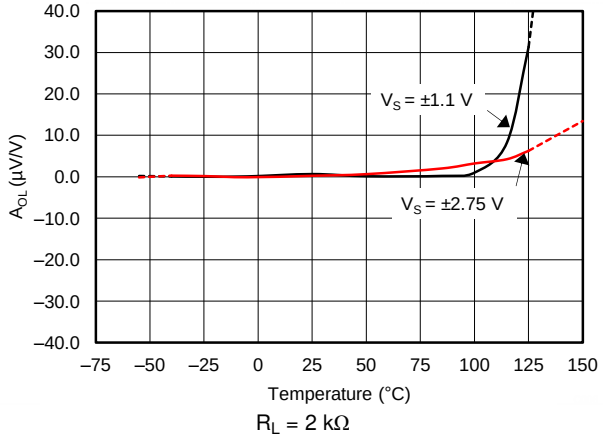


Figure 8. Open-Loop Gain vs Temperature

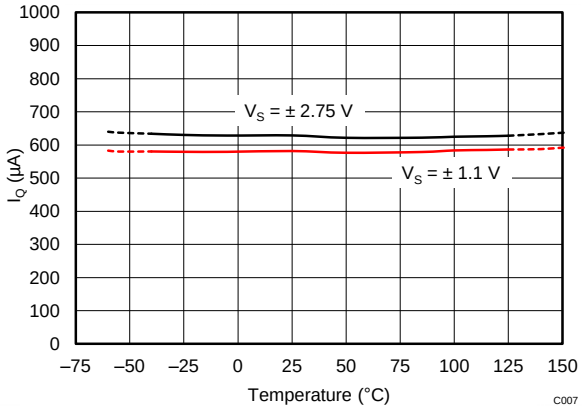


Figure 9. Quiescent Current vs Temperature

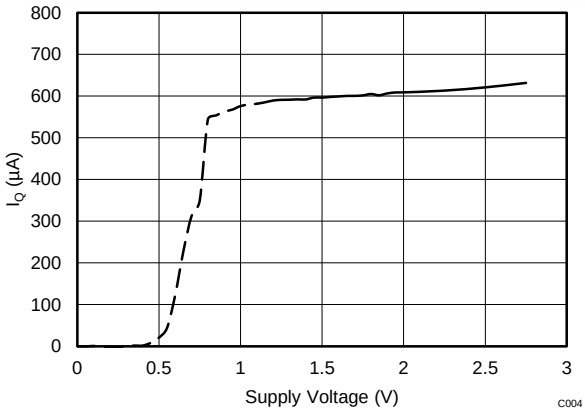


Figure 10. Quiescent Current vs Supply Voltage

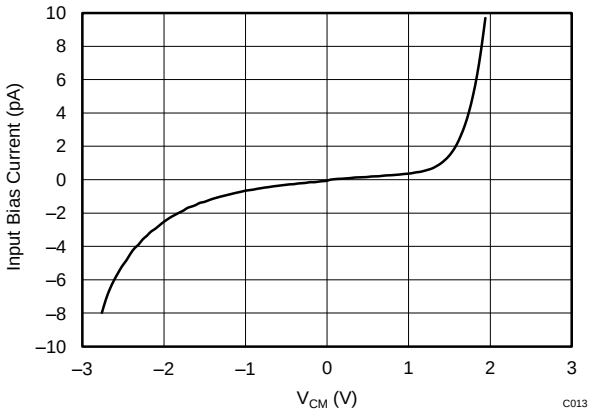


Figure 11. Input Bias Current vs Common-Mode Voltage

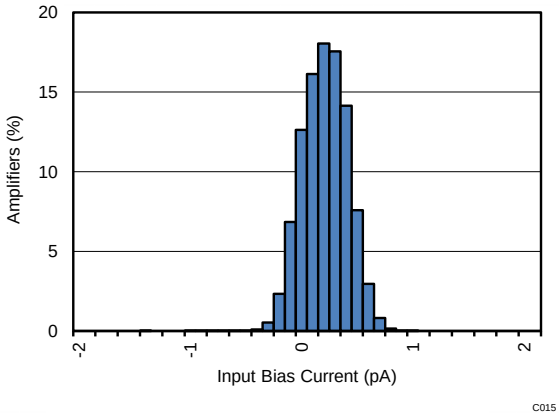


Figure 12. Input Bias Current Distribution Histogram

Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

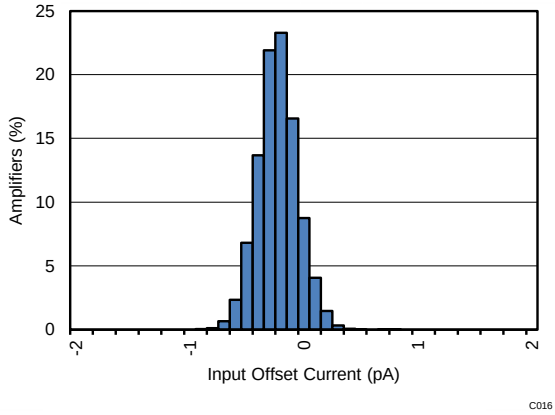


Figure 13. Input Offset Current Distribution Histogram

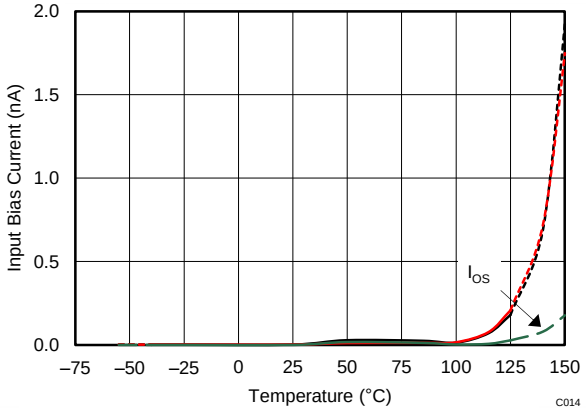


Figure 14. Input Bias Current vs Temperature

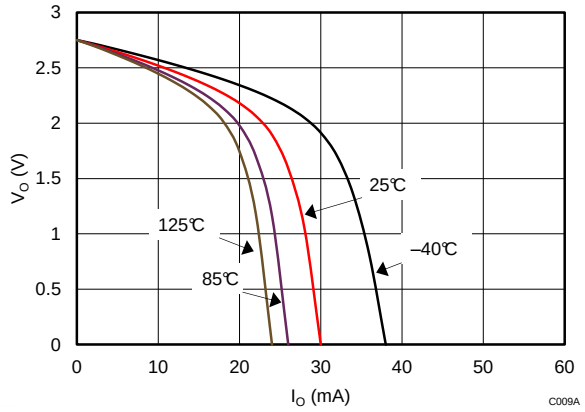


Figure 15. Output Voltage Swing (Positive) vs Output Current

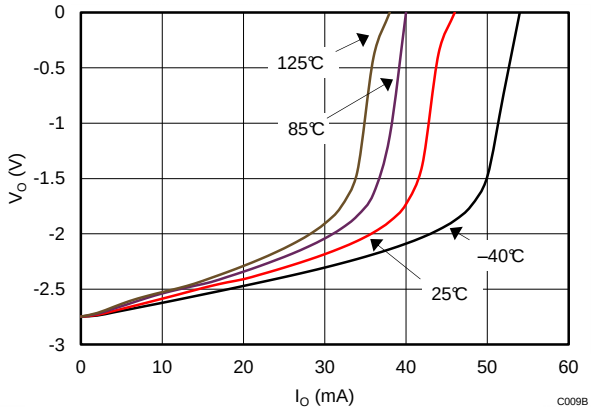


Figure 16. Output Voltage Swing (Negative) vs Output Current

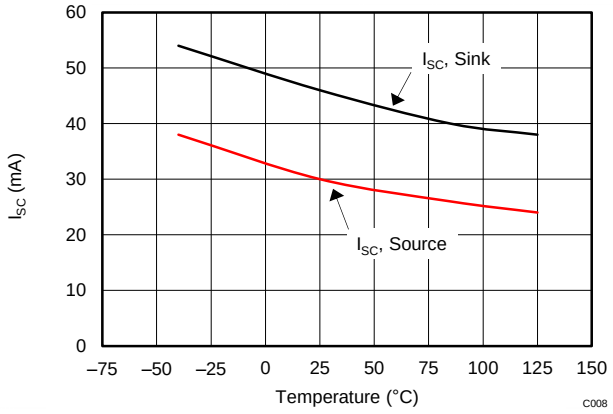


Figure 17. Short-Circuit Current vs Temperature

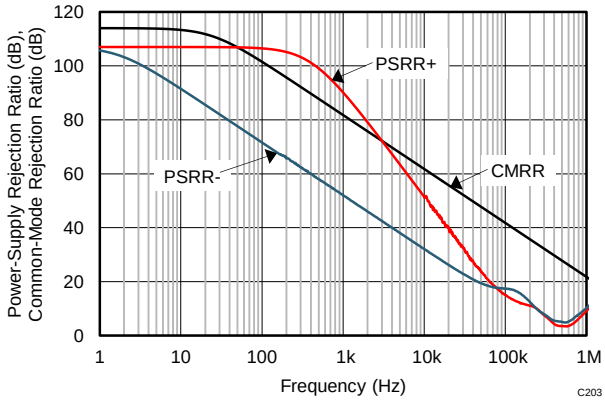


Figure 18. CMRR and PSRR vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

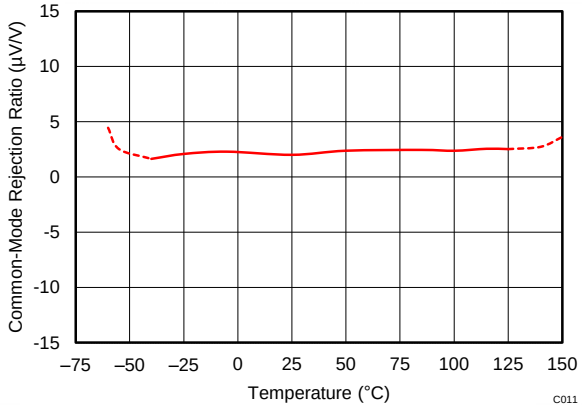


Figure 19. CMRR vs Temperature

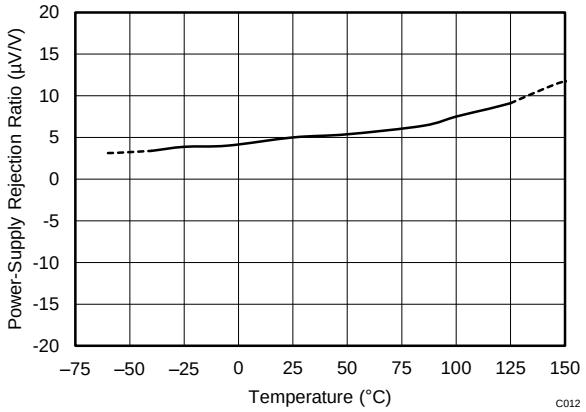


Figure 20. PSRR vs Temperature

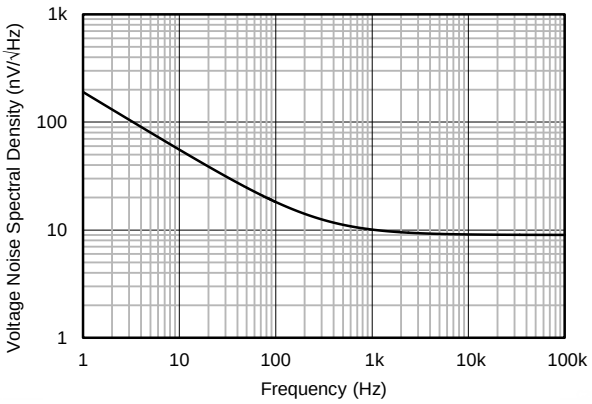


Figure 21. Input Voltage Noise Spectral Density vs Frequency

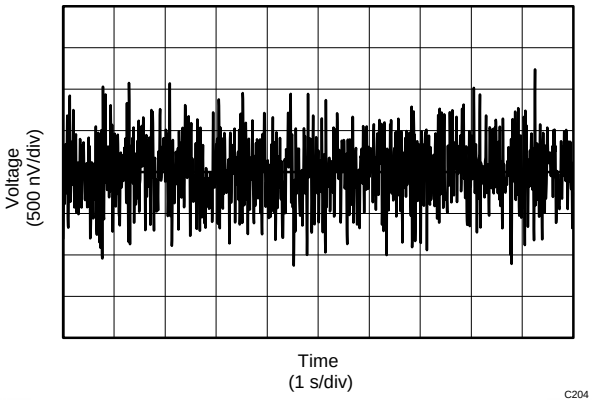
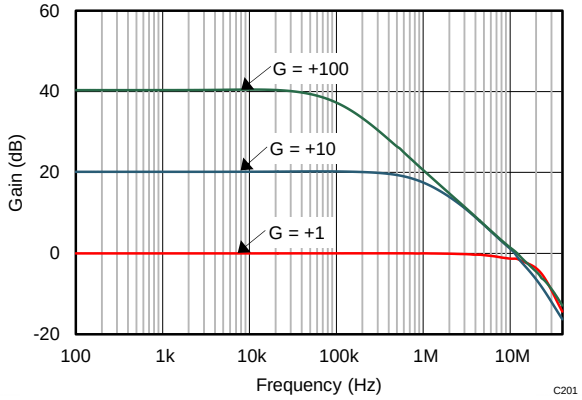
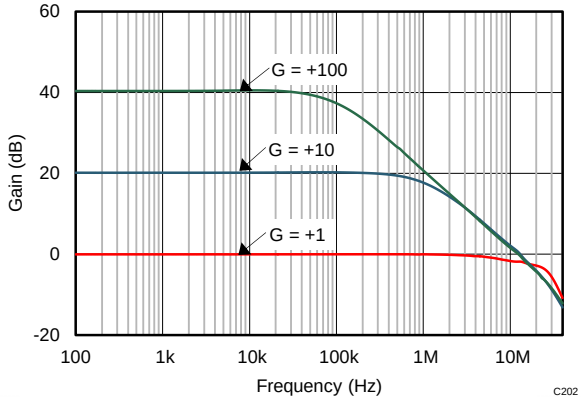


Figure 22. 0.1-Hz to 10-Hz Input Voltage Noise



V_S = 1.8 V, R_L = 10 kΩ, C_L = 15 pF

Figure 23. Closed-Loop Gain vs Frequency



V_S = 5.5 V, R_L = 10 kΩ, C_L = 15 pF

Figure 24. Closed-Loop Gain vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

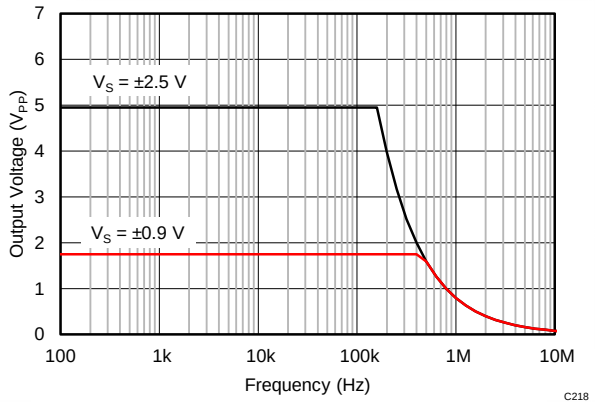


Figure 25. Maximum Output Voltage vs Frequency

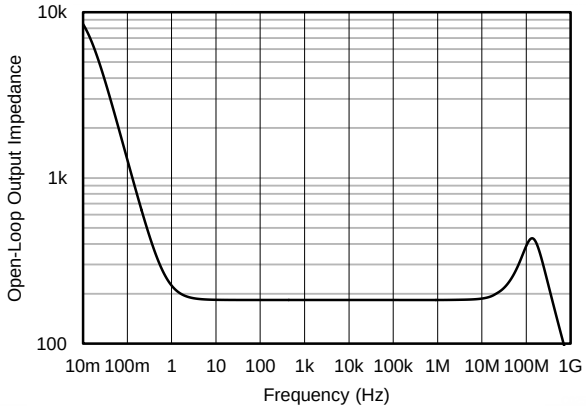


Figure 26. Open-Loop Output Impedance vs Frequency

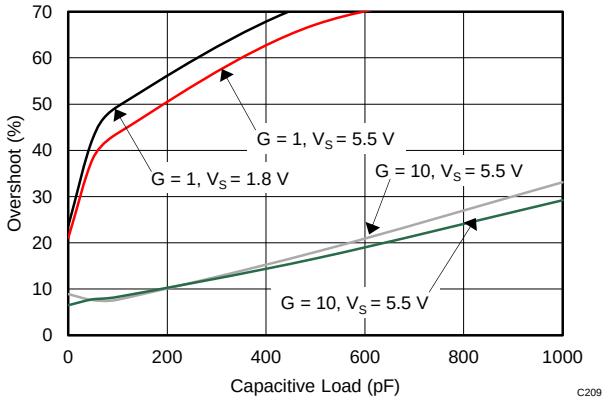
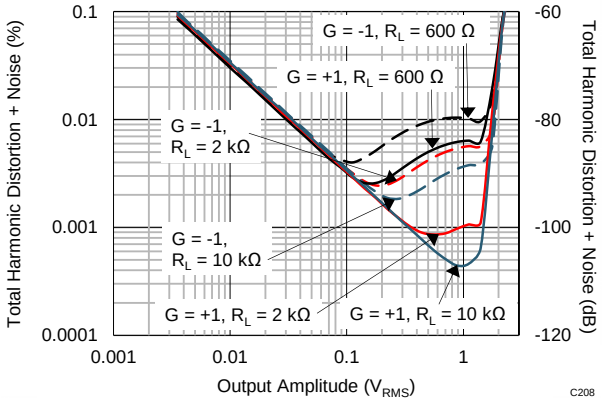
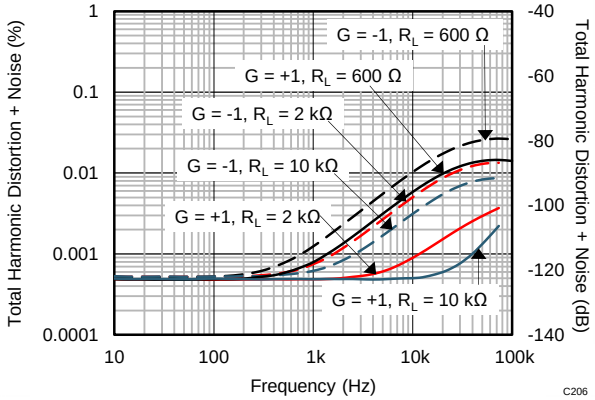


Figure 27. Small-Signal Overshoot vs Load Capacitance



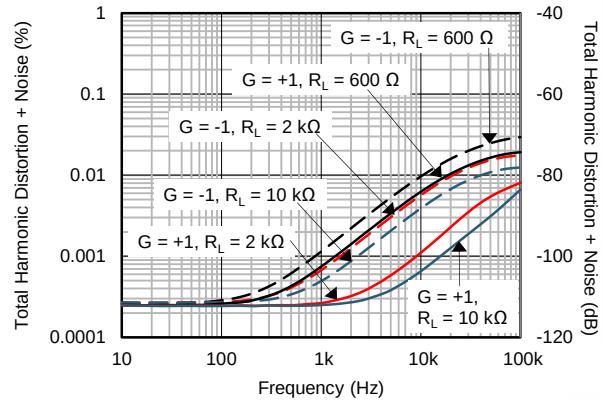
f = 10 kHz, V_S = ±2.5 V, filter bandwidth = 500 kHz

Figure 28. THD+N vs Amplitude



V_{IN} = 2 V_{PP}, V_S = ±2.5 V, filter bandwidth = 500 kHz

Figure 29. THD+N vs Frequency



V_{IN} = 4 V_{PP}, V_S = ±2.5 V, filter bandwidth = 500 kHz

Figure 30. THD+N vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)

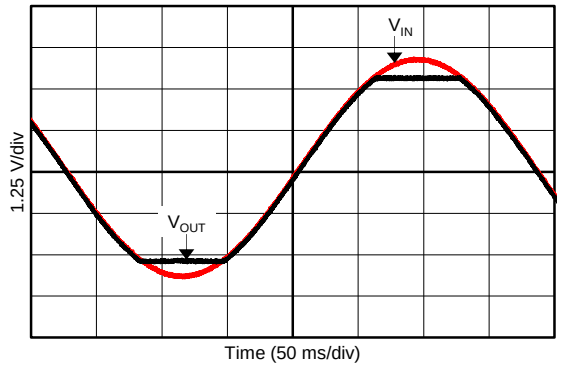


Figure 31. No Phase Reversal

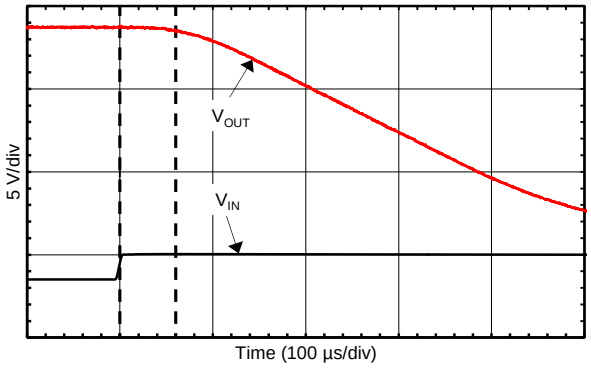


Figure 32. Positive Overload Recovery

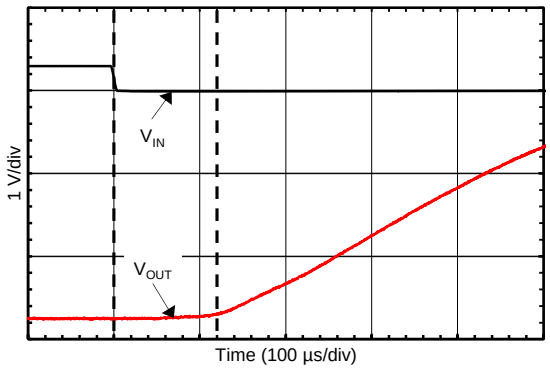
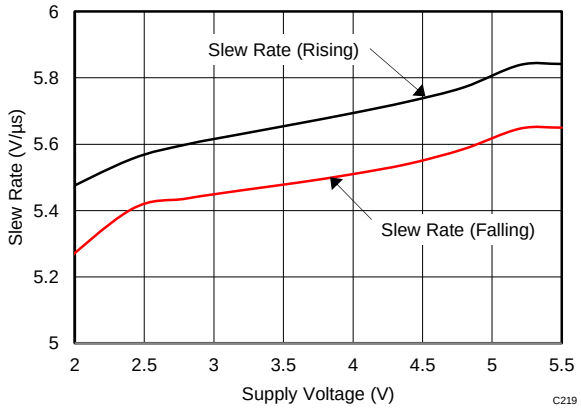
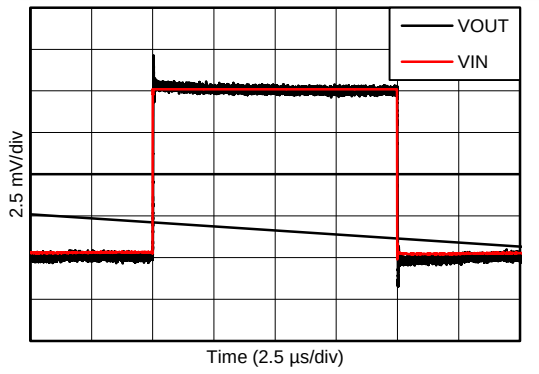


Figure 33. Negative Overload Recovery



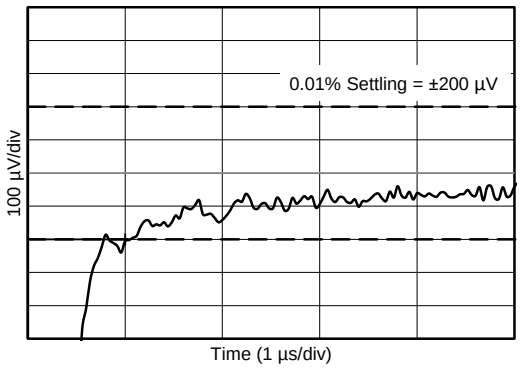
C_L = 15 pF

Figure 34. Slew Rate vs Supply Voltage



V_{IN} = 10 mV_{PP}, G = +1, C_L = 15 pF

Figure 35. Small-Signal Step Response

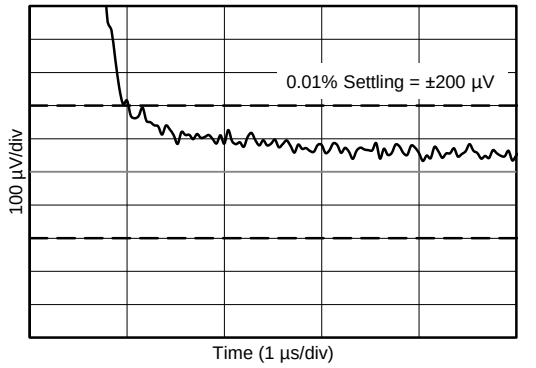


V_{IN} = 2-V step

Figure 36. 0.01% Positive Settling Time

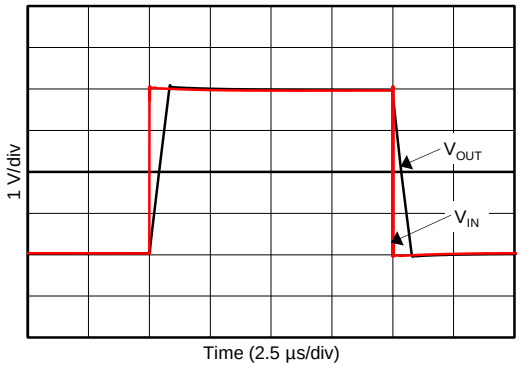
Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ (unless otherwise noted)



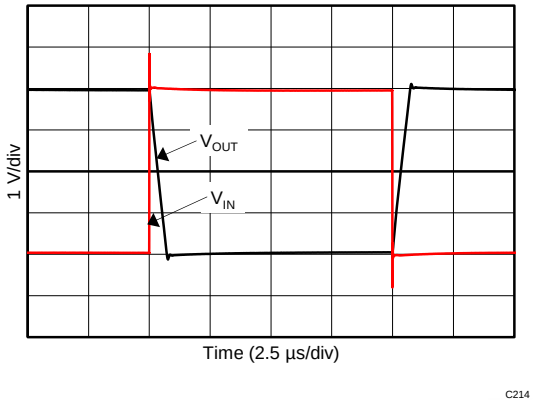
V_{IN} = 2-V step

Figure 37. 0.01% Negative Settling Time



V_{IN} = 4 V_{PP}, G = +1, C_L = 15 pF

Figure 38. Large-Signal Step Response



V_{IN} = 4 V_{PP}, G = –1, C_L = 15 pF

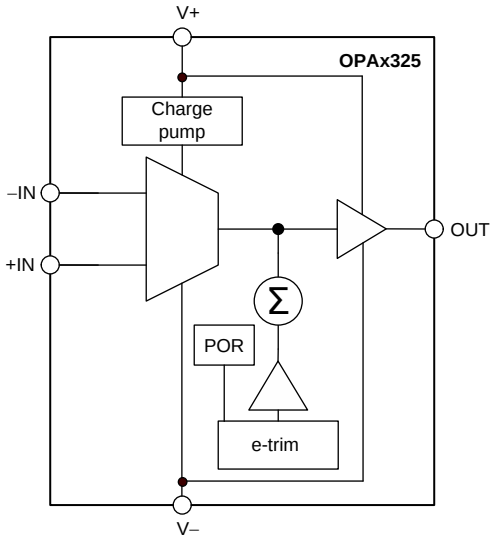
Figure 39. Large-Signal Step Response

7 Detailed Description

7.1 Overview

The OPA2325 belongs to a new generation of low-noise, e-trim™ operational amplifiers that provide outstanding dc precision. The OPA2325 also has a highly linear input stage with zero-crossover distortion that delivers excellent CMRR and distortion performance across the full rail-to-rail input range. In addition, this device has a wide supply range with excellent PSRR. This feature, combined with low quiescent current, makes the OPA2325 suitable for applications that are battery-powered without regulation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Zero-Crossover Input Stage

Traditional complementary metal-oxide semiconductor (CMOS) rail-to-rail input amplifiers use a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. This configuration results in sudden change in offset voltage when the input stage transitions from the p-channel metal-oxide-semiconductor field effect transistor (PMOS) to the n-type field effect transistor (NMOS), or vice-versa, as shown in Figure 40. This transition results in significant degradation of CMRR and PSRR performance of the amplifier.

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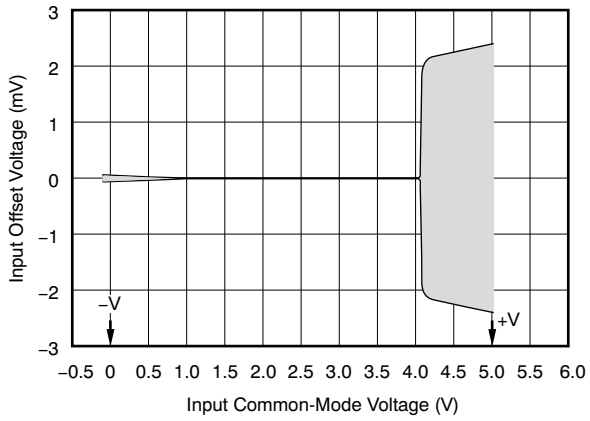

Figure 40. Input Common-Mode Voltage vs Input Offset Voltage (Traditional Rail-to-Rail Input CMOS Amplifiers)

The OPA2325 series of amplifiers includes an internal charge pump that powers the amplifier input stage with an internal supply rail that is higher than the external power supply. The internal supply rail allows a single differential pair to operate and to be linear across the entire input common-mode voltage range, thus eliminating crossover distortion. Rail-to-rail amplifiers that use this technique to eliminate crossover distortion are called *zero-crossover amplifiers*.

The single differential pair combined with the charge pump allows the OPA2325 to provide superior CMRR across the entire common-mode input range, which extends 100 mV beyond both power-supply rails. Figure 41 shows the input offset voltage versus input common-mode voltage plot for the OPA2325. Note that unlike traditional rail-to-rail CMOS amplifiers, there is no transition region for the OPA2325.

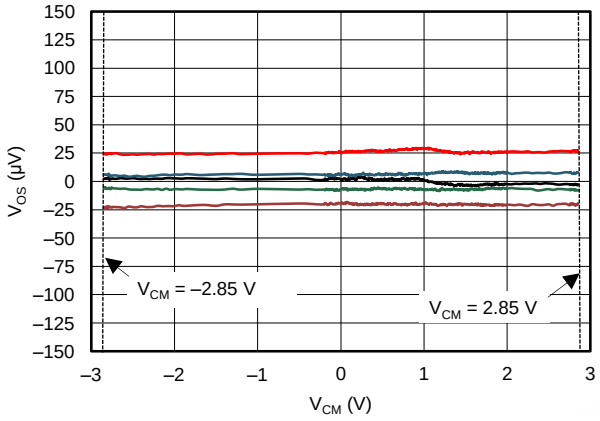

Figure 41. Offset Voltage vs Common-Mode Voltage (Zero-Crossover)

Feature Description (continued)

7.3.2 Low Input Offset Voltage

The OPA2325 is manufactured using TI's e-trim technology. Each amplifier is trimmed in production, thereby minimizing errors associated with input offset voltage. The e-trim technology is a TI proprietary method of trimming internal device parameters during either wafer probing or final testing. This process allows the OPA2325 to have excellent offset specifications of 150 µV (maximum). Figure 42 shows the offset voltage distribution for the OPA2325.

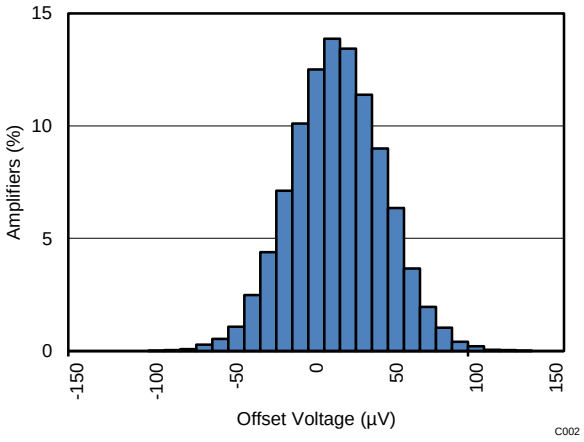

Figure 42. Offset Voltage Distribution

7.3.3 Input and ESD Protection

The OPA2325 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table. Figure 43 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input; thus, keep the value to a minimum in noise-sensitive applications.

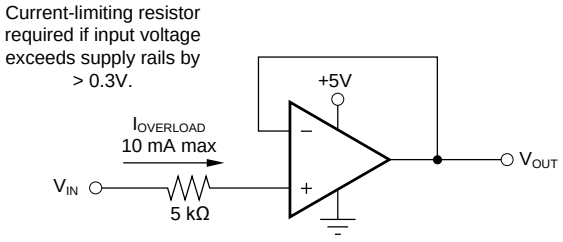

Figure 43. Input Current Protection

7.4 Device Functional Modes

The OPA2325 has a single functional mode and is operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power-supply voltage for the OPA2325 is 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA2325 series features e-trim™, a proprietary technique in which offset voltage is adjusted during the final steps of manufacturing. As a result, the OPA2325 delivers excellent offset voltage (40 μV, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and A_{OL}. The OPA2325 also features a linear input stage with zero-crossover distortion, resulting in excellent CMRR over the entire input range, which extends from 100 mV below the negative rail to 100 mV above the positive rail.

8.1.1 Operating Characteristics

The OPA2325 family of amplifiers has parameters that are fully specified from 2.2 V to 5.5 V (±1.1 V to ±2.75 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

8.1.2 Basic Amplifier Configurations

The OPA2325 is unity-gain stable. The device does not exhibit output phase inversion when the input is overdriven. A typical single-supply connection is shown in Figure 44. The OPA2325 is configured as a basic inverting amplifier with a gain of –10 V/V. This single-supply connection has an output centered on the common-mode voltage, V_{CM}. For the circuit shown, this voltage is 2.5 V, but can be any value within the common-mode input voltage range.

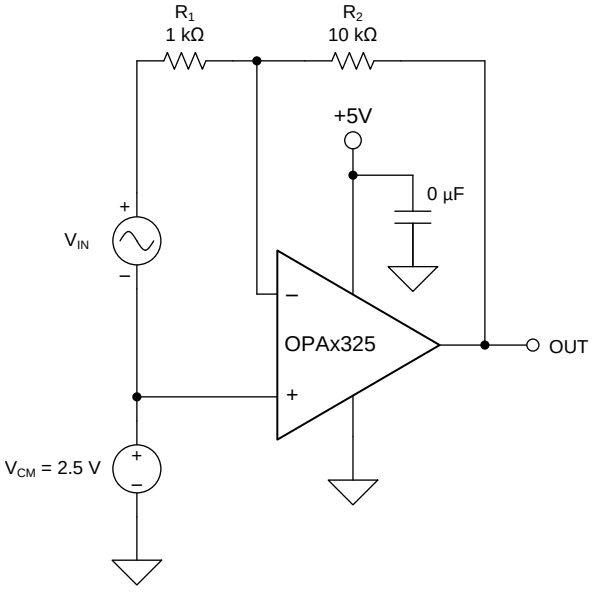

Figure 44. Basic Single-Supply Connection

Application Information (continued)

8.1.3 Driving an Analog-to-Digital Converter

The low-noise and wide-gain bandwidth of the OPA2325, combined with rail-to-rail input/output and zero-crossover distortion, make the device an ideal input driver for ADCs. Figure 45 shows the OPA2325 driving an ADC. The amplifier is connected as a unity-gain, noninverting buffer.

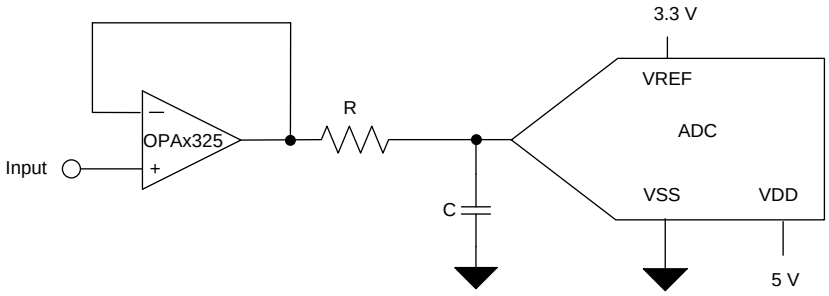

Figure 45. The OPA2325 as an Input Driver for ADCs

8.2 Typical Application

Operational amplifiers are commonly used as unity-gain buffers. Figure 46 shows the schematic for an amplifier configured as a unity-gain buffer. If the input signal range to the amplifier is very close to the rails or includes the rails, a rail-to-rail amplifier must be used. However, regular rail-to-rail amplifiers introduce significant distortion to the signal. This design compares the distortion introduced by a typical CMOS input amplifier with that of the OPA2325 (a zero-crossover amplifier).

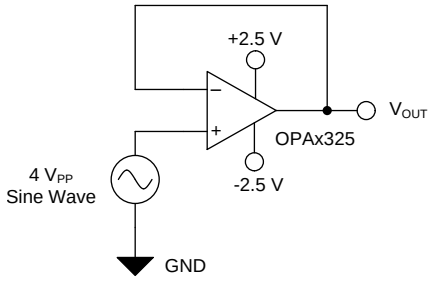

Figure 46. The OPA2325 Configured as a Unity-Gain Buffer Amplifier

8.2.1 Design Requirements

The following parameters are used for this design example:

- Gain = +1 V/V (inverting gain)
- V+ = 2.5 V, V– = –2.5 V
- Input signal = 4 V_{PP}, f = 1-kHz sine wave

Typical Application (continued)

8.2.2 Detailed Design Procedure

Traditional CMOS rail-to-rail input amplifiers use a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 47.

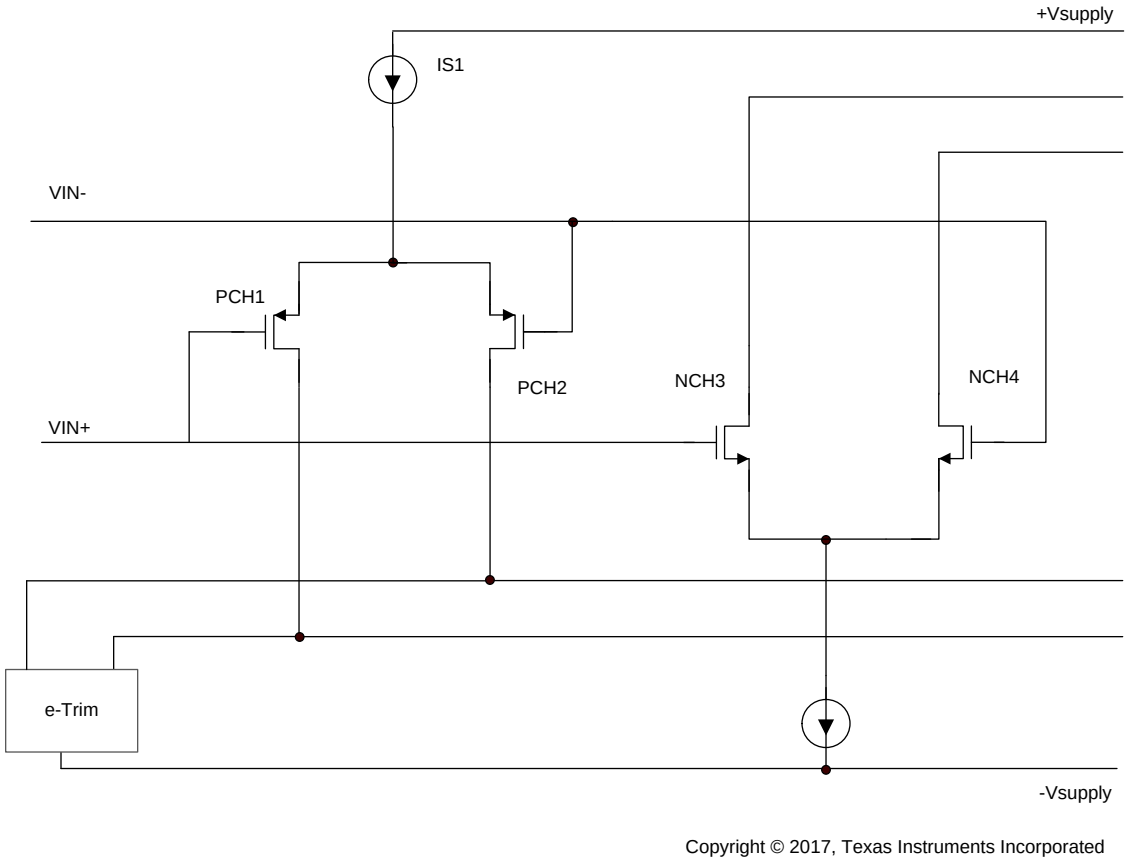

Figure 47. Complementary Input Stage (Traditional Rail-to-Rail Input CMOS Amplifiers)

Typical Application (continued)

The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1 V to 200 mV above the positive supply, and the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 1 V. There is a small transition region, typically (V+) – 1.1 V to (V+) – 0.9 V, in which both pairs are on. This transition region is shown in Figure 48 for a traditional rail-to-rail input CMOS amplifier. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded when compared to device operation outside of this region.

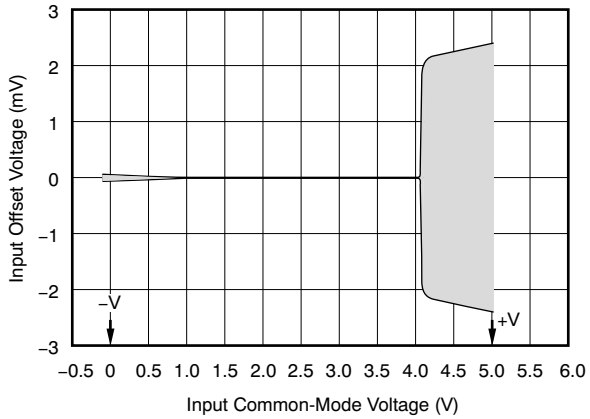

Figure 48. Input Offset Voltage vs Common-Mode Voltage (For Traditional Rail-to-Rail Input CMOS Amplifiers)

The OPA2325 amplifier includes an internal charge pump that powers the amplifier input stage with an internal supply rail that is higher than the external power supply. The internal supply rail allows a single differential pair to operate and to be linear across the entire input common-mode voltage range, as shown in Figure 49.

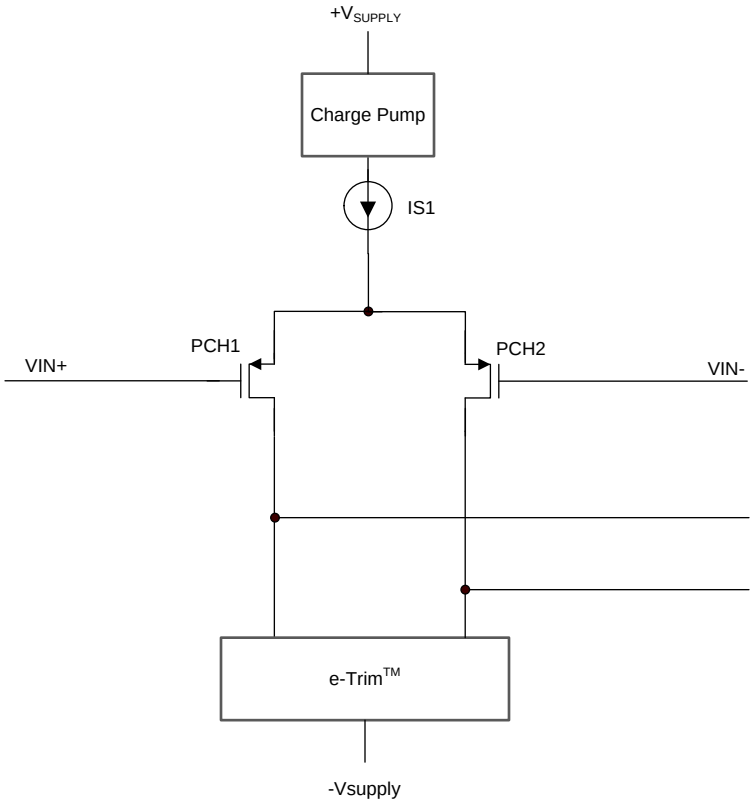

Figure 49. Single Differential Input Pair with a Charge Pump (Zero-Crossover)

Typical Application (continued)

The unique zero-crossover topology shown in Figure 49 eliminates the input offset transition region, typical of most rail-to-rail input operational amplifiers. This topology allows the OPA2325 to provide superior CMRR across the entire common-mode input range that extends 100 mV beyond both power-supply rails. Figure 50 shows the input offset voltage versus input common-mode voltage plot for the OPA2325.

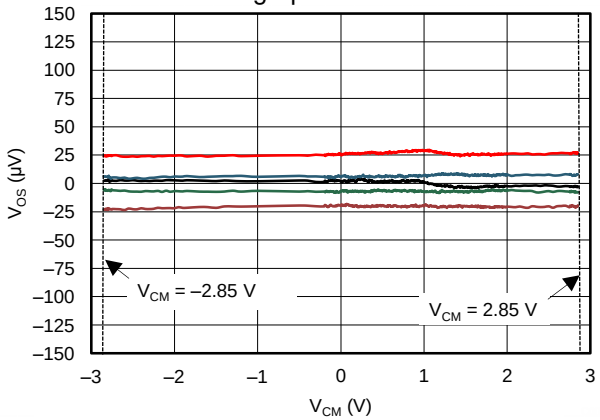

Figure 50. Offset Voltage vs Common-Mode Voltage (OPA2325, Zero-Crossover Amplifier)

The OPA2325 and a typical CMOS amplifier were used in identical circuits where these amplifiers were configured as a unity-gain buffer amplifier; see Figure 51 and Figure 52. A pure sine wave with an amplitude of 2 V (4 V_{PP}) was given as input to the two identical circuits of Figure 51 and Figure 52. The outputs of these circuits were captured on a spectrum analyzer. Figure 53 and Figure 54 illustrate the output voltage spectrum for the OPA2325 and a typical CMOS rail-to-rail amplifier, respectively. The output of the OPA2325 has very few spurs and harmonics when compared to the typical rail-to-rail CMOS amplifier, as illustrated in Figure 55.

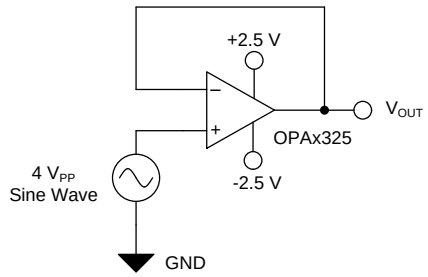

Figure 51. OPA2325 as a Unity-Gain Buffer

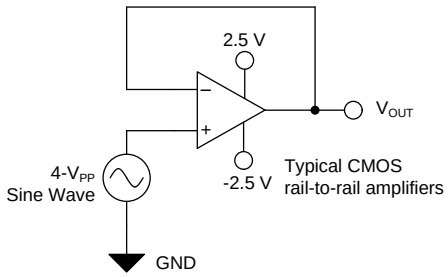

Figure 52. Typical CMOS Rail-to-Rail Amplifier as a Unity-Gain Buffer

Typical Application (continued)

8.2.3 Application Curves

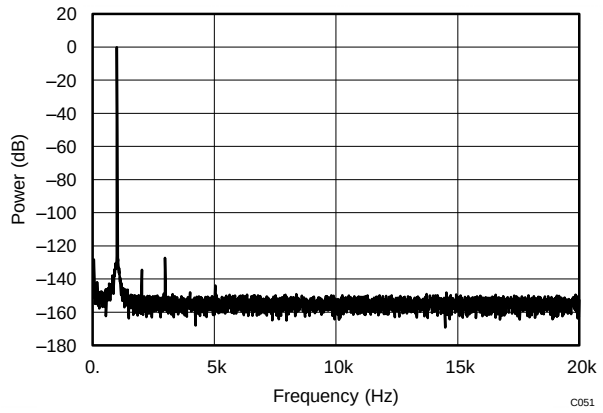

Figure 53. Output Voltage Spectrum (OPA2325)

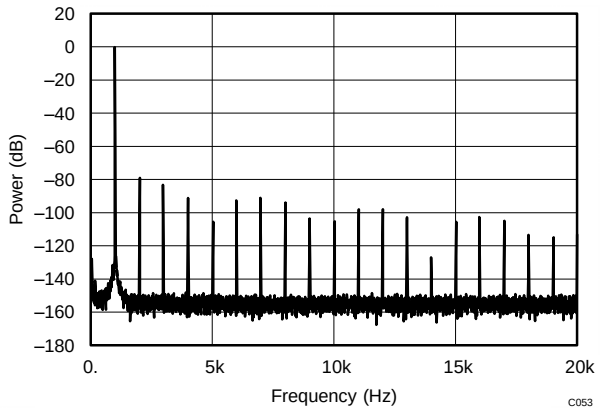

Figure 54. Output Voltage Spectrum (Typical CMOS Rail-to-Rail Amplifier)

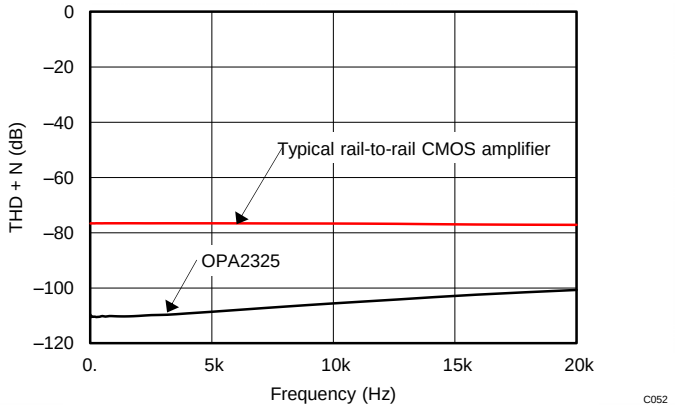

Figure 55. THD+N vs Frequency

9 Power Supply Recommendations

The OPA2325 is specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information refer to, see *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in Figure 57, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

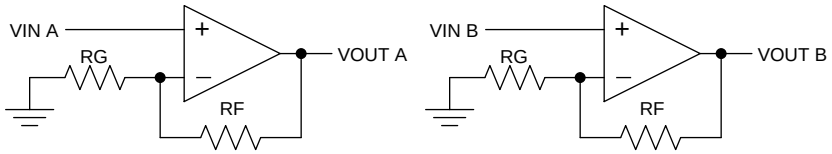

Figure 56. Schematic Representation for Figure 57

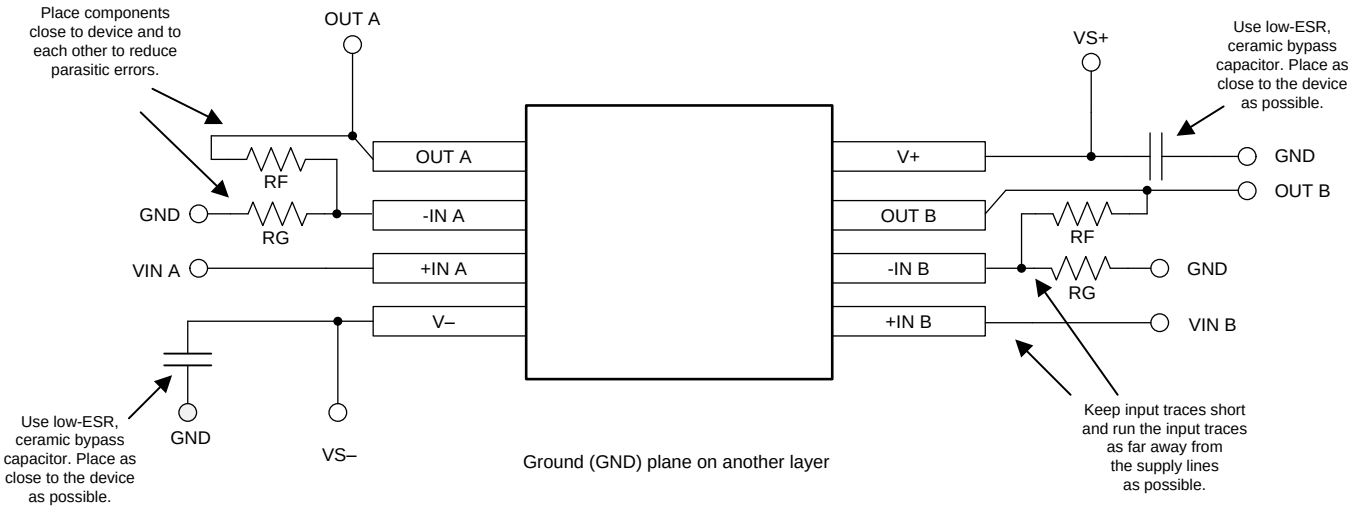

Figure 57. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Circuit Board Layout Techniques

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

e-trim, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2325ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2325	Samples
OPA2325IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	18L6	Samples
OPA2325IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	18L6	Samples
OPA2325IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2325	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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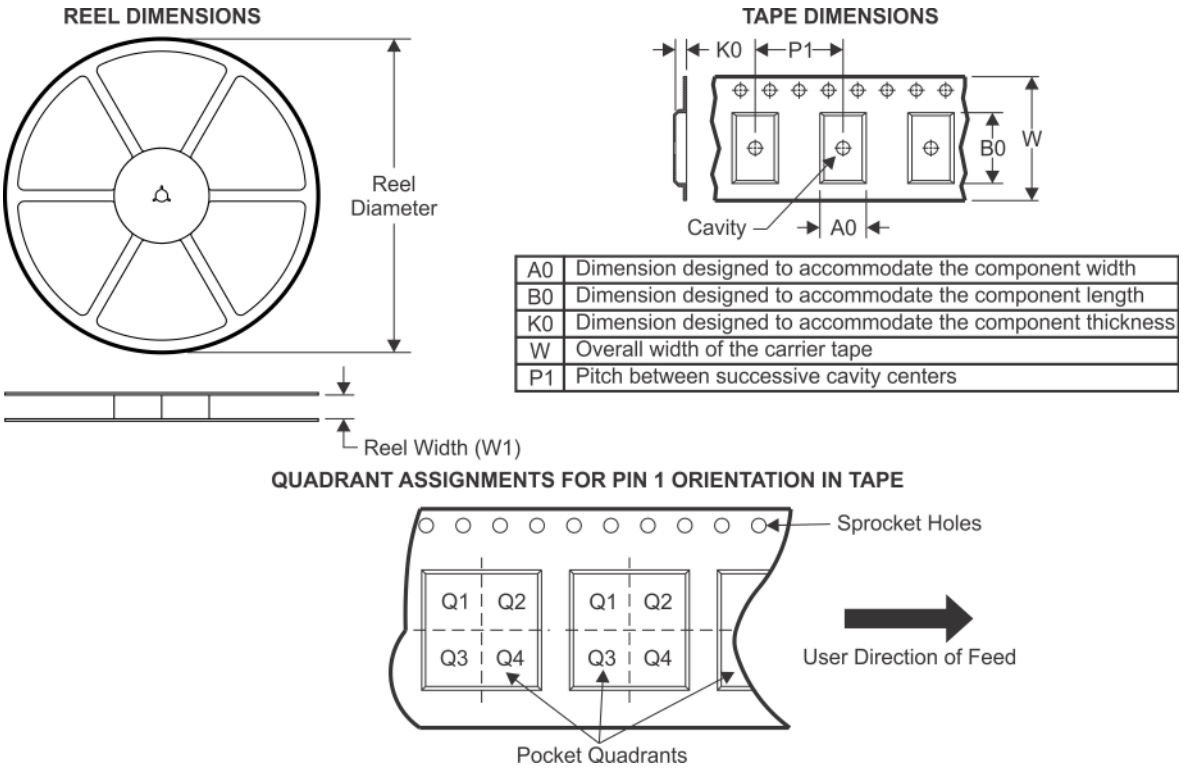
TAPE AND REEL INFORMATION

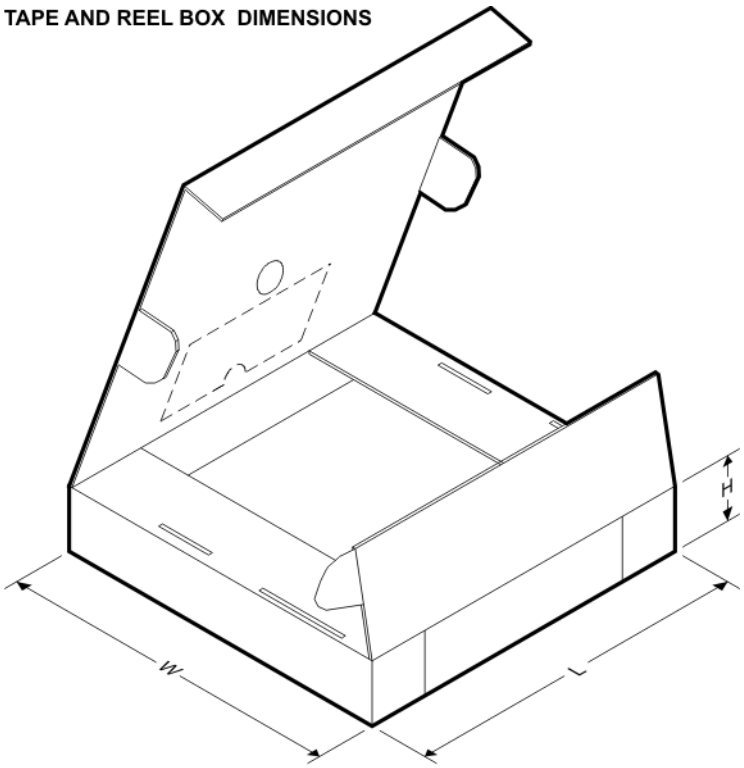


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2325IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2325IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

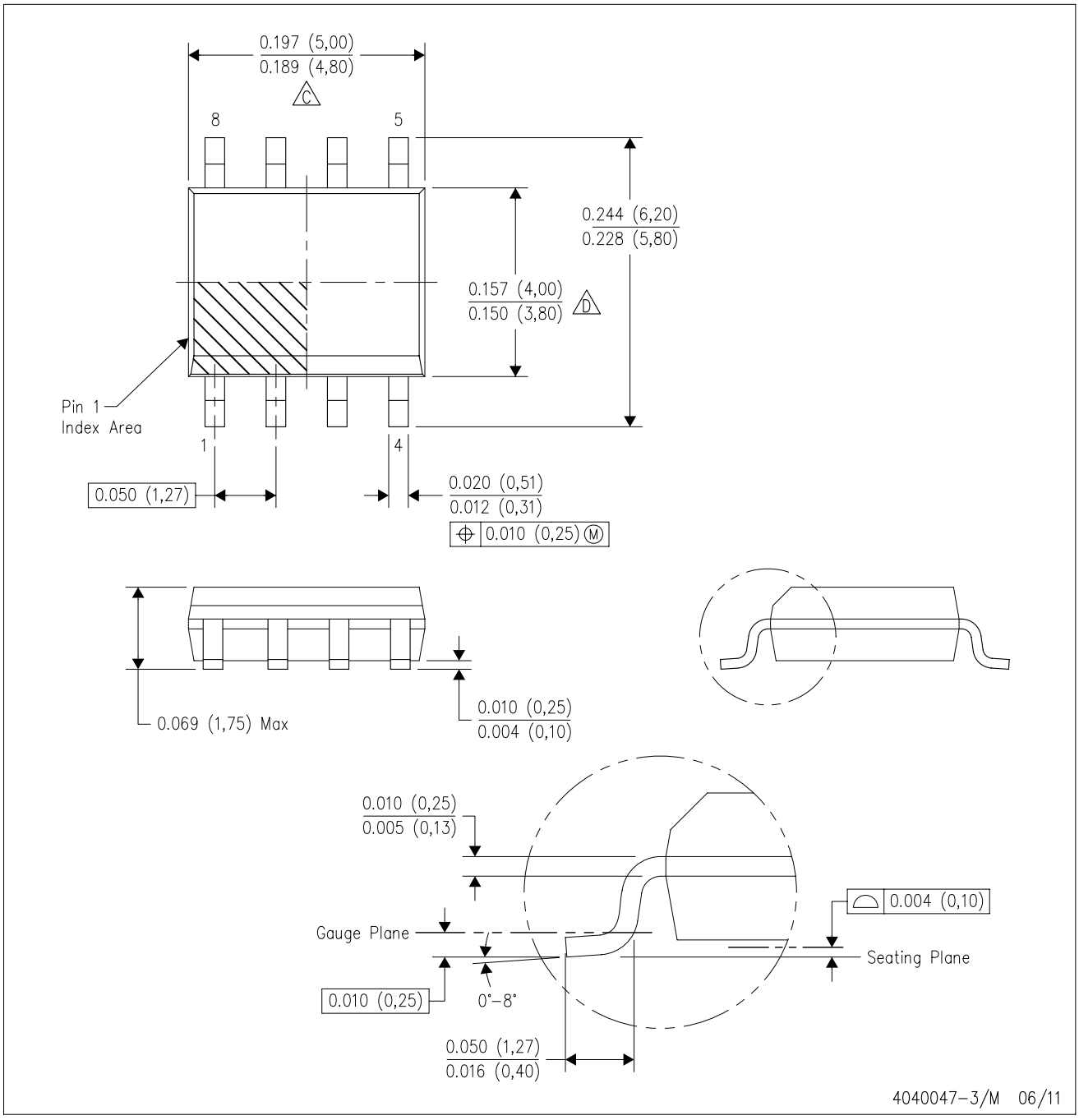
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

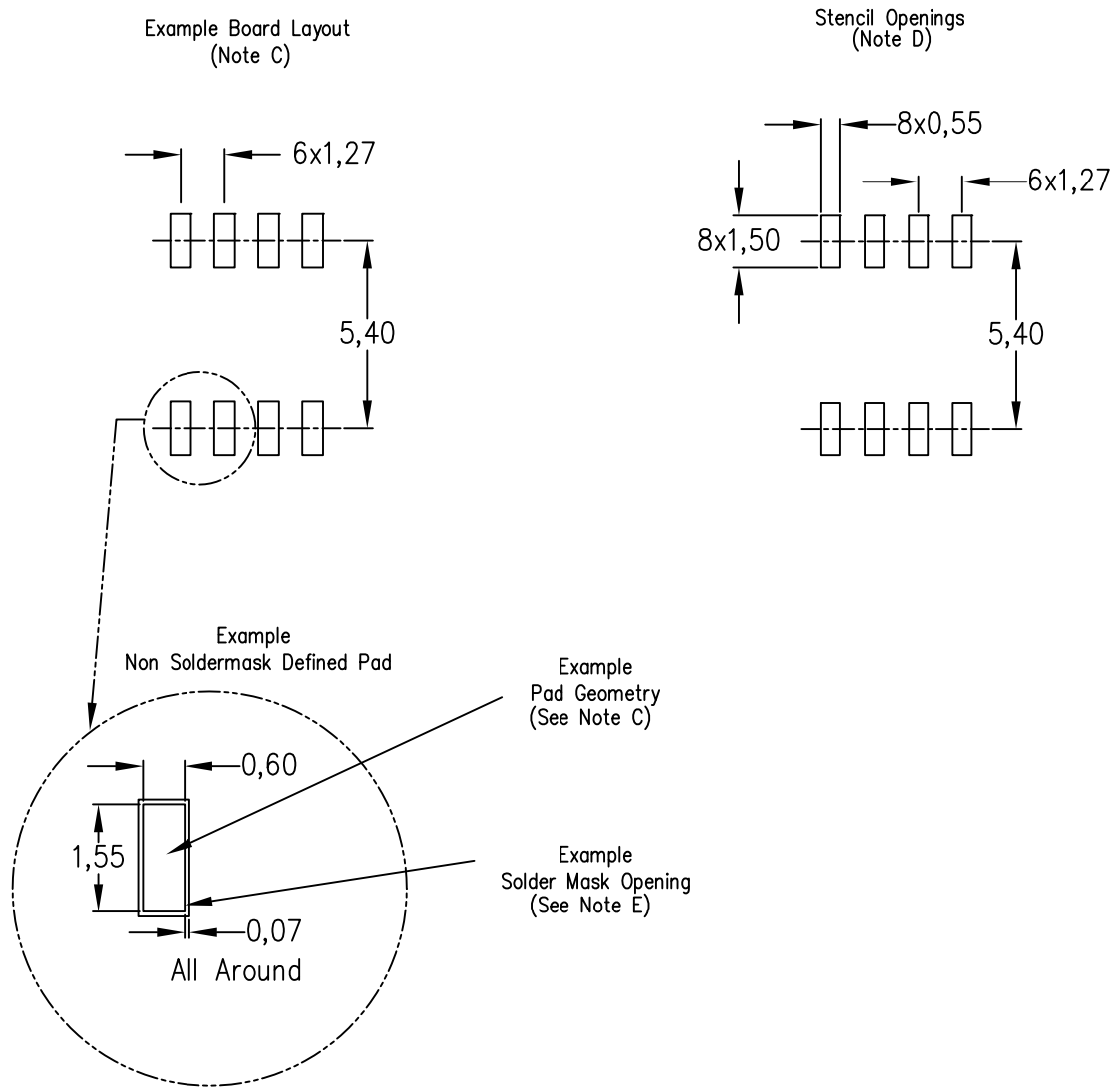
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2325IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2325IDR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



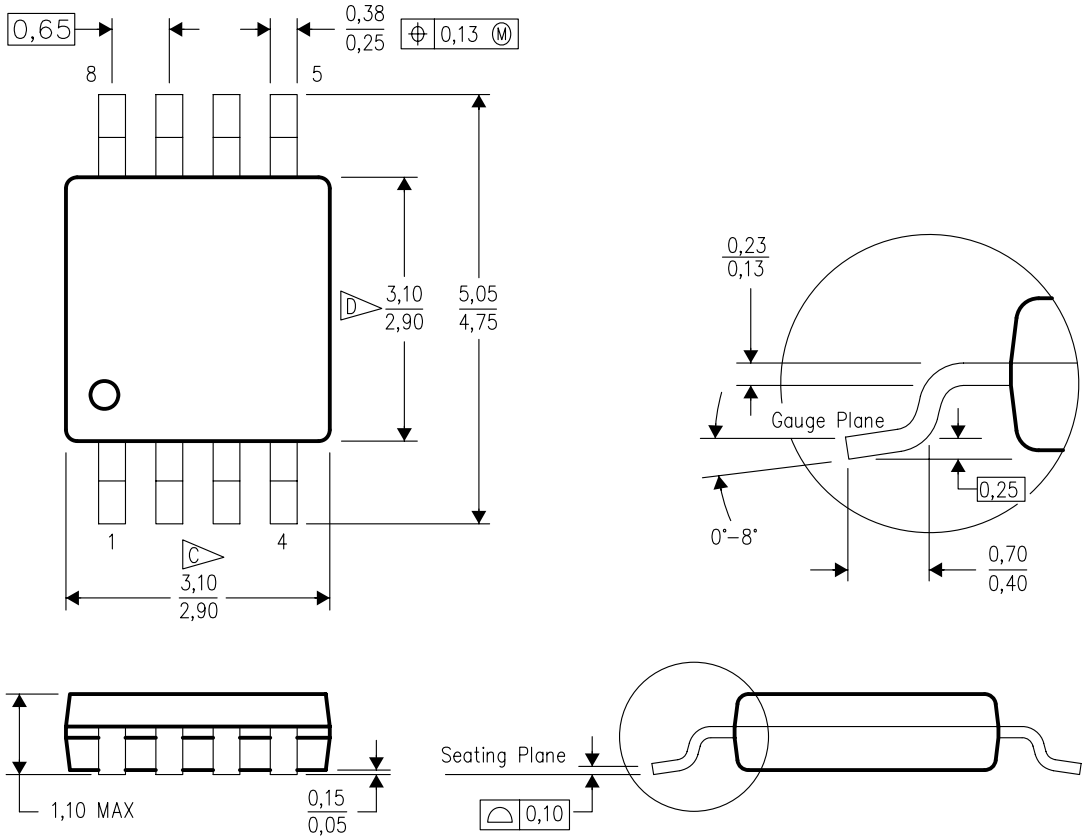
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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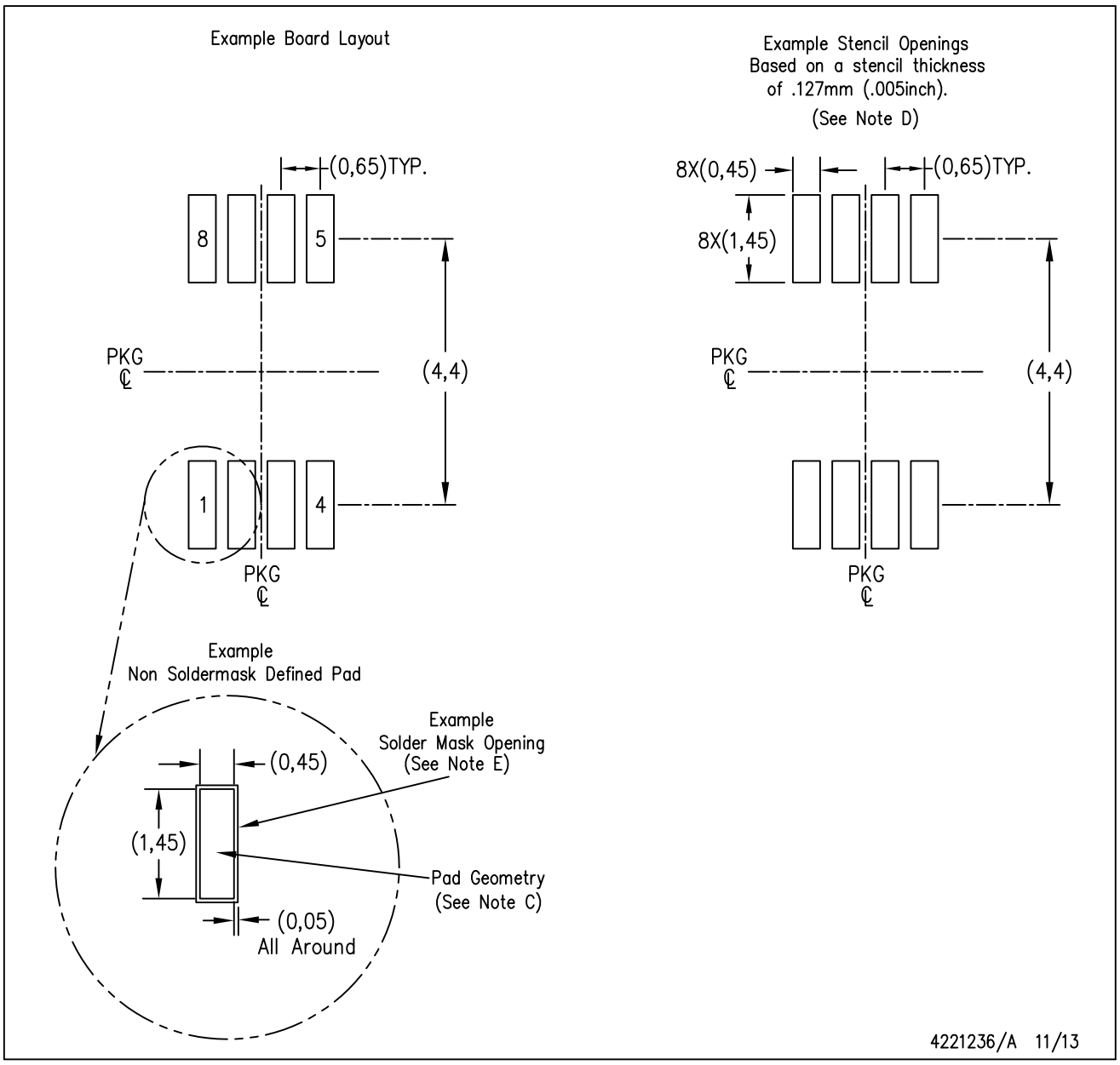
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
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