

# 74ABT648

Octal transceiver/register; inverting; 3-state

Rev. 04 — 27 April 2005

Product data sheet

## 1. General description

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The 74ABT648 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT648 transceiver/register consists of bus transceiver circuits with inverting 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes HIGH.

Output enable ( $\overline{OE}$ ) and direction (DIR) pins are provided to control the transceiver function.

In the transceiver mode, data present at the high-impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) pins determine whether data is stored or transferred through the device in real time. The DIR determines which bus will receive data when the  $\overline{OE}$  is active (LOW).

In the isolation mode ( $\overline{OE} = \text{HIGH}$ ), data from bus A may be stored in the B register and/or data from bus B may be stored in the A register. Outputs from real time or stored registers will be inverted. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses A or B may be driven at a time.

## 2. Features

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- Combines 74ABT245 and 74ABT374A type functions in one device
- Independent registers for A and B buses
- Multiplexed real time and stored data
- 3-state buffers
- Live insertion and extraction permitted
- Output capability: +64 mA and -32 mA
- Power-up 3-state
- Power-up reset
- Latch-up protection:
  - ◆ JESD78: exceeds 500 mA
- ESD protection:
  - ◆ MIL STD 883 method 3015: exceeds 2000 V
  - ◆ Machine model: exceeds 200 V

**PHILIPS**

### 3. Quick reference data

**Table 1: Quick reference data**

$GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

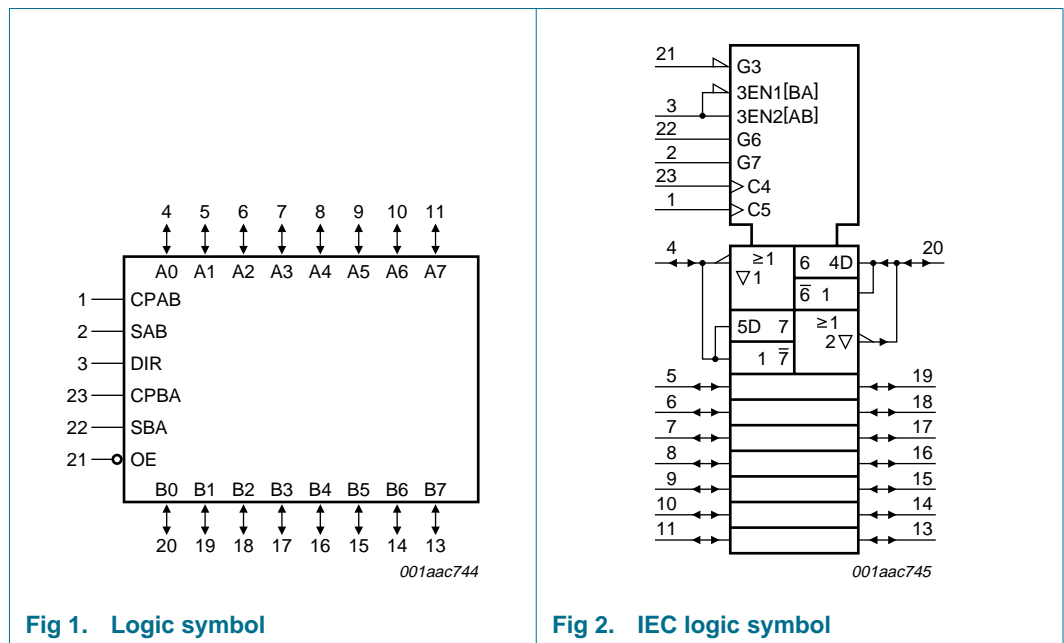
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PLH}$	propagation delay An to Bn or Bn to An	$C_L = 50\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	3.3	-	ns
$t_{PHL}$	propagation delay An to Bn or Bn to An	$C_L = 50\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	3.4	-	ns
$C_i$	input capacitance on pins CP, S, OE, DIR	$V_i = 0\text{ V}$ or $V_{CC}$	-	4	-	pF
$C_{i/O}$	I/O capacitance	outputs disabled; $V_O = 0\text{ V}$ or $V_{CC}$	-	7	-	pF
$I_{CC}$	quiescent supply current	outputs 3-state; $V_{CC} = 5.5\text{ V}$	-	110	-	$\mu\text{A}$

### 4. Ordering information

**Table 2: Ordering information**

Type number	Package			Version
	Temperature range	Name	Description	
74ABT648D	-40 °C to +85 °C	SO24	plastic small outline package; 24 leads; bodywidth 7.5 mm	SOT137-1
74ABT648PW	-40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

### 5. Functional diagram



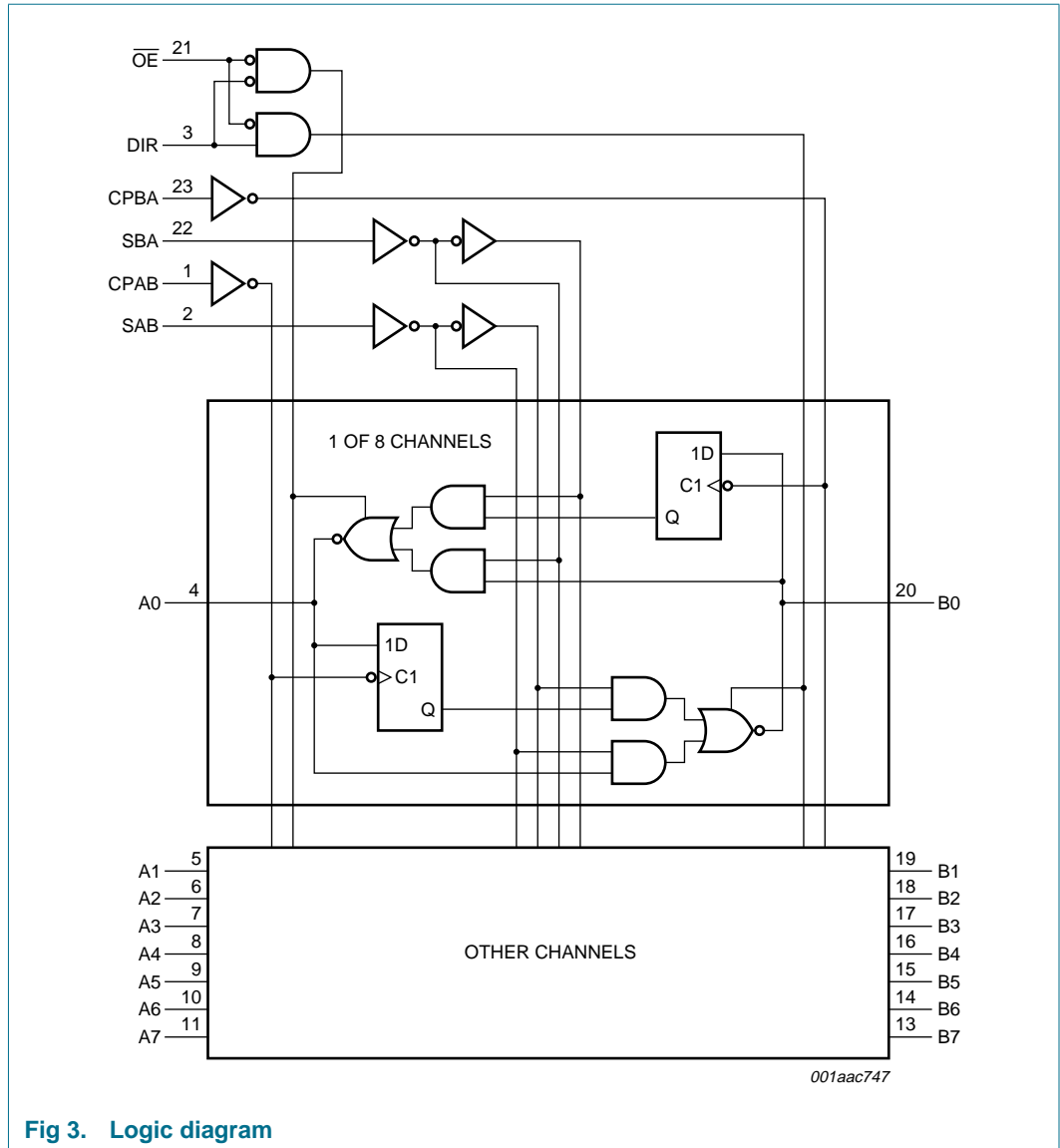
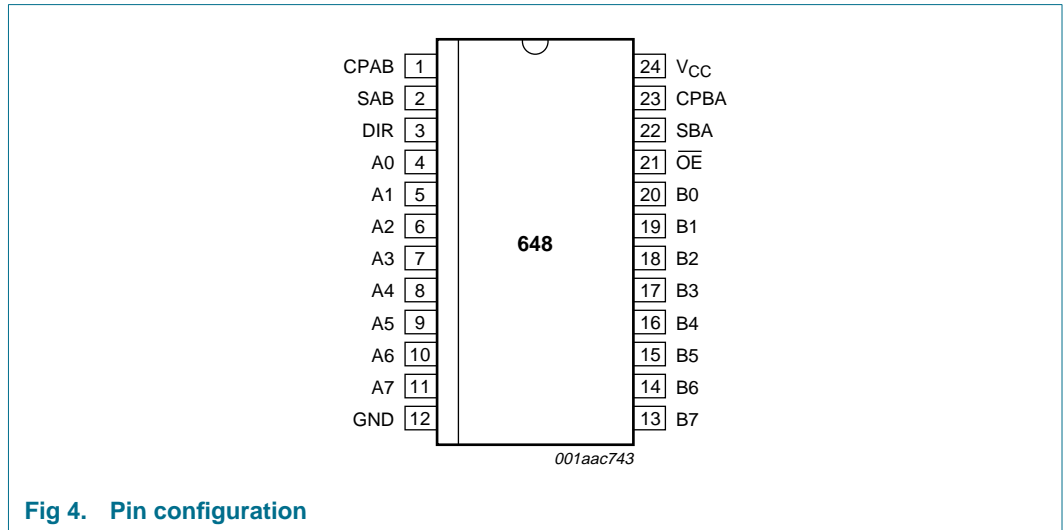


Fig 3. Logic diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
CPAB	1	A to B clock input
SAB	2	A to B select input
DIR	3	direction control input
A0	4	data input/output 0 (A side)
A1	5	data input/output 1 (A side)
A2	6	data input/output 2 (A side)
A3	7	data input/output 3 (A side)
A4	8	data input/output 4 (A side)
A5	9	data input/output 5 (A side)
A6	10	data input/output 6 (A side)
A7	11	data input/output 7 (A side)
GND	12	ground (0 V)
B7	13	data input/output 7 (B side)
B6	14	data input/output 6 (B side)
B5	15	data input/output 5 (B side)
B4	16	data input/output 4 (B side)
B3	17	data input/output 3 (B side)
B2	18	data input/output 2 (B side)
B1	19	data input/output 1 (B side)
B0	20	data input/output 0 (B side)
$\overline{\text{OE}}$	21	output enable input (active LOW)

Table 3: Pin description ...continued

Symbol	Pin	Description
SBA	22	B to A select input
CPBA	23	B to A clock input
V <sub>CC</sub>	24	supply voltage

## 7. Functional description

### 7.1 Function table

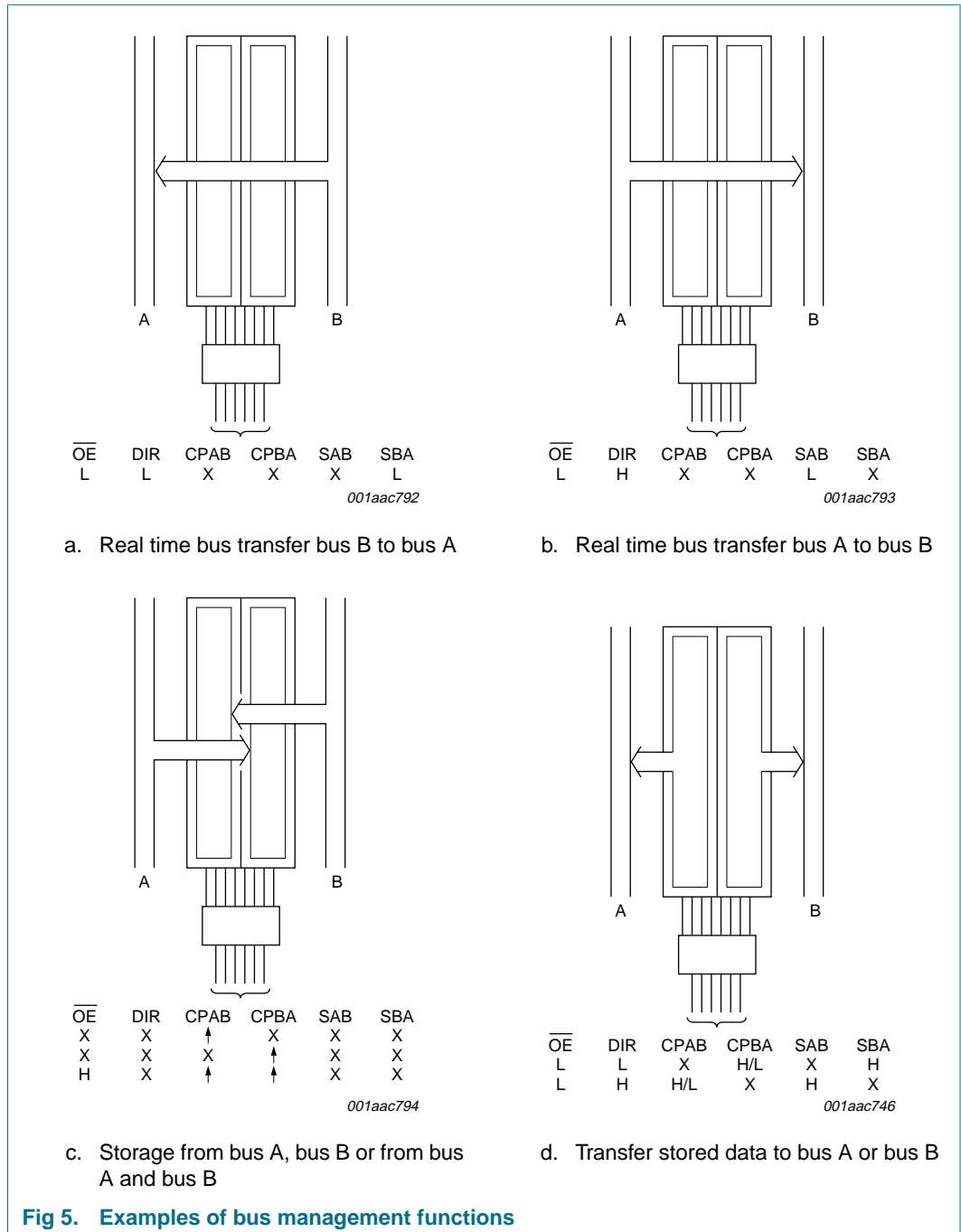
Table 4: Function table [1]

Operating mode	Input						Data I/O	
	OE	DIR	CPAB	CPBA	SAB	SBA	An	Bn
<b>Store A or B</b>								
Store A, B unspecified	X	X	↑	X	X	X	input	unspecified output [2]
Store B, A unspecified	X	X	X	↑	X	X	unspecified output [2]	input
<b>Store A and B</b>								
Store A and B data	H	X	↑	↑	X	X	input	input
Isolation, hold storage	H	X	H or L	H or L	X	X		
<b>B data to A bus</b>								
Real time B data to A bus	L	L	X	X	X	L	output	input
Stored B data to A bus	L	L	X	H or L	X	H		
<b>A data to B bus</b>								
Real time A data to B bus	L	H	X	X	L	X	input	output
Stored A data to B bus	L	H	H or L	X	H	X		

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 ↑ = LOW-to-HIGH clock transition.

- [2] The data output function may be enabled or disabled by various signals at the OE input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.

7.2 Bus management function



## 8. Limiting values

**Table 5: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		[1] -1.2	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+5.5	V
$I_{IK}$	input diode current	$V_I < 0$ V	-	-18	mA
$I_{OK}$	output diode current	$V_O < 0$ V	-	-50	mA
$I_O$	output current	output in LOW-state	-	128	mA
$T_j$	junction temperature		[2]	150	°C
$T_{stg}$	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

## 9. Recommended operating conditions

**Table 6: Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$I_{OH}$	HIGH-level output current		-	-	-32	mA
$I_{OL}$	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate		0	-	10	ns/V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C

## 10. Static characteristics

**Table 7: Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = 25 °C</b>						
V <sub>IK</sub>	input diode voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-	-0.9	-1.2	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>				
		I <sub>O</sub> = -3 mA	2.5	3.2	-	V
		I <sub>O</sub> = -32 mA	2.0	2.3	-	V
		V <sub>CC</sub> = 5.0 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>				
	I <sub>O</sub> = -3 mA	3.0	3.7	-	V	
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>				
		I <sub>O</sub> = 64 mA	-	0.42	0.55	V
V <sub>RST</sub>	power-up output low voltage	V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 1 mA; V <sub>I</sub> = GND or V <sub>CC</sub>	[1]	-	0.13	0.55 V
I <sub>LI</sub>	input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V				
	control pins		-	±0.01	±1.0	µA
	data pins		-	±5	±100	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5 V	-	±5.0	±100	µA
I <sub>PU</sub> , I <sub>PD</sub>	power-up or power-down 3-state output current	V <sub>CC</sub> = 2.1 V; V <sub>O</sub> = 0.5 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>OE</sub> = don't care	[2]	-	±5.0	±50 µA
I <sub>OZ</sub>	3-state output current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>				
		output HIGH-state at V <sub>O</sub> = 2.7 V	-	5.0	50	µA
		output LOW-state at V <sub>O</sub> = 0.5 V	-	-5.0	-50	µA
I <sub>CEx</sub>	output HIGH-state leakage current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	5.0	50	µA
I <sub>O</sub>	output current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 2.5 V	[3]	-50	-65	-180 mA
I <sub>CC</sub>	quiescent supply current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>				
		outputs HIGH-state	-	110	250	µA
		outputs LOW-state	-	20	30	mA
		outputs 3-state	-	110	250	µA
ΔI <sub>CC</sub>	additional supply current per data input pin	one data input at 3.4 V and other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	[4]	0.3	1.5	mA
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>	-	4	-	pF
C <sub>I/O</sub>	I/O capacitance	outputs disabled; V <sub>O</sub> = 0 V or V <sub>CC</sub>	-	7	-	pF



**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IK</sub>	input diode voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-	-	-1.2	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>				
		I <sub>O</sub> = -3 mA	2.5	-	-	V
		I <sub>O</sub> = -32 mA	2.0	-	-	V
		V <sub>CC</sub> = 5.0 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>				
		I <sub>O</sub> = -3 mA	3.0	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>				
		I <sub>O</sub> = 64 mA	-	-	0.55	V
V <sub>RST</sub>	power-up output low voltage	V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 1 mA; V <sub>I</sub> = GND or V <sub>CC</sub>	[1]	-	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	-	-	±1.0	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0.0 V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5 V	-	-	±100	μA
I <sub>PU</sub> , I <sub>PD</sub>	power-up or power-down down 3-state output current	V <sub>CC</sub> = 2.1 V; V <sub>O</sub> = 0.5 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>OE</sub> = don't care	[2]	-	±50	μA
I <sub>OZ</sub>	3-state output current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>				
		output HIGH-state at V <sub>O</sub> = 2.7 V	-	-	50	μA
		output LOW-state at V <sub>O</sub> = 0.5 V	-	-	-50	μA
I <sub>CEX</sub>	output HIGH-state leakage current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	-	50	μA
I <sub>O</sub>	output current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 2.5 V	[3]	-50	-	-180 mA
I <sub>CC</sub>	quiescent supply current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>				
		outputs HIGH-state	-	-	250	μA
		outputs LOW-state	-	-	30	mA
		outputs 3-state	-	-	250	μA
ΔI <sub>CC</sub>	additional supply current per data input pin	one data input at 3.4 V and other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	[4]		1.5	mA

[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any V<sub>CC</sub> between 0 V and 2.1 V, with a transition time of up to 10 ms. From V<sub>CC</sub> = 2.1 V to V<sub>CC</sub> = 5 V ± 10 % a transition time of up to 100 μs is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

## 11. Dynamic characteristics

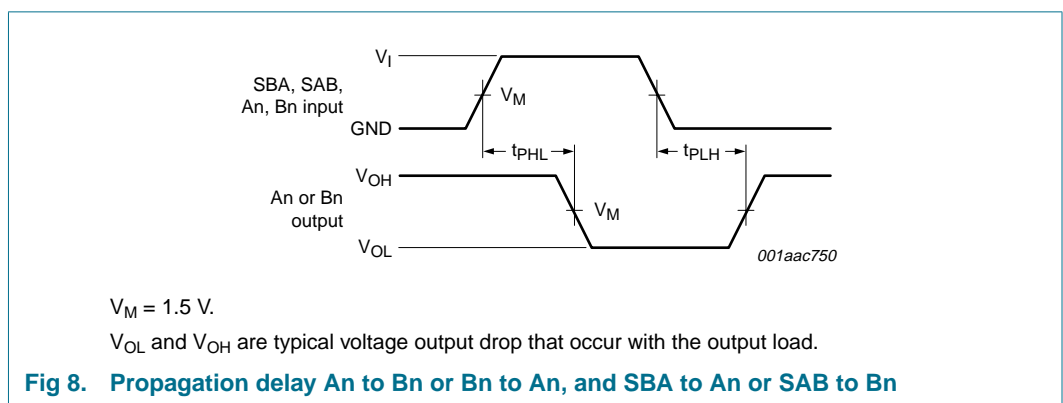
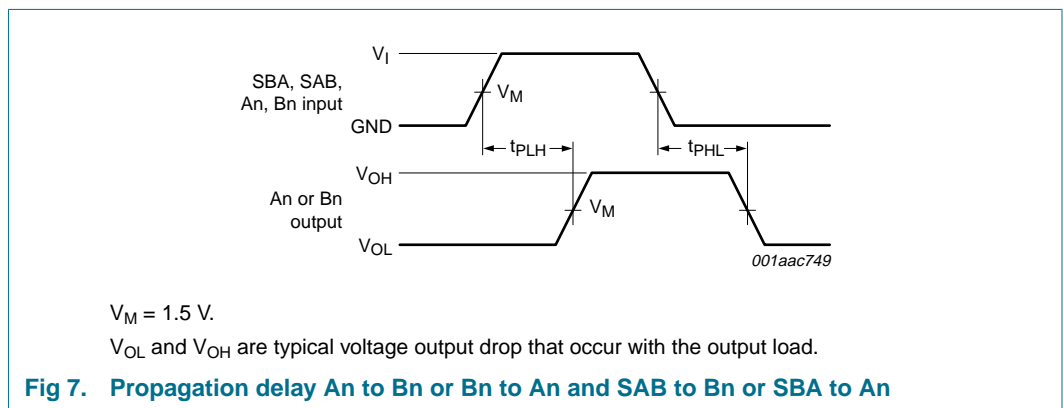
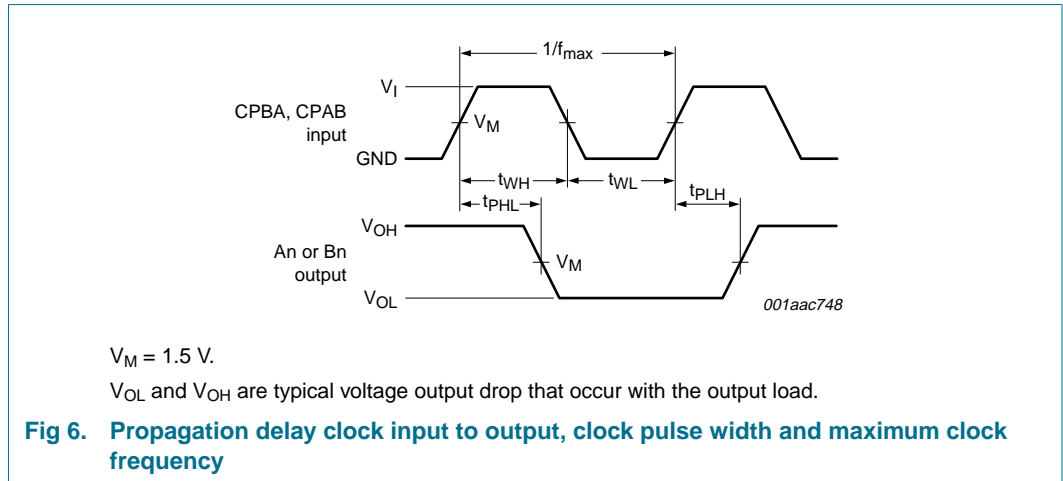
**Table 8: Dynamic characteristics**  
*GND = 0 V; for test circuit see [Figure 12](#)*

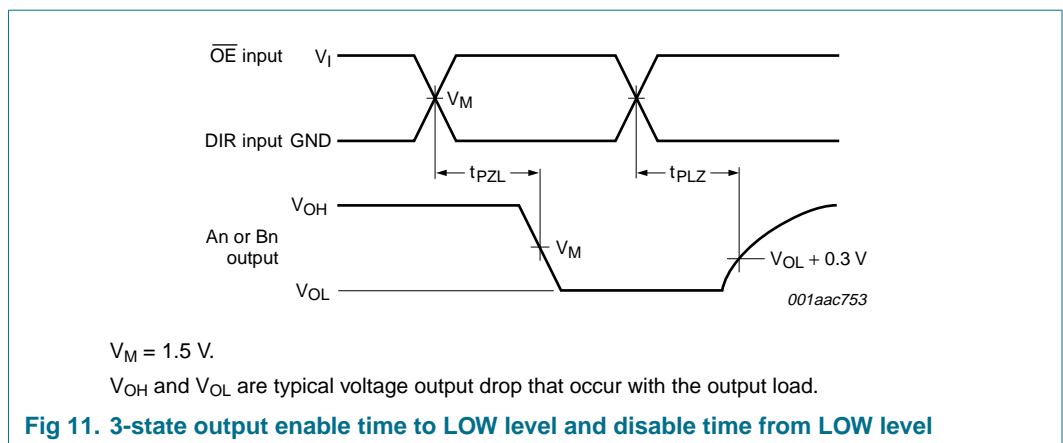
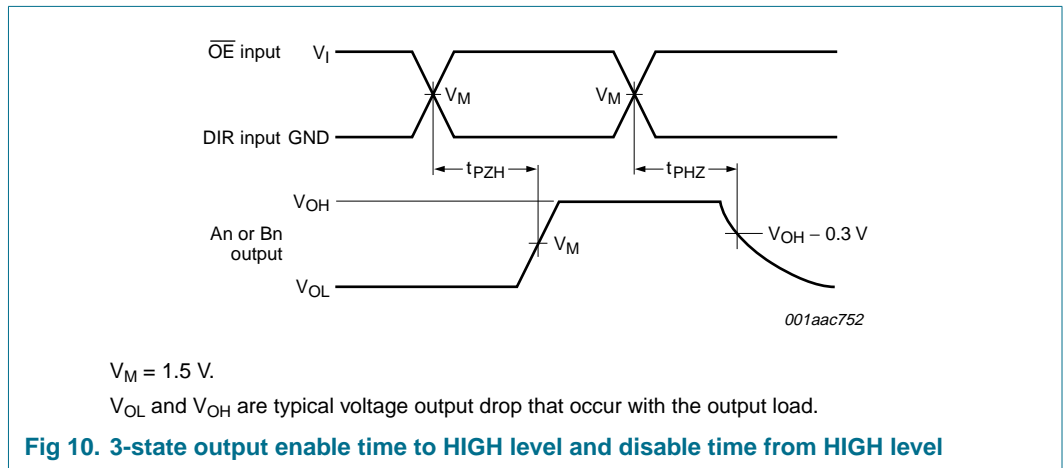
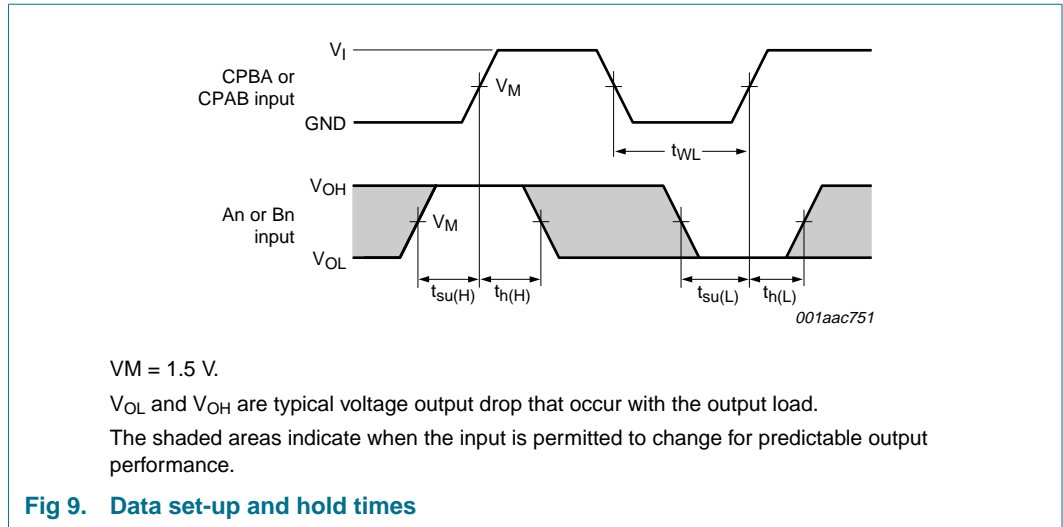
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = 25 °C; V<sub>CC</sub> = 5.0 V</b>						
t <sub>PLH</sub>	propagation delay					
	CPAB to Bn or CPBA to An	see <a href="#">Figure 6</a>	1.8	3.2	4.6	ns
	An to Bn, Bn to An	see <a href="#">Figure 7</a> and <a href="#">8</a>	1.9	3.3	4.2	ns
	SAB to Bn or SBA to An	see <a href="#">Figure 7</a> and <a href="#">8</a>	1.8	3.9	4.5	ns
t <sub>PHL</sub>	propagation delay					
	CPAB to Bn or CPBA to An	see <a href="#">Figure 6</a>	2.6	4.0	5.7	ns
	An to Bn, Bn to An	see <a href="#">Figure 7</a> and <a href="#">8</a>	2.2	3.4	5.0	ns
	SAB to Bn or SBA to An	see <a href="#">Figure 7</a> and <a href="#">8</a>	2.5	4.1	5.6	ns
t <sub>PZH</sub>	output enable time to HIGH level					ns
	OE to An or Bn	see <a href="#">Figure 10</a>	2.2	3.5	4.4	ns
	DIR to An or Bn	see <a href="#">Figure 10</a>	2.1	3.3	4.4	ns
t <sub>PHZ</sub>	output disable time from HIGH level					
	OE to An or Bn	see <a href="#">Figure 10</a>	2.3	3.6	4.6	ns
	DIR to An or Bn	see <a href="#">Figure 10</a>	1.9	3.5	4.8	ns
t <sub>PZL</sub>	output disable time to LOW level					
	OE to An or Bn	see <a href="#">Figure 11</a>	3.2	4.5	6.0	ns
	DIR to An or Bn	see <a href="#">Figure 11</a>	3.1	4.4	5.6	ns
t <sub>PLZ</sub>	output disable time from LOW level					
	OE to An or Bn	see <a href="#">Figure 11</a>	2.1	3.0	4.4	ns
	DIR to An or Bn	see <a href="#">Figure 11</a>	1.9	3.4	4.7	ns
t <sub>su(H)</sub>	set-up time HIGH An to CPAB, Bn to CPBA	see <a href="#">Figure 9</a>	3.0	1.5	-	ns
t <sub>su(L)</sub>	set-up time LOW An to CPAB, Bn to CPBA	see <a href="#">Figure 9</a>	3.0	1.0	-	ns
t <sub>h(H)</sub>	hold time HIGH An to CPAB, Bn to CPBA	see <a href="#">Figure 9</a>	0.0	-0.4	-	ns
t <sub>h(L)</sub>	hold time LOW An to CPAB, Bn to CPBA	see <a href="#">Figure 9</a>	0.0	-1.0	-	ns
t <sub>WH</sub>	pulse width HIGH CPAB or CPBA	see <a href="#">Figure 6</a>	3.5	2.6	-	ns
t <sub>WL</sub>	pulse width LOW CPAB or CPBA	see <a href="#">Figure 6</a>	4.0	1.0	-	ns
f <sub>max</sub>	maximum clock frequency	see <a href="#">Figure 6</a>	125	200	-	MHz

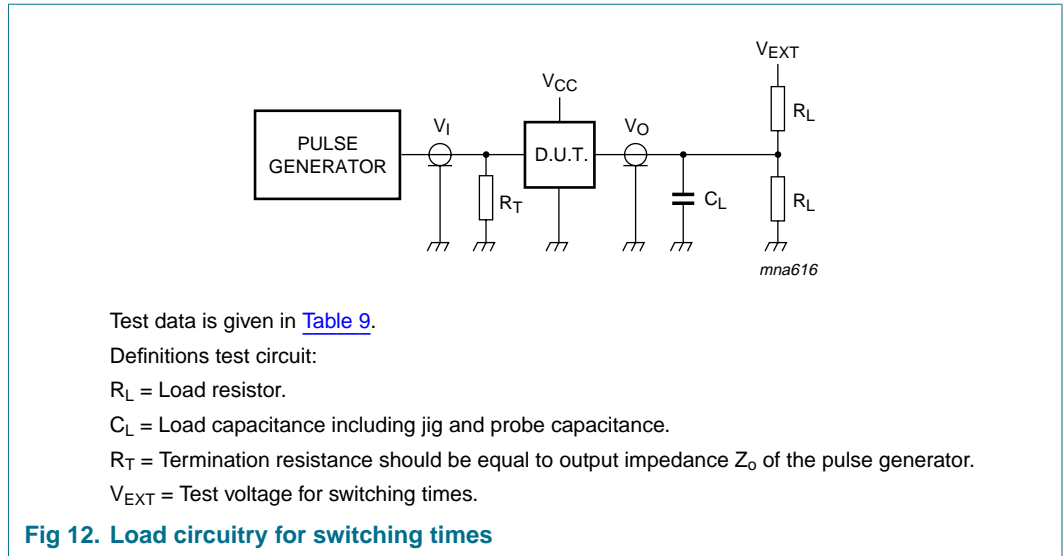
**Table 8: Dynamic characteristics ...continued**  
*GND = 0 V; for test circuit see [Figure 12](#)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C; V<sub>CC</sub> = 5 V ± 0.5 V</b>						
t <sub>PLH</sub>	propagation delay					
	CPAB to Bn or CPBA to An	see <a href="#">Figure 6</a>	1.7	-	5.1	ns
	An to Bn, Bn to An	see <a href="#">Figure 7</a> and <a href="#">8</a>	1.8	-	4.8	ns
	SAB to Bn or SBA to An	see <a href="#">Figure 7</a> and <a href="#">8</a>	1.8	-	5.1	ns
t <sub>PHL</sub>	propagation delay					
	CPAB to Bn or CPBA to An	see <a href="#">Figure 6</a>	2.7	-	6.1	ns
	An to Bn, Bn to An	see <a href="#">Figure 7</a> and <a href="#">8</a>	2.3	-	5.2	ns
	SAB to Bn or SBA to An	see <a href="#">Figure 7</a> and <a href="#">8</a>	2.7	-	6.1	ns
t <sub>PZH</sub>	output enable time					ns
	OE to An or Bn	see <a href="#">Figure 10</a>	2.0	-	5.0	ns
	DIR to An or Bn	see <a href="#">Figure 10</a>	1.6	-	5.0	ns
t <sub>PHZ</sub>	output disable time					
	OE to An or Bn	see <a href="#">Figure 10</a>	2.1	-	5.2	ns
	DIR to An or Bn	see <a href="#">Figure 10</a>	1.8	-	5.6	ns
t <sub>PZL</sub>	output disable time					
	OE to An or Bn	see <a href="#">Figure 11</a>	2.4	-	6.6	ns
	DIR to An or Bn	see <a href="#">Figure 11</a>	2.7	-	6.3	ns
t <sub>PLZ</sub>	output disable time					
	OE to An or Bn	see <a href="#">Figure 11</a>	2.1	-	5.1	ns
	DIR to An or Bn	see <a href="#">Figure 11</a>	2.0	-	5.1	ns
t <sub>su(H)</sub>	set-up time HIGH An to CPAB, Bn to CPBA	see <a href="#">Figure 9</a>	3.0	-	-	ns
t <sub>su(L)</sub>	set-up time LOW An to CPAB, Bn to CPBA	see <a href="#">Figure 9</a>	3.0	-	-	ns
t <sub>h(H)</sub>	hold time HIGH An to CPAB, Bn to CPBA	see <a href="#">Figure 9</a>	0.0	-	-	ns
t <sub>h(L)</sub>	hold time LOW An to CPAB, Bn to CPBA	see <a href="#">Figure 9</a>	0.0	-	-	ns
t <sub>W(H)</sub>	pulse width HIGH CPAB or CPBA	see <a href="#">Figure 6</a>	3.5	-	-	ns
t <sub>W(L)</sub>	pulse width LOW CPAB or CPBA	see <a href="#">Figure 6</a>	4.0	-	-	ns
f <sub>max</sub>	maximum clock frequency	see <a href="#">Figure 6</a>	125	-	-	MHz

12. Waveforms







**Table 9: Test data**

Input	Load		$V_{EXT}$		
$V_I$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
3.0 V	50 pF	500 $\Omega$	open	7.0 V	open

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

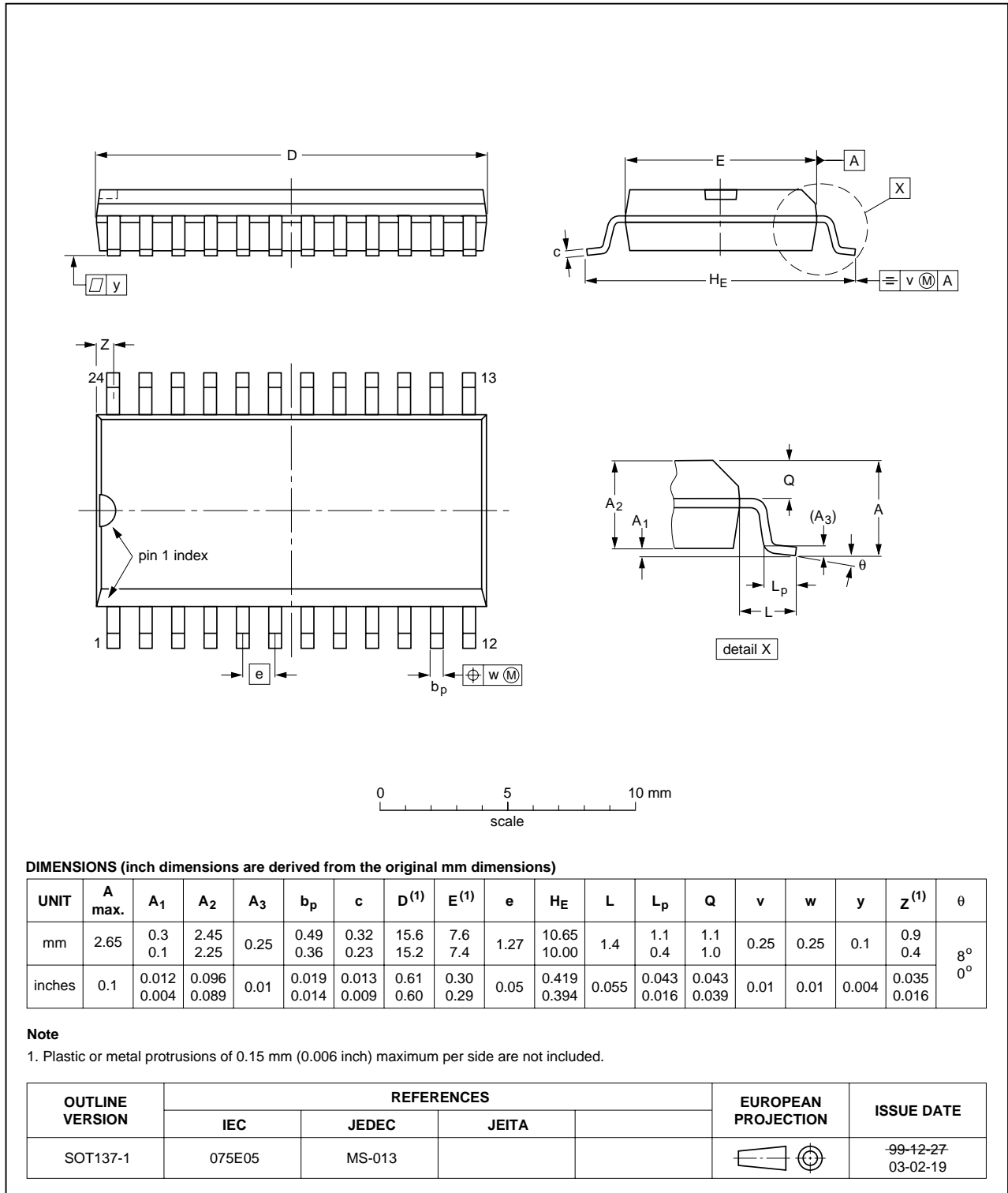


Fig 13. Package outline SOT137-1 (SO24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

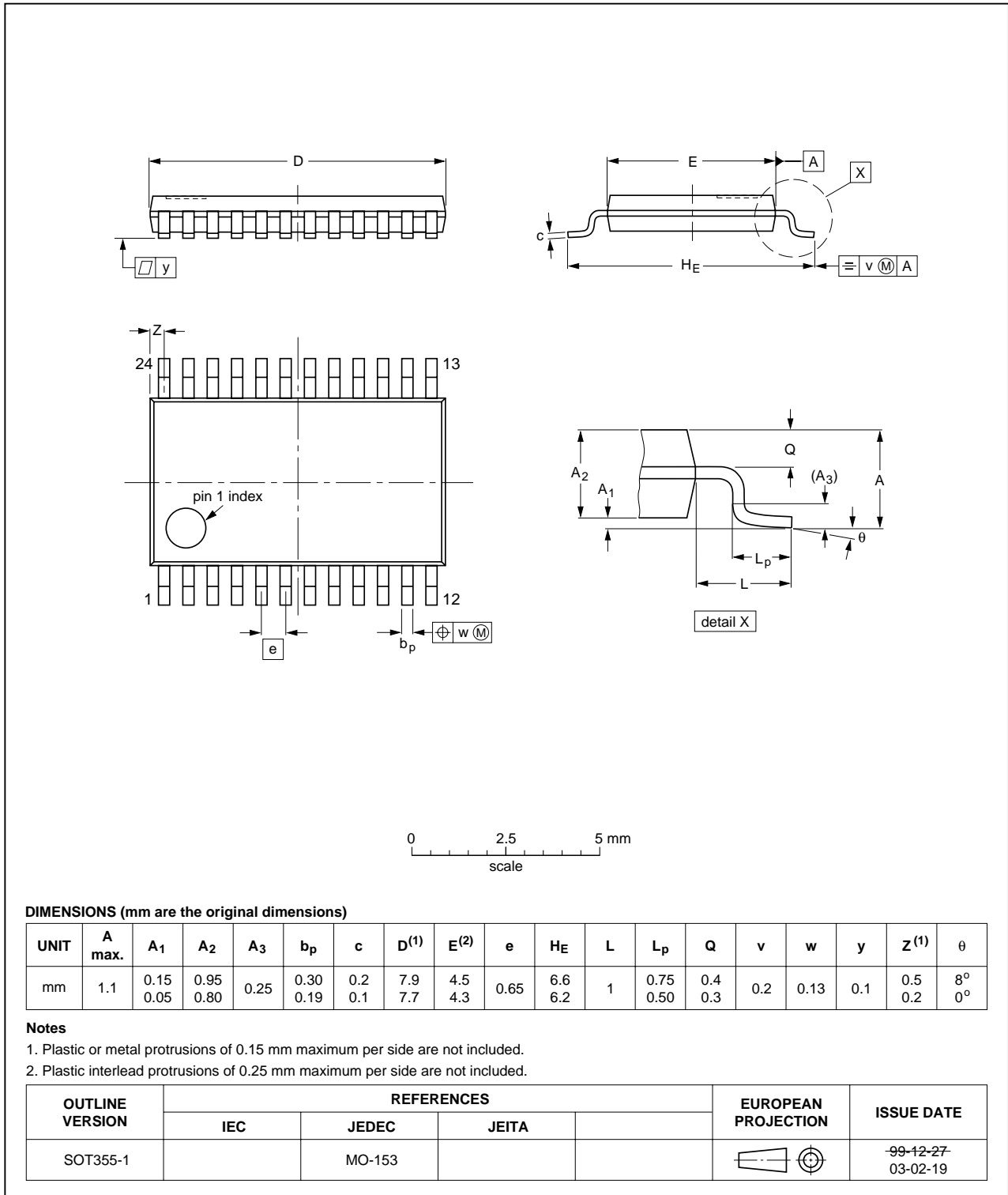


Fig 14. Package outline SOT355-1 (TSSOP24)



## 14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74ABT648_4	20050427	Product data sheet	-	9397 750 14858	74ABT648_3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li> <li><a href="#">Section 2</a>: modified 'JEDEC Std 17' into 'JESD78'.</li> <li><a href="#">Table 1</a>: changed <math>t_{PLH}</math> from 5.9 ns to 3.3 ns and <math>t_{PHL}</math> from 5.9 ns to 3.4 ns.</li> <li><a href="#">Table 8</a>: all values changed.</li> </ul>				
74ABT648_3	20021213	Product specification	-	9397 750 10848	74ABT648_2
74ABT648_2	19980608	Product specification	-	9397 750 04022	74ABT648_1
74ABT648_1	19950417	Product specification	-	-	-

## 15. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## 19. Contact information

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