APPLICATION NOTE

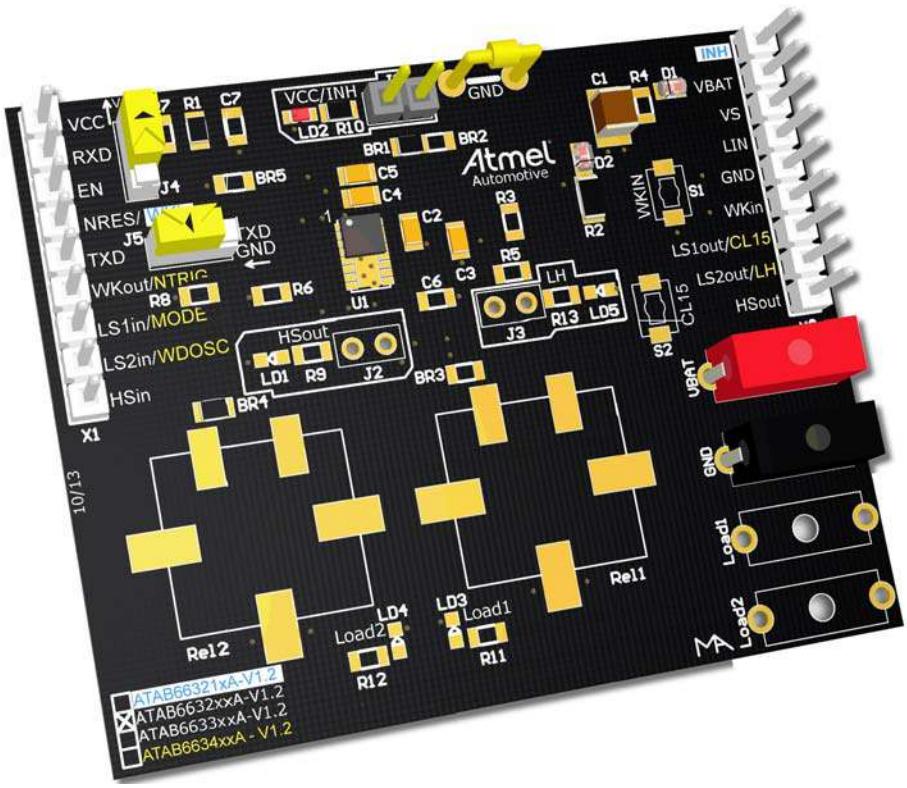
Development Board for the ATA663201, ATA663203, ATA663231, ATA663232, ATA663254, ATA663255, ATA663331, ATA663354, ATA663431 and ATA663454

ATAN0087

Introduction

The development board for the 4th generation LIN device family - Atmel® ATA6632xx, ATA6633x and ATA6634xx ICs enables users to rapidly prototype and test new LIN designs.

Figure 1. Atmel ATAB6632xxA, ATAB6633xxA, ATAB6634xxA Development Board



The Atmel ATA6632xx device family includes six basic products: four LIN system basis chips (SBC) and two low drop voltage regulators with compatible footprints. The Atmel ATA663231/54 (system basis chip) is a fully integrated LIN transceiver, designed in compliance with the LIN specifications 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2 together with a low-drop voltage regulator (3.3V/5V/85mA).

The Atmel® ATA663232/55 system basis chip is based on the ATA663231/54, the only difference is the pin 3 - instead of the VCC undervoltage output NRES it has a high voltage input WKin for local wake-up request.

The Atmel ATA663201/03 (voltage regulator) is a fully integrated low-drop voltage regulator, with 3.3V respectively 5V output voltage and 85mA current capability. It is especially designed for the automotive environment.

The Atmel ATA663331 and the ATA663354 are system basis chips with a fully integrated LIN transceiver designed in compliance with LIN specifications 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2, a low-drop voltage regulator (3.3V/5V/85mA), two low-side drivers, designed for controlling two relays, one high-side switch and one high-voltage wake input.

The Atmel ATA663431 and the ATA663454 are system basis chips with a fully integrated LIN transceiver designed in compliance with LIN specifications 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2, a low-drop voltage regulator (3.3V/5V/85mA), a window watchdog, a high-side switch and two high-voltage wake inputs.

A key feature is that the current consumption is always below 190µA (without load), even if the supply voltage is below the regulator's nominal output voltage. Sleep and silent mode guarantee minimized current consumption even in the event of a floating or short-circuited LIN bus.

Every device of the IC family is available in the space saving DFN8 (Atmel ATA6632xx) or DFN16 package (Atmel ATA6633xx and ATA6634xx) as shown in Figure 2 and Figure 3 below, in Figure 4 and Figure 5 on page 3.

Figure 2. Atmel ATA663203/31/32/54/55 DFN8 Pinning

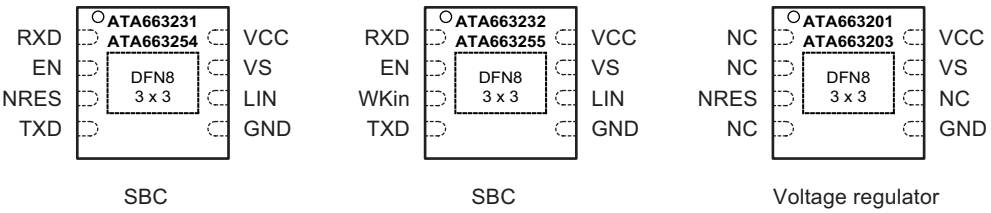


Figure 3. Atmel ATA663331/54 DFN16 Pinning

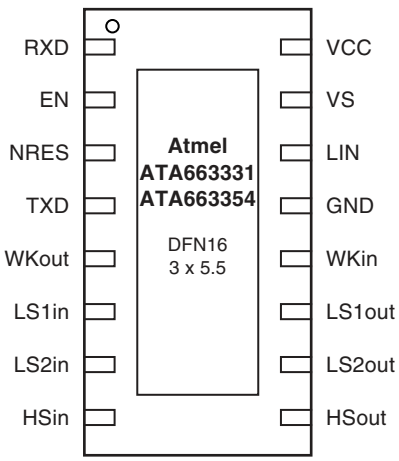
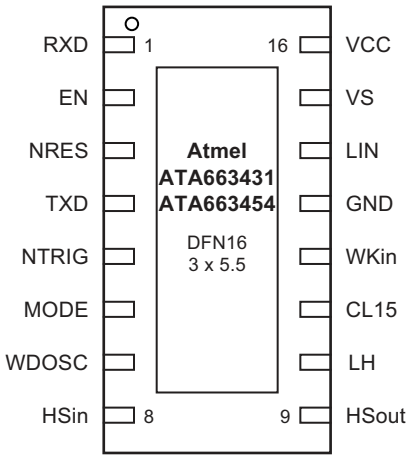
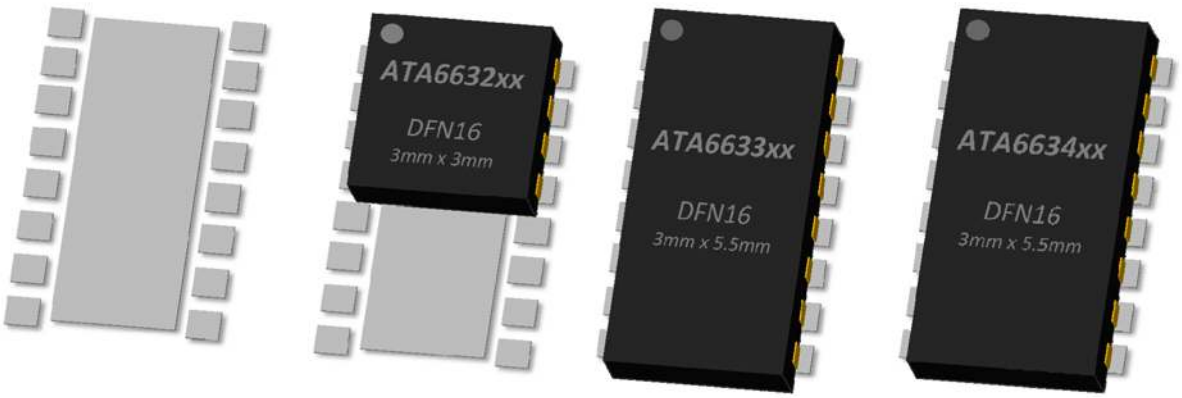


Figure 4. Atmel ATA663431/54 DFN16 Pinning



Every device of the IC family is designed in that way that one single PCB and one footprint can be used for all devices of the entire IC family. Having one PCB for different applications saves money (PCB, qualification, etc.) while also giving the user far more flexibility to cover many different applications with a single assembly option.

Figure 5. One Footprint for the Entire Device Family



The devices have the following features:

- LIN physical layer according to LIN 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2
- Low electromagnetic emission (EME) and high electromagnetic immunity (EMI)
- Up to 40V supply voltage
- Operating voltage V_S = 5V to 28V
- Typically 10µA supply current during sleep mode
- Typically 47µA supply current in silent mode
- Very low current consumption at low supply voltages (2V < V_S < 5.5V): ≤ 190µA

- Linear low-drop voltage regulator, 85mA current capability:
  - Normal, fail-safe, and silent mode
    - Atmel ATA663231, ATA663232, ATA663331, ATA663431: VCC = 3.3V
    - Atmel ATA663254, ATA663255, ATA663354, ATA663454: VCC = 5.0V
  - Sleep mode: VCC is switched off
  - Active mode
    - Atmel ATA663201: VCC = 3.3V ±2%
    - Atmel ATA663203: VCC = 5.0V ±2%
  - Works down to V_S = 2.3V
- VCC undervoltage detection with open drain reset output (NRES, 4ms reset time)
- Voltage regulator is short-circuit and over-temperature protected
- Wake-up capability
  - Via LIN bus (100µs dominant)
  - Via WKin pin (ATA6632xx, ATA6633xx, ATA6634xx only)
  - Via CL15 pin (ATA6634xx only)
- Wake-up source recognition
- TXD time-out timer
- Bus pin is over-temperature and short-circuit protected vs. GND and battery
- Advanced EMC and ESD performance
- Fulfills the OEM “Hardware Requirements for LIN in Automotive Applications Rev.1.3”
- Interference and damage protection according to ISO7637
- Protected high-side switch (ATA6633xx and ATA6634xx only)
- Adjustable watchdog time via external resistor (ATA6634xx only)
- Negative trigger input for watchdog (ATA6634xx only)
- Limp home watchdog failure output (ATA6634xx only

1. Development Kit Features

The development board supports the following features:

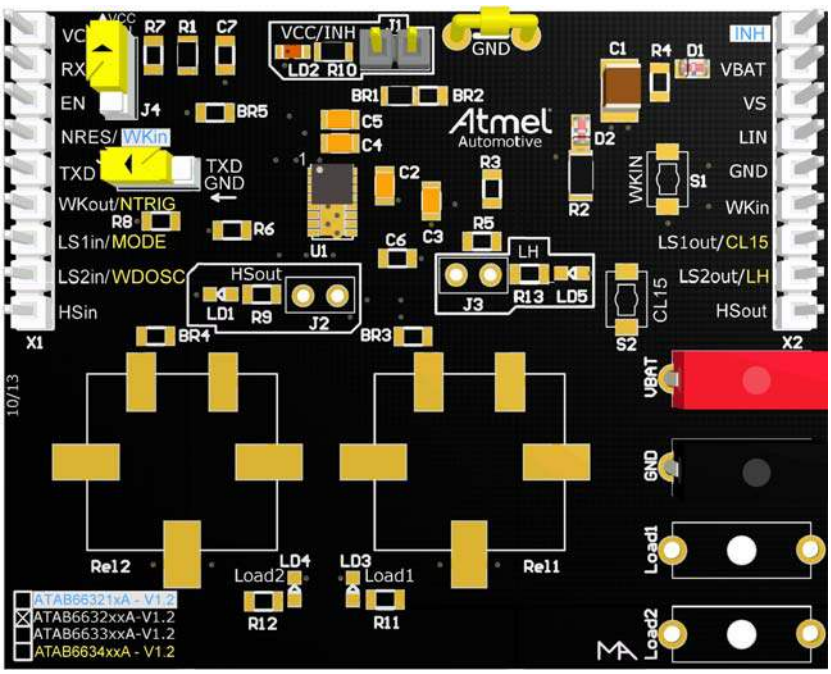
- All components necessary to support the ATA663201/03, the ATA663231/54, the ATA663232/55, the ATA663331/54 and the ATA663431/54
- All pins easily accessible
- Choice of master or slave operation (D2 and R2 mounted per default for master operation)
- Switching into normal, silent or sleep mode via two jumpers
- LEDs for operation indication
- Ground coulter clip for easy probe connection while measuring with oscilloscope
- Easily adaptable watchdog times by replacing a single resistor
- Push buttons included for creating a local wake-up from sleep or silent mode
- Relays for application specific tests of the ATA663331/54

2. Quick Start

The development board for the complete device family is shipped with all components necessary to quickly begin the development of a LIN node. Depending on which device is soldered on the development board, different components are assembled.

Connecting an external 12V DC power supply between the terminals VBAT and GND puts the IC into fail-safe mode (SBC only) (VCC = ON, communication = OFF) or into active mode (voltage regulator only). The IC can then be put into one of the three operating modes (SBC only): normal, silent, and sleep which can be selected via the TXD and EN pins (for more information, see Figure 2-2 and Table 2-1 on page 6).

Figure 2-1. ATAB6632xxA/ATAB6633xxA/ATAB6634xxA Development Board



Using the J4 and J5 jumper allows the relevant device mounted on the board to be easily put into normal, silent, or sleep mode (SBC only).

When the SBC is in sleep or silent mode, it can easily be woken up via the two push buttons (S1 at the WKin pin and S2 at the CL15 pin) (local wake-up) or a falling edge at the LIN pin (remote wake- up) followed by a dominant bus level maintained for a certain time period (> t_{bus}) together with a subsequent rising edge at the LIN pin.

2.1 Operating Modes

Figure 2-2. SBC Operating Modes

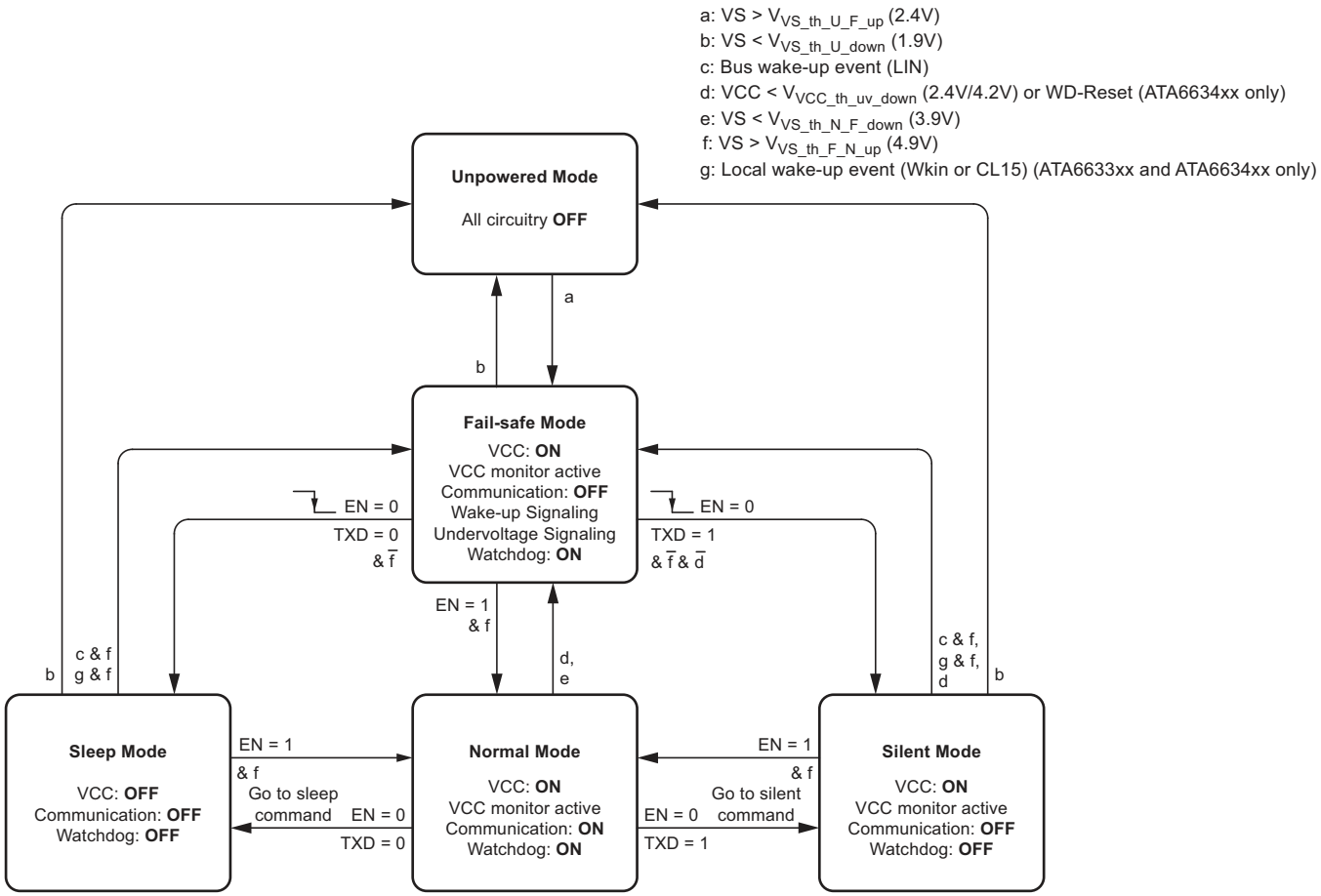
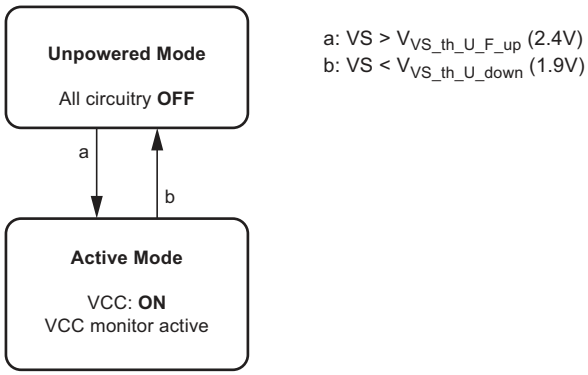


Table 2-1. SBC Operating Modes

Operating Mode	Transceiver	Voltage Regulator	High-side Output ATA6633xx and ATA6634xx only	Low-side Output ATA6633xx only	Watchdog with LH ATA6634xx only	LIN	TRX	RXD
Fail-safe	OFF	3.3V/5V	HSin-dependent	OFF	ON	Recessive	Signaling fail-safe sources	
Normal	ON	3.3V/5V	HSin-dependent	LSinx-dependent	ON	TXD-dependent	Follows data transmission	
Silent	OFF	3.3V/5V	HSin-dependent	OFF	OFF	Recessive	High	High
Sleep	OFF	0V	OFF	OFF	OFF	Recessive	Low	Low

Figure 2-3. Voltage Regulator Operating Modes



2.2 Normal Mode (SBC only)

This is the normal transmitting and receiving mode of the LIN interface, in accordance with LIN specification 2.x.

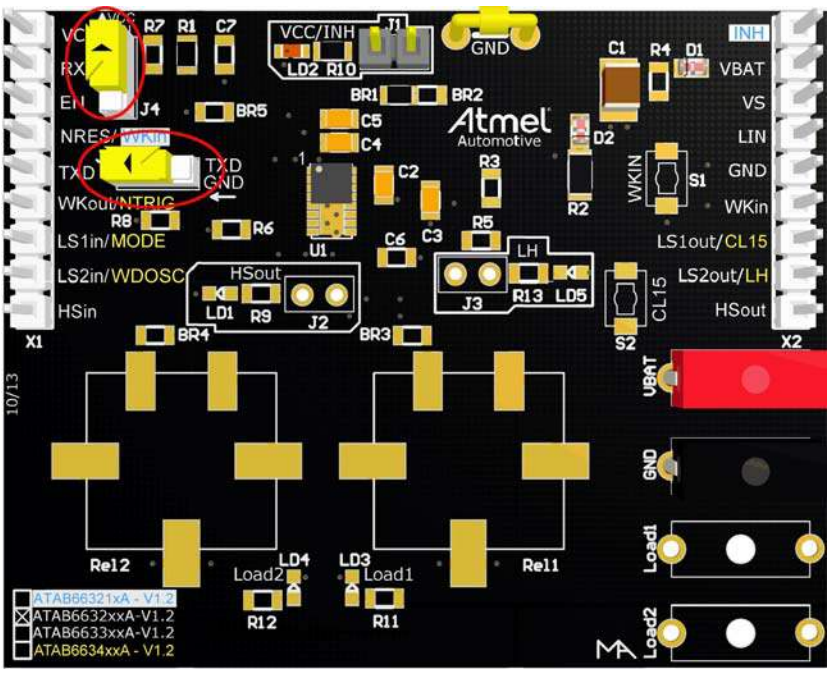
The VCC voltage regulator operates at 3.3V respectively 5V output voltage with a low tolerance of ±2% and a maximum output current of 85mA.

At the ATA663431/54 the watchdog requires a trigger signal at the NTRIG pin to avoid resets at the NRES pin. If NRES switches to low, the IC changes its state to fail-safe mode. If an undervoltage condition occurs, NRES switches to low and the IC changes its state to fail-safe mode.

In addition, the low-side drivers of the ATA663331/54 can only be activated in normal mode.

After power-on, the device is in fail-safe mode; to switch the device to normal mode set the J4 and J5 jumper as shown in Figure 2-4. If the jumper was already in this position, the device immediately switches into normal mode.

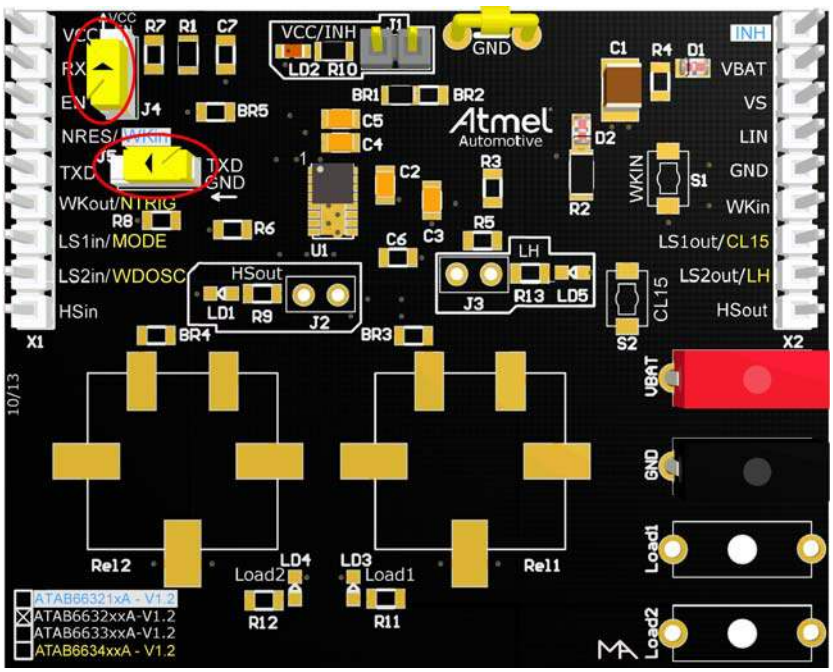
Figure 2-4. J4 and J5 Setting for Normal Mode (J4-up and J5-don't Care)



2.3 Silent Mode (SBC only)

A falling edge at EN while TXD is high switches the SBC into silent mode. The TXD signal has to be logic high during the mode select window. This is easily done by setting the J5 jumper to the position shown in Figure 2-5 and the J4 jumper to the downward position. If the jumpers were already set, just cycle the J4 jumper at the EN pin once in order to get a falling edge at the EN pin while the TXD pin is high.

Figure 2-5. J4 and J5 Setting for Silent Mode (J4-down and J5-right)



The transmission path is disabled in silent mode. The voltage regulator is active and the overall supply current from VBAT is a combination of the $I_{VSsilent}$ of typically 47µA plus the VCC regulator output current I_{VCC}.

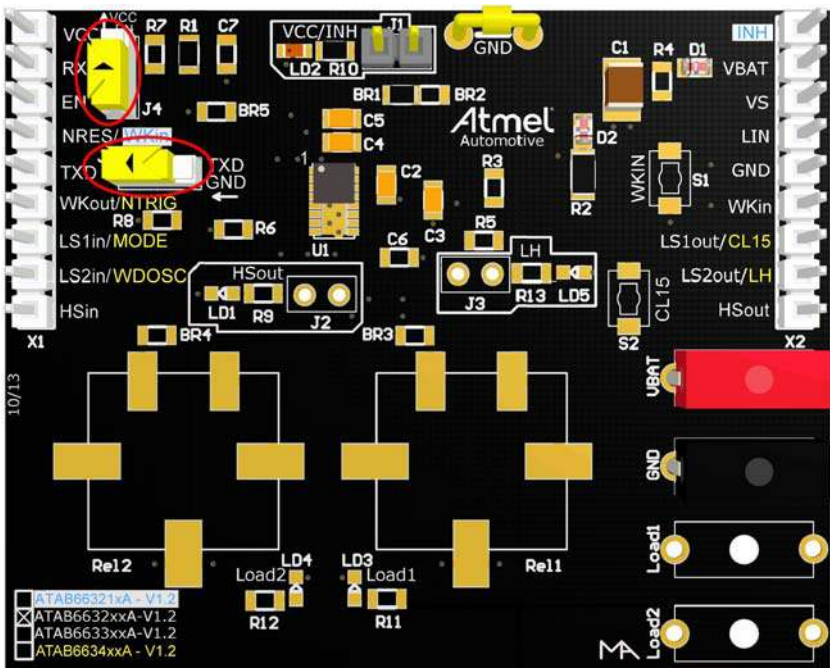
In silent mode, the internal slave termination between the LIN pin and VS pin is disabled to minimize the current consumption in case the LIN pin is short-circuited to GND. Only a weak pull-up current (typically 10µA) is present between the LIN pin and VS pin. The silent mode can be activated independently from the current level on the LIN pin.

If an undervoltage condition occurs, NRES is switched to low and the SBC switches into fail-safe mode.

2.4 Sleep Mode (SBC only)

A falling edge at EN while TXD is low switches the SBC into sleep mode. The TXD signal must be logic low during the mode select window. This is easily done by simultaneously setting the J4 and J5 jumpers to the position shown in Figure 2-6. If the jumpers were already set, simply cycle the J4 jumper once to generate a falling edge at the EN pin while the TXD pin is low.

Figure 2-6. J4 and J5 Setting for Sleep Mode (J4-down and J5-left)



To avoid any influence on the LIN pin while switching to sleep mode, it is possible to switch the EN to low up to 3.2µs earlier than the TXD. The most convenient way to do this is to generate two simultaneous falling edges at TXD and EN. In sleep mode the transmission path is disabled. The supply current from VBAT is typically $I_{VSsleep}$ = 10µA. The VCC regulator is switched off; NRES and RXD are low. The internal slave termination between the LIN pin and VS pin is disabled to minimize the current consumption in case the LIN pin is short-circuited to GND. Only a weak pull-up current (typically 10µA) between the LIN pin and VS pin is present. The sleep mode can be activated independently from the current level on the LIN pin. A voltage below the LIN pre-wake detection VLINL at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer.

If TXD is short-circuited to GND, it is possible to switch to sleep mode via EN after t > t_{dom}.

2.5 Fail-safe Mode (SBC only)

The device automatically switches to fail-safe mode at system power-up. The voltage regulator and the watchdog (ATA6634xx only) are switched on. The NRES output remains low for t_{res} = 4ms and resets the microcontroller. LIN communication is switched off. The IC stays in this mode until EN is switched to high. The IC then changes to normal mode. A low at NRES switches the IC directly into fail-safe mode. During fail-safe mode the TXD pin is an output and together with the RXD output pin signals the fail-safe source.

If due to a VS undervoltage condition (VS < $V_{VS\_th\_N\_F\_down}$) the device enters fail-safe mode coming from normal mode (EN=1), it is possible to switch to sleep or silent mode through a falling edge at the EN input. The current consumption can be reduced further with this feature.

A wake-up event from either silent mode or sleep mode is indicated to the microcontroller using the RXD and TXD pins. A VS undervoltage condition is also signalled at these two pins. The coding is shown in Table 2-2.

A wake-up event switches the IC to fail-safe mode.

Table 2-2. Signaling in Fail-safe Mode

Fail-Safe Sources	TXD	RXD
LIN wake-up (LIN pin)	Low	Low
Local wake-up (WKin pin or CL15 pin) (only ATA663431/54)	Low	High
$V_{VS\_th\_N\_F\_down}$ (battery) undervoltage detection (V_{VS} < 3.9V)	High	Low

2.6 Active Mode (Voltage Regulator only)

The ATA663201/03 automatically switches to active mode at system power-up. The voltage regulator operates with 3.3V respectively 5V output voltage, with a low tolerance of ±2% and a maximum output current of 85mA. The NRES output remains low for t_{res} = 4ms and causes the microcontroller to be reseted. The current consumption is typically 47µA. If an undervoltage condition occurs, NRES switches to low.

3. Hardware Description

3.1 Pin Description

The external elements required for some of the pins are shown and described in the following sections. For more information, see the relevant datasheet.

3.1.1 Supply Pin (VS)

LIN operating voltage is VS = 5V to 28V. Undervoltage detection is implemented to disable transmission if VS falls below typically 4.5V, thereby avoiding false bus messages. After switching VS on, the IC starts in fail-safe mode (ATA663203 in active mode) and the voltage regulator is switched on.

The supply current in sleep mode is typically 10µA and 47µA in silent mode (SBC only).

3.1.2 Ground Pin (GND)

The IC does not affect the LIN bus in the event of GND disconnection. The IC is able to handle a ground shift of up to 11.5% of VS.

3.1.3 Voltage Regulator Output Pin (VCC)

The internal 3.3V/5V voltage regulator is capable of driving loads up to 85mA, supplying the microcontroller and other devices on the PCB and is protected against overload by means of current limitation and overtemperature shutdown. Furthermore, the output voltage is monitored and causes a reset signal at the NRES output pin if it drops below a defined threshold $V_{VCC\_th\_uv\_down}$.

3.1.4 Undervoltage Reset Output (NRES) (not ATA663232/55)

If the VCC voltage falls below the undervoltage detection threshold $VCC_{th\_uv\_down}$, NRES switches to low after t_{res_f}. The NRES stays low even if VCC = 0V because NRES is internally driven from the VS voltage. If VS voltage ramps down, NRES stays low until VS < 1.5V and then becomes highly impedant.

The implemented undervoltage delay keeps NRES low for t_{Reset} = 4ms after VCC reaches its nominal value.

3.1.5 Bus Pin (LIN) (SBC only)

A low-side driver with internal current limitation and thermal shutdown as well as an internal pull-up resistor according to LIN specification 2.x is implemented. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to VS, even in the event of a GND shift or VBAT disconnection. The LIN receiver thresholds comply with the LIN protocol specification.

The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope-controlled.

During a short circuit at LIN to VBAT, the output limits the output current to IBUS_LIM. Due to power dissipation, the chip temperature exceeds T_{LINoff} and the LIN output is switched off. The chip cools down and, after a hysteresis of T_{hys}, switches the output on again. RXD stays on high because LIN is high. The VCC regulator works independently during LIN overtemperature switch-off.

During a short circuit from LIN to GND, the IC can be switched to sleep or silent mode and even in this case the current consumption is lower than 100µA in sleep mode and lower than 120µA in silent mode. If the short circuit disappears, the IC starts with a remote wake-up.

The reverse current is < 2µA at pin LIN during loss of VBAT. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.

3.1.6 Input/Output (TXD) (SBC only)

In normal mode the TXD pin is the microcontroller interface for controlling the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull-up resistor), the LIN output transistor is turned off and the bus is in the recessive state. If the TXD pin stays at GND level while switching to normal mode, it must be pulled to high level longer than 10µs before the LIN driver can be activated. This feature prevents the bus line from being accidentally driven to dominant state after normal mode has been activated (also in case of a short circuit at TXD to GND).

During fail-safe mode, this pin is used as output and signals the fail-safe source together with the RXD pin.

An internal timer prevents the bus line from being driven permanently to the dominant state. If TXD is forced to low longer than tdom > 20ms, the LIN bus driver is switched to the recessive state. Nevertheless, when switching to sleep mode, the actual level at the TXD pin is relevant.

To reactivate the LIN bus driver, switch TXD to high (> 10µs).

The TXD pin provides a pull-up resistor to force the transceiver to recessive mode if TXD is disconnected.

3.1.7 Output Pin (RXD) (SBC only)

In normal mode this pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is indicated by a high level at RXD; LIN low (dominant state) is indicated by a low level at RXD.

The output is a push-pull stage switching between VCC and GND. The AC characteristics are measured by an external load capacitor of 20pF.

In silent mode the RXD output switches to high.

3.1.8 Enable Input Pin (EN) (SBC only)

The enable input pin controls the operating mode of the device. If EN is high, the circuit is in normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active. The VCC voltage regulator operates with 3.3V/5V/85mA output capability.

If EN is switched to low while TXD is still high, the device is forced to silent mode. No data transmission is then possible, and current consumption is reduced to $I_{VSsilent}$ typically 47µA. The VCC regulator retains its full functionality.

If EN is switched to low while TXD is low, the device is forced into sleep mode. No data transmission is possible, and the voltage regulator is switched off.

The EN pin provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.

3.1.9 Wake Input Pin (WKin) (Atmel ATA663232/55, ATA663331/54 and ATA663431/54 only)

The WKin pin is a high-voltage input used for waking up the device from sleep mode or silent mode. It is usually connected to an external switch in the application to generate a local wake-up. A pull-up current source with typically 10µA is implemented. The voltage threshold for a wake-up signal is typically 2V below V_{VS}. If the WKin pin is not needed in the application, it can be connected directly to the VS pin.

3.1.10 High-side Switch Pins (HSout, HSin) (Atmel ATA663331/54 and ATA663431/54 only)

This high-side switch is designed for low-power loads such as LEDs, sensors or a voltage divider for measuring the supply voltage. It is functional in all operating modes of the chip except for sleep mode. Its structure is connected to the VS supply pin. This pin is short-circuit protected and also protected against overheating, whereas the protective shutdown is debounced and latched. In other words, after a protective shutdown of the output switch, the control line HSin has to go to low level first before the output can be restarted again.

The high-side switch is controlled via the low-voltage input pin HSin. If the input is high, the output is switched on. For fail-safe reasons, the HSin input is equipped with a pull-down resistor to GND. This keeps the high-side switch off in case of a missing connection from the controller.

Please note that in case of a disconnected system ground, the module can be supplied via the connected load on the high-side output and an internal ESD structure. This is the case if the load has a different ground connection than the PCB. See also the “Absolute Maximum Ratings” section for current limits in such cases.

3.1.11 Wake Output Pin (WKout) (Atmel ATA663331/54 only)

The WKout pin is a low-voltage output used for waking up a microcontroller or other device. It is a push-pull output stage switching between VCC and GND. It is directly controlled by the WKin pin. If $V_{WKin} \geq V_{WKinH}$, WKout is low and no wake-up is detected. If VWKin < VWKinL, WKout is high and the device is switched into fail-safe mode if it was previously in a low-power mode such as sleep or silent mode. Please note that during silent, fail-safe and normal mode, the output pin WKout is always showing the state of pin WKin.

If a local wake-up is not needed in the application, the WKout pin can be left open.

3.1.12 CL15 Pin (Atmel ATA663431/54 only)

The CL15 pin is a high-voltage input that can be used to wake up the device from sleep mode or silent mode. It is an edge-sensitive pin (low to-high transition). Thus, even if the CL15 pin is at high voltage ($V_{CL15} > V_{CL15H}$), it is possible to switch the IC into sleep mode or silent mode. It is usually connected to the ignition for generating a local wake-up in the application if the ignition is switched on. The CL15 pin should be tied directly to ground if not needed. A debounce timer with a value t_{dbCL15} of typically 100µs is implemented. To protect this pin against transients, a serial resistor with 10kΩ and a ceramic capacitor with 47nF are recommended. With this RC combination you can increase the CL15 wake-up time.

3.1.13 WDOSC Output Pin (Atmel ATA663431/54 only)

The WDOSC output pin provides a typical voltage of 1.23V intended to supply an external resistor with values between 34kΩ and 120kΩ. The value of the resistor adjusts the watchdog oscillator frequency to provide a certain range of time windows.

If the watchdog is disabled, the output voltage is switched off and the pin can either be tied to VCC or left open.

3.1.14 NTRIG Input Pin (Atmel ATA663431/54 only)

The NTRIG input pin is the trigger input for the window watchdog. A pull-up resistor is implemented. A falling edge triggers the watchdog. The trigger signal (low) must exceed a minimum time of $t_{trigmin}$ to generate a watchdog trigger and avoid false triggers caused by transients.

3.1.15 MODE Input Pin (Atmel ATA663431/54 only)

Connect the MODE pin directly or via an external resistor to GND for normal watchdog operation. To debug the software of the connected microcontroller, connect the MODE pin to VCC and the watchdog is switched off. For fail-safe reasons, the MODE pin has a self-holding function, pulling the input to ground (i.e., watchdog enabled) in case of an open connection.

Note: If you do not use the watchdog, connect the mode pin directly to VCC.

3.1.16 Limp Home Watchdog Failure Output (LH) (Atmel ATA663431/54 only)

The LH output pin indicates a failure of the watchdog. It is realized as a high-voltage open drain NMOS structure. During power up or after a wake-up from sleep mode the LH output is switched off. As the watchdog is only working in normal and fail-safe mode, the state of the LH output transistor can change only in these two modes. In silent mode the LH output remains in the same state as it was before switching into silent mode.

If a watchdog reset occurs, the LH output transistor switches on immediately, and it switches off only after three correct consecutive watchdog trigger pulses have been occurred at the NTRIG pin.

3.1.17 Low-side Driver Pins (LS1out, LS2out, LS1in, LS2in) (Atmel ATA663331/54)

LS1out and LS2out are the low-side driver outputs designed for the control of relays. They are only functional in normal mode. These outputs are both short-circuit protected by means of output voltage monitoring and protected against overheating. They additionally include active clamping circuitry to provide a freewheeling path needed for inductive loads.

The clamping voltage $V_{LSclamp}$ is typically > 44V. Please note that an upper energy limit is defined both for single and for repetitive clamping events. This must be considered when choosing the load because overheating caused by excessive clamping energy is not compensated for by the output protection and might cause damage to the device.

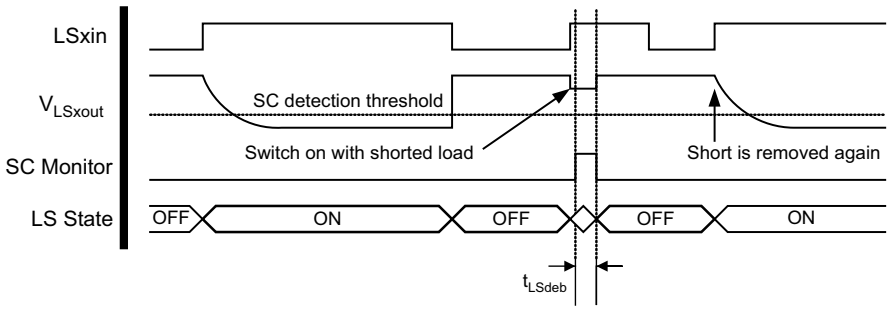
If the LS1in pin or the LS2in pin stay at GND level while switching into normal mode, it must be pulled to high level longer than 10µs before the low-side driver can be activated. This feature prevents the low-side drivers (LS1out pin or LS2out pin respectively) from being unintentionally switched ON after normal mode has been activated. To reactivate the low-side drivers, switch LS1in or LS2in to high (> 10µs).

A disconnection of VS where the low sides are still supplied by VBAT through a load does not have any impact on the clamping feature. In other words, voltages exceeding the minimum $V_{LSclamp}$ clamping voltage level activate the freewheeling path within the low-side transistor.

The low-side switches are controlled by the LS1in and LS2in low voltage input pins. If the inputs are at high level and the IC is in normal mode (i. e., EN is high and there is no undervoltage supply condition), the outputs are switched on. For fail-safe reasons, both inputs are equipped with a pull-down resistor to GND. This keeps the low-side switches off in case of a missing connection from the controller.

If an overload condition is detected, the appropriate driver stage is shut down. The protective shutdown of the low-side outputs is latched. In other words, the corresponding LSxin control line has to go to low first before the output can be reactivated. Because the short-circuit detection is handled by drain-to-source voltage monitoring, the switch-on event of the transistor is blanked out from the monitoring. As a result, a capacitor connected to the low-side output will not trigger the protection circuit upon activation of the transistor. Figure 3-1 also illustrates this,

Figure 3-1. Short-circuit Detection Timing



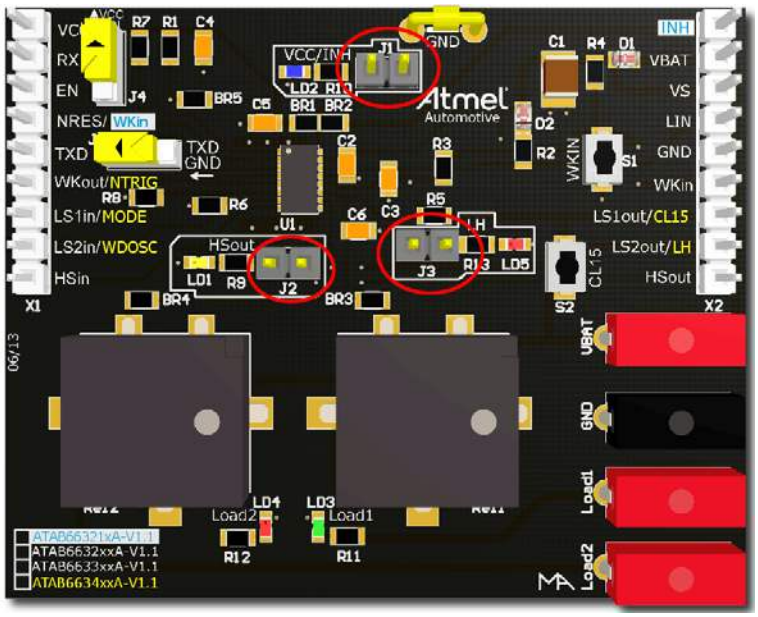
As can be seen in Figure 3-1, the output transistor is not switched on again until the LSxin control pin is switched off and on again by the microcontroller. As explained above, the short-circuit monitor is only enabled after the transistor reaches full conductivity. That is why the SC (short circuit) monitor line does not show any signal on the first and the last switch-on event in Figure 3-1. Without a short circuit at the output, the transistor takes much more time to establish its operation point than if there is a short circuit present.

3.2 Measurements on the Development Board

3.2.1 Current Consumption Measurement

Atmel recommends removing the J1, J2, and J3 jumpers when measuring current consumption, because otherwise the current flowing through the LEDs (LD1 at HSout, LD2 at VCC, LD3 at LimpHome) will result in faulty measurements.

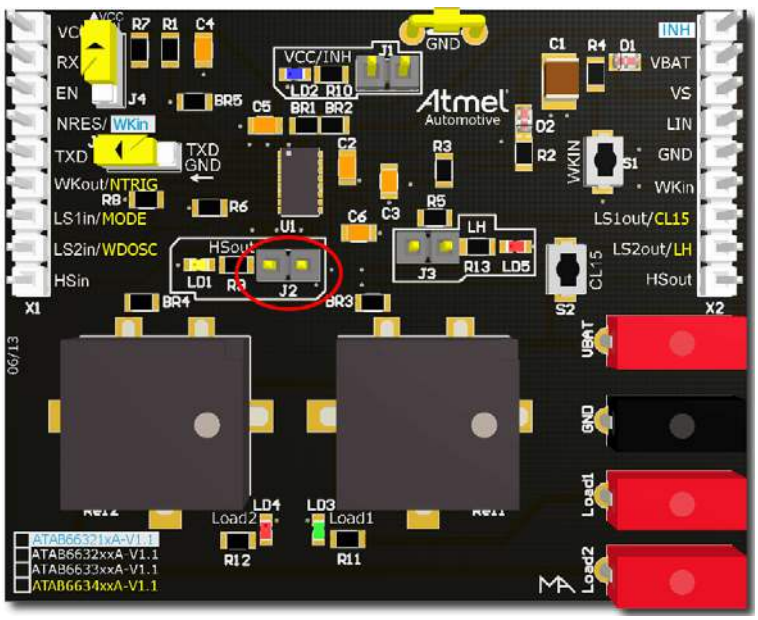
Figure 3-2. Jumper Settings for Current Consumption Measurement



3.2.2 High-side Driver Measurement (only with ATA6633xx and Atmel ATA6634xx)

An LED (LD1) and the series resistor R9 are connected to the HSout pin via the J2 jumper by default. External circuitry can be connected to the HSout pin at the X2 pin header. In this case, the J2 jumper has to be removed.

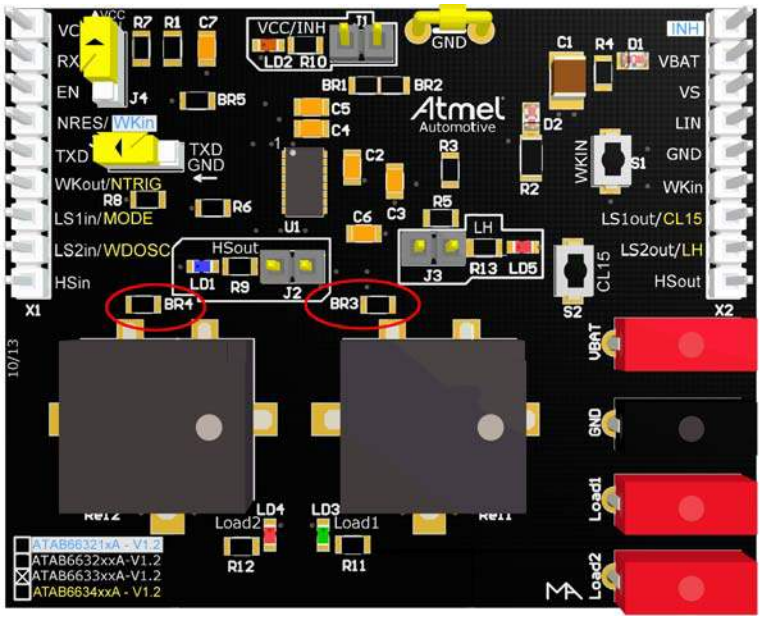
Figure 3-3. High-side Driver Measurements



3.2.3 Low-side Driver Measurements (only with Atmel ATA6633xx)

There are two relays mounted on the Atmel® ATAB663331A and the ATAB663354A board and connected to the LS1out and LS2out pins allowing the user to take measurements and conduct tests closely approximating the real application. If the relays are not needed, just remove the BR3 and BR4 0? resistances. External circuitry can then easily be connected to the LS1out and LS2out via the X2 pin header.

Figure 3-4. Low-side Driver Measurements

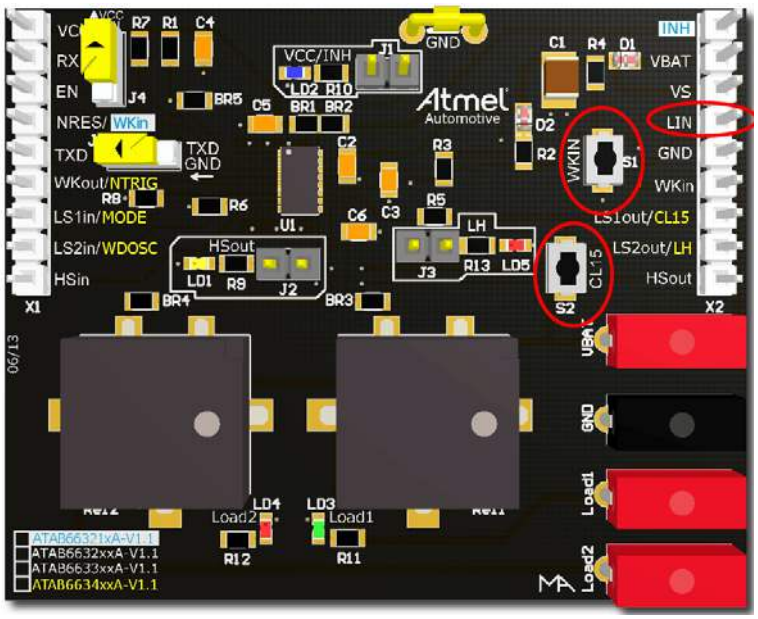


3.2.4 Wake-up Tests

The devices can distinguish between different wake-up sources (see Table 2-2 on page 10). The wake-up source can be read on the TXD and RXD pin in fail-safe mode. These flags are immediately reset if the EN pin is set to high and the IC is in normal mode. For more information regarding the wake-up behavior, please refer to the corresponding datasheet.

When the device is in sleep or silent mode, it can easily be woken up via the two push buttons (one at the WKin pin and one at the CL15 pin) (local wake-up) or via a falling edge at the LIN pin followed by a dominant bus level maintained for a given period of time (> t_{bus}) together with a subsequent rising edge at the LIN pin (remote wake-up).

Figure 3-5. Wake-up Capabilities on the Atmel ATAB663xxxA Board



3.3 PCB Design Recommendations

All parts of the device family have an excellent EMC performance, however, care must be taken by designing the PCB. Some general recommendations are listed below.

- No interlayer connections of the blocking capacitors
- C1 (10µF/50V) as close as possible between the VS pin and GND pin
- C2 (100nF ceramic) as close as possible between the VS pin and GND pin
- C3 (220pF ceramic) direct at the LIN pin and to the GND pin
- C4 (2.2µF ceramic) as close as possible to the VCC pin and to the heat slug
- C5 (100nF ceramic) as close as possible to the VCC pin and to the heat slug
- The heat slug should be connected directly to the GND pin under the package
- The GND pin connection star shaped to the module GND

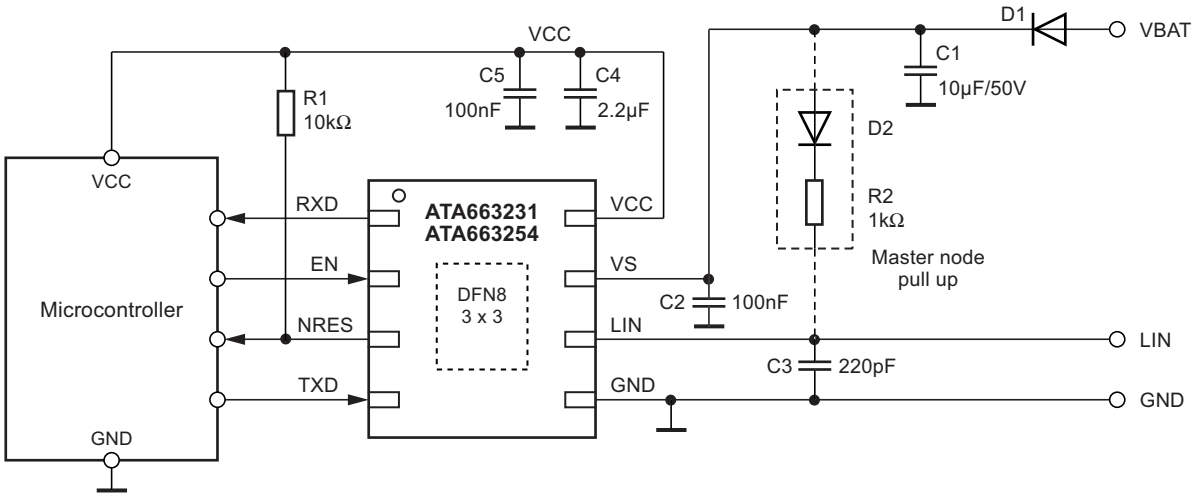
Please note that if any critical measurements on EMI (electromagnetic interference) performance, such as electromagnetic immunity or electromagnetic emission, are to be carried out, Atmel recommends using a dedicated board.

4. Applications

The following figures illustrate typical application circuit examples using one part from the device family.

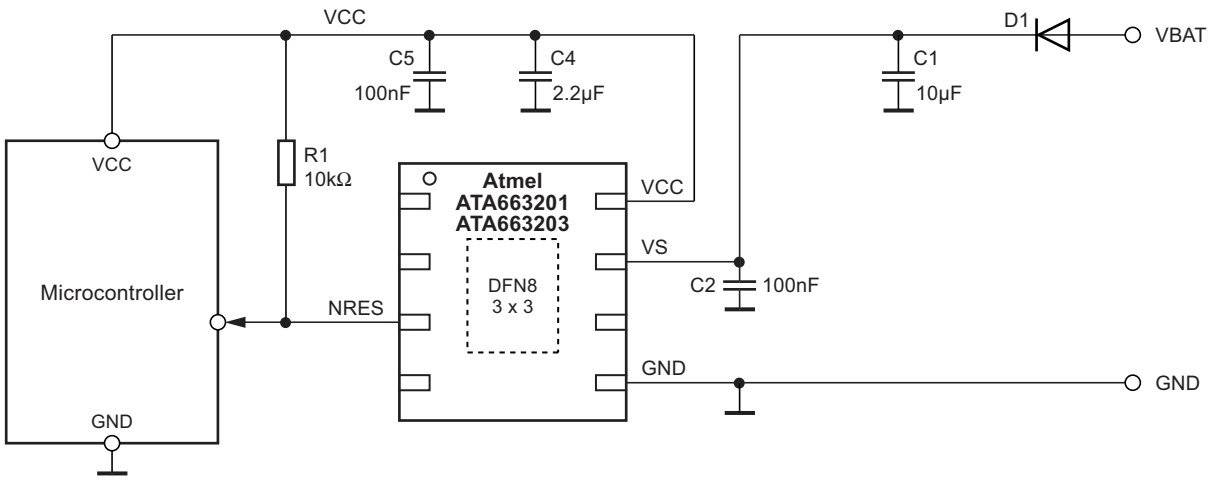
Depending on which device is soldered on the board, all corresponding components required are mounted on the board.

Figure 4-1. Typical Application Circuit Atmel ATA663231/ATA663254



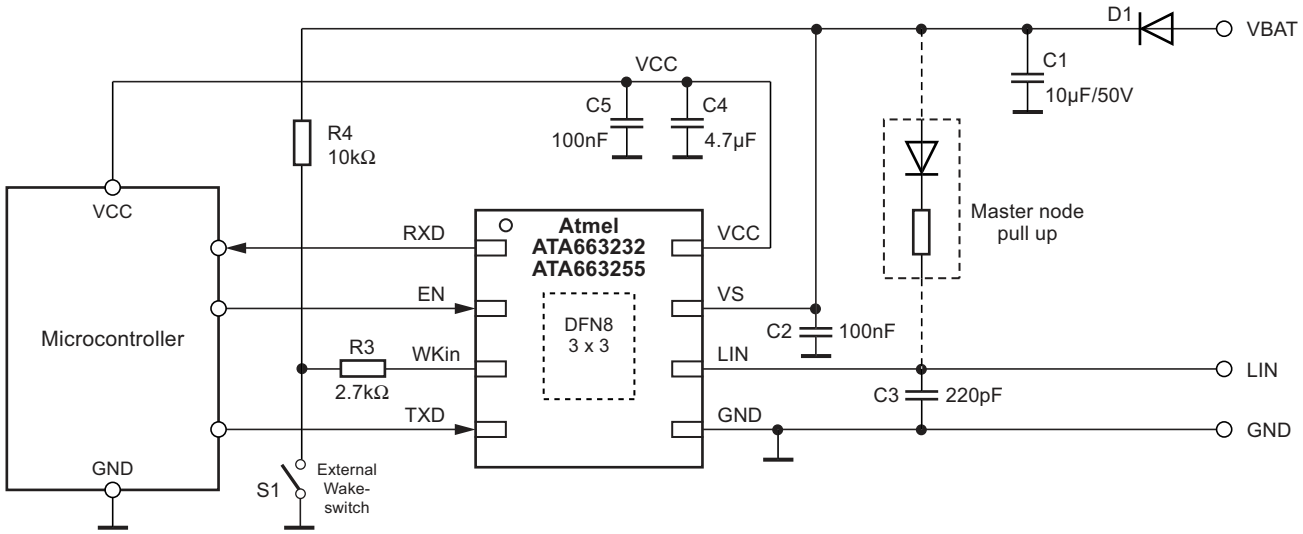
Note: Heatslug must always be connected to GND.

Figure 4-2. Typical Application Circuit Atmel ATA663201/03



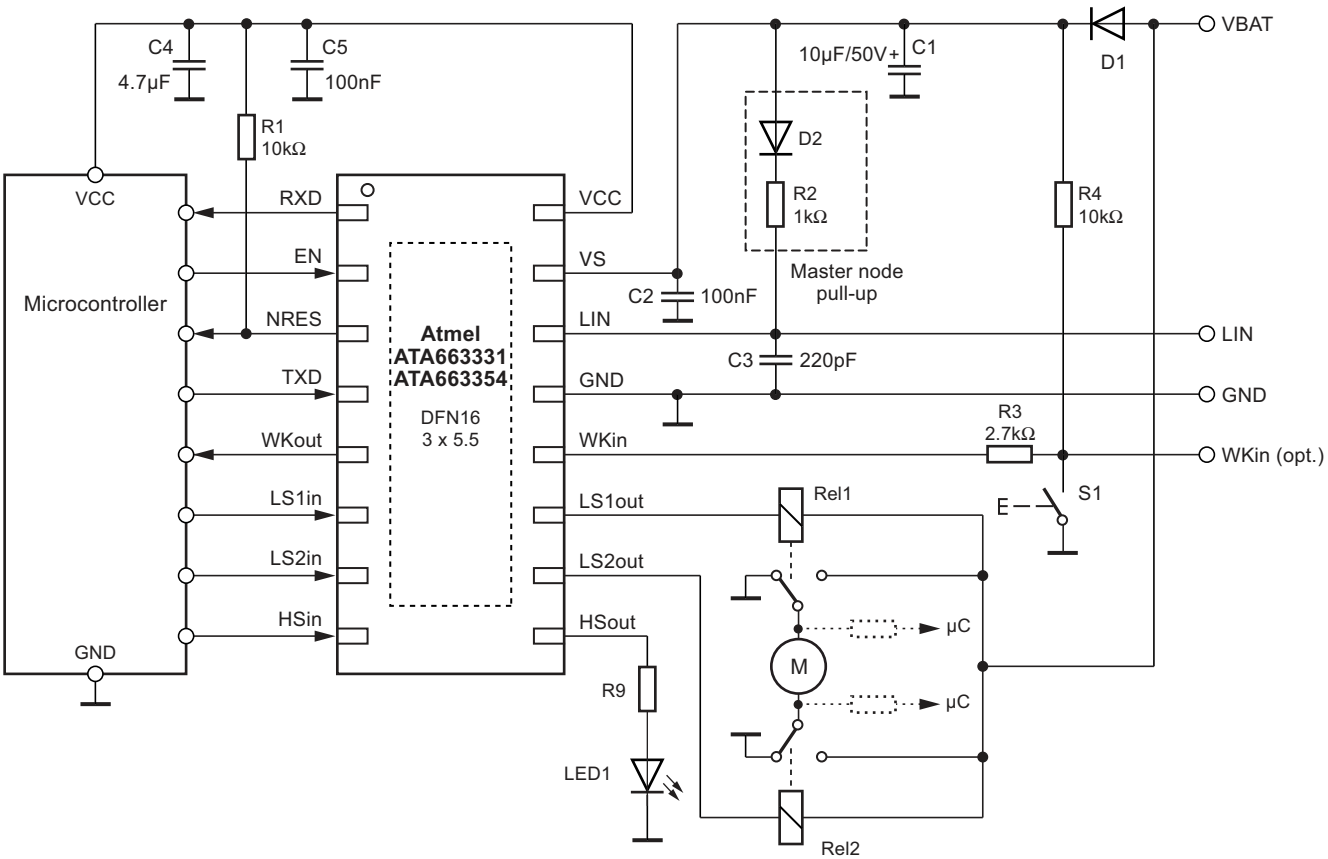
Note: Heatslug must always be connected to GND.

Figure 4-3. Typical Application Circuit Atmel ATA663232/55



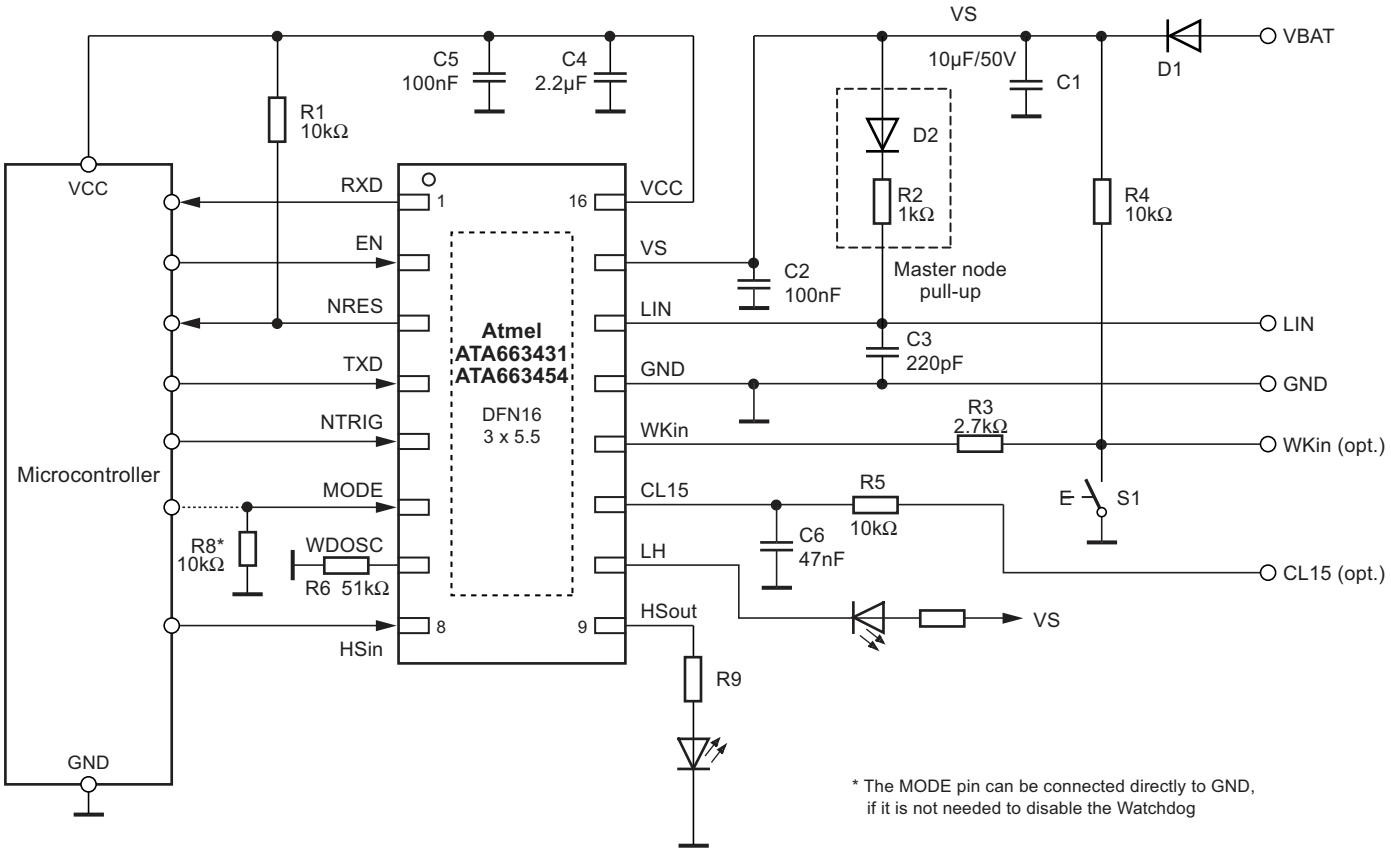
Note: Heatslug must always be connected to GND.

Figure 4-4. Typical Application Circuit Atmel ATA6633xx (LIN SBC with 2 Relay Drivers)



Note: Heatslug must always be connected to GND.

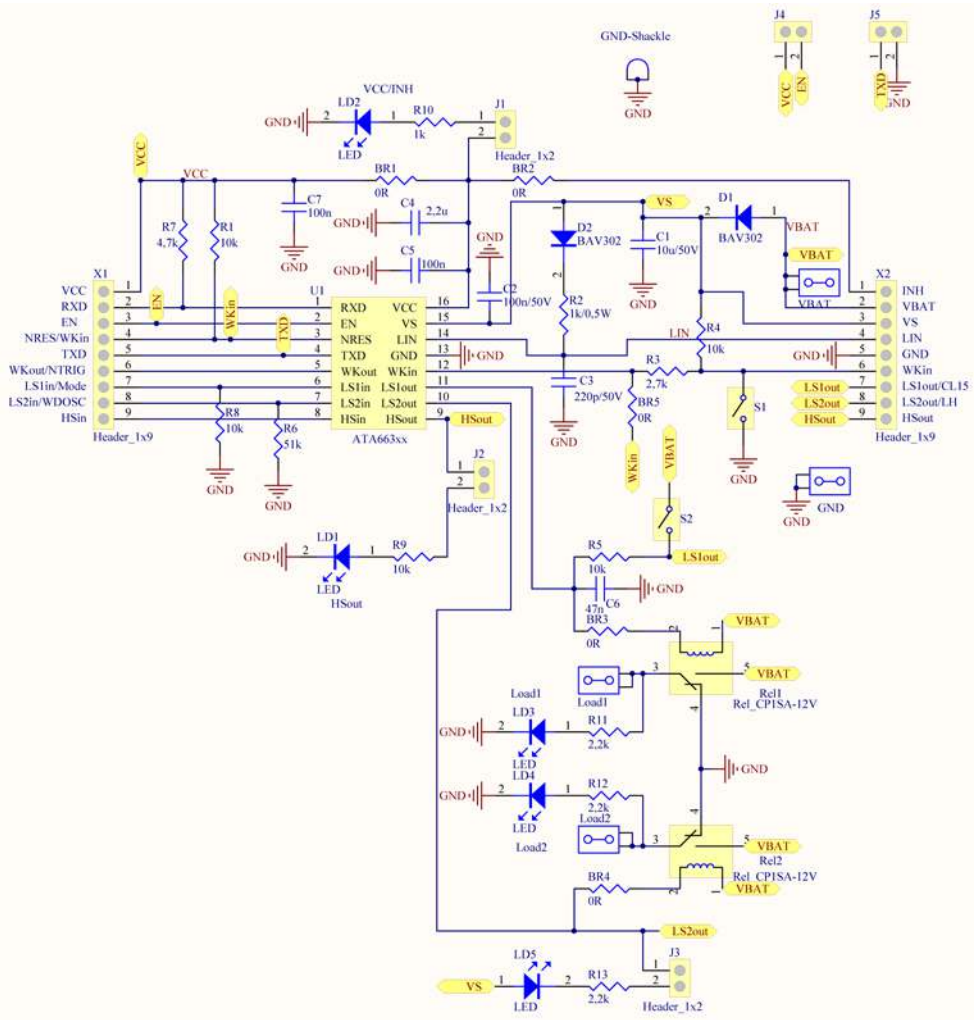
Figure 4-5. Typical Application Circuit Atmel ATA663431/ATA663454 (LIN SBC with Watchdog)



Note: Heatslug must always be connected to GND.

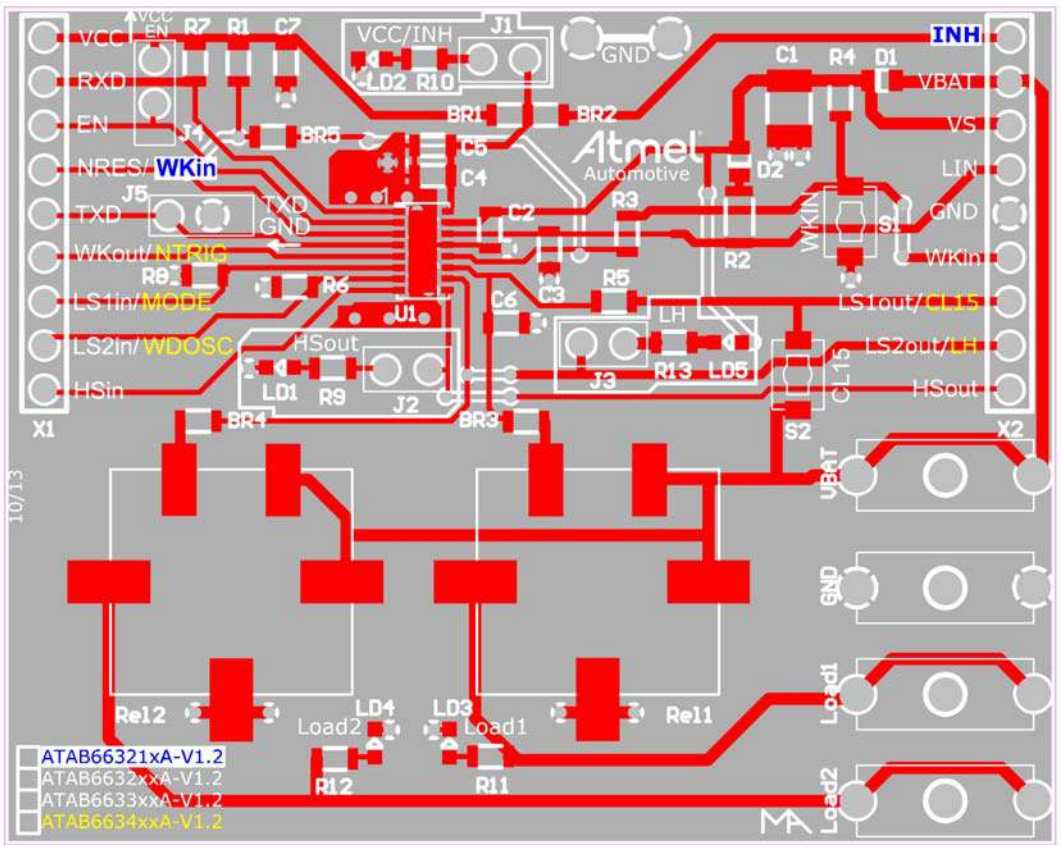
5. Schematics

Figure 5-1. Board Schematic



6. Board Layout

Figure 6-1. Board Layout; Top View – As If PCB was Transparent (Top Side Red and Bottom Side Blue)



7. Assembly Options

Depending on which evaluation kit has been ordered, the corresponding device from the IC family is soldered on the board. All components required for putting the device into operation are assembled on the board. The following figures show the different delivery options of the development board.

Figure 7-1. Atmel ATA663201 and ATA663203 (Voltage Regulator)

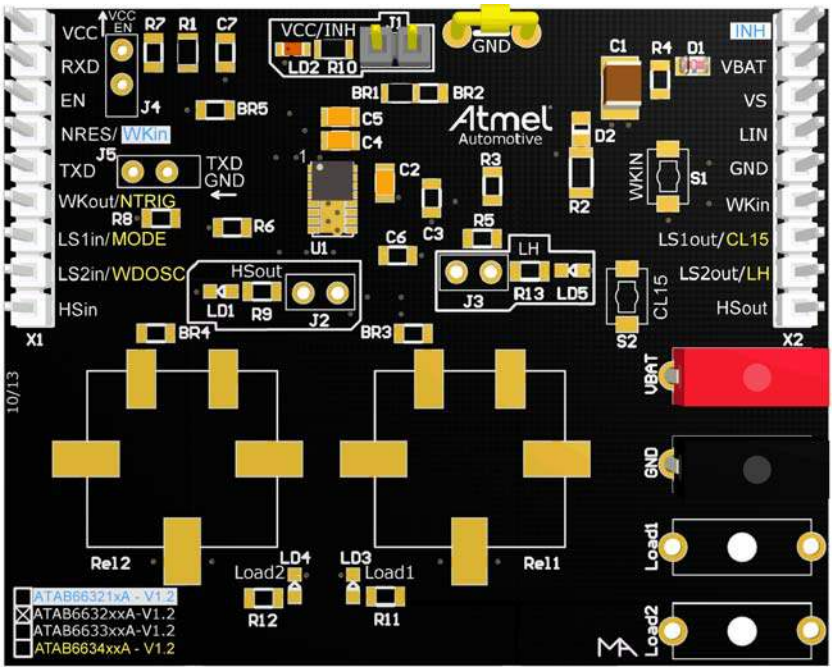


Figure 7-2. Atmel ATA663231 and ATA663254 (LIN SBC)

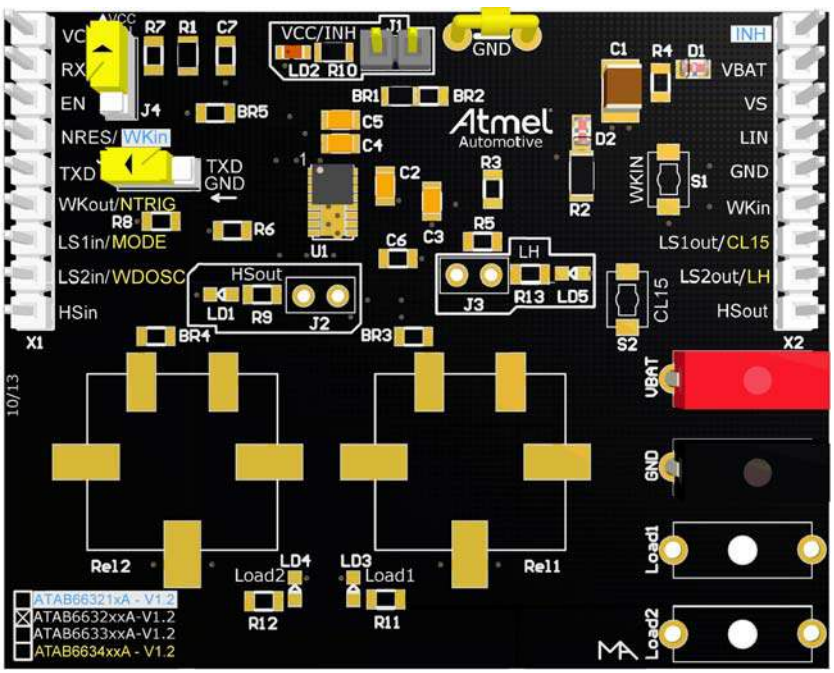


Figure 7-3. Atmel ATA663232 and ATA663255 (LIN SBC with High-voltage Wake Input)

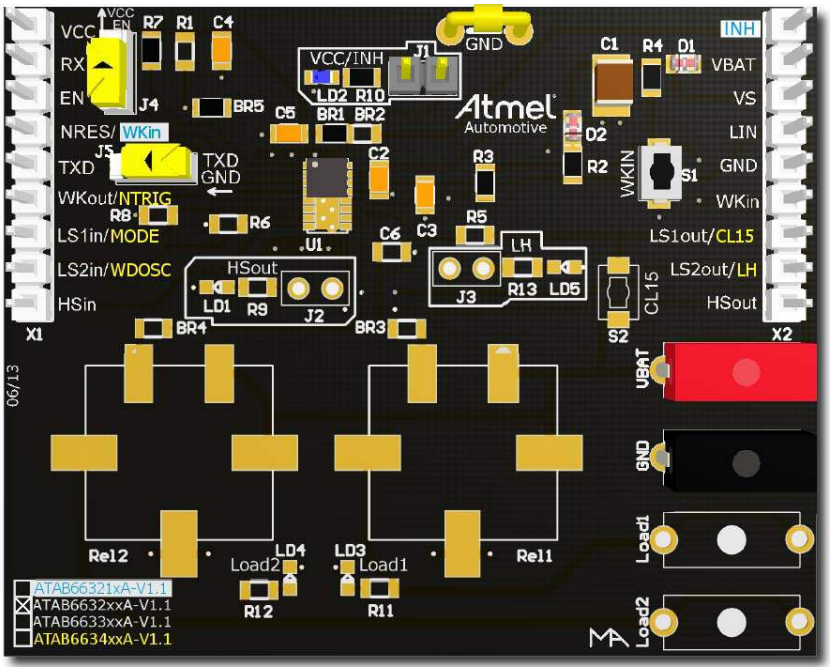


Figure 7-4. Atmel ATA663331 and ATA663354 (LIN SBC with Two Relay Drivers)

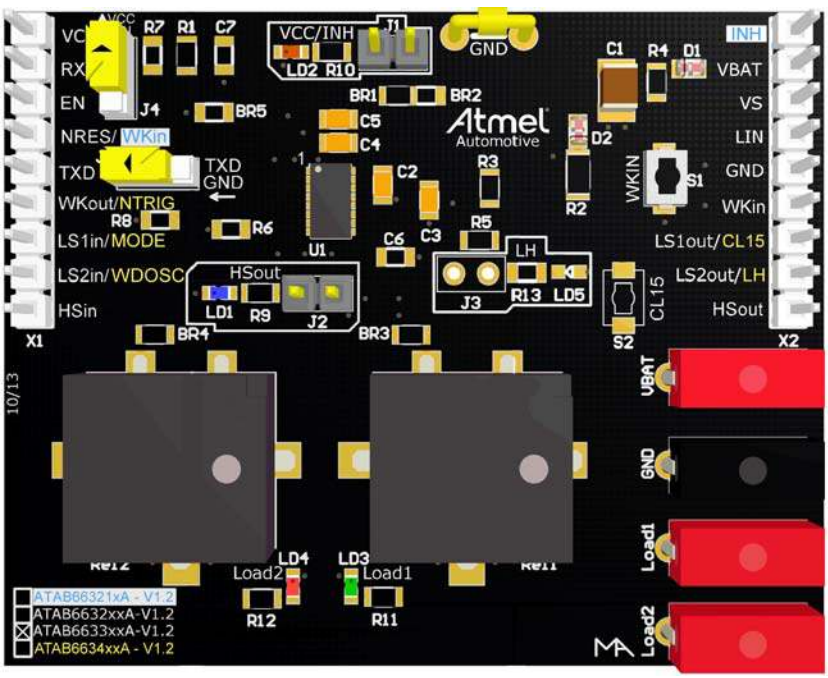
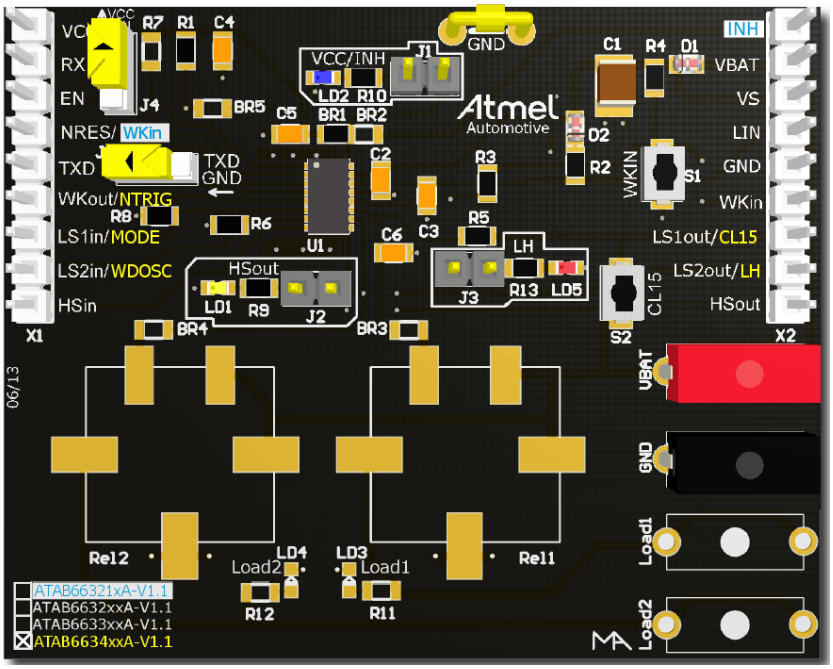


Figure 7-5. Atmel ATA663431 and ATA663454 (LIN SBC with Watchdog)



8. Bill of Material (BOM)

The development board is designed to handle the entire IC family. It is just a matter of an assembly option. Table 8-1 shows which components are used with the corresponding device from the IC family.

Table 8-1. BOM

Designator	IC Sub-family					Value	Description	Footprint	Manufacturer and Part Number
	ATA663232/55	ATA663231/54	ATA663201/03	ATA663331/54	ATA663431/54				
IC	X						LIN system basis chip – LIN transceiver with voltage regulator and high-voltage wake-input	DFN8	ATA663232/55
		X					LIN system basis chip – LIN transceiver with voltage regulator	DFN8	ATA663231/54
			X				Voltage regulator	DFN8	ATA663201/03
				X			LIN system basis chip with dual low-side driver and high-side switch	DFN16	ATA663331/54
					X		LIN system basis chip with window watchdog and high-side switch	DFN16	ATA663431/54
X1	X	X	X	X	X	Header 1x9	Header 1x9	1 × 9 2.54mm	
X2	X	X	X	X	X	Header 1x9	Header 1x9	1 × 9 2.54mm	
C1	X	X	X	X	X	10µF/50V	Capacitor	SMD 1210	
C2	X	X	X	X	X	100nF/50V	Capacitor	SMD 0805	
C3	X	X	-	X	X	220pF/50V	Capacitor	SMD 0805	
C4	-	X	X	-	X	2.2µF/10V	Capacitor	SMD 0805	
	X	-	-	X	-	4.7µF/10V			
C5	X	X	X	X	X	100nF	Capacitor	SMD 0805	
C6		-	-	-	X	47nF	Capacitor	SMD 0603	
C7	-	-	-	-	-	100nF	Capacitor	SMD 0603-	
D1	X	X	X	X	X	BAV302	Switching diode	SMD 0603	
D2	X	X	-	X	X	BAV302	Switching diode	SMD 0603	
GND shackle	X	X	X	X	X	GND1	Ground shackle	GND shackle	
R1	-	X	X	X	X	10K	Resistor	SMD 0805	
R2	X	X	-	X	X	1K/0.5W	Resistor	SMD 1206	
R3	X	-	-	X	X	2.7K	Resistor	SMD 0805	
R4	X	-	-	X	X	10K	Resistor	SMD 0805	
R5	-	-	-	-	X	10K	Resistor	SMD 0805	
	-	-	-	X	-	0Ω			
R6	-	-	-	X	X	51K	Resistor	SMD 0805	
R8	-	-	-	-	X	10K	Resistor	SMD 0805	
R9	-	-	-	X	X	10K	Resistor	SMD0805	

Table 8-1. BOM (Continued)

Designator	IC Sub-family					Value	Description	Footprint	Manufacturer and Part Number
	ATA663232/55	ATA663231/54	ATA663201/03	ATA663331/54	ATA663431/54				
R10	X	X	X	X	X	1K	Resistor	SMD0805	
R11	-	-	-	X	-	10K	Resistor	SMD0805	
R12	-	-	-	X	-	10K	Resistor	SMD0805	
R13	-	-	-	-	X	10K	Resistor	SMD 0603	
S1	X	-	-	X	X	TL1015AF	Tackle switch	Switch_TL	E-switch
S2	-	-	-	-	X	TL1015AF	Tackle switch	Switch_TL	E-switch
LD1	-	-	-	X	X	0603_LED_bl	LED	SMD 0603	
LD2	X	X	X	X	X	0603_LED_or	LED	SMD 0603	
LD3	-	-	-	X	-	0603_LED_or	LED	SMD 0603	
LD4	-	-	-	X	-	0603_LED_or	LED	SMD 0603	
LD5	-	-	-	-	X	0603_LED_or	LED	SMD 0603	
Rel1	-	-	-	X	-	CP1A-12V	Auto_SMD_relay	CP1 relay	PANASONIC EW
Rel1	-	-	-	X	-	CP1A-12V	Auto_SMD_relay	CP1 relay	PANASONIC EW
LOAD1	-	-	-	X	-	LOAD1	Test jack, HNO	Socket_MPB1	
LOAD1	-	-	-	X	-	LOAD1	Test jack, HNO	Socket_MPB1	
VBAT	X	X	X	X	X	VBAT	Supply connector	Socket_MPB1	
GND	X	X	X	X	X	GND	Ground connector	Socket_MPB1	
BR1	X	X	X	X	X	0W	Resistor	SMD 0805	
BR2	-	-	-	-	-	0W	Resistor	SMD 0805	
BR3	-	-	-	X	-	0W	Resistor	SMD 0805	
BR4	-	-	-	X	-	0W	Resistor	SMD 0805	
BR5	X	-	-	X	X	0W	Resistor	SMD 0805	
J1	X	X	X	X	X	Header 1x2	Header 1x2	1 × 2 2.54mm	
J2	-	-	-	X	X	Header 1x2	Header 1x2	1 × 2 2.54mm	
J3	-	-	-	-	X	Header 1x2	Header 1x2	1 × 2 2.54mm	
J4	X	X	-	X	X	JSA-4-01-GO	PCB jumper switch	1 × 2 2.54mm	
J5	X	X	-	X	X	JSA-4-01-GO	PCB jumper switch	1 × 2 2.54mm	

9. Ordering Information

Development Board Part Number	IC Mounted	Description	IC Package
ATAB663231A-V1.2	ATA663231	LIN transceiver with voltage regulator 3.3V	DFN8
ATAB663254A-V1.2	ATA663254	LIN transceiver with voltage regulator 5V	DFN8
ATAB663232A-V1.2	ATA663232	LIN transceiver with voltage regulator 3.3V and high-voltage wake-input	DFN8
ATAB663255A-V1.2	ATA663255	LIN transceiver with voltage regulator 5V and high-voltage wake-input	DFN8
ATAB663201A-V1.2	ATA663201	3.3V voltage regulator	DFN8
ATAB663203A-V1.2	ATA663203	5V voltage regulator	DFN8
ATAB663331A-V1.2	ATA663331	LIN transceiver, voltage regulator 3.3V, 2 relay drivers (low-side), 1 high-side driver, 1 high-voltage wake-input	DFN16
ATAB663354A-V1.2	ATA663354	LIN transceiver, voltage regulator 5V, 2 relay drivers (low-side), 1 high-side driver, 1 high-voltage wake-input	DFN16
ATAB663431A-V1.2	ATA663431	LIN transceiver, voltage regulator 3.3V, watchdog with limp home output, 1 high-side driver, 2 high-voltage wake-inputs	DFN16
ATAB663454A-V1.2	ATA663454	LIN transceiver, voltage regulator 5V, watchdog with limp home output, 1 high-side driver, 2 high-voltage wake-inputs	DFN16

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