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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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2SJ550(L), 2SJ550(S)

Silicon P Channel MOS FET

REJ03G0897-0300
 (Previous: ADE-208-633A)
 Rev.3.00
 Sep 07, 2005

Description

High speed power switching

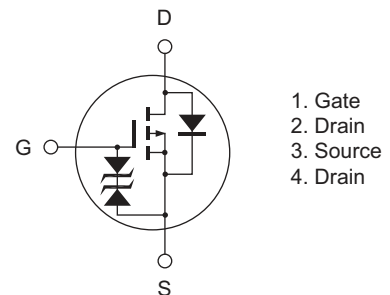
Features

- Low on-resistance
 $R_{DS(on)} = 0.075 \Omega$ typ.
- Low drive current.
- 4 V gate drive devices.
- High speed switching.

Outline

RENESAS Package code: PRSS0004AE-A
 (Package name: LDKPAK (L))

RENESAS Package code: PRSS0004AE-B
 (Package name: LDKPAK (S)-(1))



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	-60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	-15	A
Drain peak current	I _{D (pulse)} ^{Note 1}	-60	A
Body to drain diode reverse drain current	I _{DR}	-15	A
Avalanche current	I _{AP} ^{Note 3}	-15	A
Avalanche energy	E _{AR} ^{Note 3}	19	mJ
Channel dissipation	P _{ch} ^{Note 2}	50	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

- Notes: 1. PW ≤ 10 ∞s, duty cycle ≤ 1%
 2. Value at Tc = 25°C
 3. Value at Tch = 25°C, Rg ≥ 50 Ω

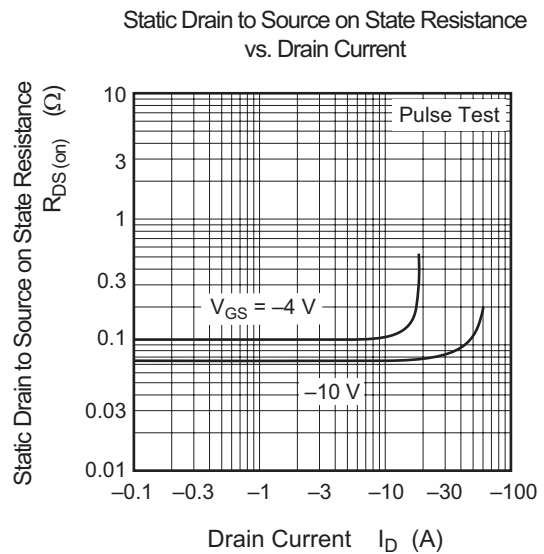
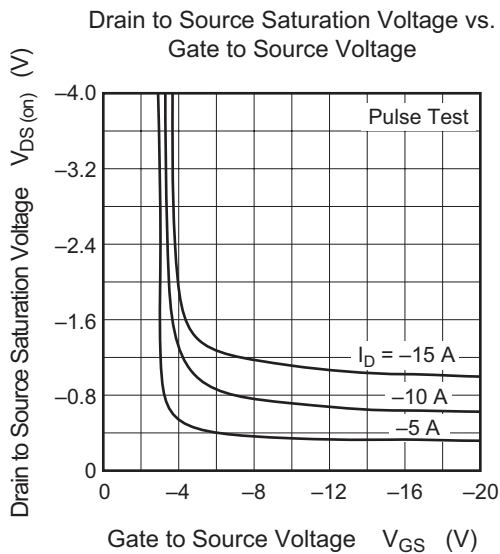
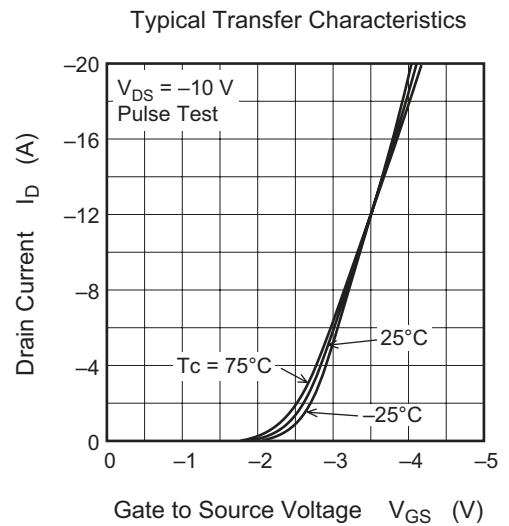
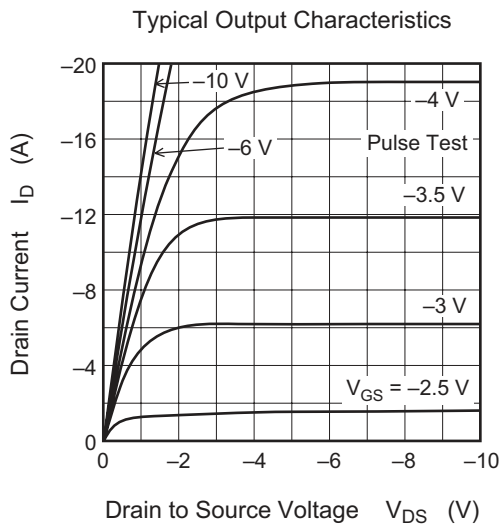
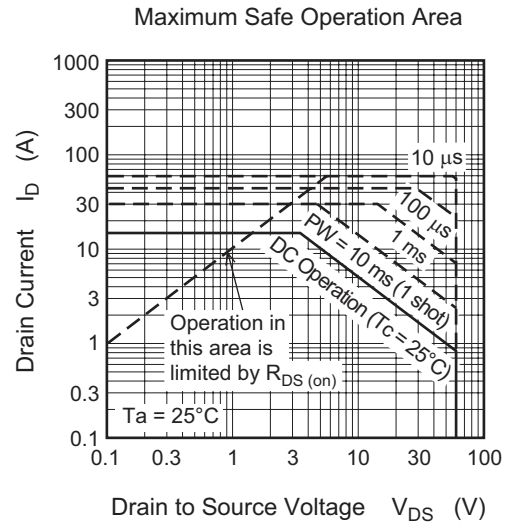
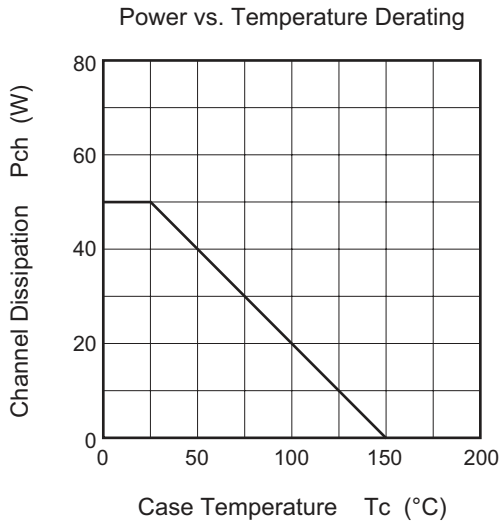
Electrical Characteristics

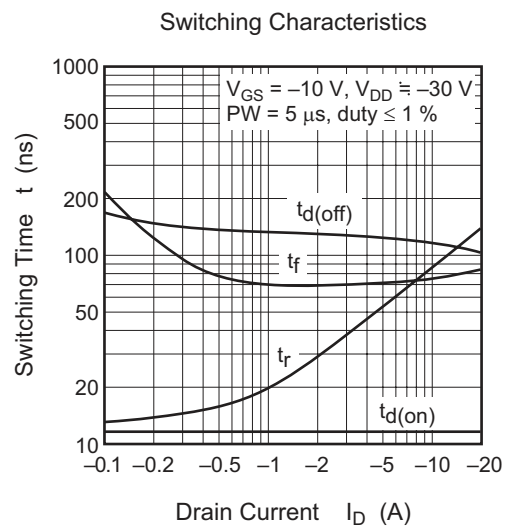
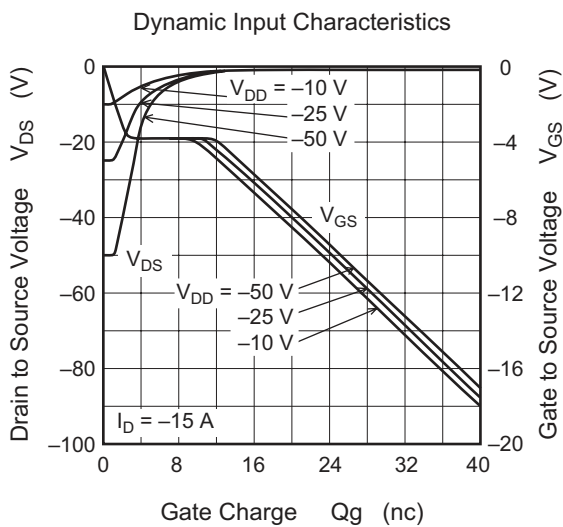
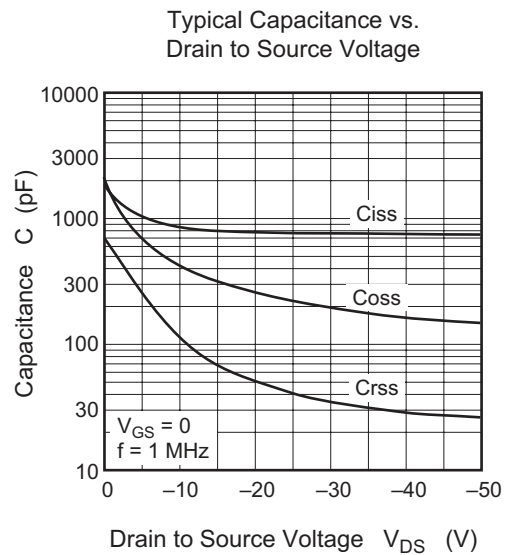
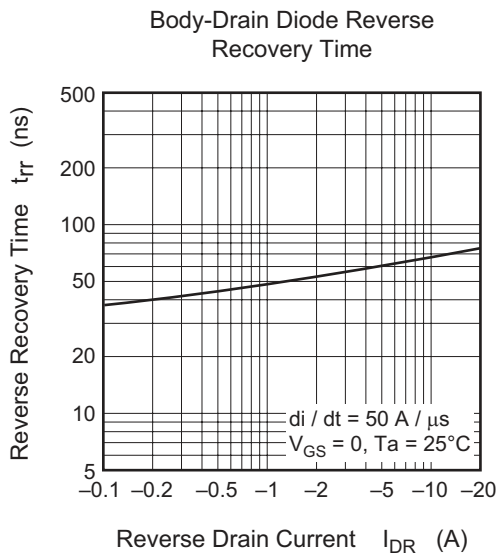
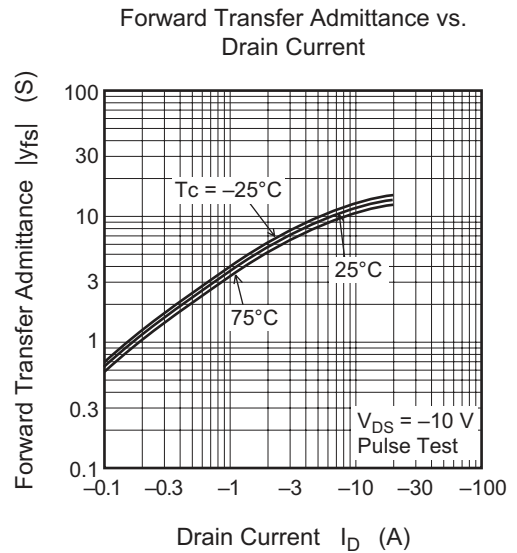
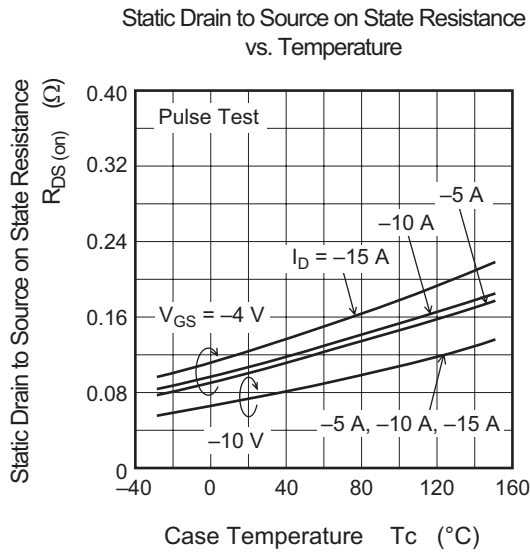
(Ta = 25°C)

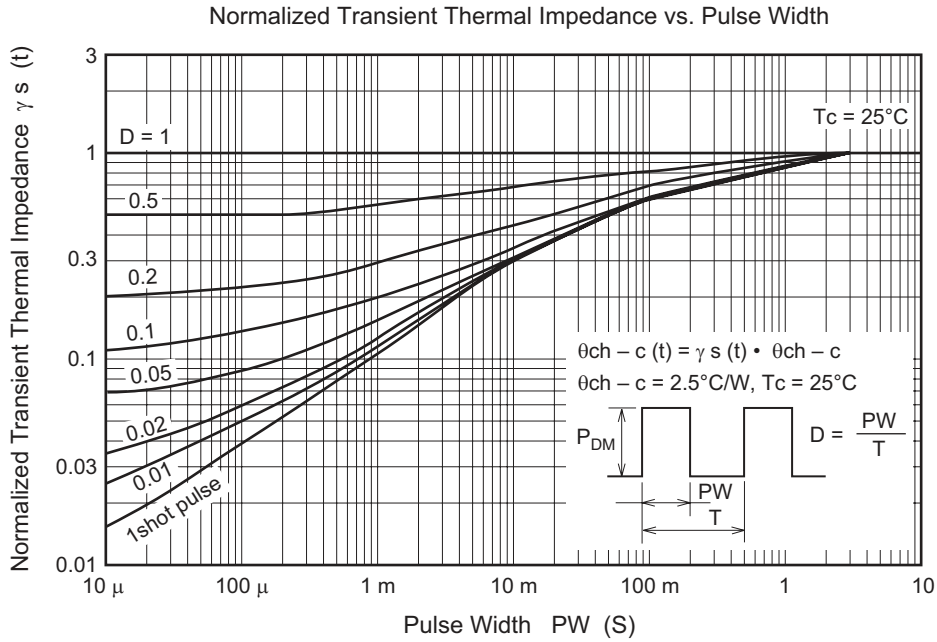
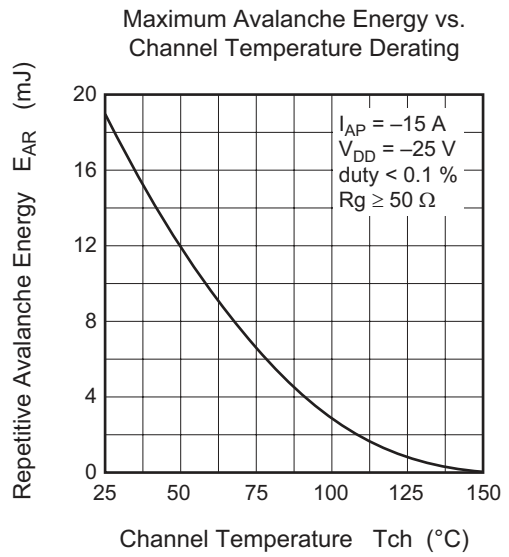
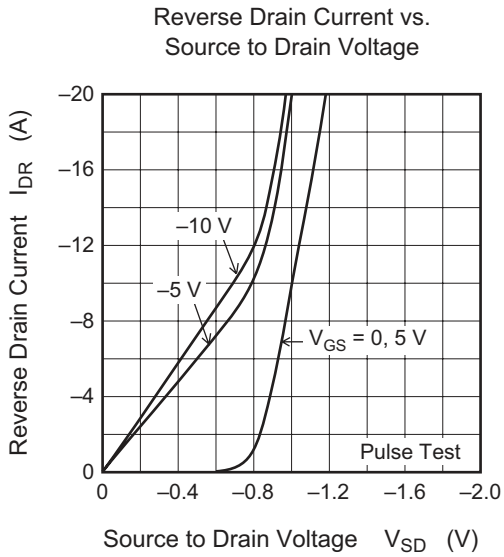
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	-60	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR) GSS}	±20	—	—	V	I _G = ±100 ∞A, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-10	∞A	V _{DS} = -60 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	∞A	V _{GS} = ±16 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS (off)}	-1.0	—	-2.0	V	I _D = -1 mA, V _{DS} = -10 V
Static drain to source on state resistance	R _{DS (on)}	—	0.075	0.095	Ω	I _D = -8 A, V _{GS} = -10 V ^{Note 4}
	R _{DS (on)}	—	0.105	0.155	Ω	I _D = -8 A, V _{GS} = -4 V ^{Note 4}
Forward transfer admittance	y _{fs}	6.5	11	—	S	I _D = -8 A, V _{DS} = -10 V ^{Note 4}
Input capacitance	C _{iss}	—	850	—	pF	V _{DS} = -10 V
Output capacitance	C _{oss}	—	420	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	110	—	pF	f = 1 MHz
Turn-on delay time	t _{d (on)}	—	12	—	ns	V _{GS} = -10 V
Rise time	t _r	—	75	—	ns	I _D = -8 A
Turn-off delay time	t _{d (off)}	—	125	—	ns	R _L = 3.75 Ω
Fall time	t _f	—	75	—	ns	
Body to drain diode forward voltage	V _{DF}	—	-1.1	—	V	I _F = -15 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	70	—	ns	I _F = -15 A, V _{GS} = 0 di _F /dt = 50 A/∞s

- Note: 4. Pulse test

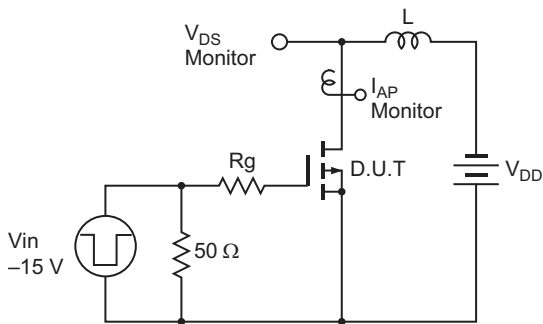
Main Characteristics





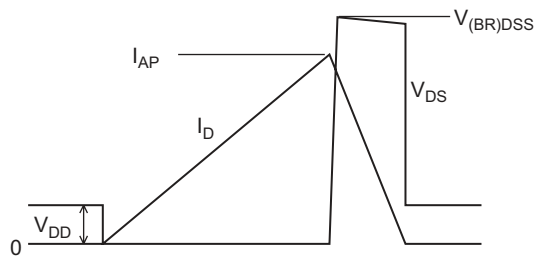


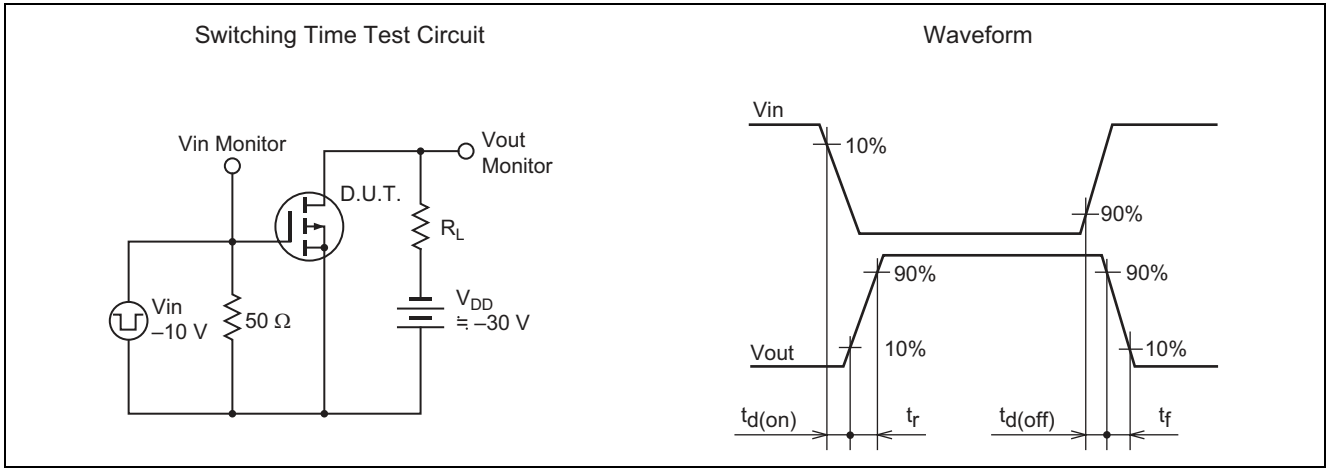
Avalanche Test Circuit



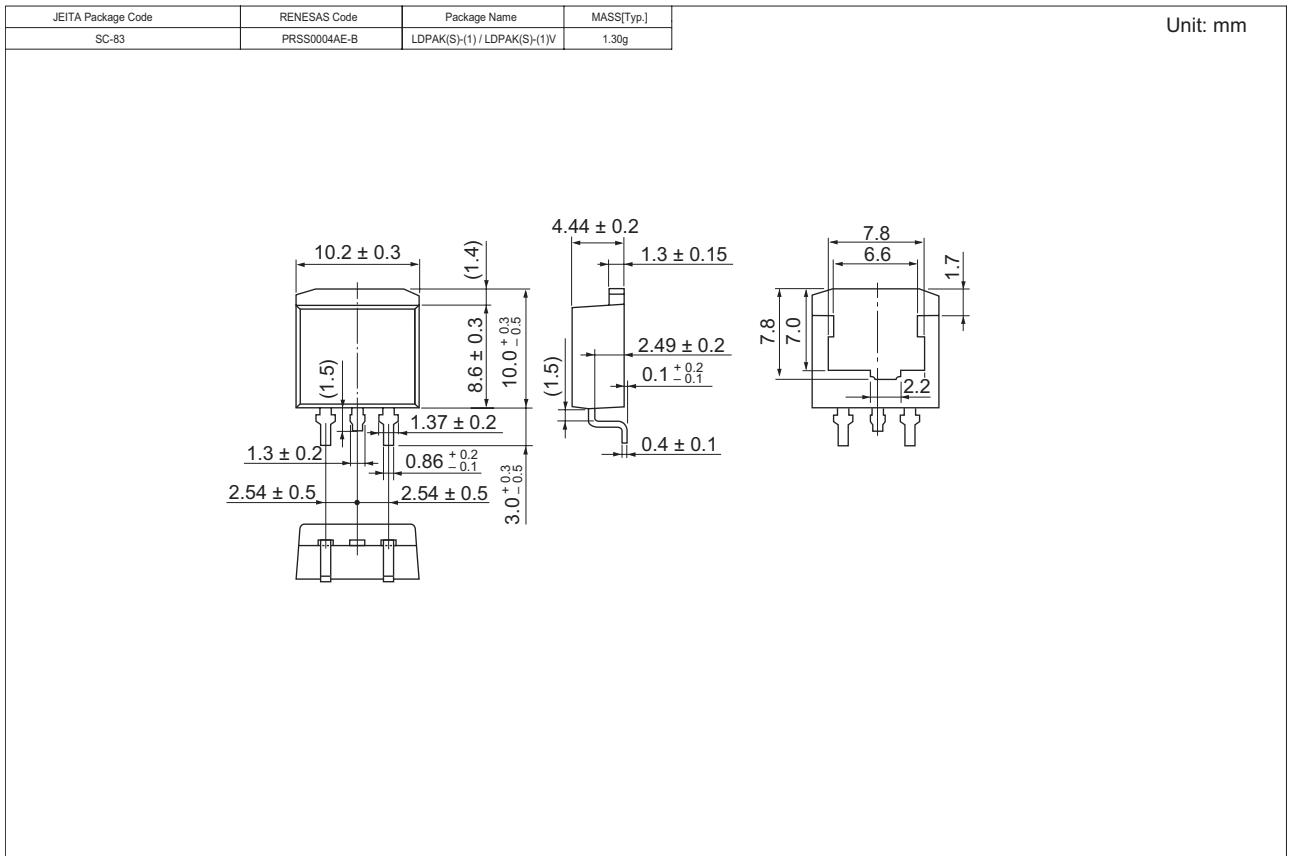
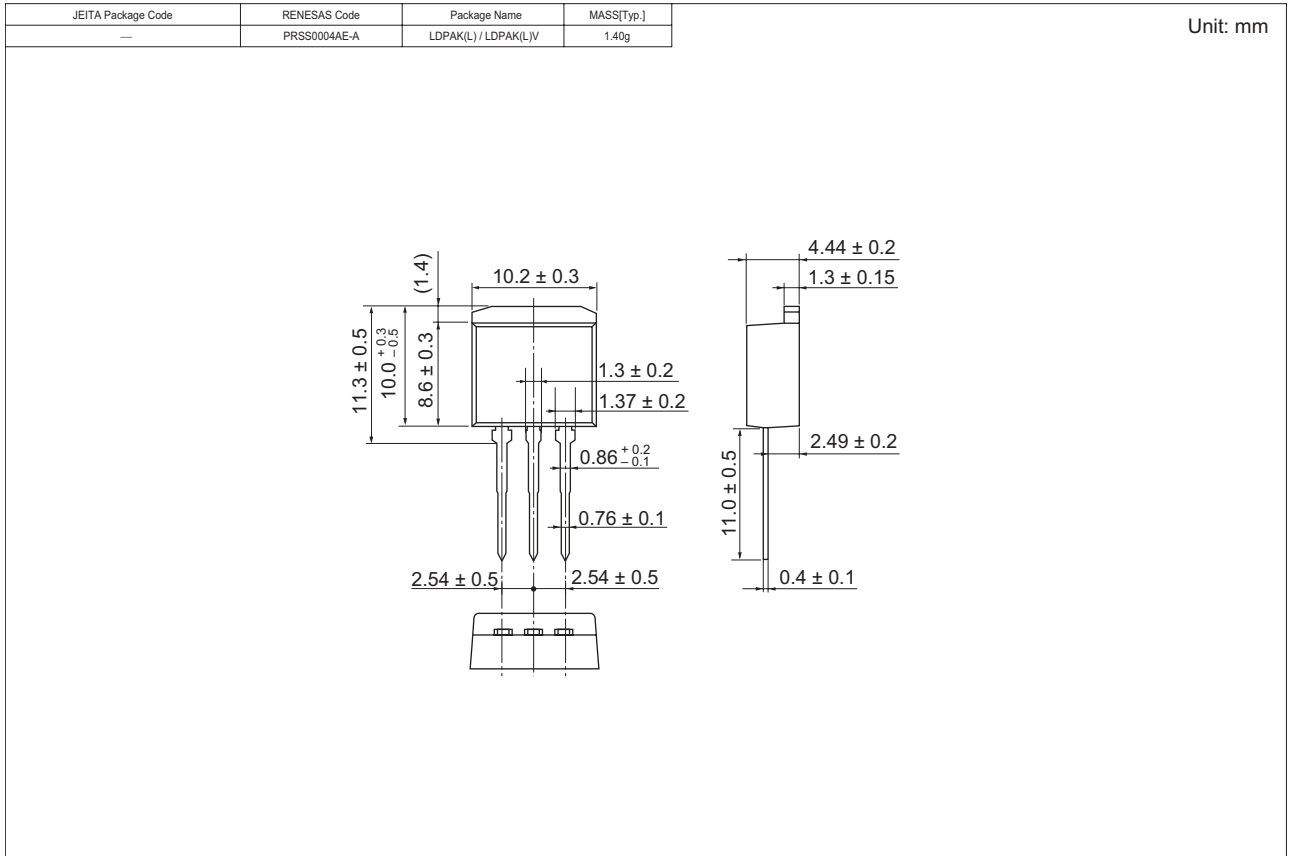
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$





Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SJ550L-E	500 pcs	Box (Sack)
2SJ550STL-E	1000 pcs	Taping

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Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510