19-1350 Rev 3; 12/00

EVALUATION KIT AVAILABLE

MAXIM

900MHz Image-Reject Receivers with Transmit Mixer

General Description

The MAX2424/MAX2426 highly integrated front-end ICs provide the lowest cost solution for cordless and ISM-band radios operating in the 900MHz band. Both devices incorporate a receive image-reject mixer (to reduce filter cost) as well as a versatile transmit mixer. The devices operate from a +2.7V to +4.8V single power supply, allowing direct connection to a 3-cell battery stack.

The receive path incorporates an adjustable-gain LNA and an image-reject downconverter with 35dB image suppression. These features yield excellent combined downconverter noise figure (4dB) and high linearity with an input third-order intercept point (IIP3) of up to +2dBm.

The transmitter consists of a double-balanced mixer and a power amplifier (PA) predriver that produces up to 0dBm (in some applications serving as the final power stage). It can be used in a variety of configurations, including BPSK modulation, direct VCO modulation, and transmitter upconversion. For devices featuring transmit as well as receive image rejection, refer to the MAX2420/MAX2421/MAX2422/MAX2460/MAX2463 data sheet.

The MAX2424/MAX2426 have an on-chip local oscillator (LO), requiring only an external varactor-tuned LC tank for operation. The integrated divide-by-64/65 dual-modulus prescaler can also be set to a direct mode, in which it acts as an LO buffer amplifier. Four separate power-down inputs can be used for system power management, including a 0.5µA shutdown mode.

The MAX2424/MAX2426 come in a 28-pin SSOP package.

Applications

Cordless Phones

Wireless Telemetry

Wireless Networks

Spread-Spectrum Communications

Two-Way Paging

Functional Diagram appears at end of data sheet.

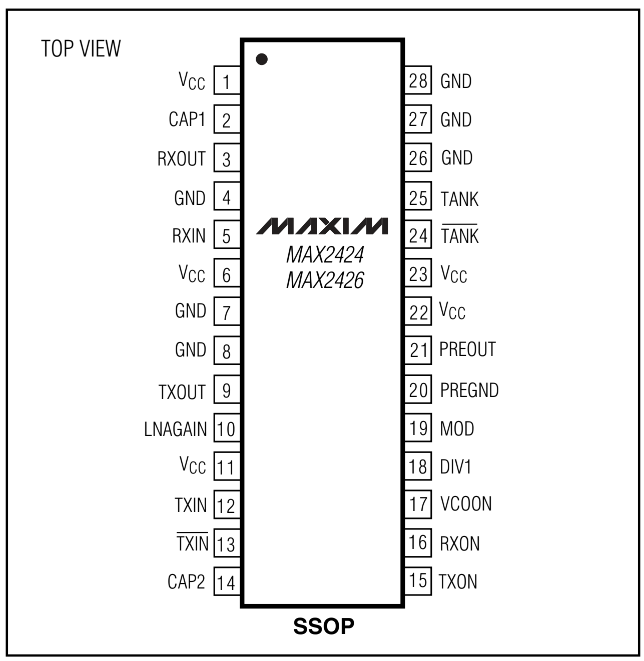
Features

- ♦ **Receive Mixer with 35dB Image Rejection**
- ♦ **Adjustable-Gain LNA**
- ♦ **Up to +2dBm Combined Receiver Input IP3**
- ♦ **4dB Combined Receiver Noise Figure**
- ♦ **Optimized for Common Receiver IF Frequencies:**
  10.7MHz (MAX2424)
  70MHz (MAX2426)
- ♦ **PA Predriver Provides up to 0dBm**
- ♦ **Low Current Consumption: 23mA Receive**
  20mA Transmit
  9.5mA Oscillator
- ♦ **0.5µA Shutdown Mode**
- ♦ **Operates from Single +2.7V to +4.8V Supply**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2424EAI	-40°C to +85°C	28 SSOP
MAX2426EAI	-40°C to +85°C	28 SSOP

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +5.5V
TXIN, $\overline{TXIN}$ Differential Voltage ....+2V
Voltage on TXOUT.....................................-0.3V to (V_{CC} + 1.0V)
Voltage on LNAGAIN, TXON, RXON, VCOON,
DIV1, MOD, TXIN, $\overline{TXIN}$...........................-0.3V to (V_{CC} + 0.3V)
RXIN Input Power..10dBm
TANK, $\overline{TANK}$ Input Power..2dBm
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 9.50mW/°C above +70°C) 762mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +165°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +4.8V, no RF signals applied, LNAGAIN = Unconnected, V_{TXIN} = $V_{\overline{TXIN}}$ = 2.3V, V_{VCOON} = 2.4V, V_{RXON} = V_{TXON} = V_{MOD} = V_{DIV1} = 0.45V, PREGND = GND, T_A = -40°C to +85°C. Typicals are at T_A = +25°C, V_{CC} = 3.3V, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply-Voltage Range			2.7		4.8	V
Oscillator Supply Current	PREGND = unconnected			9.5	14	mA
Prescaler Supply Current (÷ 64/65 mode) (Note 2)				4.2	6	mA
Prescaler Supply Current (buffer mode) (Note 3)	V_{DIV1} = 2.4V			5.4	8.5	mA
Receive Supply Current (Note 4)	V_{RXON} = 2.4V, PREGND = unconnected			23	36	mA
Transmitter Supply Current (Note 5)	V_{RXON} = 0.45V, V_{TXON} = 2.4V, PREGND = unconnected			20	32	mA
Shutdown Supply Current	VCOON = RXON = TXON = MOD = DIV1 = GND	T_A = +25°C		0.5		µA
		T_A = -40°C to +85°C			10	
Digital Input Voltage High	RXON, TXON, DIV1, VCOON, MOD		2.4			V
Digital Input Voltage Low	RXON, TXON, DIV1, VCOON, MOD				0.45	V
Digital Input Current	Voltage on any one digital input = V_{CC} or GND			±1	±10	µA

Note 1: ≥25°C guaranteed by production test, <25°C guaranteed through correlation to worst-case temperature testing.
Note 2: Calculated by measuring the combined oscillator and prescaler supply current and subtracting the oscillator supply current.
Note 3: Calculated by measuring the combined oscillator and LO buffer supply current and subtracting the oscillator supply current.
Note 4: Calculated by measuring the combined receive and oscillator supply current and subtracting the oscillator supply current. With LNAGAIN = GND, the supply current drops by 4.5mA.
Note 5: Calculated by measuring the combined transmit and oscillator supply current and subtracting the oscillator supply current.

AC ELECTRICAL CHARACTERISTICS

(MAX2424/MAX2426 EV kit, V_{CC} = +3.3V, f_{RXIN} = 915MHz, P_{RXIN} = -35dBm, V_{TXIN} = $V_{\overline{TXIN}}$ = 2.3V (DC bias), V_{TXIN} = 250mVp-p, f_{TXIN} = 1MHz, $V_{LNAGAIN}$ = 2V, V_{VCOON} = 2.4V, RXON = TXON = MOD = DIV1 = PREGND = GND, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER (V_{RXON} = 2.4V, f_{LO} = 925.7MHz (MAX2424), f_{LO} = 985MHz (MAX2426))						
Input Frequency Range	(Notes 6, 7)		800		1000	MHz
IF Frequency Range	MAX2424 (Notes 6, 7)		8.5	10.7	12.5	MHz
	MAX2426 (Notes 6, 7)		55	70	85	
Image Frequency Rejection			26	35		dB
Conversion Power Gain	$V_{LNAGAIN}$ = V_{CC}, T_A = +25°C (Note 8)	MAX2424	20	22	24.5	dB
		MAX2426	19	21	23.5	
	$V_{LNAGAIN}$ = V_{CC}, T_A = -40°C to +85°C (Notes 6, 8)	MAX2424	19		25	
		MAX2426	18		24	
	$V_{LNAGAIN}$ = 1V (Note 8)			12		
	LNAGAIN = GND (Note 8)			-16		
Noise Figure	LNAGAIN = V_{CC} (Notes 6, 8)			4	5	dB
	$V_{LNAGAIN}$ = 1V (Notes 6, 8)			12		
Input Third-Order Intercept (IIP3)	LNAGAIN = V_{CC} (Notes 6, 9)		-19	-17		dB
	$V_{LNAGAIN}$ = 1V (Notes 6, 9)			-8		
Input 1dB Compression	LNAGAIN = V_{CC}			-26		dBm
	$V_{LNAGAIN}$ = 1V			-18		
LO to RXIN Leakage	Receiver on or off			-60		dBm
Receiver Turn-On Time	(Note 10)			500		ns
TRANSMITTER (V_{TXON} = 2.4V, f_{LO} = 915MHz)						
Output Frequency Range	(Notes 6, 11)		800		1000	MHz
Baseband 3dB Bandwidth				125		MHz
Output Power	T_A = +25°C		-9.5	-7	-5	dBm
	T_A = T_{MIN} to T_{MAX} (Note 6)		-10		-4.5	
Output 1dB Compression				-0.5		dBm
Output Third-Order Intercept (OIP3)	(Note 12)			3.5		dBm
Carrier Suppression				30		dBc
Output Noise Density				-140		dBm/Hz
Transmitter Turn-On Time	(Note 13)			220		ns

900MHz Image-Reject Receiver with Transmit Mixer

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2424/MAX2426 EV kit, V_{CC} = +3.3V, f_{RXIN} = 915MHz, P_{RXIN} = -35dBm, V_{TXIN} = $V_{\overline{TXIN}}$ = 2.3V (DC bias), V_{TXIN} = 250mVp-p, f_{TXIN} = 1MHz, $V_{LNAGAIN}$ = 2V, V_{VCOON} = 2.4V, RXON = TXON = MOD = DIV1 = PREGND = GND, T_A = +25°C, unless otherwise noted.)

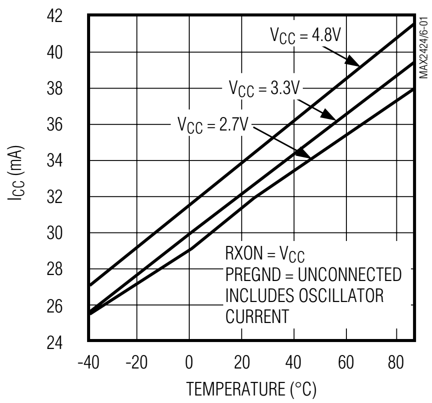
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OSCILLATOR AND PRESCALER						
Oscillator Frequency Range	(Note 6)		800		1100	MHz
Oscillator Phase Noise	10kHz offset (Note 14)	MAX2424		82		dBc/Hz
		MAX2426		72		
Oscillator Pulling	Standby to TX or Standby to RX	MAX2424		8		kHz
		MAX2426		35		
	RX to TX with P_{RXIN} = -45dBm (RX mode) to P_{RXIN} = 0dBm (TX mode) (Note 15)	MAX2424		70		
		MAX2426		110		
Prescaler Output Level	Z_L = 100kΩ ‖ 10pF			500		mVp-p
Oscillator Buffer Output Level (Notes 6, 14)	V_{DIV1} = 2.4V, Z_L = 50Ω	T_A = +25°C	-11	-8		dBm
		T_A = -40°C to +85°C	-12			
Required Modulus Setup Time (Notes 6, 16)	÷ 64/65 mode		10			ns
Required Modulus Hold Time (Notes 6, 16)	÷ 64/65 mode		0			ns

Note 6: Guaranteed by design and characterization.
Note 7: Image rejection typically falls to 30dBc at the frequency extremes.
Note 8: Refer to the *Typical Operating Characteristics* for a plot showing Receiver Gain vs. LNAGAIN Voltage, Input IP3 vs. LNAGAIN Voltage, and Noise Figure vs. LNAGAIN Voltage.
Note 9: Two tones at P_{RXIN} = -45dBm each, f1 = 915.0MHz and f2 = 915.2MHz.
Note 10: Time delay from V_{RXON} = 0.45V to V_{RXON} = 2.4V transition to the time the output envelope reaches 90% of its final value.
Note 11: Output power typically falls to -10dBm at the frequency extremes.
Note 12: Two tones at V_{TXIN} = 125mVp-p, f1 = 1.0MHz, and f2 = 1.2MHz.
Note 13: Time delay from V_{TXON} = 0.45V to V_{TXON} = 2.4V transition to the time the output envelope reaches 90% of its final value.
Note 14: Using tank components L3 = 5.0nH (Coilcraft A02T), C2 = C3 = C26 = 3.3pF, R6 = R7 = 10Ω.
Note 15: This approximates a typical application in which TXOUT is followed by an external PA and a T/R switch with finite isolation.
Note 16: Relative to the rising edge of PREOUT.

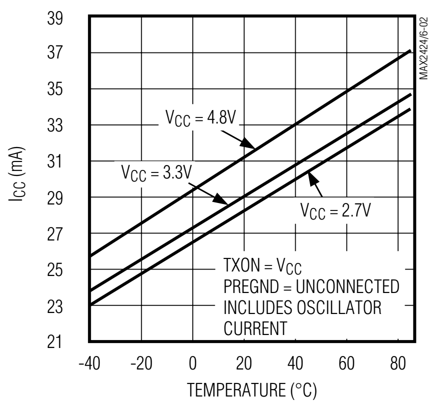
Typical Operating Characteristics

(MAX2424/MAX2426 EV kit, V_{CC} = +3.3V; $f_{LO(RX)}$ = 925.7MHz (MAX2424), 985MHz (MAX2426); f_{RXIN} = 915MHz, P_{RXIN} = -35dBm, $f_{LO(TX)}$ = 915MHz, $V_{TXIN} = V_{\overline{TXIN}}$ = 2.3V (DC bias), V_{TXIN} = 250mVp-p, f_{TXIN} = 1MHz, $V_{LNAGAIN}$ = 2V, V_{VCOON} = 2.4V, RXON = TXON = MOD = DIV1 = PREGND = GND, T_A = +25°C, unless otherwise noted.)

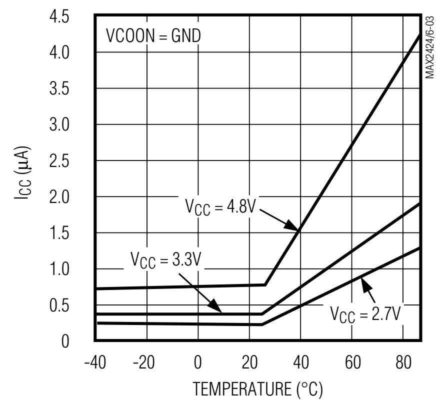
RECEIVER SUPPLY CURRENT vs. TEMPERATURE



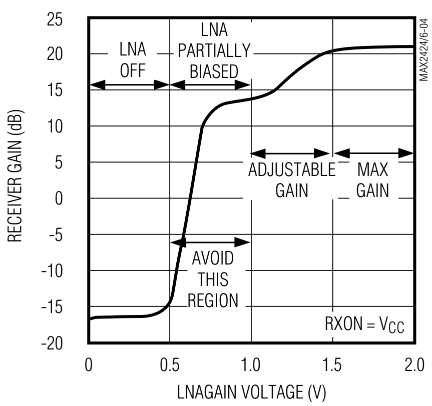
TRANSMITTER SUPPLY CURRENT vs. TEMPERATURE



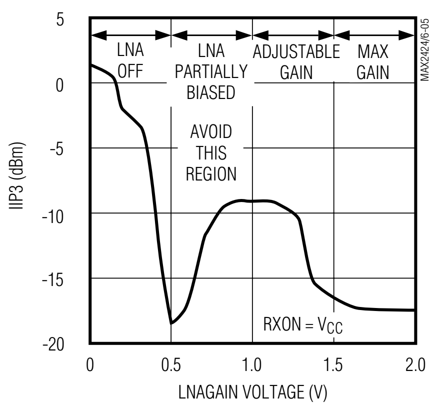
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



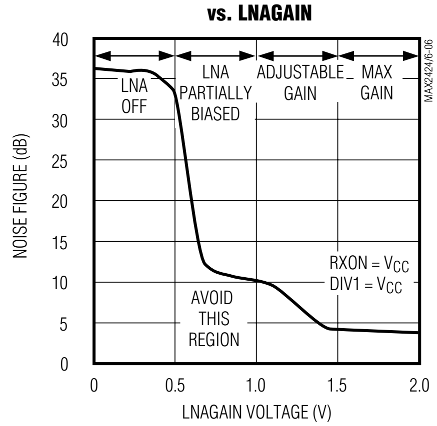
RECEIVER GAIN vs. LNAGAIN



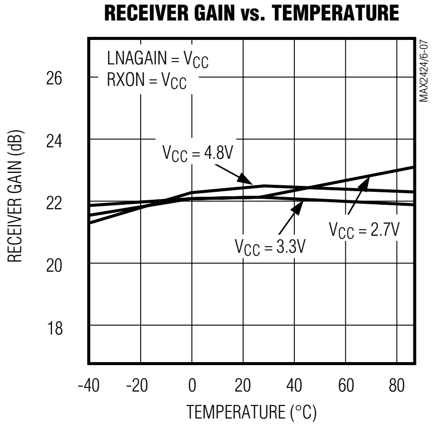
RECEIVER INPUT IP3 vs. LNAGAIN



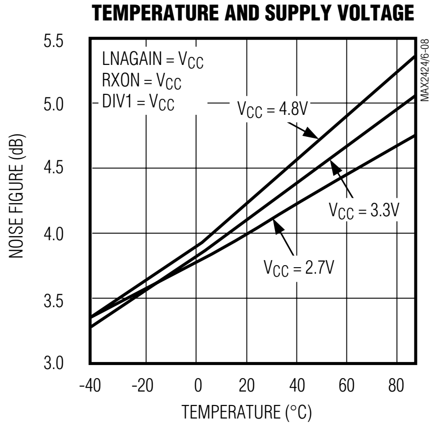
RECEIVER NOISE FIGURE vs. LNAGAIN



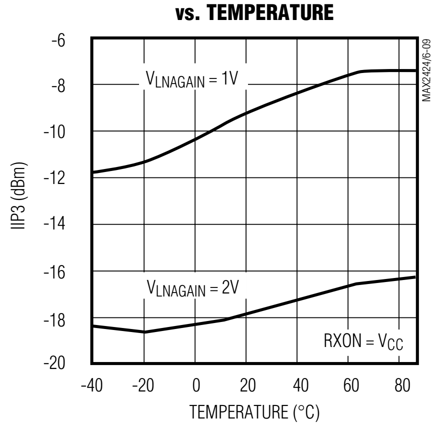
MAX2424 RECEIVER GAIN vs. TEMPERATURE



RECEIVER NOISE FIGURE vs. TEMPERATURE AND SUPPLY VOLTAGE



RECEIVER INPUT IP3 vs. TEMPERATURE

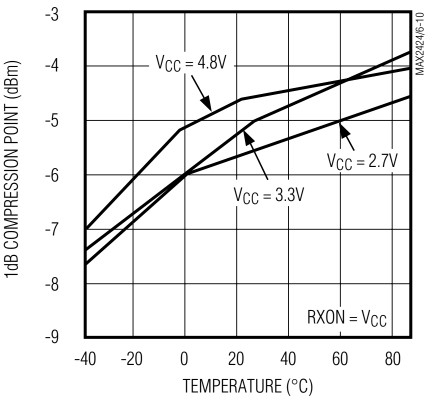


900MHz Image-Reject Receiver with Transmit Mixer

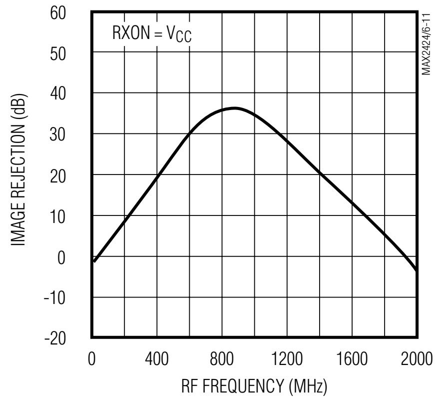
Typical Operating Characteristics (continued)

(MAX2424/MAX2426 EV kit, V_{CC} = +3.3V; $f_{LO(RX)}$ = 925.7MHz (MAX2424), 985MHz (MAX2426); f_{RXIN} = 915MHz, P_{RXIN} = -35dBm, $f_{LO(TX)}$ = 915MHz, V_{TXIN} = $V_{\overline{TXIN}}$ = 2.3V (DC bias), V_{TXIN} = 250mVp-p, f_{TXIN} = 1MHz, $V_{LNAGAIN}$ = 2V, V_{VCOON} = 2.4V, RXON = TXON = MOD = DIV1 = PREGND = GND, T_A = +25°C, unless otherwise noted.)

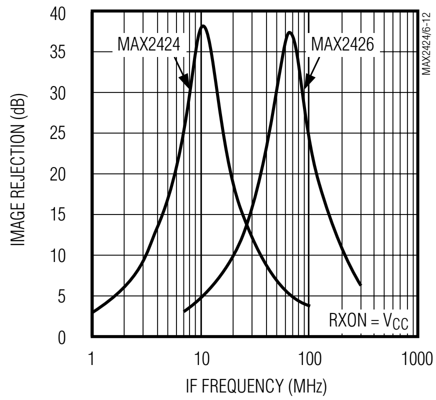
MAX2424 RECEIVER OUTPUT 1dB COMPRESSION POINT vs. TEMPERATURE



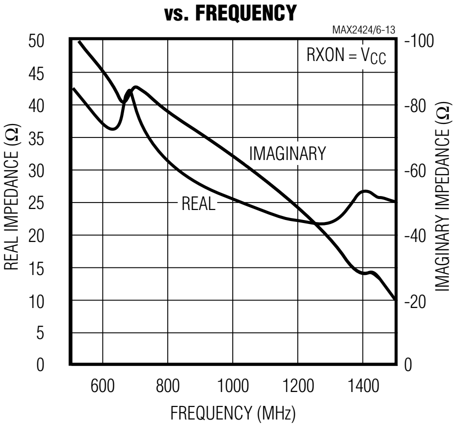
RECEIVER IMAGE REJECTION vs. RF FREQUENCY



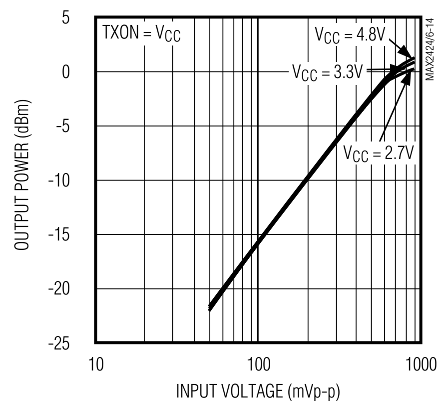
RECEIVER IMAGE REJECTION vs. IF FREQUENCY



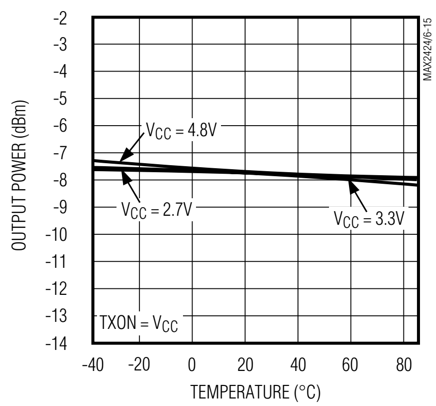
RXIN INPUT IMPEDANCE vs. FREQUENCY



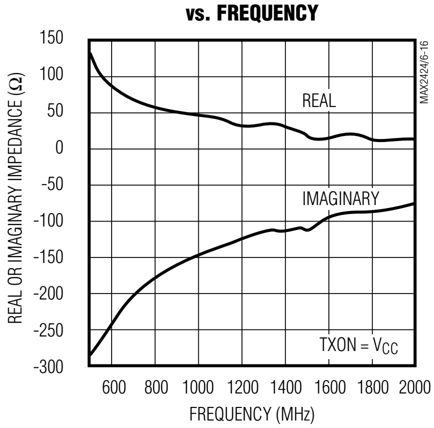
TRANSMITTER OUTPUT POWER vs. INPUT VOLTAGE



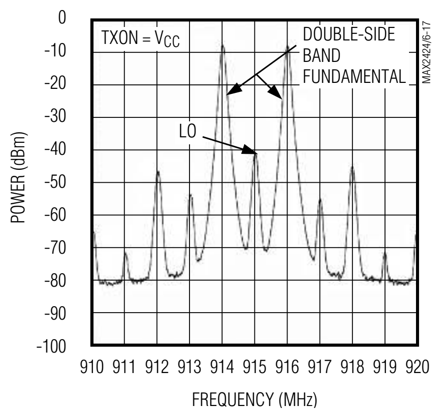
TRANSMITTER OUTPUT POWER vs. TEMPERATURE



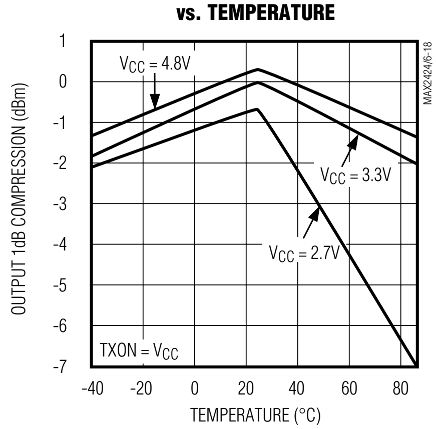
TXOUT OUTPUT IMPEDANCE vs. FREQUENCY



TRANSMITTER OUTPUT SPECTRUM

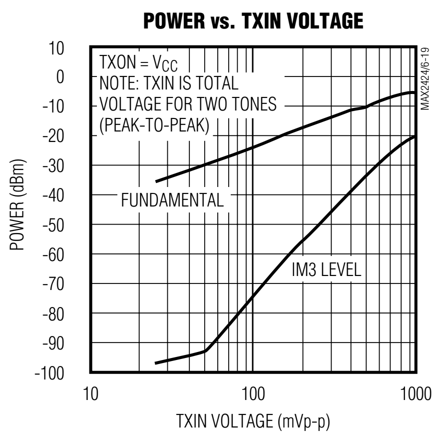


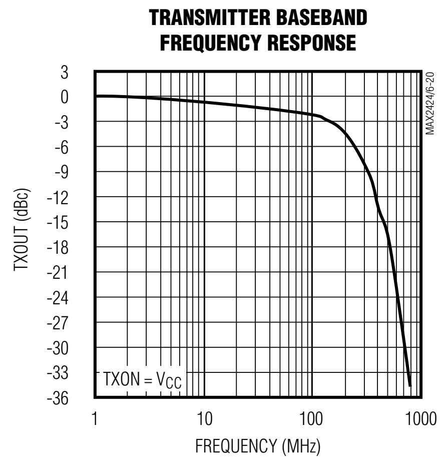
TRANSMITTER 1dB COMPRESSION POINT vs. TEMPERATURE



Typical Operating Characteristics (continued)

(MAX2424/MAX2426 EV kit, V_{CC} = +3.3V; $f_{LO(RX)}$ = 925.7MHz (MAX2424), 985MHz (MAX2426); f_{RXIN} = 915MHz, P_{RXIN} = -35dBm, $f_{LO(TX)}$ = 915MHz, $V_{TXIN} = V_{\overline{TXIN}}$ = 2.3V (DC bias), V_{TXIN} = 250mVp-p, f_{TXIN} = 1MHz, $V_{LNAGAIN}$ = 2V, V_{VCOON} = 2.4V, RXON = TXON = MOD = DIV1 = PREGND = GND, T_A = +25°C, unless otherwise noted.)



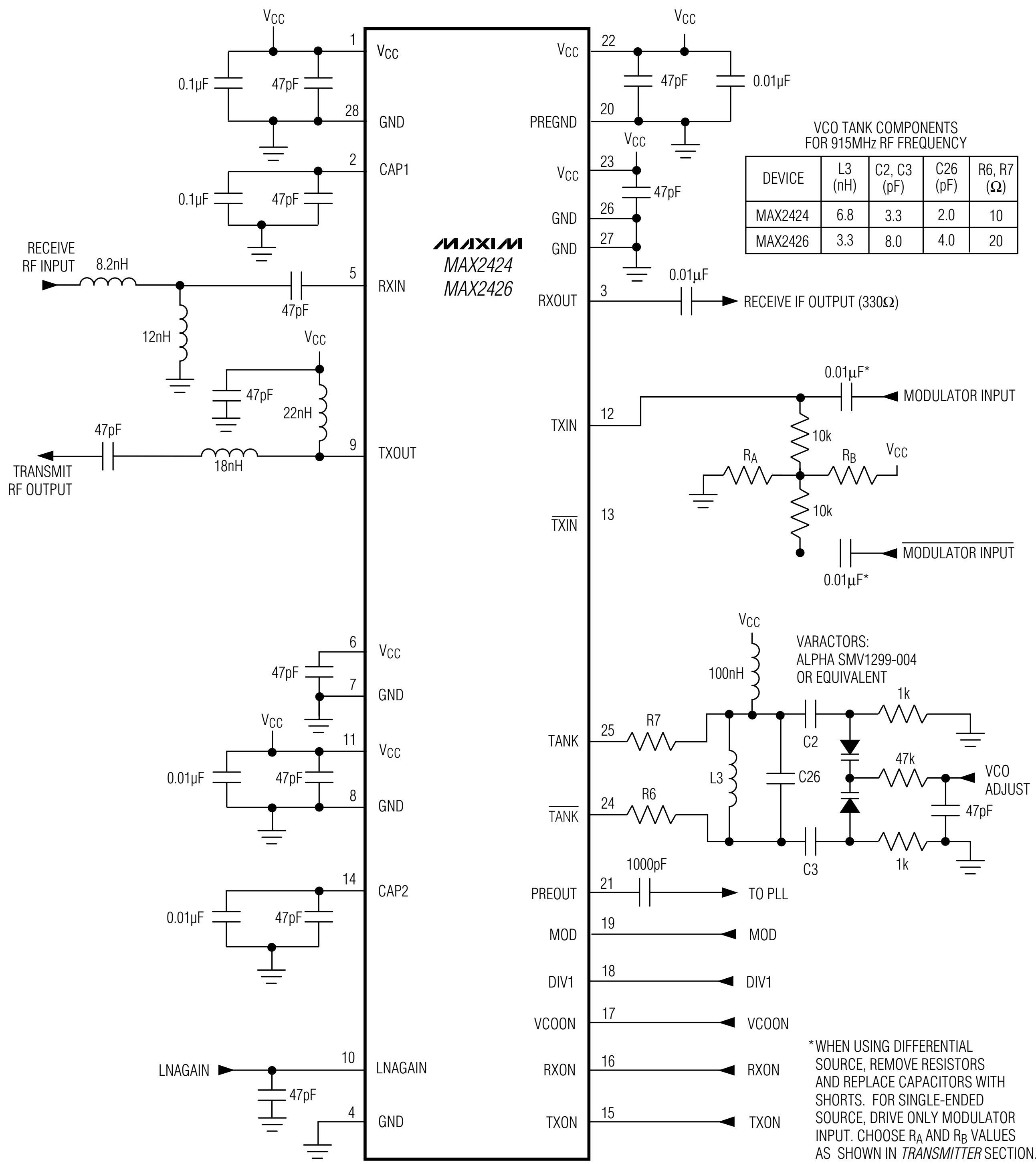


Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Supply-Voltage Input for Master Bias Cell. Bypass with a 47pF low-inductance capacitor and 0.1µF to GND (pin 28 recommended).
2	CAP1	Receive Bias Compensation Pin. Bypass with a 47pF low-inductance capacitor and 0.01µF to GND. Do not make any other connections to this pin.
3	RXOUT	Single-ended, 330Ω IF Output. AC couple to this pin.
4	GND	Ground Connection
5	RXIN	Receiver RF Input, single ended. The input match shown in Figure 1 maintains an input VSWR of better than 2:1 from 902MHz to 928MHz.
6	V_{CC}	Supply Voltage Input for the Receive Low-Noise Amplifier. Bypass with a 47pF low-inductance capacitor to GND (pin 7 recommended).
7	GND	Ground Connection for Receive Low-Noise Amplifier. Connect directly to ground plane using multiple vias.
8	GND	Ground Connection for Signal-Path Blocks, except LNA
9	TXOUT	PA Predriver Output. See Figure 1 for an example matching network, which provides better than 2:1 VSWR from 902MHz to 928MHz.
10	LNAGAIN	Low-Noise Amplifier Gain-Control Input. Drive this pin high for maximum gain. When LNAGAIN is pulled low, the LNA is capacitively bypassed and the supply current is reduced by 4.5mA. This pin can also be driven with an analog voltage to adjust the LNA gain in intermediate states. Refer to the Receiver Gain vs. LNAGAIN Voltage graph in the *Typical Operating Characteristics,* as well as Table 1.
11	V_{CC}	Supply Voltage Input for the Signal-Path Blocks, except LNA. Bypass with a 47pF low-inductance capacitor and 0.01µF to GND (pin 8 recommended).

Pin Description (continued)

PIN	NAME	FUNCTION
12	TXIN	Transmit Mixer's Noninverting Baseband/IF Input. TXIN, $\overline{TXIN}$ form a high-impedance, differential input port. See Figure 1.
13	$\overline{TXIN}$	Transmit Mixer's Inverting Baseband/IF Input. TXIN, $\overline{TXIN}$ form a high-impedance, differential input port. See Figure 1.
14	CAP2	Transmit Bias Compensation Input. Bypass with a 47pF low-inductance capacitor and 0.01µF to GND. Do not make any other connections to this pin.
15	TXON	Drive TXON and VCOON with a logic high to enable the transmit IF variable-gain amplifier, upconverter mixer, and PA predriver. See *Power Management* section.
16	RXON	Drive RXON and VCOON with a logic high to enable the LNA, receive mixer, and IF output buffer. See *Power Management* section.
17	VCOON	Drive VCOON with a logic high to turn on the VCO, phase shifters, VCO buffers, and prescaler. To disable the prescaler, leave the PREGND pin unconnected.
18	DIV1	Drive DIV1 with a logic high to disable the divide-by-64/65 prescaler and connect the PREOUT pin directly to an oscillator buffer amplifier, which outputs -8dBm into a 50Ω load. Drive DIV1 low for divide-by-64/65 operation. Drive this pin low when in shutdown to minimize shutdown current.
19	MOD	Modulus Control for the Divide-by-64/65 Prescaler. Drive MOD high for divide-by-64 mode. Drive MOD low for divide-by-65 mode.
20	PREGND	Ground connection for the Prescaler. Connect PREGND to ground for normal operation. Leave unconnected to disable the prescaler and the output buffer. Connect MOD and DIV1 to ground and leave PREOUT unconnected when disabling the prescaler.
21	PREOUT	Prescaler/Oscillator Buffer Output. In divide-by-64/65 mode (DIV1 = low), the output level is 500mVp-p into a high-impedance load. In divide-by-1 mode (DIV1 = high), this output delivers -8dBm into a 50Ω load. AC couple to this pin.
22	V_{CC}	Supply-Voltage Input for Prescaler. Bypass with a 47pF low-inductance capacitor and 0.01µF to GND (pin 20 recommended).
23	V_{CC}	Supply-Voltage Input for VCO and Phase Shifters. Bypass with a 47pF low-inductance capacitor to GND (pin 26 recommended).
24	$\overline{TANK}$	Differential Oscillator Tank Port. See *Applications Information* for information on tank circuits or on using an external oscillator.
25	TANK	Differential Oscillator Tank Port. See *Applications Information* for information on tank circuits or on using an external oscillator.
26	GND	Ground Connection for VCO and Phase Shifters
27	GND	Ground (substrate)
28	GND	Ground Connection for Master Bias Cell



VCO TANK COMPONENTS
FOR 915MHz RF FREQUENCY

DEVICE	L3 (nH)	C2, C3 (pF)	C26 (pF)	R6, R7 (Ω)
MAX2424	6.8	3.3	2.0	10
MAX2426	3.3	8.0	4.0	20

*WHEN USING DIFFERENTIAL SOURCE, REMOVE RESISTORS AND REPLACE CAPACITORS WITH SHORTS. FOR SINGLE-ENDED SOURCE, DRIVE ONLY MODULATOR INPUT. CHOOSE R_A AND R_B VALUES AS SHOWN IN *TRANSMITTER* SECTION.

Figure 1. Typical Operating Circuit

Detailed Description

The following sections describe each of the functional blocks shown in the *Functional Diagram.*

Receiver

The MAX2424/MAX2426's receive path consists of a 900MHz low-noise amplifier, an image-reject mixer, and an IF buffer amplifier.

The LNA's gain and biasing are adjustable via the LNAGAIN pin. Proper operation of this pin provides optimum performance over a wide range of signal levels. The LNA has four modes determined by the DC voltage applied on the LNAGAIN pin. See Table 1, as well as the relevant *Typical Operating Characteristics* plots.

At low LNAGAIN voltages, the LNA is shut off and the input signal capacitively couples directly into mixer to provide maximum linearity for large-signal operation (receiver close to transmitter). As the LNAGAIN voltage increases, the LNA turns on. Between 0.5V and 1V at LNAGAIN, the LNA is partially biased and behaves like a Class C amplifier. Avoid this operating mode for applications where linearity is a concern. As the LNAGAIN voltage reaches 1V, the LNA is fully biased into Class A mode, and the gain is monotonically adjustable for LNAGAIN voltages above 1V. See the receiver gain, IP3, and Noise Figure vs. LNAGAIN plots in the *Typical Operating Characteristics* for more information.

The downconverter is implemented using an image-reject mixer consisting of an input buffer with two outputs, each of which is fed to a double-balanced mixer. A quadrature LO drives the local-oscillator (LO) port of each mixer. An on-chip oscillator and an external tank circuit generates the LO. Its signal is buffered and split into two phase shifters, which provide 90° of phase shift across their outputs. This pair of LO signals is fed to the mixers. The mixers' outputs then pass through a second pair of phase shifters, which provide a 90° phase shift across their outputs. The resulting mixer outputs are then summed together. The final phase relationship is such that the desired signal is reinforced and the image signal is canceled. The downconverter mixer output appears on the RXOUT pin, a single-ended 330Ω output.

Table 1. LNA Modes

LNAGAIN VOLTAGE (V)	MODE
$0 < V_{LNAGAIN} \le 0.5$	LNA capacitively bypassed, minimum gain, maximum IP3
$0.5 < V_{LNAGAIN} < 1.0$	LNA partially biased. **Avoid this mode**— the LNA operates in a Class C manner
$1.0 < V_{LNAGAIN} \le 1.5$	LNA gain is monotonically adjustable
$1.5 < V_{LNAGAIN} \le V_{CC}$	LNA at maximum gain (remains monotonic)

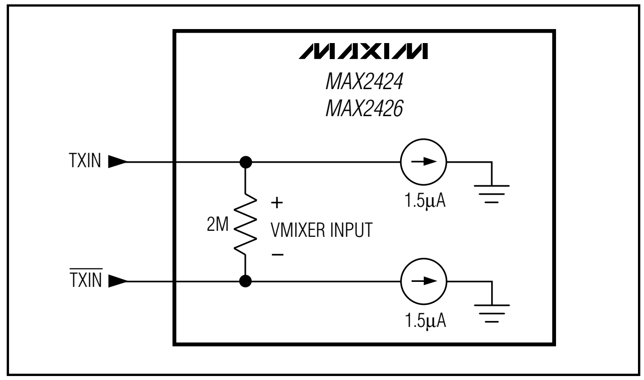


Figure 2. TXIN, $\overline{TXIN}$ Equivalent Circuit

Transmitter

The MAX2424/MAX2426 transmitter consists of a balanced mixer and a PA driver amplifier. The mixer inputs are accessible via the TXIN and $\overline{TXIN}$ pins. An equivalent circuit for the TXIN and $\overline{TXIN}$ pins is shown in Figure 2. Because TXIN and $\overline{TXIN}$ are linearly coupled to the mixer stage, they can accept spectrally shaped input signals. Typically, the mixer can be used to multiply the LO with a baseband signal, generating BPSK or ASK modulation. Transmit upconversion can also be implemented by applying a modulated IF signal to these inputs. For applications requiring image rejection on the transmitter, refer to the MAX2420/MAX2421/MAX2422/MAX2460/MAX2463 data sheet.

Set the common-mode voltage at TXIN, $\overline{TXIN}$ to 2.3V by selecting appropriate values for R_A and R_B (Figure 1). The total series impedance of R_A and R_B should be approximately 100kΩ.

Frequency modulation (FM) is realized by modulating the VCO tuning voltage. Apply the appropriate differential and common-mode voltages to TXIN and $\overline{TXIN}$ to control transmitter output power (Figure 3).

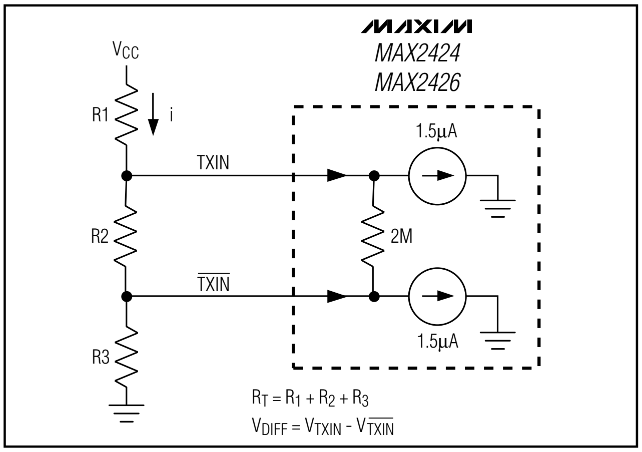


Figure 3. Biasing TXIN and $\overline{TXIN}$ for FM

For example, if V_{CC} = 3.3V and P_{OUT} = -8dBm, choose R_T = 100kΩ for sufficient current through the divider, so that bias currents for $\overline{TXIN}$ and TXIN have little effect over temperature. Set $V_{\overline{TXIN}}$ = 2.3V to satisfy common-mode voltage range requirements at V_{CC} = 3.3V.

Use the Transmit Output Power vs. Input Voltage graph in the *Typical Operating Characteristics* to determine the input voltage (in mVp-p) required to produce the desired output. Divide this value by $2\sqrt{2}$ and use it for V_{DIFF}. A -8dBm transmitter output requires 250mVp-p / $2\sqrt{2}$ = 88.4mV.

$$V_{TXIN} = 2.3V + 0.0884V = 2.3884V$$

$$R_T = R1 + R2 + R3$$

Solve for resistors R1, R2, and R3 with the following equations:

$$R3 = \frac{V_{\overline{TXIN}} \times R_T}{V_{CC}}$$

$$R2 = \left(V_{TXIN} - V_{\overline{TXIN}}\right) \times \frac{R_T}{V_{CC}}$$

$$R1 = R_T - R2 - R3$$

Since the transmit and receive sections typically require different LO frequencies, it is not recommended to have both transmit and receive active at the same time.

Phase Shifter

The MAX2424/MAX2426 uses passive networks to provide quadrature phase shifting for the receive IF and LO signals. Because these networks are frequency selective, both the RF and IF frequency operating ranges are limited. Image rejection degrades as the IF and RF moves away from the designed optimum frequencies. The MAX2424/MAX2426's phase shifters are arranged such that the LO frequency is higher than the RF carrier frequency (high-side injection).

Local Oscillator (LO)

The on-chip LO is formed by an emitter-coupled differential pair. An external LC resonant tank sets the oscillation frequency. A varactor diode is typically used to create a voltage-controlled oscillator (VCO). See the *Applications Information* section for an example VCO tank circuit.

The LO may be overdriven in applications where an external signal is available. The external LO signal should be about 0dBm from 50Ω, and should be AC coupled into either the TANK or $\overline{TANK}$ pin. Both TANK and $\overline{TANK}$ require pull-up resistors to V_{CC}. See the *Applications Information* section for details.

The local oscillator resists pulling caused by changes in load impedance that occur as the part is switched from standby mode, with just the oscillator running to either transmit or receive mode. The amount of LO pulling is affected if a signal is present at the RXIN port in transmit mode. The most common cause of pulling is imperfect isolation in an external transmit/ receive (T/R) switch. The *AC Electrical Characteristics* table contains specifications for this case as well.

Prescaler

The on-chip prescaler operates in two different modes: as a dual-modulus divide-by-64/65, or as an oscillator buffer amplifier. The DIV1 pin controls this function. When DIV1 is low, the prescaler is in dual-modulus divide-by-64/65 mode; when it is high, the prescaler is disabled and the oscillator buffer amplifier is enabled. The buffer typically outputs -8dBm into a 50Ω load. To minimize shutdown supply current, pull the DIV1 pin low when in shutdown mode.

In divide-by-64/65 drive mode, the division ratio is controlled by the MOD pin. Drive MOD high to operate the prescaler in divide-by-64 mode. Drive MOD and DIV1 low to operate the prescaler in divide-by-65 mode.

900MHz Image-Reject Receiver with Transmit Mixer

To disable the prescaler entirely, leave PREGND and PREOUT unconnected. Also connect the MOD and DIV1 pins to GND. Disabling the prescaler does not affect operation of the VCO stage.

Power Management

The MAX2424/MAX2426 supports four different power-management features to conserve battery life. The VCO section has its own control pin (VCOON), which also serves as a master bias pin. When VCOON is high, the LO, quadrature LO phase shifters, and prescaler or LO buffer are all enabled. Stabilize VCO by powering it up prior to transmitting or receiving. For transmit-to-receive switching, the receiver and transmitter sections have their own enable control inputs, RXON and TXON. With VCOON high, bringing RXON high enables the receive path, which consists of the LNA, image-reject mixers, and IF output buffer. When this pin is low, the receive path is inactive. The TXON input enables the upconverter mixer and PA predriver. VCOON must be high for the transmitter to operate. When TXON is low, the transmitter is off.

To disable all chip functions and reduce the supply current to typically 0.5µA, pull VCOON, DIV1, MOD, RXON, and TXON low.

Applications Information

Oscillator Tank

The on-chip oscillator requires a parallel-resonant tank circuit connected across TANK and $\overline{TANK}$. Figure 4 shows an example of an oscillator tank circuit. Inductor L4 provides DC bias to the tank ports. Inductor L3, capacitor C26, and the series combination of capacitors C2, C3, and both halves of the varactor diode capacitance set the resonant frequency as follows:

$$f_r = \frac{1}{\left[2\pi\sqrt{(L3)(C_{EFF})}\right]}$$

$$C_{EFF} = \frac{1}{\left(\frac{1}{C2} + \frac{1}{C3} + \frac{2}{C_{D1}}\right)} + C26$$

where C_{D1} is the capacitance of one varactor diode.

Choose tank components according to your application needs, such as phase-noise requirements, tuning range, and VCO gain. High Q inductors such as air-core micro springs yield low phase noise. Use a low-tolerance inductor (L3) for predictable oscillation frequency. Resistors R6 and R7 can be chosen from 0 to 20Ω to reduce the Q of parasitic resonance due to series package inductance L_T. Keep R6 and R7 as small as possible to minimize phase noise, yet large enough to ensure oscillator start-up in fundamental mode. Oscillator start-up with be most critical with high tuning bandwidth (low tank Q) and high temperature. Capacitors C2 and C3 couple in the varactor. Light coupling of the varactor is a way to reduce the effects of high varactor tolerance and increase loaded Q. For a wider tuning range, use larger values for C2 and C3 or a varactor with a large capacitance ratio. Capacitor C26 is used to trim the tank oscillator frequency. Larger values for C26 will help negate the effect of stray PCB capacitance and parasitic inductor capacitance (L3). Choose a low-tolerance capacitor for C26.

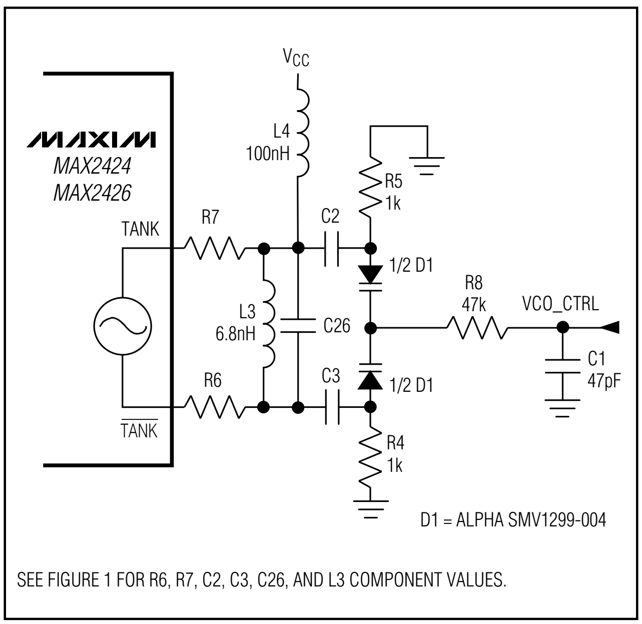


Figure 4. Oscillator Tank Schematic Using the On-Chip VCO

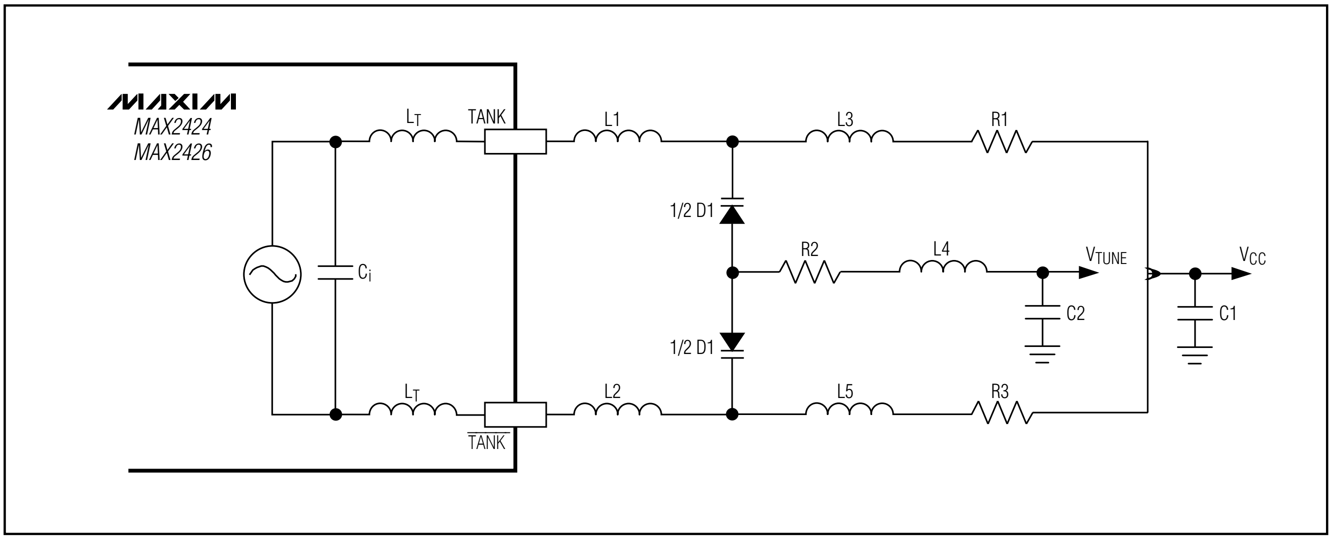


Figure 5. Series-Coupled Resonant Tank for Wide Tuning Range and Low Phase Noise

For applications that require a wide tuning range and low phase noise, a series-coupled resonant tank may be required as shown in Figure 5. This tank will use the package inductance in series with inductors L1, L2, and capacitance of varactor D1 to set the net equivalent inductance which resonates in parallel with the internal oscillator capacitance. Inductors L1 and L2 may be implemented as microstrip inductors, saving component cost. Bias is provided to the tank port through chokes L3 and L5. R1 and R3 should be chosen large enough to de-Q the parasitic resonance due to L3 and L5 but small enough to minimize the voltage drop across them due to bias current. Values for R1 and R3 should be kept between 0 and 50Ω. Proper high frequency bypassing (C1) should be used for the bias voltage to eliminate power supply noise from entering the tank.

Oscillator Tank PC Board Layout

The parasitic PC board capacitance, as well as PCB trace inductance and package inductance, affect oscillation frequency, so be careful in laying out the PC board for the oscillator tank. Keep the tank layout as symmetrical, tightly packed, and close to the device as possible to minimize LO feedthrough. When using a PC board with a ground plane, a cut-out in the ground plane (and any other planes) below the oscillator tank reduces parasitic capacitance.

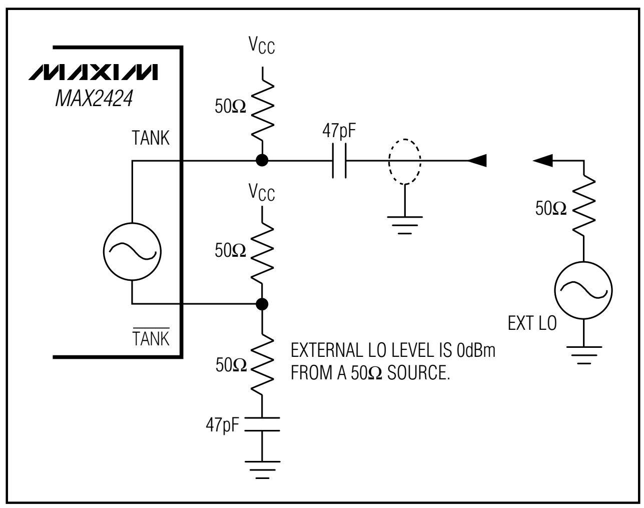


Figure 6. Using an External Local Oscillator

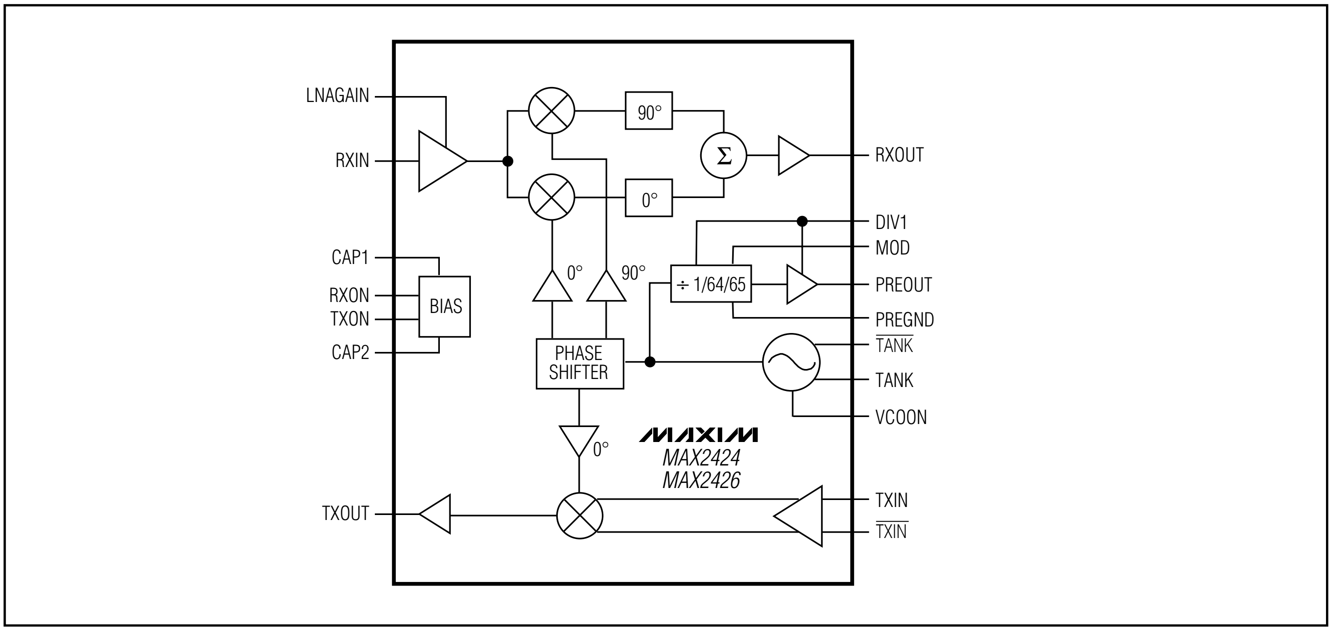
Using an External Oscillator

If an external 50Ω LO signal source is available, it can be used as an input to the TANK or $\overline{\text{TANK}}$ pin in place of the on-chip oscillator (Figure 6). The oscillator signal is AC coupled into the TANK pin and should have a level of about 0dBm from a 50Ω source. For proper biasing of the oscillator input stage, pull up the TANK and $\overline{\text{TANK}}$ pins to the V_{CC} supply via 50Ω resistors.

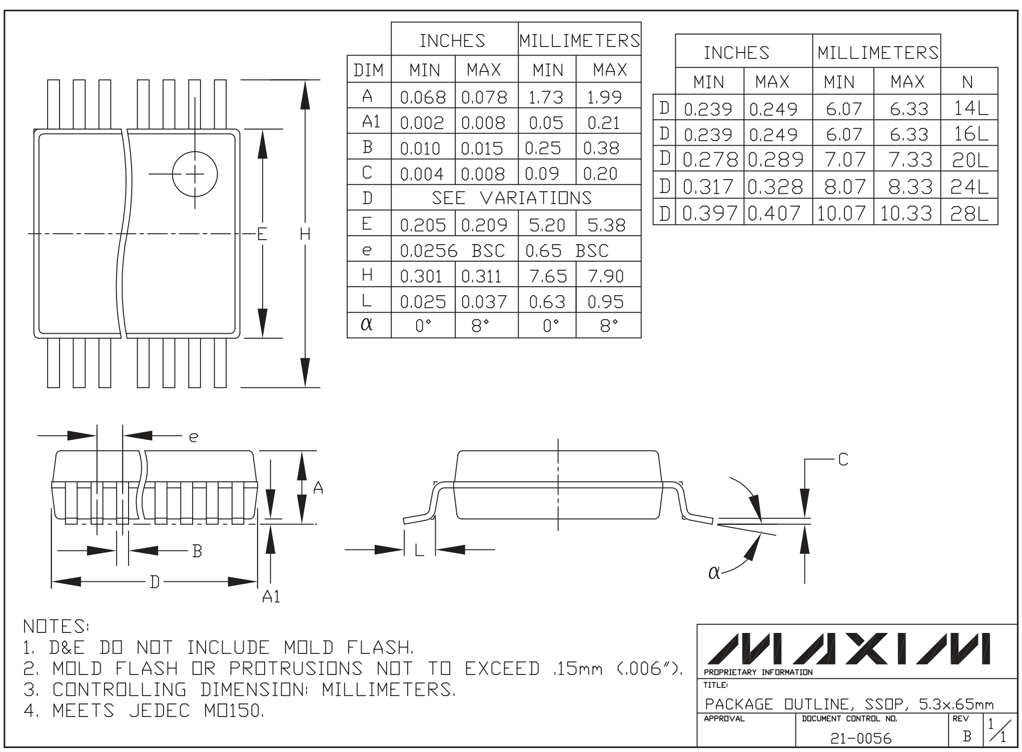
If a differential LO source such as the MAX2620 is available, AC-couple the inverting output into $\overline{\text{TANK}}$.

900MHz Image-Reject Receiver with Transmit Mixer

Functional Diagram



Package Information



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.

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