AK4499
Premium Switched Resistor 4ch DAC

1. General Description

The AK4499 is a 32-bit 4ch Switched Resistor DAC which adopts newly developed technology, achieving the industry's leading level low distortion and low noise characteristics. It corresponds to a 768kHz PCM input and an DSD512 input at maximum, suitable for playback of high resolution audio sources that are becoming widespread in Network Audio and USB-DACs Audio systems. In addition, it is capable of supporting a wide range of signals and achieving low out-of-band noise. The AK4499 has six types of 32-bit digital filters, realizing simple and flexible sound reproduction in wide range of applications.

2. Features

- 4-ch Switched Resistor DAC
- THD+N: -124 dB
- Dynamic Range, S/N: 140 dB (Mono), 137 dB (Stereo), 134 dB (4ch)
- 128x Over Sampling
- Sampling Rate: 8 kHz to 768 kHz
- 32-bit 8x Digital Filter
  - Short Delay Sharp Roll-off, GD = 6.0/fs
  - Short Delay Slow Roll-off, GD = 5.0/fs
  - Sharp Roll-off
  - Slow Roll-off
  - Super Slow Roll-off
  - Low Dispersion Short Delay Filter
- DSD64, DSD128, DSD256, DSD512 Input Support
  - Filter1 (fc = 37 kHz, DSD64 mode)
  - Filter2 (fc = 65 kHz, DSD64 mode)
- Digital De-emphasis for 32, 44.1 and 48kHz sampling
- Soft Mute
- Digital Attenuator (0 dB to -127 dB, 0.5 dB step + mute)
- Mono Mode
- External Digital Filter Interface (EXDF Mode)
- PCM/DSD, EXDF/DSD Mode Automatic Mode Switching Function
- Audio I/F Format
  - MSB Justified
  - LSB Justified
  - I^2S
  - DSD
  - TDM
- Daisy Chain
- Master Clock
  - fs = 8 kHz to 32 kHz : 256fs, 384fs, 512fs, 768fs, 1152fs
  - fs = 32 kHz to 54 kHz : 256fs, 384fs, 512fs, 768fs
  - fs = 54 kHz to 108 kHz : 256fs, 384fs
  - fs = 108 kHz to 216 kHz : 128fs, 192fs
  - fs = 384 kHz : 32fs, 48fs, 64fs, 96fs
  - fs = 768 kHz :16fs, 32fs, 48fs, 64fs
- Register Control Mode with 3-wire Serial or I^2C interface

- Pin Control Mode
- Power Supply:
  Internal LDO (LDOE pin = “H”); TVDD = 3.0 ~ 3.6 V, AVDD = 4.75 ~ 5.25 V,
  VDDL1/R1/L2/R2 = 4.75 ~ 5.25 V
  External Supply (LDOE pin = “L”); TVDD = 1.7 ~ 3.6 V, DVDD = 1.7 to 1.98 V,
  AVDD = 4.75 ~ 5.25 V, VDDL1/R1/L2/R2 = 4.75 ~ 5.25 V
- Operational Temperature: -40 to 85 °C
- Digital Input Level: CMOS
- Package: 128-pin HTQFP

3. Table of Contents

4. Block Diagram and Functions

4.1. Block Diagram

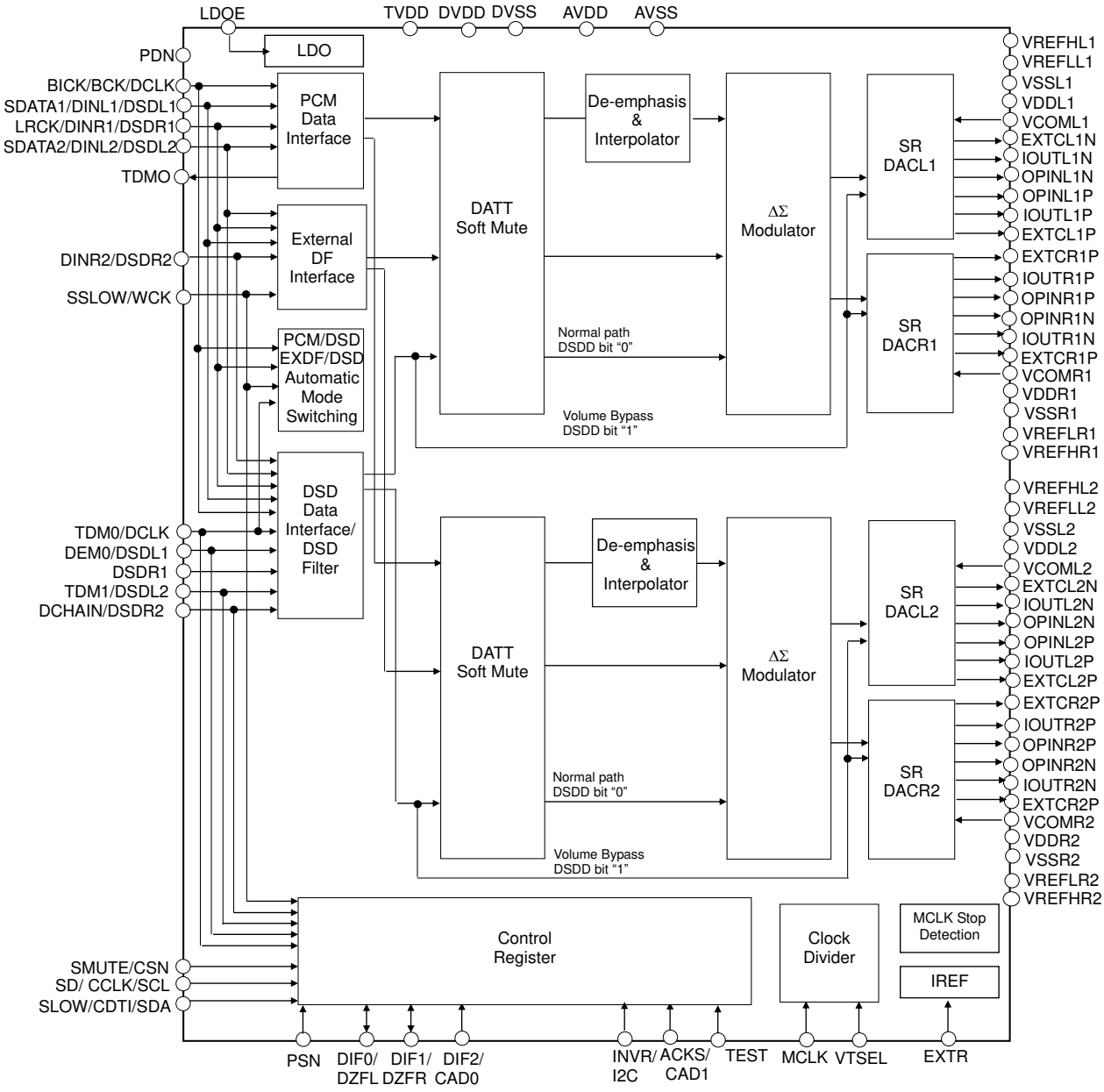


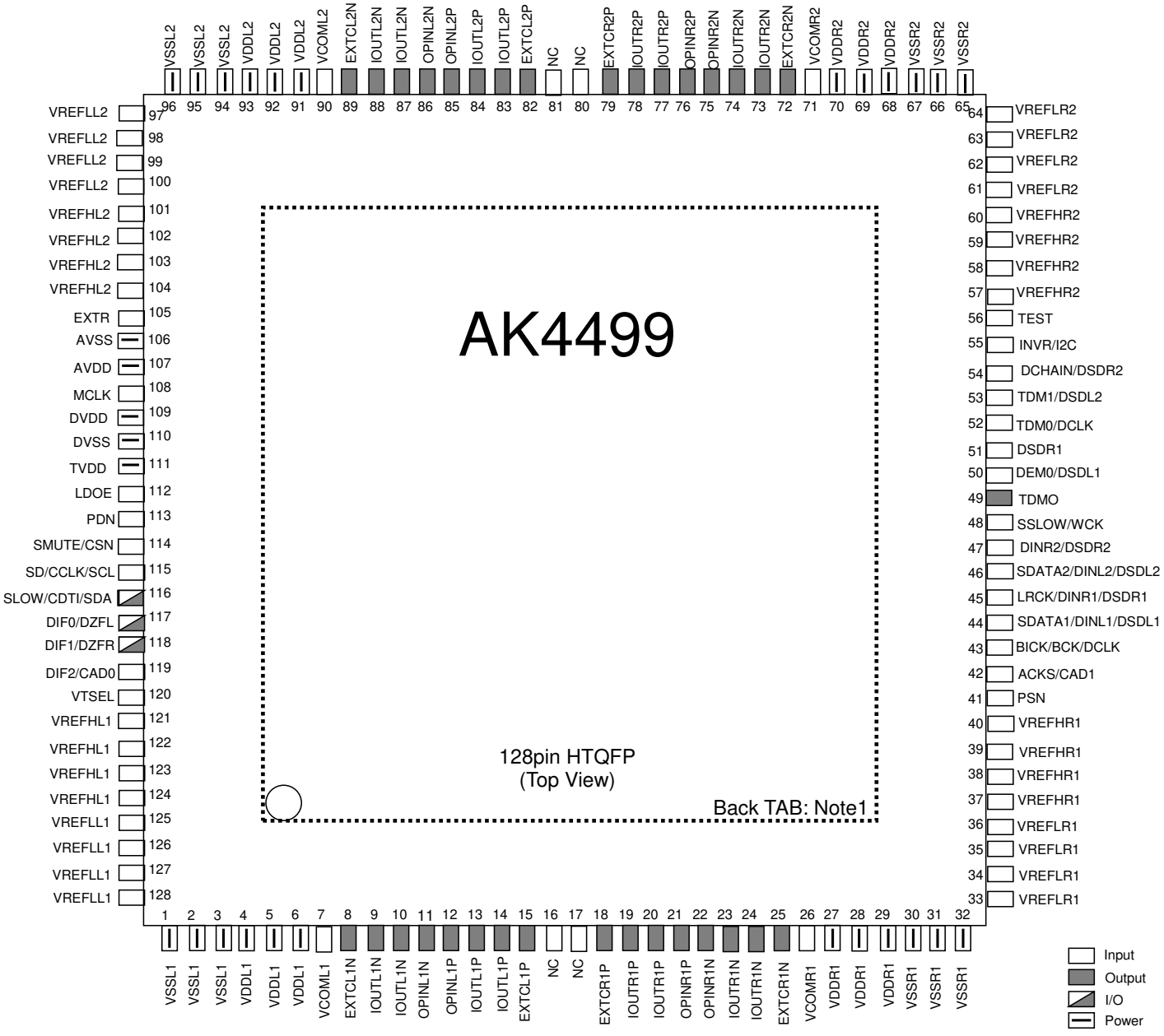
Figure 1. AK4499 Block Diagram

4.2. Functions

Block	Function
PCM Data Interface	Execute serial/parallel conversion of SDATA1/2 input data by synchronizing with LRCK and BICK, and generate TDM output data.
External DF Interface	Receive external digital filter outputs. Execute serial/parallel conversion of DINL1/2 and DINR1/2 input data by synchronizing with BICK.
DSD Data Interface	1-bit data that is input from DSDL1/2 and DSDR1/2 pins is received by synchronizing with DCLK.
DSD Filter	FIR filter that reduces high frequency noise of DSD input data
DATT, Soft Mute	Apply DATT and Soft Mute process to input data.
De-emphasis & Interpolator	A digital filter that applies De-emphasis process to input data and executes over sampling.
ΔΣ Modulator	Output multi-bit data to SR DAC. This block consists of a third-order digital delta-sigma modulator.
SR DAC	Convert multi bit output of ΔΣ Modulator into analog signal. This block consists of a switched resistor DAC.
Control Register	Keep register settings for each mode. Control registers are accessed in 3-wire (CSN, CCLK, CDTI) or I2C-Bus (SCL, SDA) control mode.
Clock Divider	Divide Master Clock In PCM mode, master clock is divided automatically by fs rate auto detection function. In DSD mode, the master clock frequency is set by DCKS bit.
MCLK Stop Detection	Detects when the master clock input is absent.
IREF	Generate reference current from the reference voltage generated internally, using an external resistor.
LDO	Generate power for internal digital circuit (1.8V typ.).

5. Pin Configurations and Functions

5.1. Pin Configurations



Note 1: The exposed pad on the bottom surface of the package should be connected to AVSS.

5.2. Functions

No.	Pin Name	I/O	Function	Power Down State
1-3	VSSL1	-	L1ch Analog Ground pin.	-
4-6	VDDL1	-	L1ch Analog Power Supply pin.	-
7	VCOML1	I	L1ch VCOM pin. VCOML1 is connected to the midpoint of resistors between VREFHL1 and VREFLL1.	Hi-Z
8	EXTCL1N	O	External Capacitor connection pin. This pin should be connected to 1 µF to VSSL1.	Pull-down to VSSL1 (250 kΩ, typ)
9,10	IOUTL1N	O	Current Output pin (L1ch Negative Signal).	Connected to OPINL1N (64 Ω, typ)
11	OPINL1N	O	Common Voltage Input pin (L1ch Negative Signal).	Connected to IOUTL1N (64 Ω, typ)
12	OPINL1P	O	Common Voltage Input pin (L1ch Positive Signal).	Connected to IOUTL1P (64 Ω, typ)
13,14	IOUTL1P	O	Current Output pin (L1ch Positive Signal).	Connected to OPINL1P (64 Ω, typ)
15	EXTCL1P	O	External Capacitor connection pin. This pin should be connected to 1 µF to VSSL1.	Pull-down to VSSL1 (250 kΩ, typ)
16,17	NC	-	No internal bonding. Connect to AVSS.	-
18	EXTCR1P	O	External Capacitor connection pin. This pin should be connected to 1 µF to VSSR1.	Pull-down to VSSR1 (250 kΩ, typ)
19,20	IOUTR1P	O	Current Output pin (R1ch positive signal).	Connected to OPINR1P (64 Ω, typ)
21	OPINR1P	O	Common Voltage input pin (R1ch positive signal).	Connected to IOUTR1P (64 Ω, typ)
22	OPINR1N	O	Common Voltage input pin (R1ch negative signal).	Connected to IOUTR1N (64 Ω, typ)
23,24	IOUTR1N	O	Current Output pin (R1ch negative signal).	Connected to OPINR1N (64 Ω, typ)
25	EXTCR1N	O	External Capacitor connection pin. This pin should be connected to 1 µF to VSSR1.	Pull-down to VSSR1 (250 kΩ, typ)
26	VCOMR1	I	R1ch VCOM pin. VCOMR1 is connected to the midpoint of resistors between VREFHR1 and VREFLR1.	Hi-Z
27-29	VDDR1	-	R1ch Analog Power Supply pin.	-
30-32	VSSR1	-	R1ch Analog Ground pin.	-
33-36	VREFLR1	I	R1ch Low Level Reference Voltage Input pin.	Hi-Z
37-40	VREFHR1	I	R1ch High Level Reference Voltage Input pin.	Hi-Z
41	PSN	I	Control Mode Select pin (Internal pull-up pin) "L": Register Control mode "H": Pin Control mode	Pull-Up to TVDD (100 kΩ, typ)

No.	Pin Name	I/O	Function	Power Down State
42	ACKS	I	Clock Setting Mode Select pin in Pin Control mode “L”: Fixed Speed mode “H”: Auto Setting mode	Hi-Z
	CAD1	I	Chip Address 1 pin in Register Control mode	
43	BICK	I	Audio Serial Data Clock pin in PCM mode	Hi-Z
	BCK	I	Audio Serial Data Clock pin in EXDF mode	
	DCLK	I	DSD Clock Pin in DSD mode (@DSDPATH bit = ”1”)	
44	SDATA1	I	Audio Serial Data Input pin in PCM mode	Hi-Z
	DINL1	I	Audio Serial Data Input pin in EXDF mode	
	DSDL1	I	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”1”)	
45	LRCK	I	Input Channel Clock pin in PCM mode	Hi-Z
	DINR1	I	Audio Serial Data Input pin in EXDF mode	
	DSDR1	I	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”1”)	
46	SDATA2	I	Audio Serial Data Input pin in PCM mode	Hi-Z
	DINL2	I	Audio Serial Data Input pin in EXDF mode	
	DSDL2	I	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”1”)	
47	DINR2	I	Audio Serial Data Input pin in EXDF mode	Hi-Z
	DSDR2	I	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”1”)	
48	SSLOW	I	Digital Filter Select pin in Pin Control mode	Hi-Z
	WCK	I	Word Clock input pin in EXDF mode	
49	TDMO	O	Audio Serial Data Output pin in Daisy Chain mode (Internal pull-down pin)	Pull-down to DVSS (100 kΩ, typ)
50	DEM0	I	De-emphasis Enable pin in Pin Control mode	Hi-Z
	DSDL1	I	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”0”)	
51	DSDR1	I	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”0”)	Hi-Z
52	TDM0	I	TDM Mode select 0 pin in Pin control mode.	Hi-Z
	DCLK	I	DSD Clock pin in DSD mode (@DSDPATH bit =”0”)	
53	TDM1	I	TDM Mode select 1 pin in Pin control mode.	Hi-Z
	DSDL2		Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”0”)	
54	DCHAIN	I	Daisy Chain Mode Select pin in Pin Control mode.	Hi-Z
	DSDR2	I	Audio Serial Data Input Pin in DSD mode (@DSDPATH bit = ”0”)	
55	INVR	I	R1/2ch Signal Invert pin in Pin Control mode	Hi-Z
	I2C	I	Serial Control Interface Select pin in Register Control mode. “L”: 3-wire serial control interface. “H”: I^2C Bus serial control interface.	
56	TEST	I	Connect to DVSS (Internal pull-down pin)	Pull-down to DVSS (100 kΩ, typ)

No.	Pin Name	I/O	Function	Power Down State
57-60	VREFHR2	I	R2ch High Level Reference Voltage Input pin.	Hi-Z
61-64	VREFLR2	I	R2ch Low Level Reference Voltage Input pin.	Hi-Z
65-67	VSSR2	-	R2ch Analog Ground pin.	-
68-70	VDDR2	-	R2ch Analog Power Supply pin.	-
71	VCOMR2	I	R2ch VCOM pin. VCOMR2 is connected to the midpoint of resistors between VREFHR2 and VREFLR2.	Hi-Z
72	EXTCR2N	O	External Capacitor Connection pin. This pin should be connected to 1 µF to VSSR2.	Pull-down to VSSR2 (250 kΩ, typ)
73,74	IOUTR2N	O	Current Output pin (R2ch negative signal).	Connected to OPINR2N (64 Ω, typ)
75	OPINR2N	O	Common Voltage Input pin (R2ch negative signal).	Connected to IOUTR2N (64 Ω, typ)
76	OPINR2P	O	Common Voltage Input pin (R2ch positive signal).	Connected to IOUTR2P (64 Ω, typ)
77,78	IOUTR2P	O	Current Output pin (R2ch positive signal).	Connected to OPINR2P (64 Ω, typ)
79	EXTCR2P	O	External Capacitor connection pin. This pin should be connected to 1 µF to VSSR2.	Pull-down to VSSR2 (250 kΩ, typ)
80,81	NC	-	No internal bonding. Connect to AVSS.	-
82	EXTCL2P	O	External Capacitor connection pin. This pin should be connected to 1 µF to VSSL2.	Pull-down to VSSL2 (250 kΩ, typ)
83,84	IOUTL2P	O	Current Output pin (L2ch positive signal).	Connected to OPINL2P (64 Ω, typ)
85	OPINL2P	O	Common Voltage Input pin (L2ch positive signal).	Connected to IOUTL2P (64 Ω, typ)
86	OPINL2N	O	Common Voltage Input pin (L2ch negative signal).	Connected to IOUTL2N (64 Ω, typ)
87,88	IOUTL2N	O	Current Output pin (L2ch negative signal).	Connected to OPINL2N (64 Ω, typ)
89	EXTCL2N	O	External Capacitor connection pin. This pin should be connected to 1 µF to VSSL2.	Pull-down to VSSL2 (250 kΩ, typ)
90	VCOML2	I	L2ch VCOM pin. VCOML2 is connected to the midpoint of resistors between VREFHL2 and VREFLL2.	Hi-Z
91-93	VDDL2	-	L2ch Analog Power Supply pin.	-
94-96	VSSL2	-	L2ch Analog Ground pin.	-
97-100	VREFLL2	I	L2ch Low Level Reference Voltage Input pin.	Hi-Z
101-104	VREFHL2	I	L2ch High Level Reference Voltage Input pin.	Hi-Z
105	EXTR	I	External Resistor connection pin. This pin should be connected to 33 kΩ (±1 %) to AVSS.	Hi-Z
106	AVSS	-	Analog Ground pin	-
107	AVDD	-	Clock Interface Power Supply Pin, 4.75 to 5.25 V	-

No.	Pin Name	I/O	Function	Power Down State
108	MCLK	I	Master Clock Input pin	Hi-Z
109	DVDD	O	(LDOE pin = "H") LDO Output pin. This pin should be connected to DVSS with 1.0 µF. This pin is prohibited to connect to other devices.	DVSS
		-	(LDOE pin = "L") 1.7 V to 1.98V Digital Power Supply pin	-
110	DVSS	-	Digital Ground pin	-
111	TVDD	-	Digital Power Supply pin, 3.0 V to 3.6 V	-
112	LDOE	I	Internal LDO Enable pin. "L": Disable, "H": Enable	Hi-Z
113	PDN	I	Power-Up, Power-Down pin When at "L", the AK4499 is in Power-Down mode. The AK4499 must always be in Power-Down mode upon supply power on.	Hi-Z (PDN = "L")
114	SMUTE	I	When this pin is changed to "H", Soft Mute cycle is initiated. When returning to "L", Soft Mute releases.	Hi-Z
	CSN	I	Chip Select pin in 3-wire serial Register Control mode	
115	SD	I	Digital Filter Select pin in Pin Control mode	Hi-Z
	CCLK	I	Control Data Clock pin in 3-wire serial Register Control mode	
	SCL	I	Control Data Clock Input pin in I^2C Bus Register Control mode	
116	SLOW	I	Digital Filter Select pin in Pin Control mode	Hi-Z
	CDTI	I	Control Data Input pin in 3-wire serial Register Control mode	
	SDA	I/O	Control Data Input pin in I^2C Bus Register Control mode	
117	DIF0	I	Digital Input Format 0 pin in Pin Control mode	Pull-down to DVSS (100 kΩ, typ)
	DZFL	O	Lch Zero Input Detect pin in Register Control mode (Internal pull-down pin)	
118	DIF1	I	Digital Input Format 1 pin in Pin Control mode	Pull-down to DVSS (100 kΩ, typ)
	DZFR	O	Rch Zero Input Detect pin in Register Control mode (Internal pull-down pin)	
119	DIF2	I	Digital Input Format 2 pin in Pin Control mode	Hi-Z
	CAD0	I	Chip Address 0 pin in Register Control mode	
120	VTSEL	I	MCLK VIH/L Level Select pin. VTSEL = "L"; VIH = 1.36 V, VIL = 0.34 V VTSEL = "H"; VIH = 2.2 V, VIL = 0.8 V	Hi-Z
121-124	VREFHL1	I	L1ch High Level Reference Voltage Input pin.	Hi-Z
125-128	VREFLL1	I	L1ch Low Level Reference Voltage Input pin.	Hi-Z
-	TAB	-	The TAB on the bottom surface of the package should be connected to AVSS.	-

Note 2. All input pins except internal pull-up/down pins must not be left floating.
Note 3. The AK4499 must be powered down by the PDN pin when changing Pin Control/Register Control modes by the PSN pin.
Note 4. PCM mode, DSD mode, and EXDF mode are selectable in Register Control mode.

5.3. Handling of Unused Pin

Unused I/O pins must be connected appropriately.

5.3.1. Pin Control Mode (PCM mode only)

Classification	Pin Name	Setting
Analog	IOUTL1P, IOUTL1N, OPINL1P, OPINL1N	Open
	IOUTR1P, IOUTR1N, OPINR1P, OPINR1N	
	IOUTL2P, IOUTL2N, OPINL2P, OPINL2N	
	IOUTR2P, IOUTR2N, OPINR2P, OPINR2N	
Digital	TEST	Connect to DVSS or Open

5.3.2. Register Control Mode

5.3.2.1. PCM Mode

Classification	Pin Name	Setting
Analog	IOUTL1P, IOUTL1N, OPINL1P, OPINL1N	Open
	IOUTR1P, IOUTR1N, OPINR1P, OPINR1N	
	IOUTL2P, IOUTL2N, OPINL2P, OPINL2N	
	IOUTR2P, IOUTR2N, OPINR2P, OPINR2N	
Digital	WCK, DEM0, DINR2, DSDR1/SDTO4, TDM0, TDM1, DCHAIN	Connect to DVSS
	TEST	Connect to DVSS or Open
	TDMO, DZFL, DZFR	Open

5.3.2.2. DSD Mode

5.3.2.2.1. DSDPATH bit = “0”

Classification	Pin Name	Setting
Analog	IOUTL1P, IOUTL1N, OPINL1P, OPINL1N	Open
	IOUTR1P, IOUTR1N, OPINR1P, OPINR1N	
	IOUTL2P, IOUTL2N, OPINL2P, OPINL2N	
	IOUTR2P, IOUTR2N, OPINR2P, OPINR2N	
Digital	WCK, BICK, SDATA1, LRCK, SDATA2, DINR2	Connect to DVSS
	TEST	Connect to DVSS or Open
	TDMO, DZFL, DZFR	Open

5.3.2.2.2. DSDPATH bit = “1”

Classification	Pin Name	Setting
Analog	IOUTL1P, IOUTL1N, OPINL1P, OPINL1N	Open
	IOUTR1P, IOUTR1N, OPINR1P, OPINR1N	
	IOUTL2P, IOUTL2N, OPINL2P, OPINL2N	
	IOUTR2P, IOUTR2N, OPINR2P, OPINR2N	
Digital	WCK, DEM0, DSDR1/TSTO4, TDM0, TDM1, DCHAIN	Connect to DVSS
	TEST	Connect to DVSS or Open
	TDMO, DZFL, DZFR	Open

5.3.2.3. EXDF Mode

Classification	Pin Name	Setting
Analog	IOUTL1P, IOUTL1N, OPINL1P, OPINL1N	Open
	IOUTR1P, IOUTR1N, OPINR1P, OPINR1N	
	IOUTL2P, IOUTL2N, OPINL2P, OPINL2N	
	IOUTR2P, IOUTR2N, OPINR2P, OPINR2N	
Digital	DEM0, DSDR1/TSTO4, TDM0, TDM1, DCHAIN	Connect to DVSS
	TEST	Connect to DVSS or Open
	TDMO, DZFL, DZFR	Open

5.3.2.4. In case I2C-Bus control mode

Classification	Pin Name	Setting
Digital	CSN	Connect to DVSS

5.3.3. Pull-up, Pull-down Pin List

Classification	Pin Name	Internal Termination
pull-up pin (typ = 100 kΩ)	PSN	TVDD
pull-down pin (typ = 100 kΩ)	TDMO, DZFL, DZFR, TEST	DVSS

6. Absolute Maximum Ratings

(AVSS = DVSS = VSSL1/R1/L2/R2 = 0 V; Note 5)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Digital I/O	VDD	-0.3	4.0	V
	Digital Core	DVDD	-0.3	2.5	V
	Clock Interface	AVDD	-0.3	6.0	V
	Analog	VDD L1/R1/L2/R2	-0.3	6.0	V
	Each VSS Difference (Note 6)	ΔGND	0	0.3	V
	|VDDL1/R1－AVDD| (Note 7)	ΔVD	0	0.3	V
	|VDDL2/R2－AVDD| (Note 7)	ΔVD	0	0.3	V
Reference Voltage (Note 8)	High VREF	VREFHL1	-0.3	VDDL1+0.3 or 6.0	V
		VREFHR1	-0.3	VDDR1+0.3 or 6.0	V
		VREFHL2	-0.3	VDDL2+0.3 or 6.0	V
		VREFHR2	-0.3	VDDR2+0.3 or 6.0	V
	Low VREF	VREFLL1	-0.3	VDDL1+0.3 or 6.0	V
		VREFLR1	-0.3	VDDR1+0.3 or 6.0	V
		VREFLL2	-0.3	VDDL2+0.3 or 6.0	V
		VREFLR2	-0.3	VDDR2+0.3 or 6.0	V
	Common Voltage	VCOML1	-0.3	VDDL1+0.3 or 6.0	V
		VCOMR1	-0.3	VDDR1+0.3 or 6.0	V
		VCOML2	-0.3	VDDL2+0.3 or 6.0	V
		VCOMR2	-0.3	VDDR2+0.3 or 6.0	V
Input Current, Any Pin Except Supplies and VREF		IIN	-	±10	mA
Analog Output Voltage (Note 9)	IOUTL1P/L1N/R1P/R1N, OPINL1P/L1N/R1P/R1N	VOUTA	-0.3	VDDL1/R1+0.3 or 6.0	V
	IOUTL2P/L2N/R2P/R2N, OPINL2P/L2N/R2P/R2N	VOUTA	-0.3	VDDL2/R2+0.3 or 6.0	V
Digital Input Voltage		VIND	-0.3	TVDD+0.3	V
Ambient Temperature (Power applied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 5. All voltages are with respect to ground.

Note 6. AVSS, DVSS, VSSL1, VSSR1, VSSL2, and VSSR2 must be connected to the same analog ground plane. The exposed pad on the bottom surface of the package must be connected to AVSS.

Note 7. VDDL1, VDDR1, VDDL2, VDDR2, and AVDD must be referenced to the same voltage level.

Note 8. Maximum input voltage of VREFHL1/R1/L2/R2 pins is lower value between (VDDL1/R1/L2/R2 +0.3) V and 6.0 V.

Note 9. Maximum value of the Analog Output Voltage must not exceed 6.0V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS = DVSS = VSSL1/R1/L2/R2 = 0 V; Note 5)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	(LDOE pin = "L"; Note 10)					
	Digital I/O	TVDD	DVDD	1.8/3.3	3.6	V
	Digital Core	DVDD	1.7	1.8	1.98	V
	Clock Interface	AVDD	4.75	5.0	5.25	V
	Analog	VDD L1/R1/L2/R2	4.75	5.0	5.25	V
	(LDOE pin = "H"; Note 11)					
	Digital I/O	TVDD	3.0	3.3	3.6	V
	Clock Interface	AVDD	4.75	5.0	5.25	V
	Analog	VDD L1/R1/L2/R2	4.75	5.0	5.25	V
Reference Voltage (Note 12)	High VREF	VREFHL1	VDDL1-0.5	-	VDDL1	V
		VREFHR1	VDDR1-0.5	-	VDDR1	V
		VREFHL2	VDDL2-0.5	-	VDDL2	V
		VREFHR2	VDDR2-0.5	-	VDDR2	V
	Low VREF	VREFLL1	-	VSSL1	-	V
		VREFLR1	-	VSSR1	-	V
		VREFLL2	-	VSSL2	-	V
		VREFLR2	-	VSSR2	-	V
	Common Voltage	VCOML1	-	(VREFHL1+VREFLL1)/2	-	V
		VCOMR1	-	(VREFHR1+VREFLR1)/2	-	V
		VCOML2	-	(VREFHL2+VREFLL2)/2	-	V
		VCOMR2	-	(VREFHR2+VREFLR2)/2	-	V

Note 10. When the LDOE pin = "L", TVDD must be supplied before DVDD is powered up or at the same time. The power up sequence between other power supplies is not critical.

Note 11. When the LDOE pin = "H", the internal LDO supplies 1.8 V (typ) from the DVDD pin. The power up sequence between AVDD and TVDD is not critical.

Note 12. Reference voltage of VREFHL1/R1/L2/R2 must be input after VDDL1/R1/L2/R2 is powered up or at the same time. Assuming that VREF Voltage divides into Common Voltage.

*** AKM assumes no responsibility for the usage beyond the conditions in this data sheet.**

8. Electical Characteristics

8.1. Analog Characteristics

8.1.1. PCM Mode

(Ta = 25°C; LDOE pin = "L", TVDD = 3.3 V, DVDD = 1.8 V, AVDD = 5.0 V, AVSS = DVSS = 0 V; VDDL1/R1/L2/R2 = VREFHL1/R1/L2/R2 = 5.0 V, VSSL1/R1/L2/R2 = VREFLL1/R1/L2/R2 = 0 V; VCOML1/R1/L2/R2 = (VREFHL1/R1/L2/R2 + VREFLL1/R1/L2/R2)/2; 32-bit Input data; BICK = 64fs; Signal Frequency = 1 kHz; fs = 44.1 kHz; Measurement bandwidth = 20 Hz to 20 kHz; External Circuit: (Figure 82); GC[1:0] bits = "00"; unless otherwise specified.)

Parameter				Min.	Typ.	Max.	Unit
Resolution				-	-	32	bit
Dynamic Characteristics							
THD	fs = 44.1 kHz	BW = 20 kHz	0dBFS	-	-124	-110	dB
	fs = 96 kHz	BW = 40 kHz	0dBFS	-	-124	-	dB
	fs = 192 kHz	BW = 80 kHz	0dBFS	-	-124	-	dB
THD+N	fs = 44.1 kHz	BW = 20 kHz	0dBFS	-	-124	-	dB
			–60dBFS	-	-71	-	dB
	fs = 96 kHz	BW = 40 kHz	0dBFS	-	-121	-	dB
			–60dBFS	-	-67	-	dB
	fs = 192 kHz	BW = 80 kHz	0dBFS	-	-118	-	dB
			–60dBFS	-	-62	-	dB
	fs = 384 kHz	BW = 80 kHz	0dBFS	-	-118	-	dB
	fs = 768 kHz	BW = 80 kHz	0dBFS	-	-118	-	dB
Dynamic Range (–60 dBFS with A-weighting)				-	134	-	dB
S/N (A-weighted)			4-ch mode	129	134		
			Stereo mode	-	137	-	dB
			Mono mode (Note 13)	-	140	-	dB
Interchannel Isolation (1 kHz)				110	120	-	dB
DC Accuracy							
Interchannel Gain Mismatch)				-	0.15	0.3	dB
Gain Drift				-	100	-	ppm/°C
Differential Output Current (IOUTP-IOUTN)			(Note 14)	61.8	72.8	83.8	mApp
Center Current			(Note 15)	-	0	-	mA
Load Capacitance (Analog Output Pins)			(Note 16)	-	-	5	pF

Note 13. External circuits shown in Figure 83 are used in Mono mode.

Note 14. When the input signal is 0dBFS, the output current can be calculated by the following formula:
IOUTL1 (Typ. @ 0dBFS) = (IOUTL1P) – (IOUTL1N) = 72.8 mApp × (VREFHL1 – VREFLL1)/5.
IOUTR1 (Typ. @ 0dBFS) = (IOUTR1P) – (IOUTR1N) =72.8 mApp × (VREFHR1 – VREFLR1)/5.
IOUTL2 (Typ. @ 0dBFS) = (IOUTL2P) – (IOUTL2N) = 72.8 mApp × (VREFHL2 – VREFLL2)/5.
IOUTR2 (Typ. @ 0dBFS) = (IOUTR2P) – (IOUTR2N) =72.8 mApp × (VREFHR2 – VREFLR2)/5.

Note 15. Center current is the current that flows each IOUT pin during common output.
(When positive input of operational amplifier in I-V Conversion = VCOML1/R1/L2/R2 = (VREFHL1/R1/L2/R2 + VREFLL1/R1/L2/R2)/2V)

Note 16. The load capacitance value of analog output pins (IOUTL1P/L1N/R1P/R1N pins, OPINL1P/L1N/R1P/R1N pins, IOUTL2P/L2N/R2P/R2N pins, OPINL2P/L2N/R2P/R2N pins) is with respect to ground.

Note 17. Absolute resistance error of subsequent stage circuits recommended to be 0.1% in order to meet specifications.

(Ta = -40 to 85 °C; LDOE pin = “L”, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V, AVDD = 4.75 to 5.25 V, VDDL1/R1/L2/R2 = 4.75 to 5.25 V, VREFHL1/R1/L2/R2 = 4.75 to 5.25 V, DVSS = AVSS = VSSL1/R1/L2/R2 = VREFLL1/R1/L2/R2 = 0 V; VCOML1/R1/L2/R2 = (VREFHL1/R1/L2/R2 + VREFLL1/R1/L2/R2)/2; 32-bit Input data; BICK = 64fs; Signal Frequency = 1 kHz; fs = 44.1 kHz; External Circuit: Figure 82; GC[1:0] bits = ”00”; unless otherwise specified.)

Power Supplies						
Parameter			**Min.**	**Typ.**	**Max.**	**Unit**
Power Supply Current						
Normal operation (PDN pin = “H”)						
VDDL1/L2/R1/R2 total (Note 18)			-	32 (44)	48 (66)	mA mA
VREFHL1/L2/R1/R2 total			-	92	116	mA
AVDD			-	4.4	6.6	mA
TVDD						
	LDOE pin = “H”	fs = 44.1 kHz	-	12	18	mA
		fs = 96 kHz	-	20	30	mA
		fs = 192 kHz	-	33	50	mA
	LDOE pin = “L”			1	1.5	mA
DVDD						
	LDOE pin = “L”	fs = 44.1 kHz	-	12	18	mA
		fs = 96 kHz	-	20	30	mA
		fs = 192 kHz	-	33	50	mA
Total power dissipation (LDOE pin = “L”) (VDDL1/L2/R1/R2+VREFHL1/L2/R1/R2+AVDD+TVDD+ DVDD)		fs = 44.1 kHz	-	667	-	mW
Power down (PDN pin = “L”) (VDDL1/L2/R1/R2+VREFHL1/L2/R1/R2+AVDD+TVDD+ DVDD)		(Note 18)	-	10	250	μA

Note 18. In power down mode, the PSN pin = TVDD and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held to DVSS.

Note 19. The DVDD pin becomes an output pin when the LDOE pin = “H”.

Note 20. The values in () at VDDL1/L2/R1/R2 total power supply current indicate consumption current when there is zero input data.

8.1.2. DSD Mode

(Ta = 25 °C; LDOE pin = “L”, TVDD = 3.3 V, DVDD = 1.8 V, AVDD = 5.0 V, AVSS = DVSS = 0 V; VDDL1/R1/L2/R2 = VREFHL1/R1/L2/R2 = 5.0 V, VSSL1/R1/L2/R2 = VREFLL1/R1/L2/R2 = 0 V; VCOML1/R1/L2/R2 = (VREFHL1/R1/L2/R2 + VREFLL1/R1/L2/R2)/2; Signal Frequency = 1 kHz; Measurement bandwidth = 20 Hz to 20 kHz; External Circuit: Figure 82; GC[1:0] bits = ”00”); unless otherwise specified.)

Dynamic Characteristics						
Parameter			**Min.**	**Typ.**	**Max.**	**Unit**
THD	DSD data stream: DSD64	0 dB (Note 21)	-	-124	-	dB
	DSD data stream: DSD128	0 dB (Note 21)	-	-124	-	dB
	DSD data stream: DSD256	0 dB (Note 21)	-	-124	-	dB
	DSD data stream: DSD512	0 dB (Note 21)	-	-106	-	dB
S/N (A-weighted, Normal path)	DSD data stream: DSD64	Digital “0” (Note 22)	-	134	-	dB
	DSD data stream: DSD128	Digital “0” (Note 22)	-	134	-	dB
	DSD data stream: DSD256	Digital “0” (Note 22)	-	134	-	dB
	DSD data stream: DSD512	Digital “0” (Note 22)	-	131	-	dB

Note 21. The output level is assumed as 0dB when a 1kHz 25% to 75% duty sine wave is input. Click noise may occur if the input signal exceeds 0dB.

Note 22. Digital “0” is a “01101001” digital zero code pattern.

DSD Data Stream: Power Supplies in 22.5792MHz Operation

(Ta = -40 to 85 °C; LDOE pin = “L”, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V, AVDD = 4.75 to 5.25 V, VDDL1/R1/L2/R2 = 4.75~5.25 V, VREFHL1/R1/L2/R2 = 4.75 to 5.25 V, DVSS = AVSS = VSSL1/R1/L2/R2 = VREFLL1/R1/L2/R2 = 0 V; VCOML1/R1/L2/R2 = (VREFHL1/R1/L2/R2 + VREFLL1/R1/L2/R2)/2; Signal Frequency = 1 kHz; Measurement bandwidth = 20Hz to 20kHz; External Circuit: Figure 82; 36.4mApp circuit output mode (GC[1:0] bits = ”00”); unless otherwise specified.)

Power Supplies					
Parameter		**Min.**	**Typ.**	**Max.**	**Unit**
Power Supply Current					
Normal operation (PDN pin = “H”)					
VDDL1/L2/R1/R2 total		-	52 (76)	78 (114)	mA mA
VREFHL1/L2/R1/R2 total		-	92	116	mA
AVDD		-	4.4	6.6	mA
TVDD					
	LDOE pin = “H”	-	20	30	mA
	LDOE pin = “L”		1	1.5	mA
DVDD					
	LDOE pin = “L”	-	20	30	mA
Total power dissipation (LDOE pin = “L”) (VDDL1/L2/R1/R2+VREFHL1/L2/R1/R2+AVDD+TVDD+ DVDD)		-	798	-	mW

8.2. DAC Digital Filter Characteristics (PCM Mode)

8.2.1. Sharp Roll-Off Filter Characteristics

▪ fs = 44.1 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Normal Speed mode; DEM = OFF; SD bit or SD pin = “0”, SLOW bit or SLOW pin = “0”, SSLOW bit or SSLOW pin = “0”)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.01 dB	-	0	-	20.0	kHz
	−6.0 dB	-	-	22.05	-	kHz
Pass band	(Note 24)	PB	0	-	20.0	kHz
Stop band	(Note 24)	SB	24.1	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.005	dB
Stop band Attenuation	(Note 23)	SA	100	-	-	dB
Group Delay	(Note 26)	GD	-	29.2	-	1/fs

▪ fs = 96 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Double Speed mode; DEM = OFF; SD bit or SD pin = “0”, SLOW bit or SLOW pin = “0”, SSLOW bit or SSLOW pin = “0”)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.01 dB	-	0	-	43.5	kHz
	−6.0 dB	-	-	48.0	-	kHz
Pass band	(Note 24)	PB	0	-	43.5	kHz
Stop band	(Note 24)	SB	52.5	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.005	dB
Stop band Attenuation	(Note 23)	SA	100	-	-	dB
Group Delay	(Note 26)	GD	-	29.2	-	1/fs

▪ fs = 192 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Quad Speed mode; DEM = OFF; SD bit or SD pin = “0”, SLOW bit or SLOW pin = “0”, SSLOW bit or SSLOW pin = “0”)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.01 dB	-	0	-	87	kHz
	−6.0 dB	-	-	96.0	-	kHz
Pass band	(Note 24)	PB	0	-	87	kHz
Stop band	(Note 24)	SB	104.9	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.005	dB
Stop band Attenuation	(Note 23)	SA	100	-	-	dB
Group Delay	(Note 26)	GD	-	29.2	-	1/fs

Note 23. Frequency response refers to the output level of 1 kHz. Stopband attenuation band ranges from SB to fs.

Note 24. The passband and stopband frequencies scale with fs.
For example, PB = 0.4535 × fs (@±0.01 dB), SB = 0.546 × fs.

Note 25. This value is the gain amplitude in pass band width.

Note 26. The calculating delay time which occurred by digital filtering. This value is from setting the 16/20/24/32 bit data of both channels to the output of analog signal.

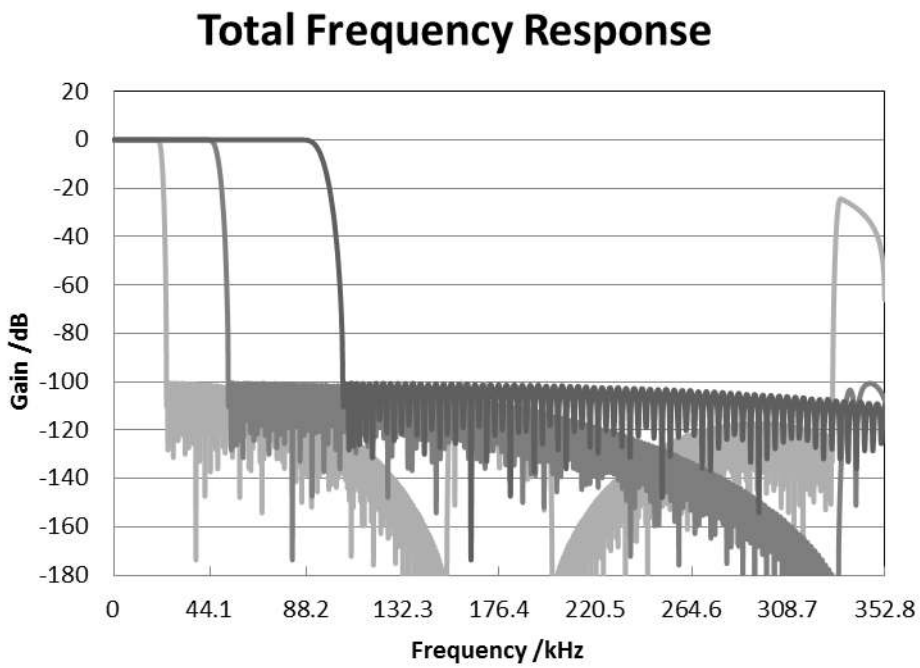


Figure 2. Sharp Roll-Off Filter Frequency Response

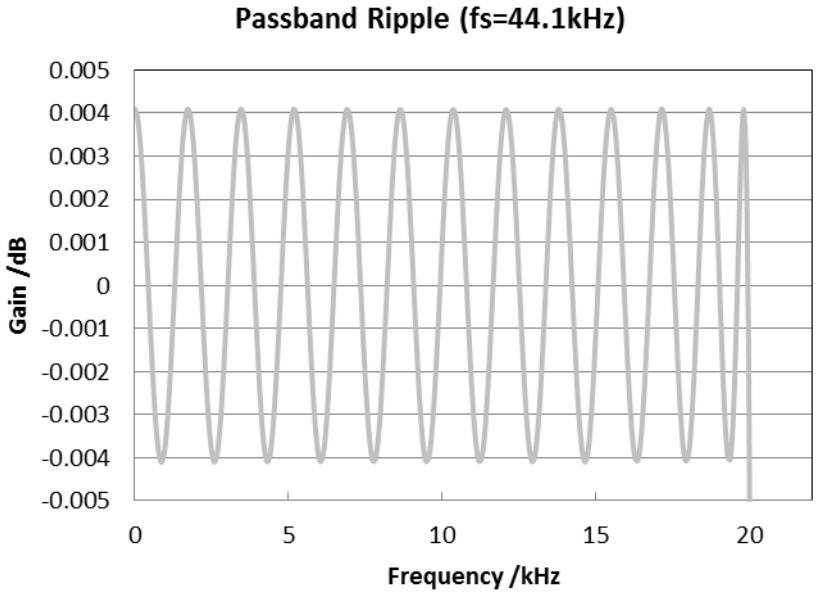


Figure 3. Sharp Roll-Off Filter Pass Band Ripple

8.2.2. Slow Roll-Off Filter Characteristics

▪ fs = 44.1 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Normal Speed mode; DEM = OFF; SD bit or SD pin = "0", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.01 dB	-	0	-	8.0	kHz
	−6.0 dB	-	-	21.0	-	kHz
Pass band	(Note 27)	PB	0	-	8.0	kHz
Stop band	(Note 27)	SB	39.2	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.007	dB
Stop band Attenuation	(Note 23)	SA	92	-	-	dB
Group Delay	(Note 26)	GD	-	6.5	-	1/fs

▪ fs = 96 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Double Speed mode; DEM = OFF; SD bit or SD pin = "0", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.01 dB	-	0	-	17.6	kHz
	−6.0 dB	-	-	45.6	-	kHz
Pass band	(Note 27)	PB	0	-	17.6	kHz
Stop band	(Note 27)	SB	85.4	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.007	dB
Stop band Attenuation	(Note 23)	SA	100	-	-	dB
Group Delay	(Note 26)	GD	-	6.5	-	1/fs

▪ fs = 192 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Quad Speed mode; DEM = OFF; SD bit or SD pin = "0", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.01 dB	-	0	-	35.2	kHz
	−6.0 dB	-	-	91.2	-	kHz
Pass band	(Note 27)	PB	0	-	35.2	kHz
Stop band	(Note 27)	SB	170.7	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.007	dB
Stop band Attenuation	(Note 23)	SA	100	-	-	dB
Group Delay	(Note 26)	GD	-	6.5	-	1/fs

Note 27. The passband and stopband frequencies scale with fs.
For example, PB = 0.1836 × fs (@±0.01 dB), SB = 0.8889 × fs.

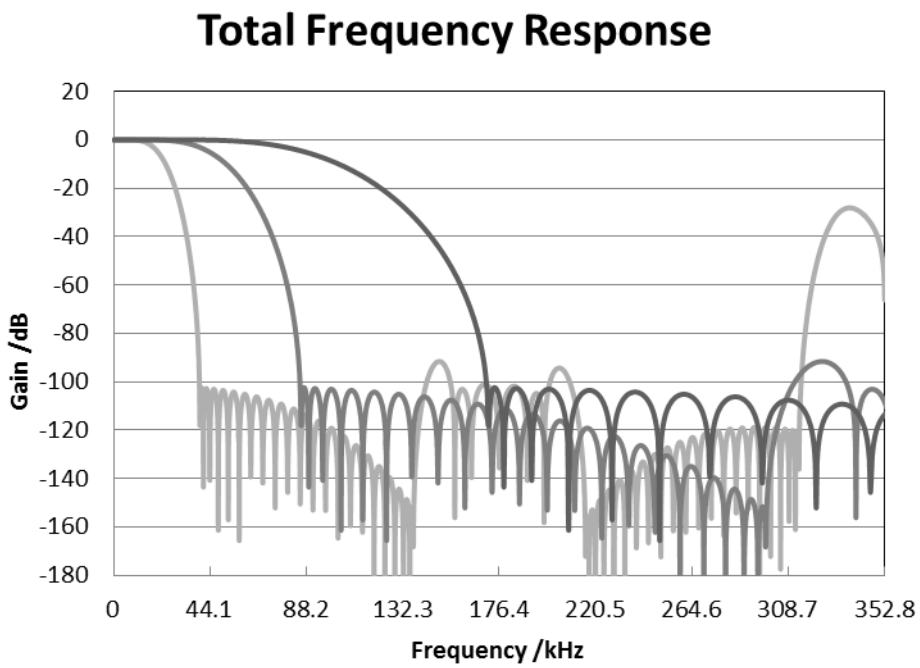


Figure 4. Slow Roll-Off Filter Frequency Response

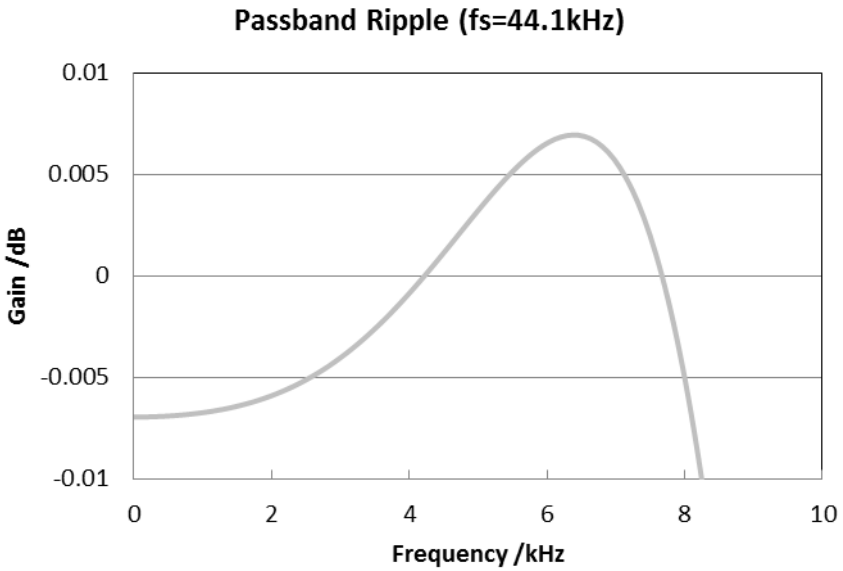


Figure 5. Slow Roll-Off Filter Pass Band Ripple

8.2.3. Short Delay Sharp Roll-Off Filter Characteristics

▪ fs = 44.1 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Normal Speed mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.01 dB	-	0	-	20.0	kHz
	−6.0 dB	-	-	22.05	-	kHz
Pass band	(Note 28)	PB	0	-	20.0	kHz
Stop band	(Note 28)	SB	24.1	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.005	dB
Stop band Attenuation	(Note 23)	SA	100	-	-	dB
Group Delay	(Note 26)	GD	-	6.0	-	1/fs

▪ fs = 96 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Double Speed mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.01 dB	-	0	-	43.5	kHz
	−6.0 dB	-	-	48.0	-	kHz
Pass band	(Note 28)	PB	0	-	43.5	kHz
Stop band	(Note 28)	SB	52.5	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.005	dB
Stop band Attenuation	(Note 23)	SA	100	-	-	dB
Group Delay	(Note 26)	GD	-	6.0	-	1/fs

▪ fs = 192 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Quad Speed mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.01 dB	-	0	-	87.0	kHz
	−6.0 dB	-	-	96.0	-	kHz
Pass band	(Note 28)	PB	0	-	87.0	kHz
Stop band	(Note 28)	SB	104.9	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.005	dB
Stop band Attenuation	(Note 23)	SA	100	-	-	dB
Group Delay	(Note 26)	GD	-	6.0	-	1/fs

Note 28. The passband and stopband frequencies scale with fs.
For example, PB = 0.4535 × fs (@±0.01 dB), SB = 0.546 × fs.

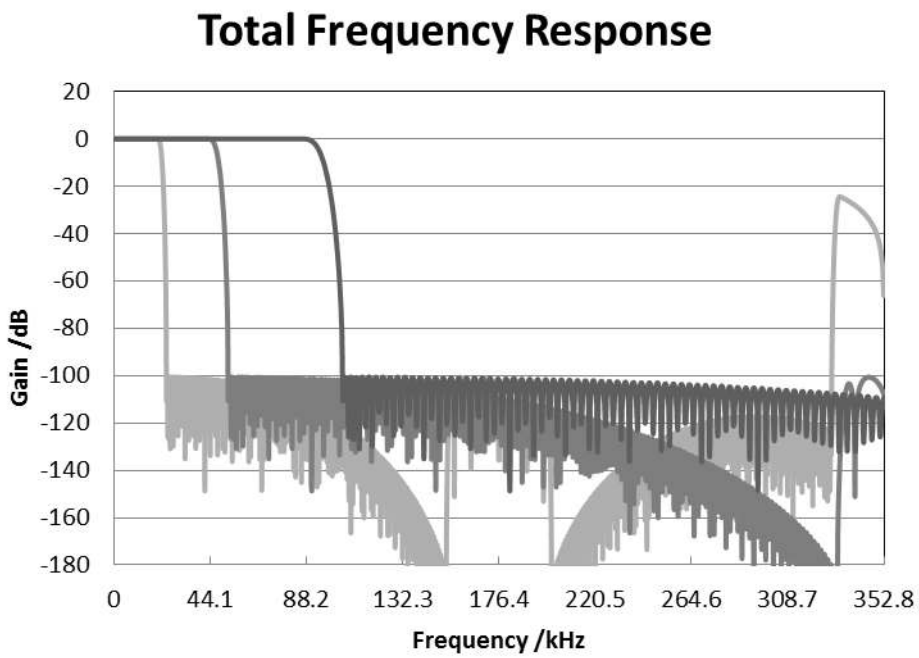


Figure 6. Short Delay Sharp Roll-Off Filter Frequency Response

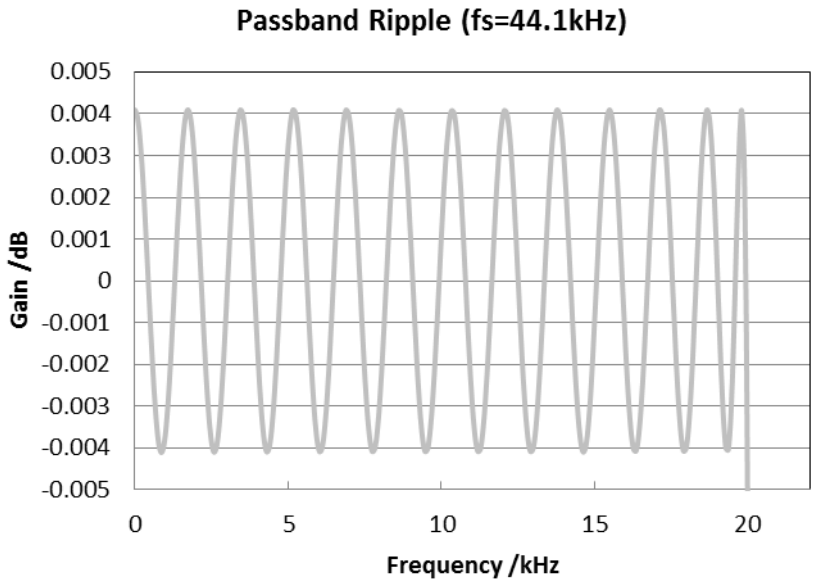


Figure 7. Short Delay Sharp Roll-Off Filter Pass Band Ripple

8.2.4. Short Delay Slow Roll-Off Filter Characteristics

▪ fs = 44.1 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Normal Speed mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.01 dB	-	0	-	8.0	kHz
	−6.0 dB	-	-	21.0	-	kHz
Pass band	(Note 29)	PB	0	-	8.0	kHz
Stop band	(Note 29)	SB	39.2	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.007	dB
Stop band Attenuation	(Note 23)	SA	92	-	-	dB
Group Delay	(Note 26)	GD	-	5.0	-	1/fs

▪ fs = 96 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Double Speed mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.01 dB	-	0	-	17.6	kHz
	−6.0 dB	-	-	45.6	-	kHz
Pass band	(Note 29)	PB	0	-	17.6	kHz
Stop band	(Note 29)	SB	85.4	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.007	dB
Stop band Attenuation	(Note 23)	SA	100	-	-	dB
Group Delay	(Note 26)	GD	-	5.0	-	1/fs

▪ fs = 192 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Quad Speed mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.01 dB	-	0	-	35.2	kHz
	−6.0 dB	-	-	91.2	-	kHz
Pass band	(Note 29)	PB	0	-	35.2	kHz
Stop band	(Note 29)	SB	170.7	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.007	dB
Stop band Attenuation	(Note 23)	SA	100	-	-	dB
Group Delay	(Note 26)	GD	-	5.0	-	1/fs

Note 29. The passband and stopband frequencies scale with fs.
For example, PB = 0.1836 × fs (@±0.01dB), SB = 0.8866 × fs.

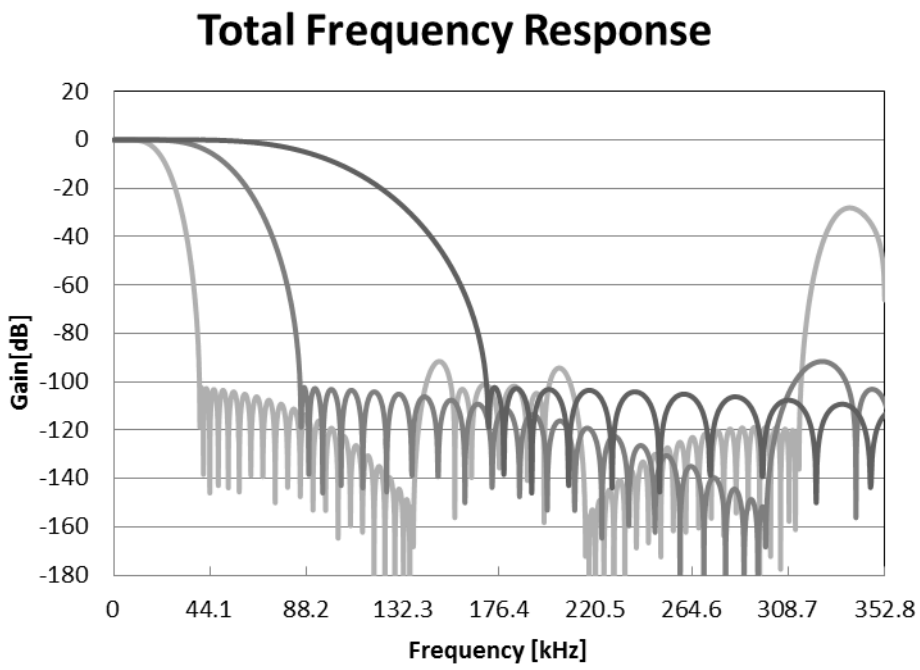


Figure 8. Short Delay Slow Roll-Off Filter Frequency Response

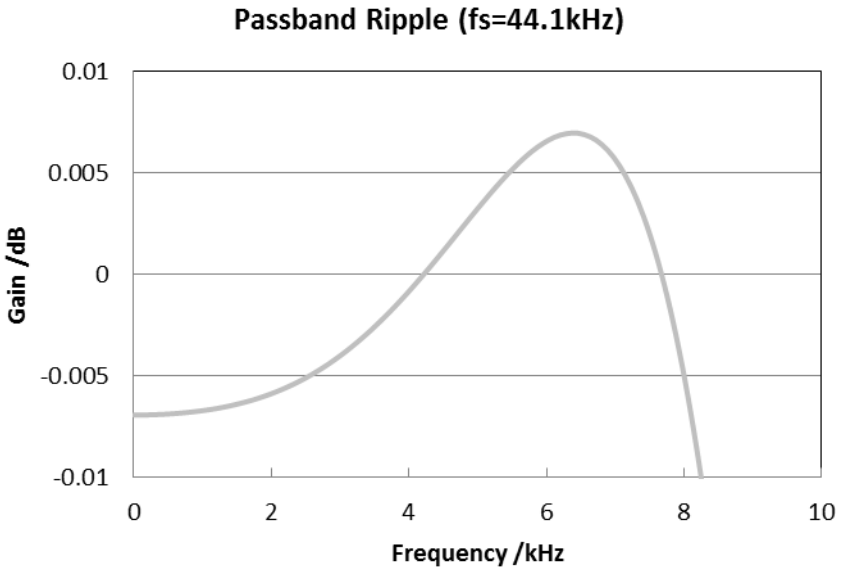


Figure 9. Short Delay Slow Roll-Off Filter Passband Ripple

8.2.5. Low-dispersion Short Delay Filter Characteristics

▪ fs = 44.1 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Normal Speed mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	18.4	kHz
	−6.0 dB	-	-	22.05	-	kHz
Pass band	(Note 30)	PB	0	-	18.4	kHz
Stop band	(Note 30)	SB	25.7	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.05	dB
Stop band Attenuation	(Note 23)	SA	80	-	-	dB
Group Delay	(Note 26)	GD	-	10.0	-	1/fs
Group Delay Distortion		Δ GD	-	±0.035	-	1/fs

▪ fs = 96 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Double Speed mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	40.1	kHz
	−6.0 dB	-	-	48.0	-	kHz
Pass band	(Note 30)	PB	0	-	40.1	kHz
Stop band	(Note 30)	SB	55.9	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.05	dB
Stop band Attenuation	(Note 23)	SA	80	-	-	dB
Group Delay	(Note 26)	GD	-	10.0	-	1/fs
Group Delay Distortion		ΔGD	-	±0.035	-	1/fs

▪ fs = 192 kHz

(Ta = -40 to 85°C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; Quad Speed mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 23)	±0.05 dB	-	0	-	80.2	kHz
	−6.0 dB	-	-	96.0	-	kHz
Pass band	(Note 30)	PB	0	-	80.2	kHz
Stop band	(Note 30)	SB	111.8	-	-	kHz
Pass band Ripple	(Note 25)	PR	-	-	±0.05	dB
Stop band Attenuation	(Note 23)	SA	80	-	-	dB
Group Delay	(Note 26)	GD	-	10.0	-	1/fs
Group Delay Distortion		ΔGD	-	±0.035	-	1/fs

Note 30. The passband and stopband frequencies scale with fs.
For example, PB = 0.418 × fs (@±0.05 dB), SB = 0.582 × fs.

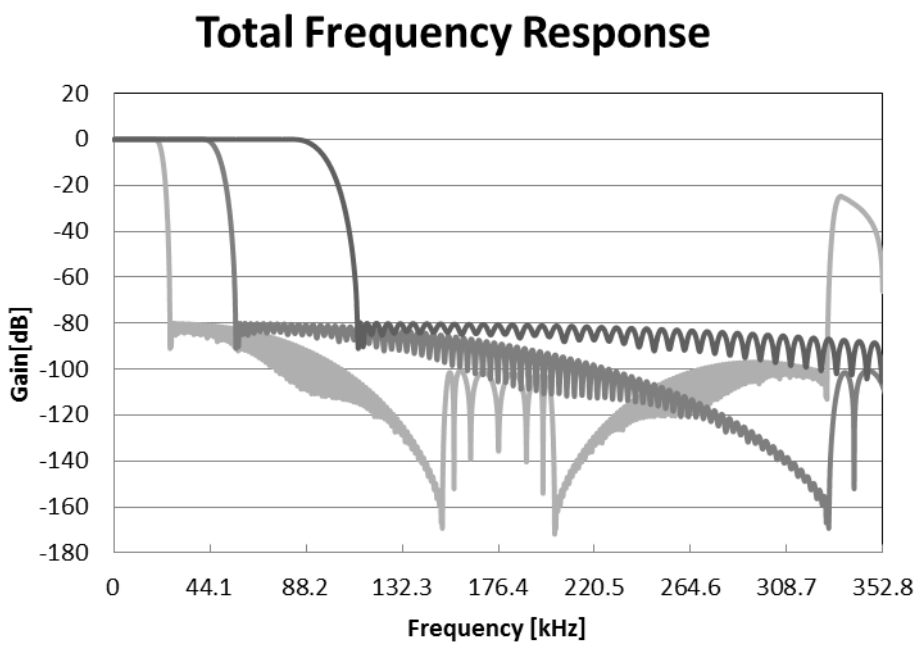


Figure 10. Low Dispersion Short Delay Filter Frequency Response

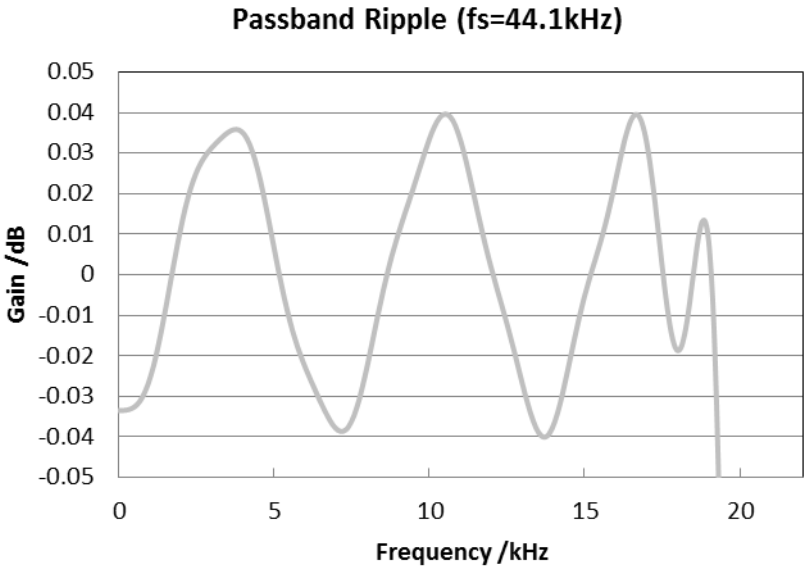


Figure 11. Low Dispersion Short Delay Filter Passband Ripple

8.3. DAC Digital-Filter Characteristics (DSD Mode)

(Ta = -40 to 85 °C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; fs = 44.1 kHz; DSDSEL[1:0] bits = "00")

(1) DSD64

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response (Note 31)					
DSDF="0" Cut off frequency; 37kHz	20 kHz	-	-0.8	-	dB
	50 kHz	-	-5.8	-	dB
	100 kHz	-	-21.1	-	dB
DSDF="1" Cut off frequency; 65kHz	20 kHz	-	-0.3	-	dB
	100 kHz	-	-7.6	-	dB
	150 kHz	-	-21.4	-	dB

(2) DSD128 (128fs frequency tracks from 64fs.)

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response (Note 31)					
DSDF="0" Cut off frequency; 74kHz	40 kHz	-	-0.8	-	dB
	100 kHz	-	-5.8	-	dB
	200 kHz	-	-21.1	-	dB
DSDF="1" Cut off frequency; 131kHz	40 kHz	-	-0.3	-	dB
	200 kHz	-	-7.6	-	dB
	300 kHz	-	-21.4	-	dB

(3) DSD256

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response (Note 31)					
DSD filter Cut off frequency; 238kHz	80 kHz	-	-0.3	-	dB
	200 kHz	-	-2.1	-	dB
	400 kHz	-	-9.3	-	dB

(4) DSD512 (512fs frequency tracks from 256fs)

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response (Note 31)					
DSD filter Cut off frequency; 476kHz	160 kHz	-	-0.3	-	dB
	400 kHz	-	-2.1	-	dB
	800 kHz	-	-9.3	-	dB

Note 31. The output level is assumed as 0dB when a 1kHz 25% to 75% duty sine wave is input. Click noise may occur if the input signal exceeds 0dB.

8.4. DC Characteristics

(Ta = -40 to 85 °C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK pin (VTSEL pin = "L")					
High-Level Input Voltage	VIH	1.36	-	-	V
Low-Level Input Voltage	VIL	-	-	0.34	V
MCLK pin (VTSEL pin = "H")					
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
1.7 V ≤ TVDD < 3.0 V (except MCLK pin)					
High-Level Input Voltage	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	20%TVDD	V
3.0 V ≤ TVDD ≤ 3.6 V (except MCLK pin)					
High-Level Input Voltage	VIH	70%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%TVDD	V
High-Level Output Voltage (TDMO, DZFL, DZFR pins: Iout = -100 μA)	VOH	TVDD−0.3	-	-	V
Low-Level Output Voltage (except SDA pin: Iout = 100 μA)	VOL	-	-	0.3	V
(SDA pin, 2.0 V < TVDD ≤ 3.6 V: Iout = 3 mA)	VOL	-	-	0.4	V
(SDA pin, 1.7 V ≤ TVDD ≤ 2.0 V: Iout = 3 mA)	VOL	-		20%TVDD	V
Input Leakage Current (Note 32)	Iin	-	-	±10	μA

Note 32. The TEST, TDMO, DIF0, and DIF1 pin have internal pull-down and the PSN pin has internal pull-up resistors. The resistance is 100 kΩ (typ). Therefore, the TEST, TDMO, DIF0, DIF1, and PSN pins are not included in this specification.

8.5. Switching Characteristics

(Ta = -40 to 85 °C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V, C_L = 20 pF, AFSD bit = "0")

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing (Note 33)					
Frequency	fCLK	2.048	-	49.152	MHz
Duty Cycle	dCLK	40	-	60	%
Pulse Width	tCLKH	9.155	-	-	ns
	tCLKL	9.155	-	-	ns
LRCK Clock Timing					
Normal Mode (TDM[1:0] bits/pins = 00)					
Normal Speed mode	fsn	8	-	54	kHz
Double Speed mode	fsd	54	-	108	kHz
Quad Speed mode	fsq	108	-	216	kHz
Oct Speed mode	fso	216	-	388	kHz
Hex Speed mode	fsh	388	-	776	kHz
Duty Cycle	Duty	45	-	55	%
TDM128 Mode (TDM[1:0] bits/pins = 01)					
Normal Speed mode	fsn	8	-	54	kHz
Double Speed mode	fsd	54	-	108	kHz
Quad Speed mode	fsq	108	-	216	kHz
High time	tLRH	1/128fs	-	-	ns
Low time	tLRL	1/128fs	-	-	ns
TDM256 Mode (TDM[1:0] bits/pins = 10)					
Normal Speed mode High time	fsn	8	-	54	kHz
Double Speed mode	fsd	54	-	108	kHz
High time	tLRH	1/256fs	-	-	ns
Low time	tLRL	1/256fs	-	-	ns
TDM512 Mode (TDM[1:0] bits/pins = 11)					
Normal Speed mode	fsn	8	-	54	kHz
High time	tLRH	1/512fs	-	-	ns
Low time	tLRL	1/512fs	-	-	ns

Note 33. The MCLK frequency should be changed while the AK4499 is in reset state by setting the PDN pin = "L" or RSTN bit = "0".

(Ta = -40 to 85 °C; VDDL1/R1/L2/R2 = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V, C_L = 20 pF, AFSD bit = "1")

Parameter (fs auto detect mode, Note 34)	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing					
Frequency	fCLK	7.68	-	49.152	MHz
Duty Cycle	dCLK	40	-	60	%
Pulse Width	tCLKH	9.155	-	-	ns
	tCLKL	9.155	-	-	ns
LRCK Clock Timing					
Normal Mode (TDM[1:0] bits = "00")					
Normal Speed mode	fsn	30	-	54	kHz
Double Speed mode	fsd	87	-	108	kHz
Quad Speed mode	fsq	174	-	216	kHz
Oct Speed mode	fso	348	-	388	kHz
Hex Speed mode	fsh	696	-	776	kHz
Duty Cycle	Duty	45	-	55	%
TDM128 Mode (TDM[1:0] bits = "01")					
Normal Speed mode	fsn	30	-	54	kHz
Double Speed mode	fsd	87	-	108	kHz
Quad Speed mode	fsq	174	-	216	kHz
High time	tLRH	1/128fs	-	-	ns
Low time	tLRL	1/128fs	-	-	ns
TDM256 Mode (TDM[1:0] bits = "10")					
Normal Speed mode High time	fsn	30	-	54	kHz
Double Speed mode	fsd	87	-	108	kHz
High time	tLRH	1/256fs	-	-	ns
Low time	tLRL	1/256fs	-	-	ns
TDM512 Mode (TDM[1:0] bits = "11")					
Normal Speed mode	fsn	30	-	54	kHz
High time	tLRH	1/512fs	-	-	ns
Low time	tLRL	1/512fs	-	-	ns

Note 34. In fs Auto Detection mode (AFSD bit = "1"), normal operation is not guaranteed if a clock of a frequency other than the above is input to the MCLK pin and the LRCK pin.

Parameter	Symbol	Min.	Typ.	Max.	Unit
PCM Audio Interface Timing					
Normal Mode (TDM[1:0] bits/pins = "00")					
BICK Period					
Normal Speed mode	tBCK	1/256fsn	-	-	ns
Double Speed mode	tBCK	1/128fsd	-	-	ns
Quad Speed mode	tBCK	1/64fsq	-	-	ns
Oct Speed mode	tBCK	1/64fso	-	-	ns
Hex Speed mode	tBCK	1/64fsh	-	-	ns
BICK Pulse Width Low	tBCKL	9	-	-	ns
BICK Pulse Width High	tBCKH	9	-	-	ns
BICK "↑" to LRCK Edge (Note 35)	tBLR	5	-	-	ns
LRCK Edge to BICK "↑" (Note 35)	tLRB	5	-	-	ns
SDATA1/2 Hold Time	tSDH	5	-	-	ns
SDATA1/2 Setup Time	tSDS	5	-	-	ns
TDM128 Mode (TDM[1:0] bits/pins = "01")					
BICK Period					
Normal Speed mode	tBCK	1/128fsn	-	-	ns
Double Speed mode	tBCK	1/128fsd	-	-	ns
Quad Speed mode	tBCK	1/128fsq	-	-	ns
BICK Pulse Width Low	tBCKL	14	-	-	ns
BICK Pulse Width High	tBCKH	14	-	-	ns
BICK "↑" to LRCK Edge (Note 35)	tBLR	14	-	-	ns
LRCK Edge to BICK "↑" (Note 35)	tLRB	14	-	-	ns
SDATA1/2 Hold Time	tSDH	5	-	-	ns
SDATA1/2 Setup Time	tSDS	5	-	-	ns
TDM256 Mode (TDM[1:0] bits/pins = "10")					
BICK Period					
Normal Speed mode	tBCK	1/256fsn	-	-	ns
Double Speed mode	tBCK	1/256fsd	-	-	ns
BICK Pulse Width Low	tBCKL	14	-	-	ns
BICK Pulse Width High	tBCKH	14	-	-	ns
BICK "↑" to LRCK Edge (Note 35)	tBLR	14	-	-	ns
LRCK Edge to BICK "↑" (Note 35)	tLRB	14	-	-	ns
TDMO Setup time BICK "↑"	tBSS	5	-	-	ns
TDMO Hold time BICK "↑"	tBSH	5	-	-	ns
SDATA1/2 Hold Time	tSDH	5	-	-	ns
SDATA1/2 Setup Time	tSDS	5	-	-	ns
TDM512 Mode (TDM[1:0] bits/pins = "11")					
BICK Period					
Normal Speed mode	tBCK	1/512fsn	-	-	ns
BICK Pulse Width Low	tBCKL	14	-	-	ns
BICK Pulse Width High	tBCKH	14	-	-	ns
BICK "↑" to LRCK Edge (Note 35)	tBLR	14	-	-	ns
LRCK Edge to BICK "↑" (Note 35)	tLRB	14	-	-	ns
TDMO Setup time BICK "↑"	tBSS	5	-	-	ns
TDMO Hold time BICK "↑"	tBSH	5	-	-	ns
SDATA Hold Time	tSDH	5	-	-	ns
SDATA Setup Time	tSDS	5	-	-	ns

Note 35. It is defined so that LRCK edges do not occur at the same timing of a rising edge of BICK.

Parameter	Symbol	Min.	Typ.	Max.	Unit
PCM Audio Interface Timing					
External Digital Filter Mode					
BCK Period	tB	27	-	-	ns
BCK Pulse Width Low	tBL	10	-	-	ns
BCK Pulse Width High	tBH	10	-	-	ns
BCK "↑" to WCK Edge	tBW	5	-	-	ns
WCK Period	tWCK	1.3	-	-	μs
WCK Edge to BCK "↑"	tWB	5	-	-	ns
WCK Pulse Width Low	tWCKL	54	-	-	ns
WCK Pulse Width High	tWCKH	54	-	-	ns
DINL/R Hold Time	tDH	5	-	-	ns
DINL/R Setup Time	tDS	5	-	-	ns
BCK Period	tB	27	-	-	ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
DSD Audio Interface Timing					
Sampling Frequency	fs	30	44.1	48	kHz
(DSD64 Mode, DSDSEL[1:0] bits= "00")					
DCLK Period	tDCK	-	1/64fs	-	ns
DCLK Pulse Width Low	tDCKL	144	-	-	ns
DCLK Pulse Width High	tDCKH	144	-	-	ns
DCLK Edge to DSDL/R (Note 36)	tDDD	−20	-	20	ns
(DSD128 Mode, DSDSEL[1:0] bits = "01")					
DCLK Period	tDCK	-	1/128fs	-	ns
DCLK Pulse Width Low	tDCKL	72	-	-	ns
DCLK Pulse Width High	tDCKH	72	-	-	ns
DCLK Edge to DSDL/R (Note 36)	tDDD	−10	-	10	ns
(DSD256 Mode, DSDSEL[1:0] bits = "10")					
DCLK Period	tDCK	-	1/256fs	-	ns
DCLK Pulse Width Low	tDCKL	36	-	-	ns
DCLK Pulse Width High	tDCKH	36	-	-	ns
DCLK Edge to DSDL/R (Note 36)	tDDD	−5	-	5	ns
(DSD512 Mode, DSDSEL[1:0] bits = "11")					
DCLK Period	tDCK	-	1/512fs	-	ns
DCLK Pulse Width Low	tDCKL	18	-	-	ns
DCLK Pulse Width High	tDCKH	18	-	-	ns
DSDL/R Setup Time	tDDS	5	-	-	ns
DSDL/R Hold Time	tDDH	5	-	-	ns

Note 36. DSD data transmitting device must meet this time. "tDDD" is defined from DCLK "↓" until DSDL/R edge when DCKB bit = "0" (default), "tDDD" is defined from DCLK "↑" until DSDL/R edge when DCKB bit = "1". If the audio data format is in phase modulation mode, "tDDD" is defined from DCLK edge "↓" or "↑" until DSDL/R edge regardless of DCKB bit setting.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (3-wire Serial Control Mode):					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
Control Interface Timing (I^2C-Bus Control Mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 37)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF
Power-down & Reset Timing					
PDN Accept Pulse Width	tAPD	600	-	-	ns
PDN Reject Pulse Width	tRPD	-	-	30	ns

Note 37. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 38. I^2C -bus is a trademark of NXP B.V.

8.6. Timing Diagram

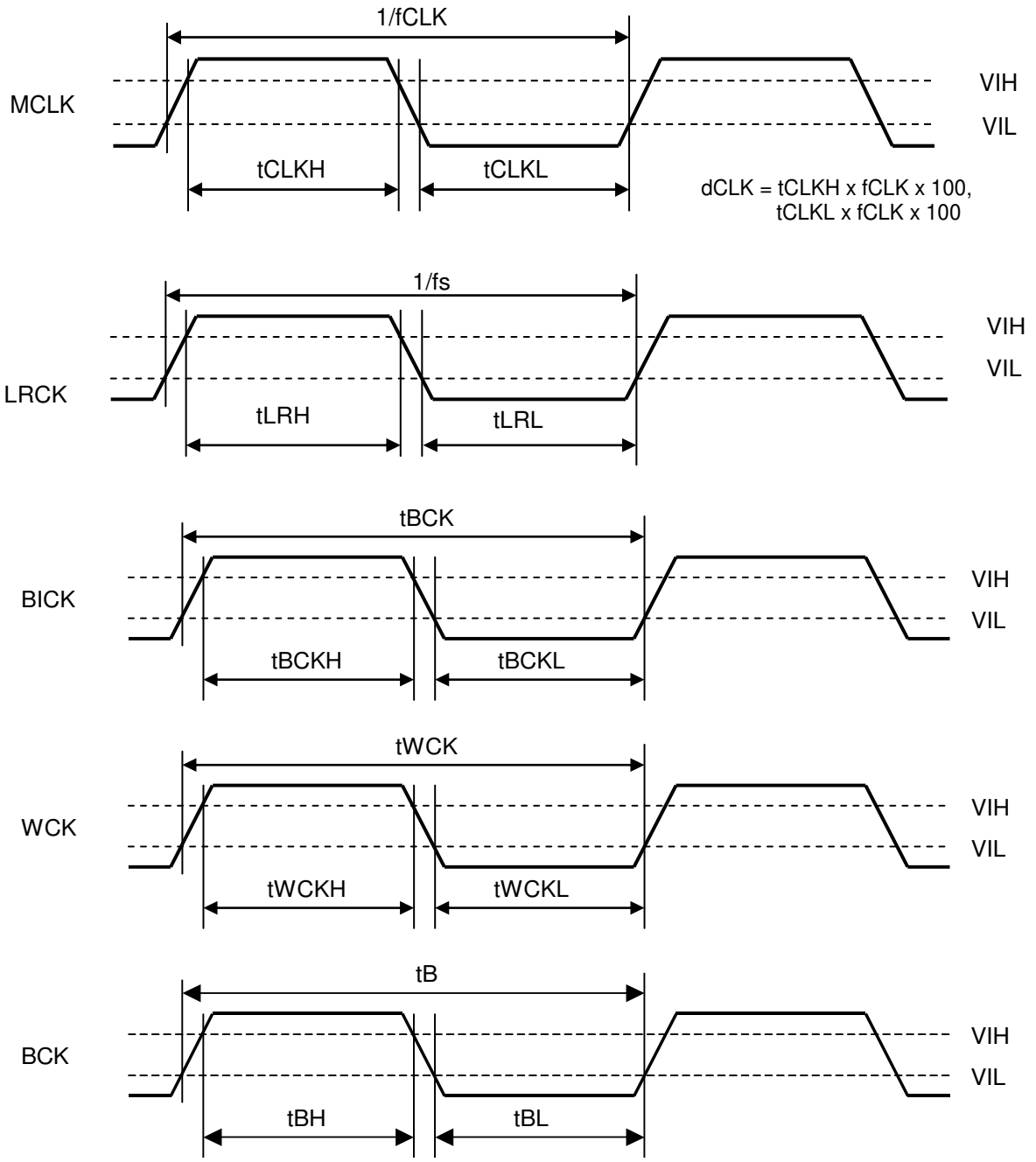


Figure 12. Clock Timing

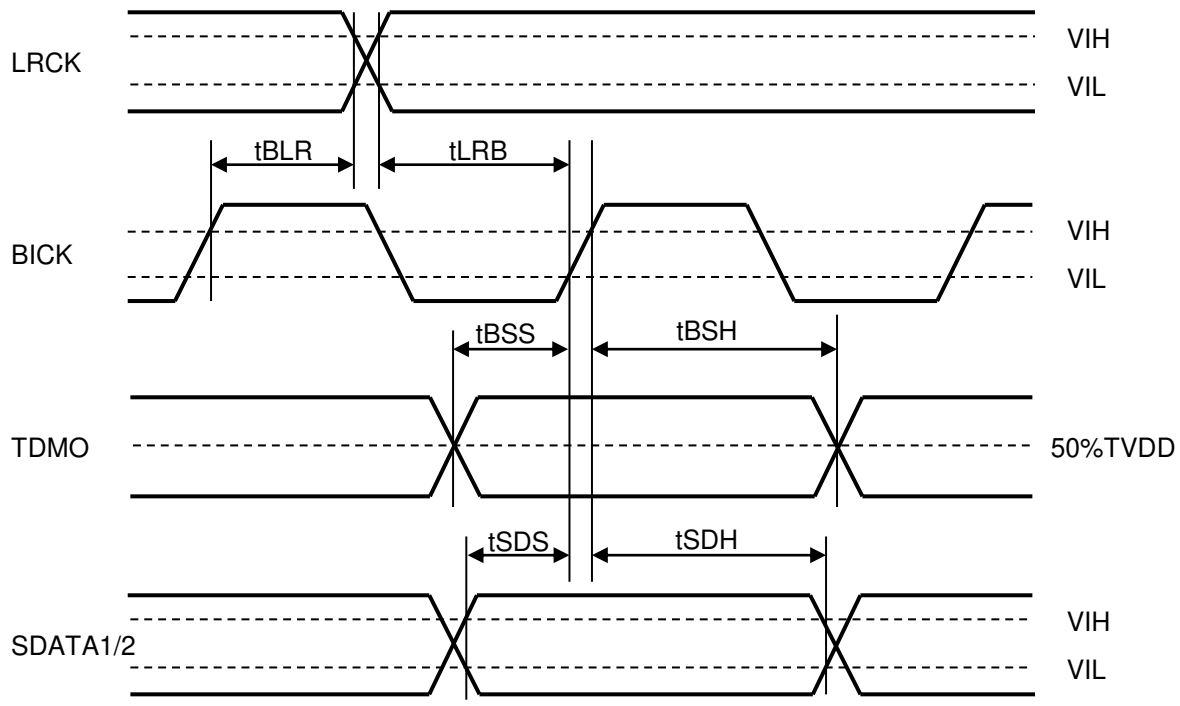


Figure 13. Audio Interface Timing (PCM Mode)

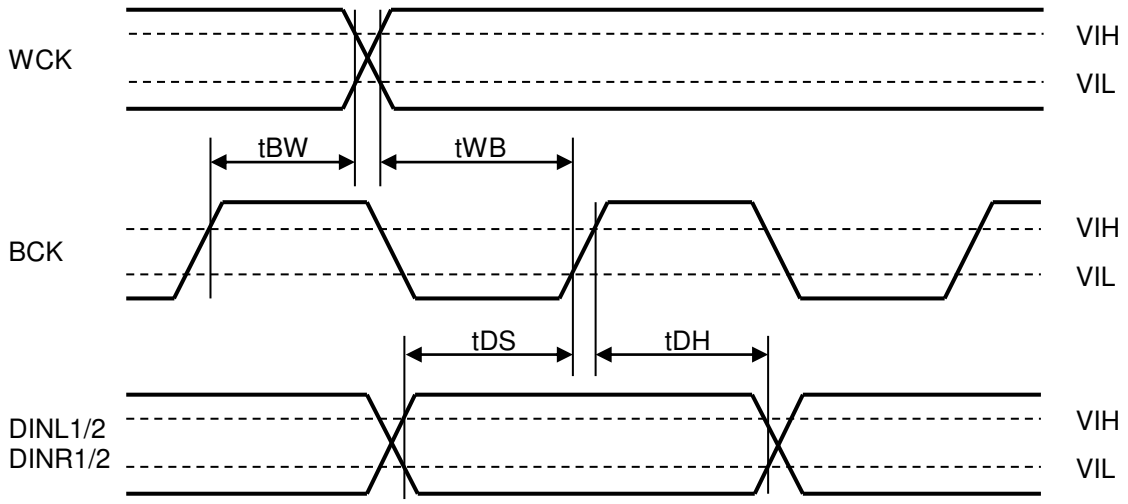
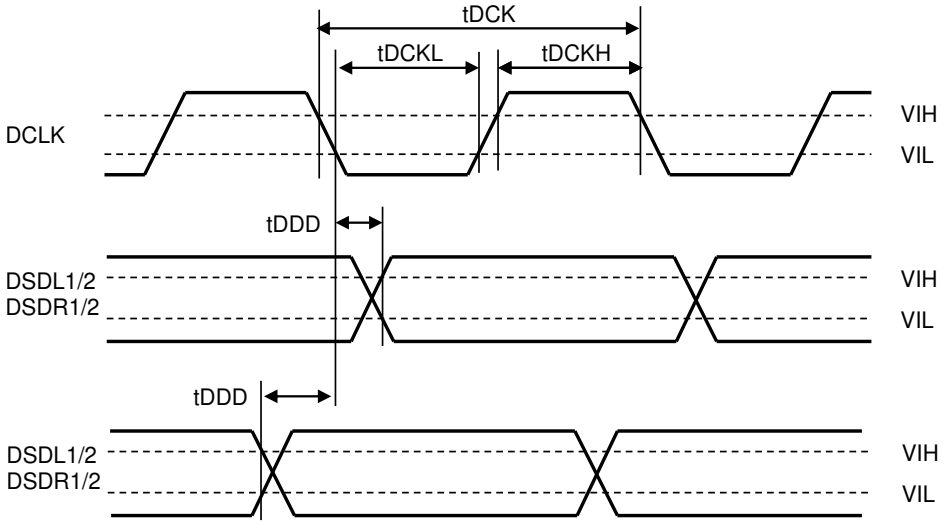
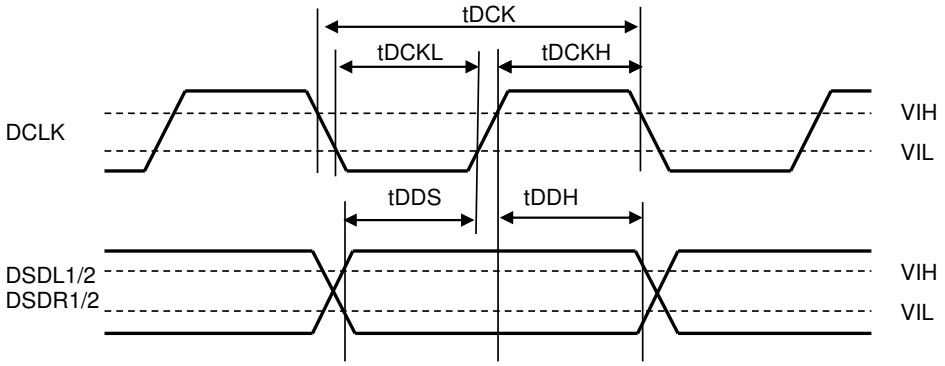


Figure 14. Audio Interface Timing (External Digital Filter I/F Mode)



DSD Audio Interface Timing (DSD64/128/256 Mode)



DSD Audio Interface Timing (DSD512 Mode)

Figure 15. Audio Interface Timing (DSD Mode, DCKB bit = “0”)

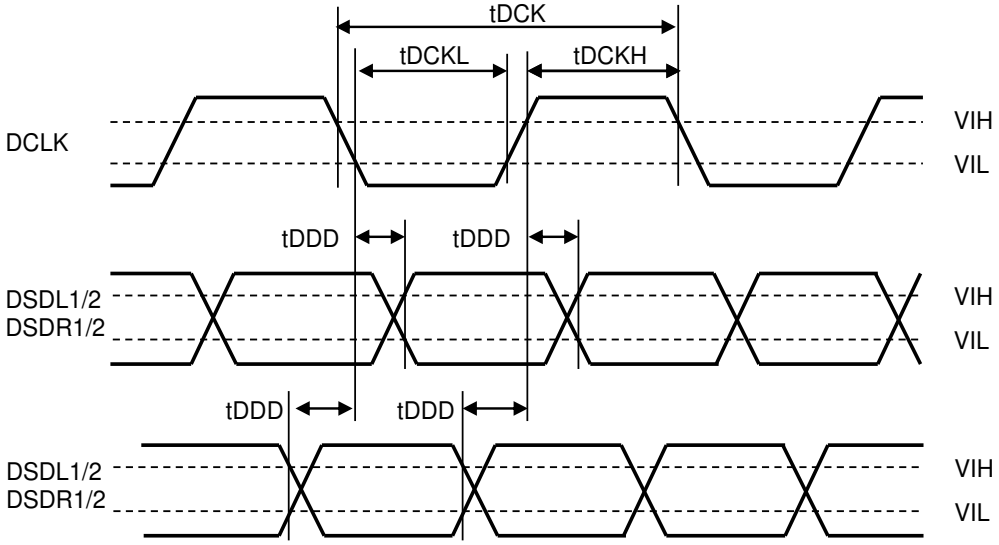


Figure 16. Audio Interface Timing (DSD Mode, Phase Modulation Format, DCKB bit = “0”)

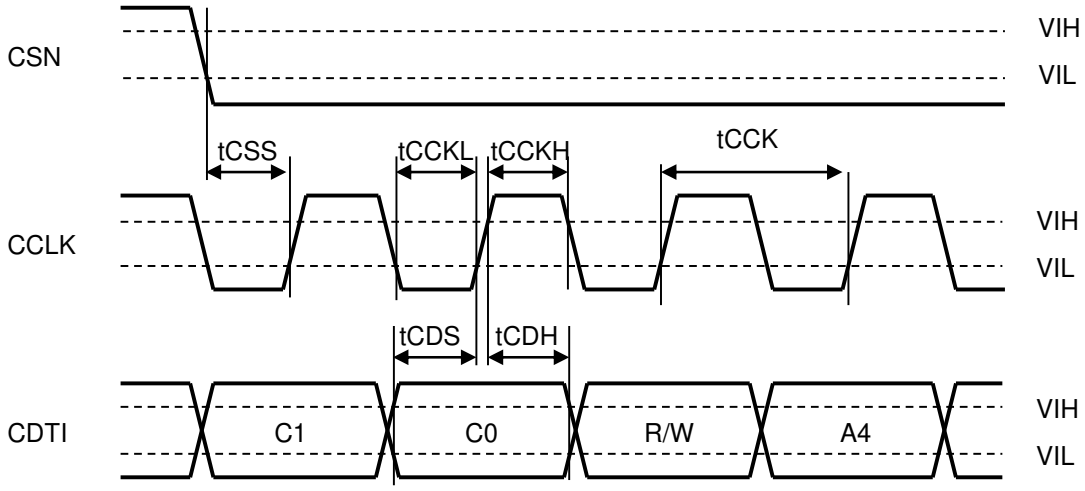


Figure 17. WRITE Command Input Timing (3-wire Serial Control Mode)

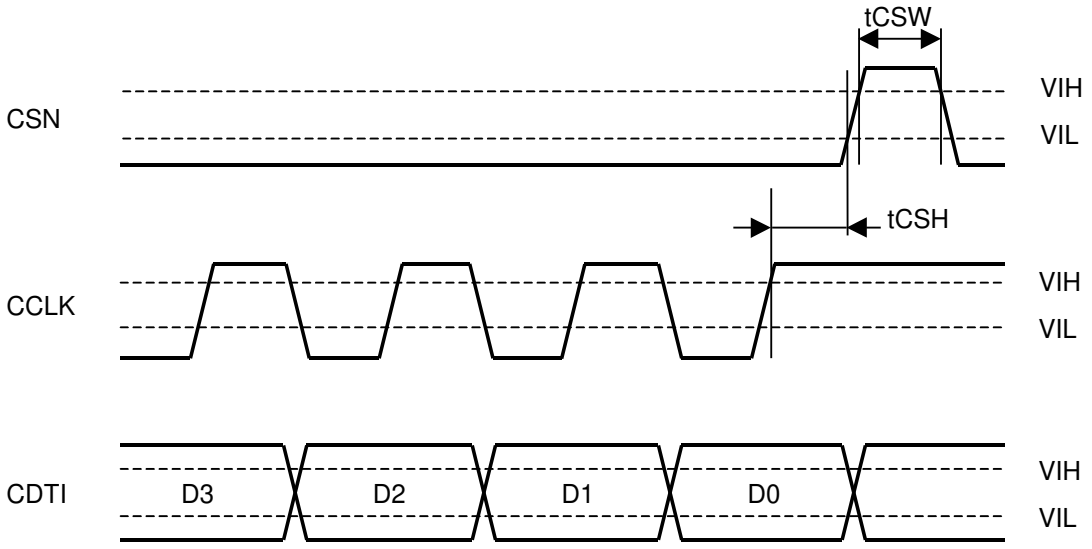


Figure 18. WRITE Data Input Timing (3-wire Serial Control Mode)

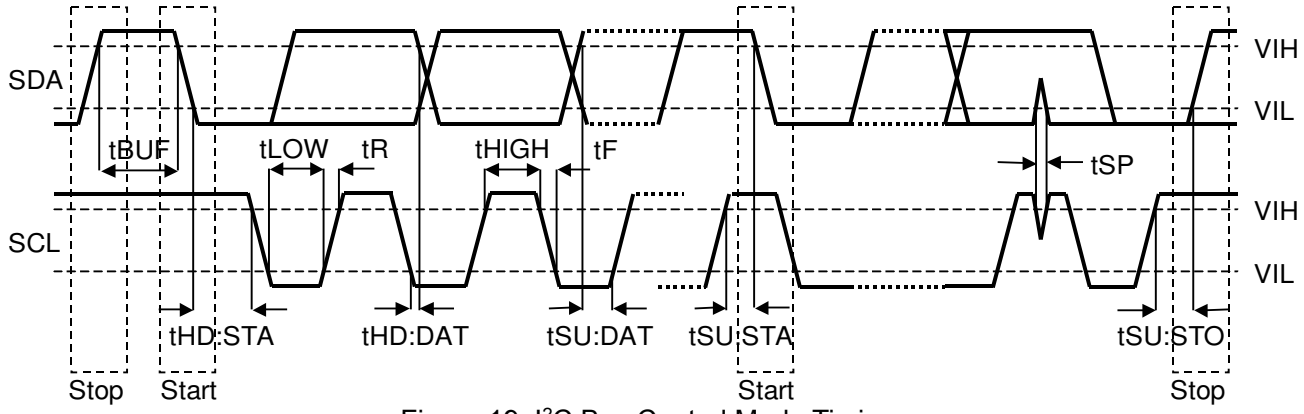


Figure 19. I²C Bus Control Mode Timing

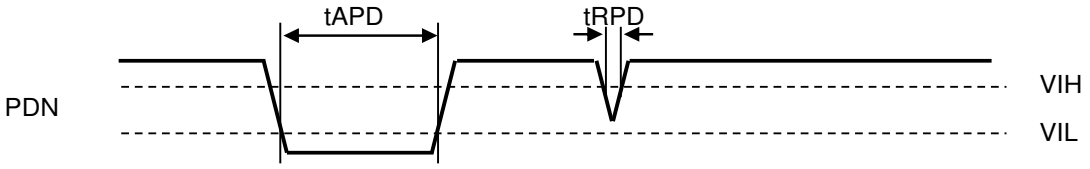


Figure 20. Power Down & Reset Timing

9. Functional Descriptions

9.1. Control Mode

Each function of the AK4499 is controlled by pins (Pin Control mode) or registers (Register Control mode) (Table 1). Select the control mode by setting the PSN pin. The AK4499 must be powered down by the PDN pin when changing the PSN pin setting. There is a possibility of malfunction if the device is not powered down when changing the control mode since the previous setting is not reinitialized. Register settings are invalid in Pin Control mode, and pin settings are invalid in Register Control mode. Table 2 shows available functions of each control mode.

Table 1. Pin/Register Control Mode Select

PSN pin	Control Mode
L	Register Control mode
H	Pin Control mode

Table 2. Function List @Pin/Register Control Mode
(Y: Available, N/A: Not available)

Function	Pin Control Mode	Register Control Mode
DSD Mode Select	N/A	Y
EXDF Mode Select	N/A	Y
System Clock Setting Select	Y	Y
Audio Format Select	Y	Y
TDM Mode	Y	Y
Daisy Chain	Y	Y
Digital Filter Select	Y	Y
De-emphasis Filter Select	Y	Y
Digital Attenuator	N/A	Y
Zero Detection	N/A	Y
Mono Mode	N/A	Y
Output signal select (Mono, Channel select)	N/A	Y
Output signal polarity select (Invert)	Y	Y
DSD Full Scale Detect	N/A	Y
Soft Mute	Y	Y
Register Reset	N/A	Y
Clock Synchronization Function disable (default: enable)	N/A	Y
Automatic Mode Switching (PCM/DSD, EXDF/DSD)	N/A	Y
Register Control	N/A	Y
Gain Control	N/A	Y

9.2. D/A Conversion Mode

The AK4499 is able to convert either PCM or DSD data to an analog signal. D/A conversion mode is in common for DAC1 and DAC2. In PCM mode, clocks and PCM data can be input from the BICK, LRCK and SDTI1/2 pins. In DSD mode, clocks and DSD data can be input from the DCLK, DSDL1/2 and DSDR1/2 pins.

The AK4499 supports external Digital Filter I/F (EXDF) in PCM data input mode. In EXDF mode, clocks and PCM data can be input from the MCLK, BCK, WCK, DINL1/2 and DINR1/2 pins. Table 3 shows available functions in PCM/DSD/EXDF mode.
The AK4499 only supports PCM mode in pin control mode.

Table 3. Function List of PCM/EXDF/DSD Mode @Register Control Mode
(Y: Available, N/A: Not available)

Function	Default State	Addr	Bit	PCM	EXDF	DSD
Automatic Mode Switching (PCM/DSD, EXDF/DSD)	Disable	15H	ADPE	Y	Y	Y
System clock setting @DSD mode	512fs	02H	DCKS	N/A	N/A	Y
System clock setting @EXDF mode	16fs (fs = 44.1 kHz)	00H	ECS	N/A	Y	N/A
Digital Filter select @DSD mode	39 kHz filter	09H	DSDF	N/A	N/A	Y
Digital Filter select @PCM mode	Short Delay Sharp Roll-off filter	01H, 02H, 05H	SD SLOW SSLOW	Y	N/A	N/A
De-emphasis Response	OFF	01H 0AH	DEM1[1:0] DEM2[1:0]	Y	N/A	N/A
Path select @ DSD mode	Normal Path	06H	DSDD	N/A	N/A	Y
Audio Data Interface Format @ PCM mode	32-bit MSB	00H	DIF[2:0]	Y	N/A	N/A
Audio Data Interface Format @ EXDF mode	32-bit LSB	00H	DIF[2:0]	N/A	Y	N/A
TDM Interface Format	Normal Mode	0AH	TDM[1:0]	Y	N/A	N/A
Daisy Chain	Disable	0BH	DCHAIN	Y	N/A	N/A
Attenuation Level	0 dB	03-04H 0C-0DH	ATTL1/2[7:0] ATTR1/2[7:0]	Y	Y	Y
Data Zero Detect Enable	Disable	01H	DZFE	Y	Y	Y
Inverting Enable of DZF	“H” active	02H	DZFB	Y	Y	Y
Mono/Stereo mode select	Stereo	02H, 0BH	MONO1/2	Y	Y	Y
Data Invert mode select	OFF	05H	INVL1/2 INVR1/2	Y	Y	Y
The data selection of L channel and R channel	L/R channel	02H-05H	SELLR1/2	Y	Y	Y
DSD Mute Function @ Full-scale Detected	Disable	06H	DDM	N/A	N/A	Y
Soft Mute Enable	Normal Operation	01H	SMUTE	Y	Y	Y
RSTN	Reset	00H	RSTN	Y	Y	Y
Clock Synchronization Function	Enable	07H	SYNCE	Y	Y	N/A

9.2.1. D/A Conversion Mode Setting and Pin Assignment

Switching PCM/DSD/EXDF mode is executed by setting DP bit and EXDF bit. In DSD mode, the input clock and the data input pin can be changed by DSDPATH bit. Register settings and pin assignment for each mode are shown below.

・PCM Mode
The AK4499 enters PCM mode by setting DP bit = “0” and EXDF bit = ”0”. Clock and data are input to the #43, #44, #45 and #46 pins in PCM mode (Table 4).

・DSD Mode
The AK4499 enters DSD mode by setting DP bit = “1”. In this case, EXDF bit setting will not be reflected on the circuit operation. In DSD mode, clock and data are input to the #50, #51, #52, #53 and #54 pins if DSDPATH bit = “0”, and are input to the #43, #44, #45, #46 and #47 pins if DSDPATH bit = “1” (Table 4).

・EXDF Mode
The AK4499 enters EXDF mode by setting DP bit = “0” and EXDF bit = “1”. Clock and data are input to the #43, #44, #45, #46 and #47 pins in EXDF mode (Table 4).

Table 4. PCM/DSD/EXDF Mode Control and Pin Assign (×: Do Not Care)

DP bit	EXDF bit	DSD PATH bit	D/A Conv. Mode	Pin Assign										
				#43 pin	#44 pin	#45 pin	#46 pin	#47 pin	#48 pin	#50 pin	#51 pin	#52 pin	#53 pin	#54 pin
0	0	×	PCM	BICK	SDATA1	LRCK	SDATA2	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
0	1	×	EXDF	BCK	DINL1	DINR1	DINL2	DINR2	WCK	Not Used	Not Used	Not Used	Not Used	Not Used
1	×	0	DSD	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	DSD L1	DSD R1	DCLK	DSD L2	DSD R2
		1		DCLK	DSDL1	DSDR1	DSDL2	DSDR2	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used

The AK4499 must be in reset state by setting RSTN bit = “0” when switching the data input mode (PCM/DSD/EXDF) by DP bit and EXDF bit or when changing DSD signal input path by DSDPATH bit. RSTN bit should not be changed for 4/fs after switching these modes. It takes 2 to 3/fs for mode transition.

Switching to DSD mode, manual and automatic settings are selectable. The AK4499 is in manual setting mode when ADPE bit = “0” and it is in automatic setting mode when ADPE bit = “1”. In automatic setting mode, the AK4499 monitors input signals to select PCM or DSD mode if EXDF bit = “0”, and it monitors input signals to select EXDF or DSD mode if EXDF bit = “1”. DP bit setting is ignored in this mode (ADPE bit = “1”). Refer to “9.11. PCM/DSD, EXDF/DSD Automatic Mode Switching Function” for details.

9.2.2. D/A Conversion Mode Switching Timing (Manual Setting)

Figure 21, Figure 22 and Figure 23 show switching timing of PCM, DSD and EXDF modes in manual mode (ADPE bit = "0"). To prevent noise caused by excessive input, DSD signal should be input 4/fs after setting RSTN bit = "0" until the device is completely reset internally when the conversion mode is changed to DSD mode from PCM/EXDF mode. DSD signal should be stopped 4/fs after setting RSTN bit = "0" until the device is completely reset internally when the conversion mode is changed to PCM/EXDF from DSD mode.

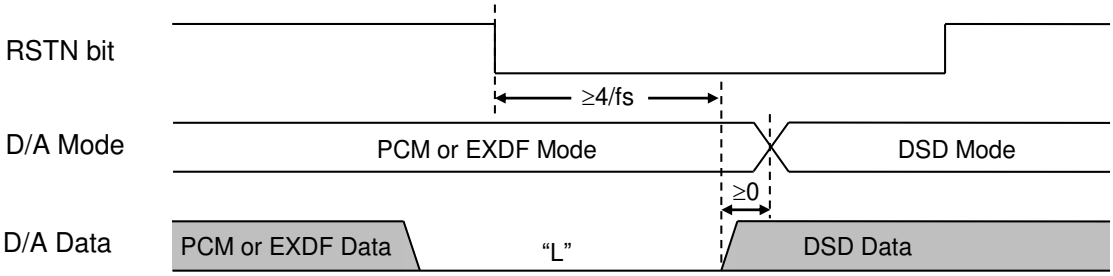


Figure 21. D/A Mode Switching Timing (from PCM/EXDF Mode to DSD Mode)

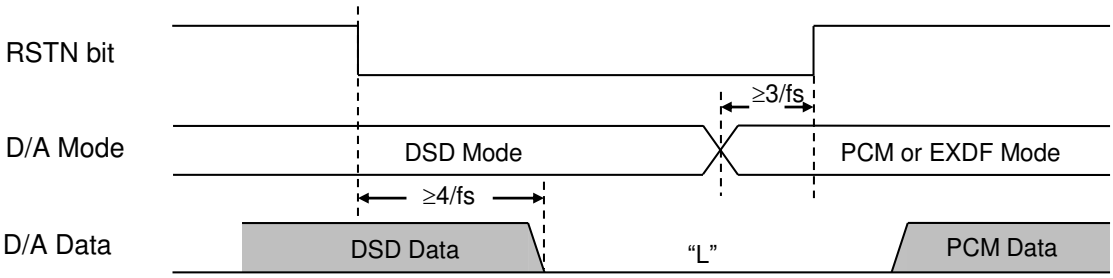


Figure 22. D/A Mode Switching Timing (from DSD Mode to PCM/EXDF Mode)

Figure 23 shows switching timing of PCM and EXDF modes. Set EXDF bit 4/fs after setting RSTN bit = "0" until the device is completely reset internally when changing the conversion mode.

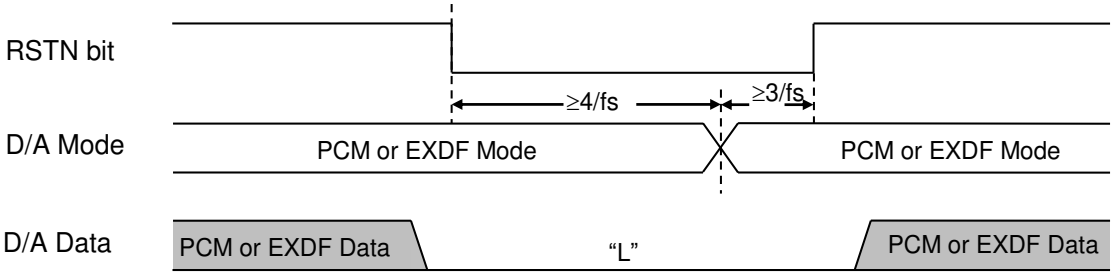


Figure 23. D/A Mode Switching Timing (from PCM Mode to EXDF Mode)

9.3. System Clock

9.3.1. PCM Mode

The external clocks, which are required to operate the AK4499, are MCLK, BICK and LRCK. MCLK, BICK and LRCK should be synchronized but the phase of MCLK is not critical. MCLK is used to operate the digital filter, the delta sigma modulator and SR DAC.
For the internal sampling speed mode and MCLK-to-LRCK divider setting, there are two system clock setting modes in pin control mode and there are three setting modes in register control mode (Table 5, Table 6).

Table 5. System Clock Setting Mode @Pin Control Mode

ACKS pin	Mode	
0	Fixed Speed mode	(default)
1	Auto Setting mode	

Table 6. System Clock Setting Mode @Register Control Mode (×: Do not care)

AFSD bit	ACKS bit	Mode	
0	0	Manual Setting mode	(default)
0	1	Auto Setting mode	
1	×	fs Auto Detect mode	

The AK4499 is automatically placed in standby state when MCLK is stopped for more than 1 μs during normal operation, and the analog output becomes Hi-z state (Table 47).
When MCLK is input again, the AK4499 exits this power down state and starts operation again. In this case, register settings are not initialized. The AK4499 is in power down state and the analog output is floating state (Hi-z) until MCLK, BICK and LRCK are supplied.

9.3.1.1. Fixed Speed Mode (Pin Control Mode)

The AK4499 will be in fixed speed mode by setting ACKS pin = “L” in pin control mode. In this mode, the sampling speed is fixed to normal speed mode. The MCLK frequency corresponding to each sampling speed should be provided externally (Table 7).

Table 7. System Clock Example (Fixed Speed Mode) (N/A: Not available)

LRCK	MCLK (MHz)								BICK	Sampling
fs	128fs	192fs	256fs	384fs	512fs	768fs	1024fs	1152fs	64fs	Speed
32.0 kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	2.0480 MHz	Normal
44.1 kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	N/A	2.8224 MHz	
48.0 kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	N/A	3.0720 MHz	

9.3.1.2. Manual Setting Mode (Register Control Mode Only)

The AK4499 will be in manual setting mode by setting AFSD bit = "0" and ACKS bit = "0" in register control mode. In manual setting mode, sampling speed is set by DFS[2:0] bits (Table 8). The MCLK frequency corresponding to each sampling speed should be provided externally (Table 9, Table 10). The AK4499 is in manual setting mode when power down is released (PDN pin = "L" → "H"). After changing the sampling speed by DFS[2:0] bits, reset the AK4499 once by setting RSTN bit. This function is only supported in register control mode.

Table 8. Sampling Speed (Manual Setting Mode)

DFS[2:0] bits	Sampling Speed	Sampling Rate (fs)	
000	Normal Speed mode	7.2 kHz ~ 54 kHz	(default)
001	Double Speed mode	54 kHz ~ 108 kHz	
010	Quad Speed mode	108 kHz ~ 216 kHz	
011	Quad Speed mode	108 kHz ~ 216 kHz	
100	Oct Speed mode	216 kHz ~ 388 kHz	
101	Hex Speed mode	388 kHz ~ 776 kHz	
110	Oct Speed mode	216 kHz ~ 388 kHz	
111	Hex Speed mode	388 kHz ~ 776 kHz	

Table 9. System Clock Example (Manual Setting Mode) (N/A: Not available)

LRCK	MCLK(MHz)						Sampling Speed
fs	16fs	32fs	48fs	64fs	96fs	128fs	
32.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal
44.1 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
48.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	N/A	22.5792	Quad
192.0 kHz	N/A	N/A	N/A	N/A	N/A	24.5760	
352.8 kHz	N/A	11.2896	16.9344	22.5792	33.8688	N/A	Oct
384 kHz	N/A	12.2880	18.4320	24.5760	36.8640	N/A	
705.6 kHz	11.2896	22.5792	33.8688	45.1584	N/A	N/A	Hex
768 kHz	12.2880	24.5760	36.8640	49.1520	N/A	N/A	

Table 10. System Clock Example (Manual Setting Mode) (N/A: Not available)

LRCK	MCLK(MHz)							Sampling Speed
fs	192fs	256fs	384fs	512fs	768fs	1024fs	1152fs	
32.0 kHz	N/A	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	Normal
44.1 kHz	N/A	11.2896	16.9344	22.5792	33.8688	N/A	N/A	
48.0 kHz	N/A	12.2880	18.4320	24.5760	36.8640	N/A	N/A	
88.2 kHz	N/A	22.5792	33.8688	45.1584	N/A	N/A	N/A	Double
96.0 kHz	N/A	24.5760	36.8640	49.1520	N/A	N/A	N/A	
176.4 kHz	33.8688	45.1584	N/A	N/A	N/A	N/A	N/A	Quad
192.0 kHz	36.8640	49.1520	N/A	N/A	N/A	N/A	N/A	
352.8 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Oct
384 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
705.6 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Hex
768 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

9.3.1.3. Auto Setting Mode

The AK4499 will be in auto setting mode by setting ACKS pin = “H” in pin control mode, or AFSD bit = “0” and ACKS bit = “1” in register control mode. In auto setting mode, the MCLK and LRCK frequency ratio is detected to automatically set the sampling speed mode (Table 11). Therefore, sampling speed setting is not necessary. The frequencies of MCLK corresponding to each sampling speed mode should be input externally (Table 12, Table 13).

Table 11. Sampling Speed (Auto Setting Mode)

MCLK		Sampling Speed
1024fs/1152fs		Normal (fs ≤ 32 kHz)
512fs/256fs (*)	768fs/384fs (*)	Normal
256fs	384fs	Double
128fs	192fs	Quad
64fs	96fs	Oct
16fs/32fs	48fs	Hex

Table 12. System Clock Example (Auto Setting Mode) (N/A: Not available)

LRCK	MCLK (MHz)						Sampling Speed
fs	32fs	48fs	64fs	96fs	128fs	192fs	
32.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal
44.1 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
48.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	22.5792	33.8688	Quad
192.0 kHz	N/A	N/A	N/A	N/A	24.5760	36.8640	
352.8 kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	Oct
384.0 kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	
705.6 kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	Hex
768.0 kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	

Table 13. System Clock Example (Auto Setting Mode) (N/A: Not available)

LRCK	MCLK (MHz)						Sampling Speed
fs	256fs	384fs	512fs	768fs	1024fs	1152fs	
32.0 kHz	8.1920(*)	12.2880(*)	16.3840	24.5760	32.7680	36.8640	Normal
44.1 kHz	11.2896(*)	16.9344(*)	22.5792	33.8688	N/A	N/A	
48.0 kHz	12.2880(*)	18.4320(*)	24.5760	36.8640	N/A	N/A	
88.2 kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	Double
96.0 kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Quad
192.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
352.8 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Oct
384.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
705.6 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Hex
768.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	

(*) When MCLK = 256fs/384fs, auto setting mode supports sampling rates of 8kHz to 96kHz. However, the oversampling ratio is adjusted from 128 to 64 resulting in ~3dB SNR loss and increased out-of-band noise for sampling rates under 54 kHz.

9.3.1.4. fs Auto Detect Mode (Register Control Mode Only)

The AK4499 will be in fs auto setting mode by setting AFSD bit = "1" in register control mode. In fs auto setting mode, the MCLK and LRCK frequency ratio is detected to set the sampling speed mode automatically. Therefore, sampling speed setting is not necessary. The frequencies of MCLK corresponding to each sampling speed mode should be input externally (Table 14, Table 15).
It takes 8/fs to 9/fs for mode transition after setting AFSD bit = "1".

Table 14. System Clock Example (N/A: Not available)

LRCK	MCLK (MHz)						Sampling Speed
fs	16fs	32fs	48fs	64fs	96fs	128fs	
32.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal
44.1 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
48.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	N/A	22.5792	Quad
192.0 kHz	N/A	N/A	N/A	N/A	N/A	24.5760	
352.8 kHz	N/A	11.2896	16.9344	22.5792	33.8688	N/A	Oct
384 kHz	N/A	12.2880	18.4320	24.5760	36.8640	N/A	
705.6 kHz	11.2896	22.5792	33.8688	45.1584	N/A	N/A	Hex
768 kHz	12.2880	24.5760	36.8640	49.1520	N/A	N/A	

Table 15. System Clock Example (N/A: Not available)

LRCK	MCLK (MHz)							Sampling Speed
fs	192fs	256fs	384fs	512fs	768fs	1024fs	1152fs	
32.0 kHz	N/A	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	Normal
44.1 kHz	N/A	11.2896	16.9344	22.5792	33.8688	N/A	N/A	
48.0 kHz	N/A	12.2880	18.4320	24.5760	36.8640	N/A	N/A	
88.2 kHz	N/A	22.5792	33.8688	45.1584	N/A	N/A	N/A	Double
96.0 kHz	N/A	24.5760	36.8640	49.1520	N/A	N/A	N/A	
176.4 kHz	33.8688	45.1584	N/A	N/A	N/A	N/A	N/A	Quad
192.0 kHz	36.8640	49.1520	N/A	N/A	N/A	N/A	N/A	
352.8 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Oct
384 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
705.6 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Hex
768 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

In fs auto detect mode, auto detection result of the sampling speed can be read out by ADFS[2:0] bits (Table 16).

Table 16. Relationship between ADFS[2:0] bits and Sampling Speed

ADFS[2:0] bits Read Result	Mode
000	Normal Speed mode
001	Double Speed mode
010	Quad Speed mode
011	Quad Speed mode
100	Oct Speed mode
101	Hex Speed mode
110	Oct Speed mode
111	Hex Speed mode

9.3.2. DSD Mode (Register Control Mode Only)

The external clocks that are required in DSD mode are MCLK and DCLK. MCLK should be synchronized with DCLK but the phase is not critical. The frequency of MCLK is set by DCKS bit (Table 17). The AK4499 is automatically placed in standby state when MCLK is stopped during normal operation (PDN pin = "H"), and the analog output becomes Hi-z state. When the reset is released (PDN bit = "0" → "1"), the AK4499 is in power-down state until MCLK and DCLK are input.

Table 17. System Clock (DSD Mode, fs = 32 kHz, 44.1 kHz, 48 kHz)

DCKS bit	MCLK Frequency	DCLK Frequency	
0	512fs	64fs/128fs/256fs/512fs	(default)
1	768fs	64fs/128fs/256fs/512fs	

The AK4499 supports DSD data stream rates of DSD64, DSD128, DSD256 and DSD512 modes. The data sampling speed is selected by DSDSEL[1:0] bits (Table 18).

Table 18. DSD data stream select DSDSEL[1:0] bits	DSD Mode	DCLK Frequency	DSD data stream			
			fs = 32 kHz	fs = 44.1 kHz	fs = 48 kHz	
00	DSD64	64fs	2.048 MHz	2.8224 MHz	3.072MHz	(default)
01	DSD128	128fs	4.096 MHz	5.6448 MHz	6.144MHz	
10	DSD256	256fs	8.192 MHz	11.2896 MHz	12.288MHz	
11	DSD512	512fs	16.284 MHz	22.5792 MHz	24.576MHz	

The AK4499 has a Volume bypass function for play backing DSD signal. Two modes are selectable by DSDD bit (Table 19). When setting DSDD bit = "1", the output volume control and zero detect functions are not available.

Table 19. DSD Play Back Path Selection

DSDD	Mode	
0	Normal Path	(default)
1	Volume Bypass	

9.3.3. External Digital Filter Mode (EXDF Mode, Register Control Mode Only)

The external clocks that are required in EXDF mode are MCLK, BCK and WCK. The BCK and MCLK clocks must be the same frequency and continuous, not burst mode. BCK and MCLK frequencies for each sampling speed are shown in Table 20. Set ECS bit according to Table 20.

The AK4499 is automatically placed in standby state when an MCLK edge is not detected during normal operation, and the analog output becomes Hi-Z state. When the reset is released (RSTN bit = "0" → "1"), the AK4499 is in standby state until MCLK, BCK and WCK are input.

Table 20. System Clock Example (EXDF Mode) N/A: Not available

Sampling Speed[kHz]	ECS bit	MCLK&BCK (MHz)			
		32fs	48fs	64fs	96fs
352.8 kHz	1	11.2896	16.9344	22.5792	33.8688
384 kHz	1	12.288	18.432	24.576	36.864
705.6 kHz	0	22.5792	33.8688	N/A	N/A
768 kHz	0	24.576	36.864	N/A	N/A

9.4. Audio Interface Format

9.4.1. PCM Mode

9.4.1.1. Input Data Format

Four data modes, such as Normal Mode, TDM128, TDM256, and TDM512 Modes, are available. Mode settings are available by the pins (TDM0/1 pins and DIF0/1/2 pins) and registers (TDM[1:0] bits and DIF[2:0] bits). The AK4499 must be reset by setting RSTN bit when the format setting is changed during operation.

Normal Mode (TDM[1:0] bits = “00” or TDM1 pin = “L”, TDM0 pin = “L”)

4-ch Data is shifted in via the SDATA1/2 pins using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF0/1/2 pins or DIF[2:0] bits as shown in Table 21. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Mode 2 can be used for 16-bit and 20-bit, Mode 6 can be used for 16-bit, 20-bit and 24-bit MSB justified formats by zeroing the unused LSBs.

TDM128 Mode (TDM[1:0] bits = “01” or TDM1 pin = “L”, TDM0 pin = “H”)

In Register Control mode up to 8-ch Data is shifted in via the SDATA1/2 pins using BICK and LRCK inputs. In Pin Control mode up to 4-ch data is supported via the SDATA1 pin. BICK is fixed to 128fs. Six data formats are supported and selected by the DIF[2:0] bits or DIF0/1/2 pins as shown in Table 21. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Refer to Data Slot Selection Function or Daisy Chain mode for options to route data to DAC outputs.

TDM256 Mode (TDM[1:0] bits = “10” or TDM1 pin = “H”, TDM0 pin = “L”)

In Register Control mode up to 16-ch Data is shifted in via the SDATA1/2 pins using BICK and LRCK inputs. In Pin Control mode up to 8-ch data is supported via the SDATA1 pin. .BICK is fixed to 256fs. Six data formats are supported and selected by the DIF[2:0] bits or DIF0/1/2 pins as shown in Table 21. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Refer to Data Slot Selection Function or Daisy Chain mode for options to route data to DAC outputs.

TDM512 Mode (TDM[1:0] bit = “11” or TDM1 pin = “H”, TDM0 pin = “H”)

Up to 16-ch Data is shifted in via the SDATA1 pin using BICK and LRCK inputs. Input data to the SDATA2 pin is ignored. BICK is fixed to 512fs. Six data formats are supported and selected by the DIF[2:0] bits or DIF0/1/2 pins as shown in Table 21. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Refer to Data Slot Selection Function or Daisy Chain mode for options to route data to DAC outputs.

Table 21. Audio Interface Format (N/A: Not available)

Mode		TDM[1:0] bits/pins	DIF[2:0] bits/pins	SDATA1/2 Format	LRCK	BICK	Figure	
Normal (Note 39)	0	00	000	16-bit LSB justified	H/L	≥32fs	Figure 24	
	1		001	20-bit LSB justified	H/L	≥40fs	Figure 25	
	2		010	24-bit MSB justified	H/L	≥48fs	Figure 26	
	3		011	16-bit I²S compatible	L/H	32fs	Figure 27	
				24-bit I²S compatible	L/H	≥48fs		
	4		100	24-bit LSB justified	H/L	≥48fs	Figure 25	
	5		101	32-bit LSB justified	H/L	≥64fs	Figure 28	
	6		110	32-bit MSB justified	H/L	≥64fs	Figure 29	(default)
	7		111	32-bit I²S compatible	L/H	≥64fs	Figure 30	
TDM128		01	000	N/A	N/A	N/A	N/A	
			001	N/A	N/A	N/A	N/A	
	8		010	24-bit MSB justified	H/L	128fs	Figure 31	
	9		011	24-bit I²S compatible	L/H	128fs	Figure 32	
	10		100	24-bit LSB justified	H/L	128fs	Figure 33	
	11		101	32-bit LSB justified	H/L	128fs	Figure 31	
	12		110	32-bit MSB justified	H/L	128fs	Figure 31	
	13		111	32-bit I²S compatible	L/H	128fs	Figure 32	
TDM256		10	000	N/A	N/A	N/A	N/A	
			001	N/A	N/A	N/A	N/A	
	14		010	24-bit MSB justified	H/L	256fs	Figure 34	
	15		011	24-bit I²S compatible	L/H	256fs	Figure 35	
	16		100	24-bit LSB justified	H/L	256fs	Figure 36	
	17		101	32-bit LSB justified	H/L	256fs	Figure 34	
	18		110	32-bit MSB justified	H/L	256fs	Figure 34	
	19		111	32-bit I²S compatible	L/H	256fs	Figure 35	
TDM512		11	000	N/A	N/A	N/A	N/A	
			001	N/A	N/A	N/A	N/A	
	20		010	24-bit MSB justified	H/L	512fs	Figure 37	
	21		011	24-bit I²S compatible	L/H	512fs	Figure 38	
	22		100	24-bit LSB justified	H/L	512fs	Figure 39	
	23		101	32-bit LSB justified	H/L	512fs	Figure 37	
	24		110	32-bit MSB justified	H/L	512fs	Figure 37	
	25		111	32-bit I²S compatible	L/H	512fs	Figure 38	

Note 39. The cycle numbers of BICK for each channel must be the same as the bit length setting or more. L channel data can be input when LRCK = “H” and R channel data can be input when LRCK = “L” if the LRCK indication is “H/L”. L channel data can be input when LRCK = “L” and R channel data can be input when LRCK = “H” if the LRCK indication is “L/H”.

Note 40. In Pin Control mode, replace “0” to “L” and “1” to “H” for setting.

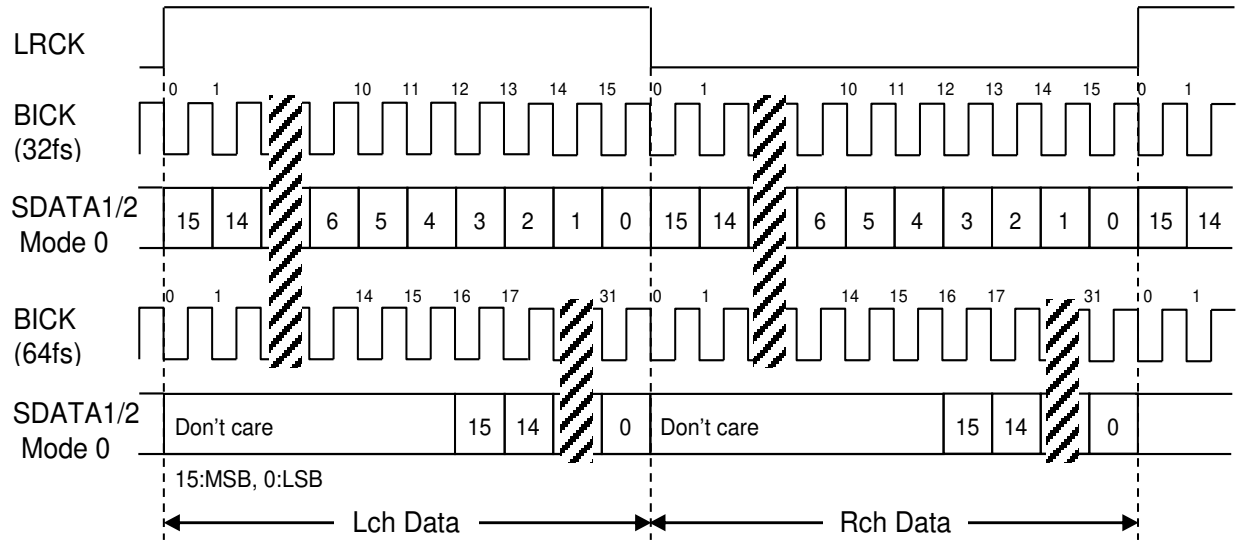


Figure 24. Mode 0 Timing

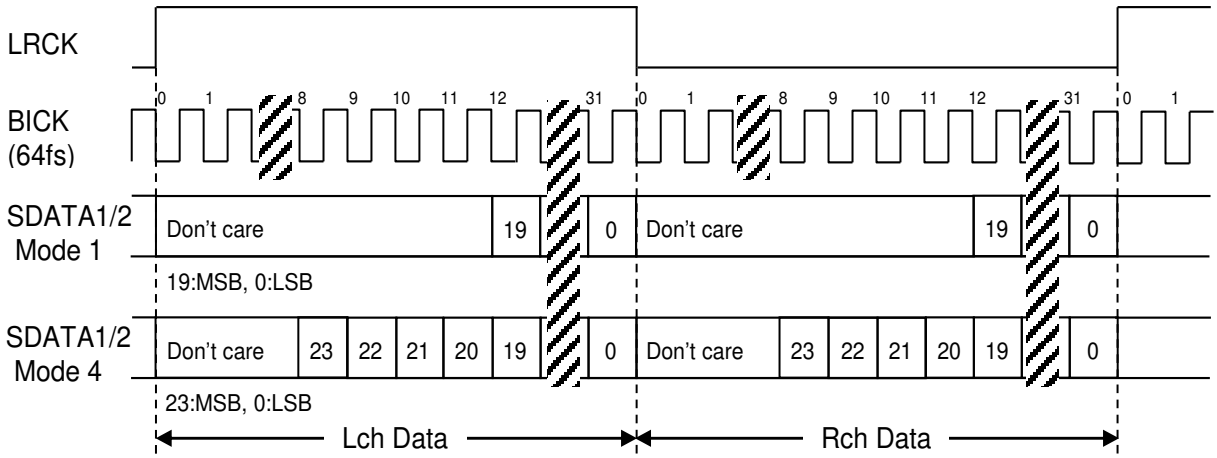


Figure 25. Mode 1, 4 Timing

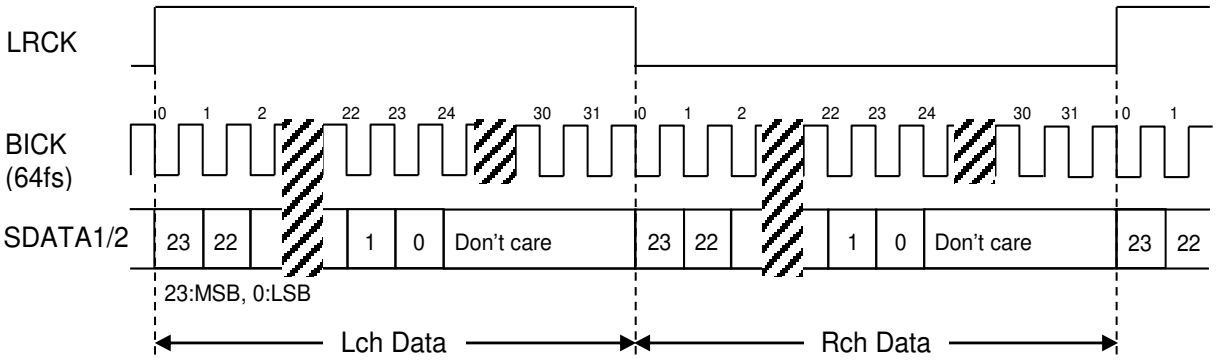


Figure 26. Mode 2 Timing

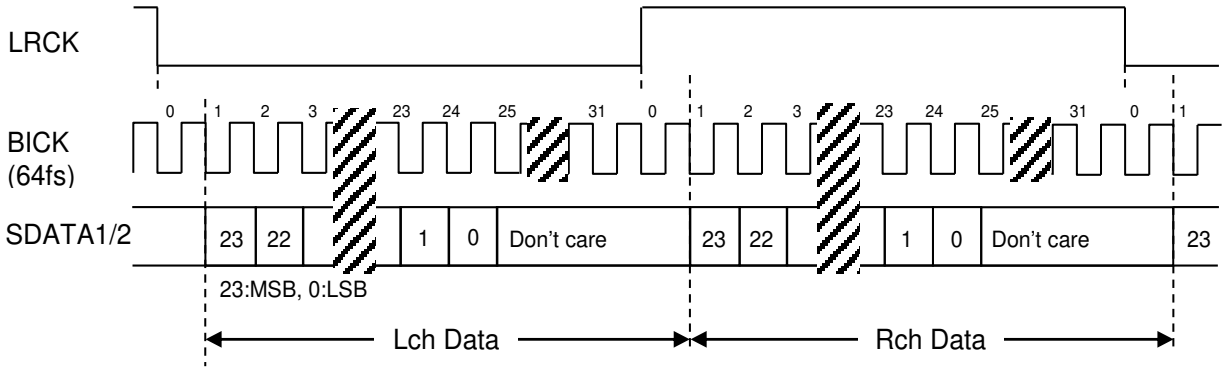


Figure 27. Mode 3 Timing

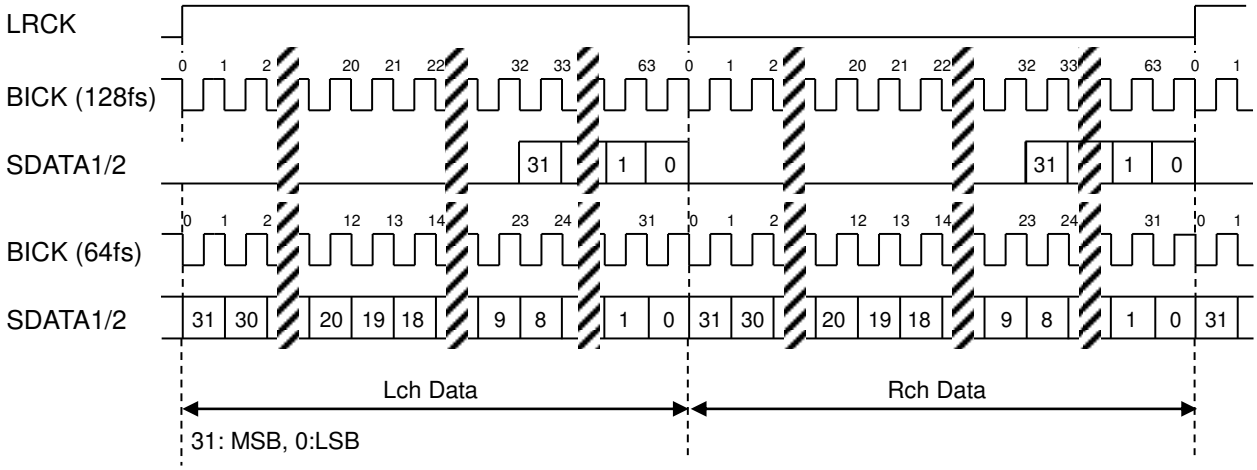


Figure 28. Mode 5 Timing

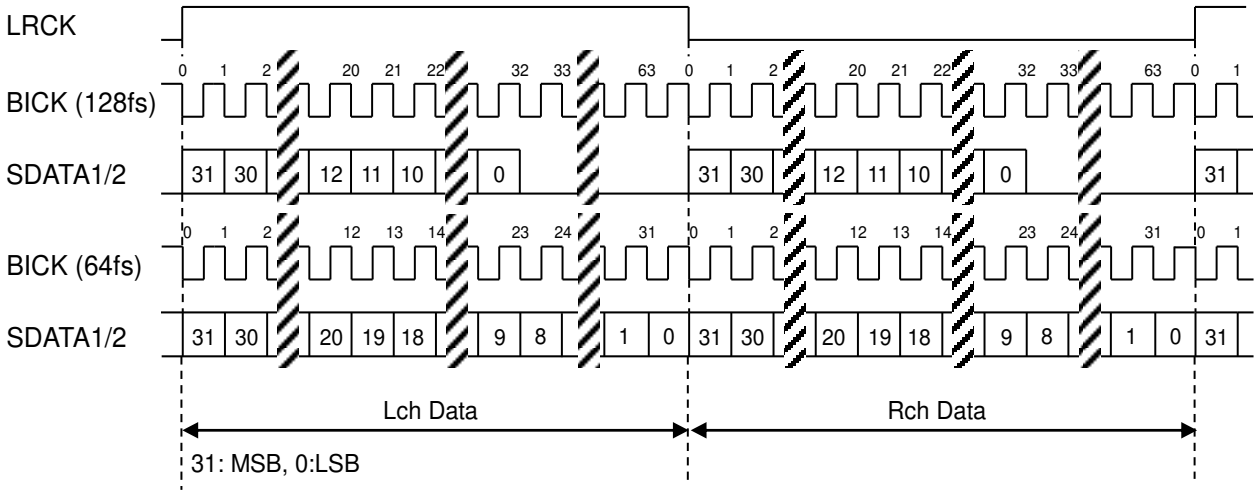


Figure 29. Mode 6 Timing

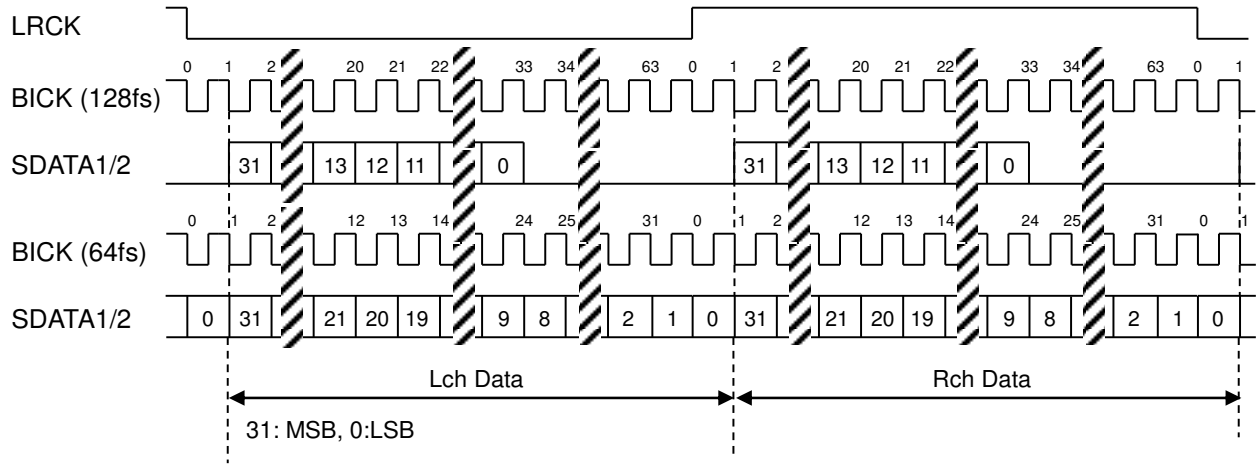


Figure 30. Mode 7 Timing

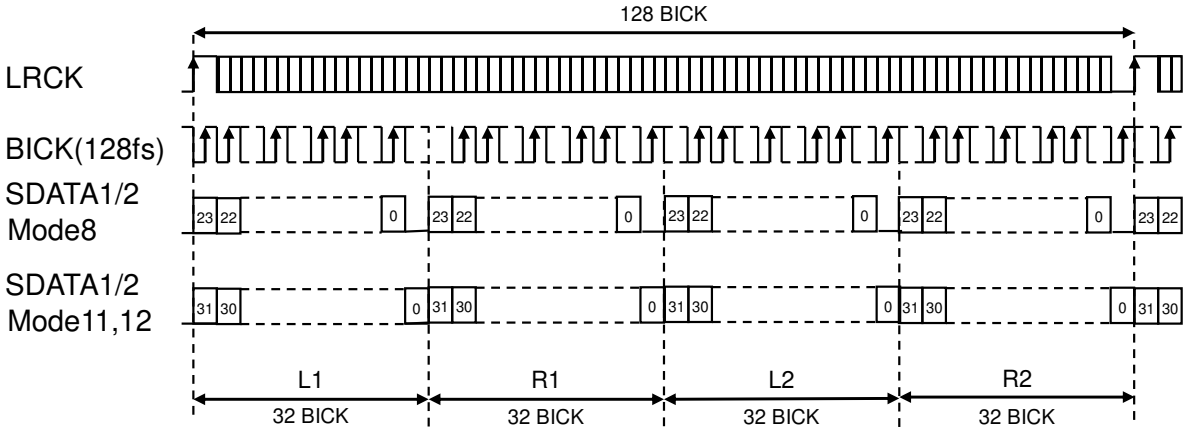


Figure 31. Mode 8/11/12 Timing

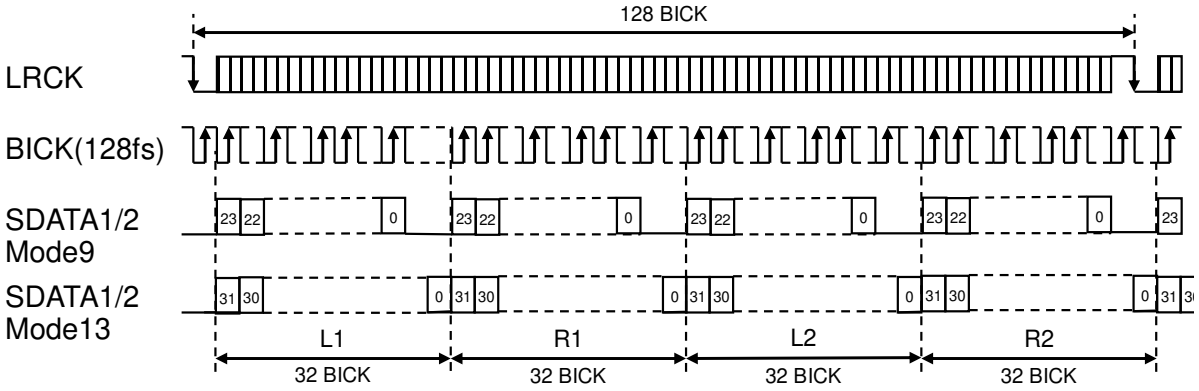


Figure 32. Mode 9/13 Timing

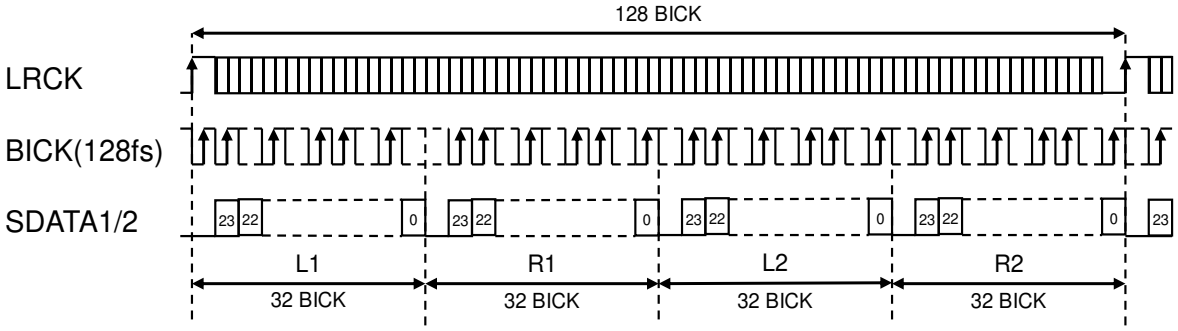


Figure 33. Mode 10 Timing

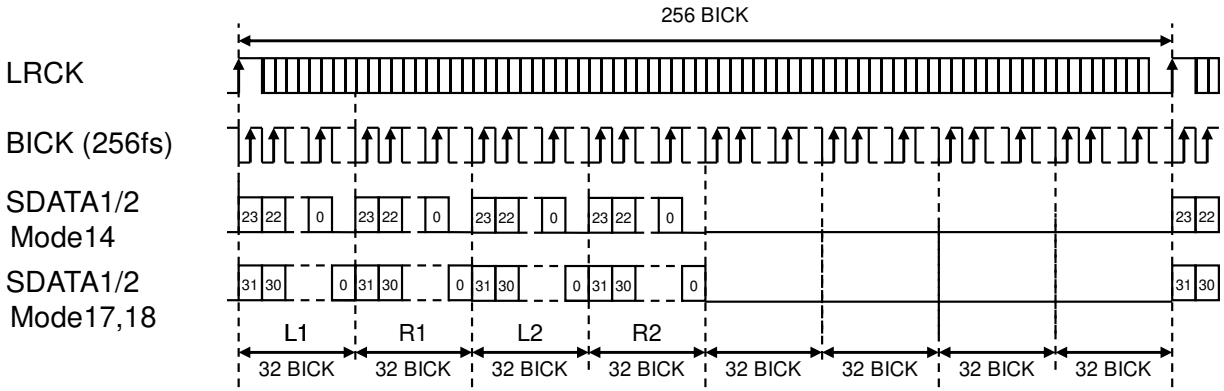


Figure 34. Mode 14/17/18 Timing

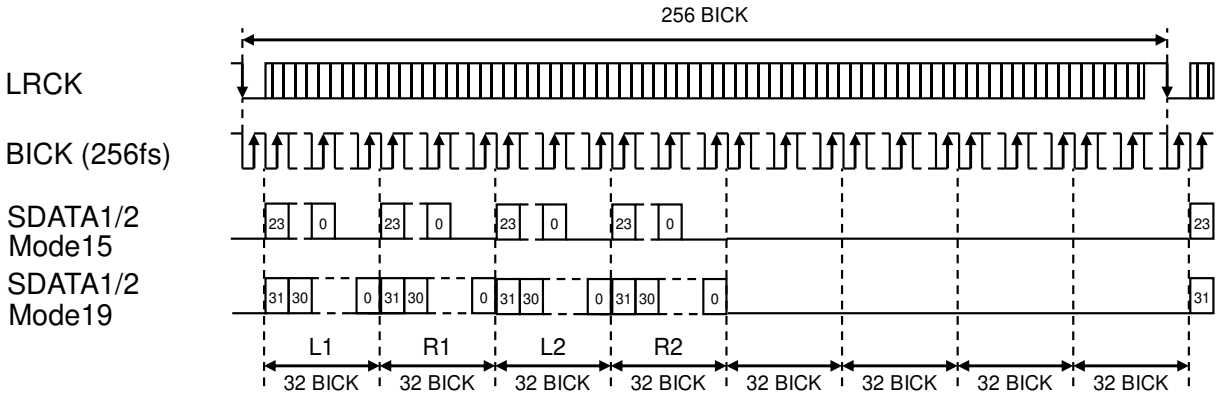


Figure 35. Mode 15/19 Timing

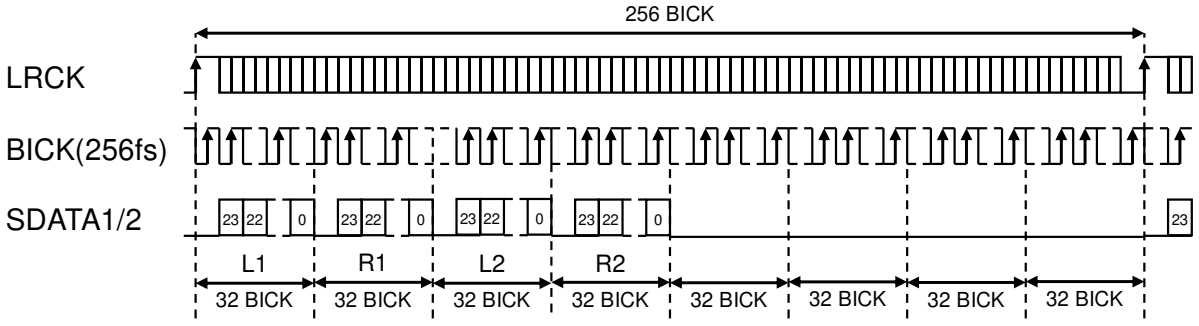


Figure 36. Mode 16 Timing

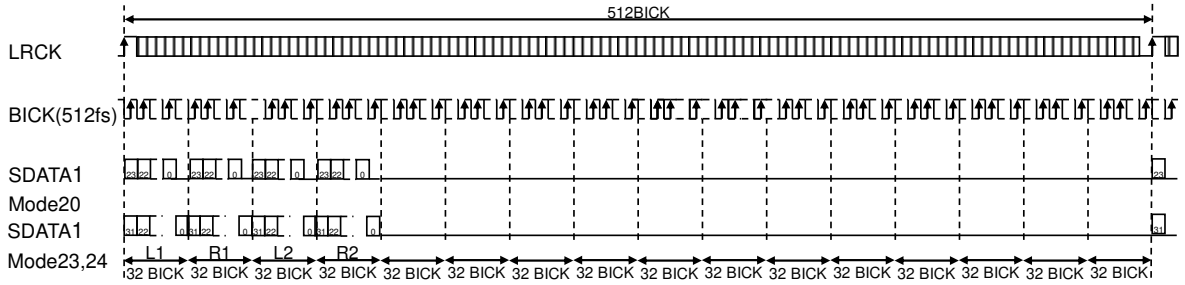


Figure 37. Mode 20/23/24 Timing

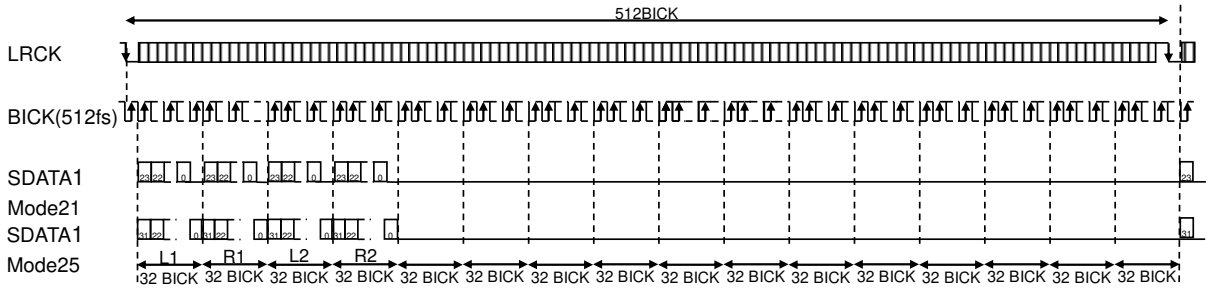


Figure 38. Mode 21/25 Timing

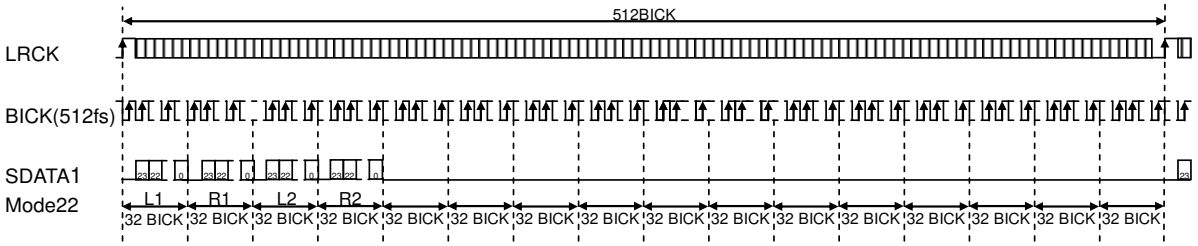


Figure 39. Mode 22 Timing

9.4.1.2. Data Slot Selection Function (Register Control Mode)

Data slot of 1cycle LRCK for each audio data format is defined as Figure 40, Figure 41, Figure 42 and Figure 43. DAC output data can be selected by SDS[2:0] bits (Register Control mode only), as shown in Table 22.

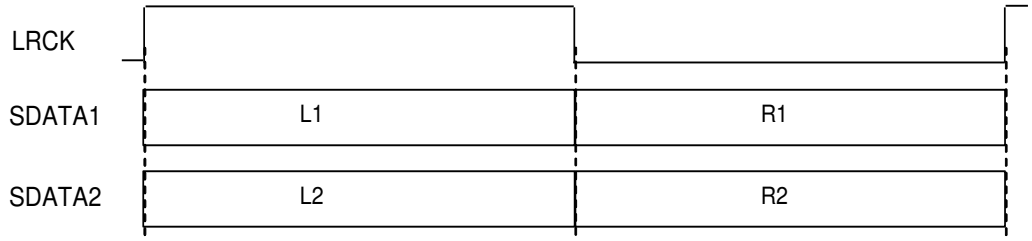


Figure 40. Data Slot in Normal Mode

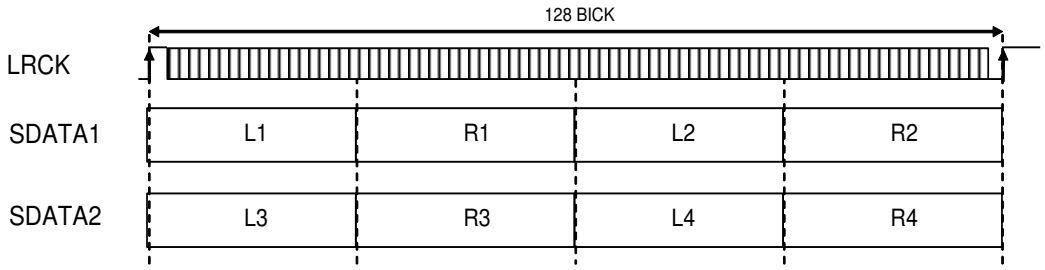


Figure 41. Data Slot in TDM128 Mode

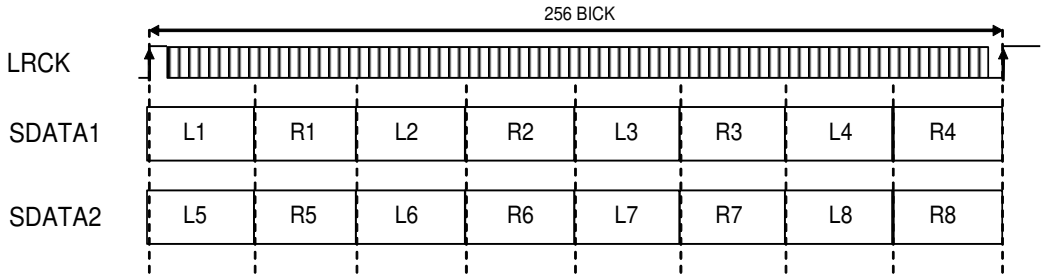


Figure 42. Data Slot in TDM256 Mode

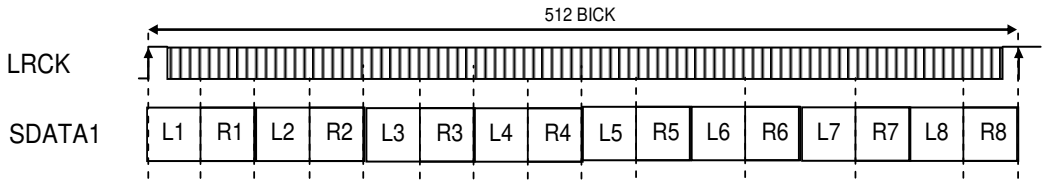


Figure 43. Data Slot in TDM512 Mode

Table 22. Data Select (×: Do not care)

TDM[1:0] bits	SDS[2:0] bits	DAC1		DAC2	
		Lch	Rch	Lch	Rch
00	×××	L1	R1	L2	R2
01	×00	L1	R1	L2	R2
	×01	L2	R2	L3	R3
	×10	L3	R3	L4	R4
	×11	L4	R4	L1	R1
10	000	L1	R1	L2	R2
	001	L2	R2	L3	R3
	010	L3	R3	L4	R4
	011	L4	R4	L5	R5
	100	L5	R5	L6	R6
	101	L6	R6	L7	R7
	110	L7	R7	L8	R8
	111	L8	R8	L1	R1
11	000	L1	R1	L2	R2
	001	L2	R2	L3	R3
	010	L3	R3	L4	R4
	011	L4	R4	L5	R5
	100	L5	R5	L6	R6
	101	L6	R6	L7	R7
	110	L7	R7	L8	R8
	111	L8	R8	L1	R1

9.4.1.3. Daisy Chain

In TDM512/256 mode, multiple AK4499s can be connected by Daisy Chain. Daisy Chain mode can be configured from DCHAIN bit or DCHAIN pin (Table 23). SDS[2:0] bits setting will be ignored in Daisy Chain mode.

Table 23 Daisy Chain Control

DCHAIN bit DCHAIN pin	Daisy Chain Mode	TDMO pin	
0	Disable	L	(default)
1	Enable	Data output	

9.4.1.3.1. TDM512 Mode

Figure 44 shows an example of TDM512 mode Daisy Chain structure (TDM[1:0] bits= “11”). 16ch data is input to the second AK4499’s SDATA1 pin from a DSP. Connect the second AK4499’s TDMO pin to the first AK4499’s SDATA1 pin.

Figure 45 shows a data I/O example of TDM512 mode. SDATA1 (L/7/8, R7/8) data is the input for the DAC of the second AK4499, and the second AK4499 outputs the data from TDMO by shifting 4ch. The first AK4499 accepts SDATA1 (L5/6, R5/6) data as input data of DAC. DIF[2:0] bits setting or DIF0/1/2 pins setting of both first AK4499 and the second AK4499 must be the same.

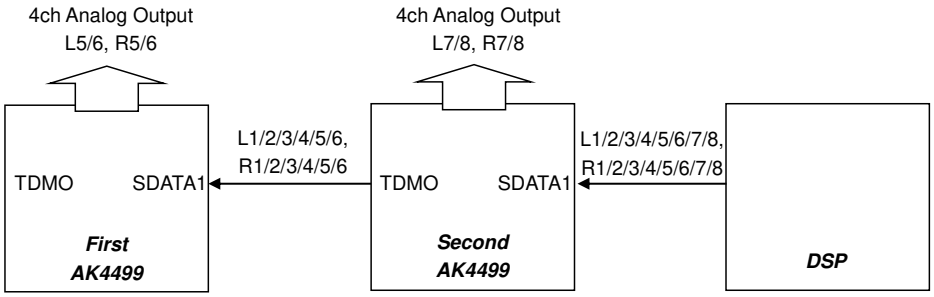


Figure 44. Daisy Chain (TDM512 Mode)

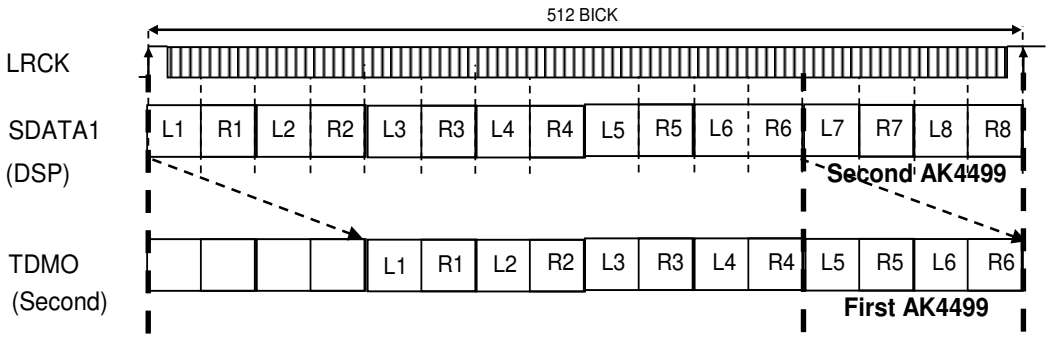


Figure 45. Daisy Chain (TDM512 Mode)

9.4.1.3.2. TDM256 Mode

Figure 46 shows an example of TDM256 mode Daisy Chain structure (TDM[1:0] bits = “10”). 8ch data is input to the second AK4499’s SDATA1 pin from a DSP. Connect the second AK4499’s TDMO pin to the first AK4499’s SDATA1 pin.

Figure 47 shows a data I/O example of TDM256 mode. SDATA1 (L3/4, R3/4) data is the input for the DAC of the second AK4499, and the second AK4499 outputs the data from TDMO by shifting 4ch. The first AK4499 accepts SDATA1 (L1/2, R1/2) data as input data of DAC. DIF[2:0] bits setting or DIF0/1/2 pins setting of both first AK4499 and the second AK4499 must be the same.

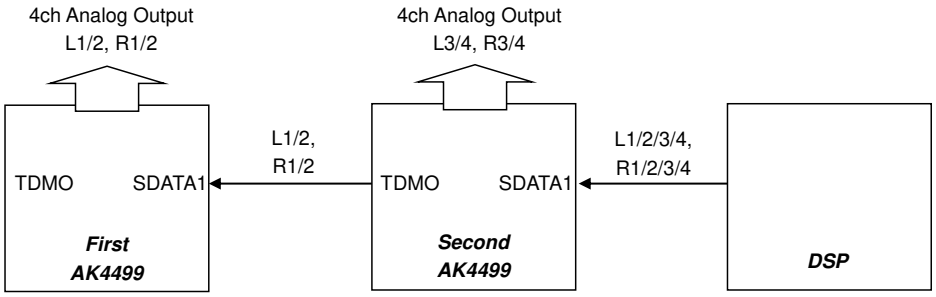


Figure 46. Daisy Chain (TDM256 Mode)

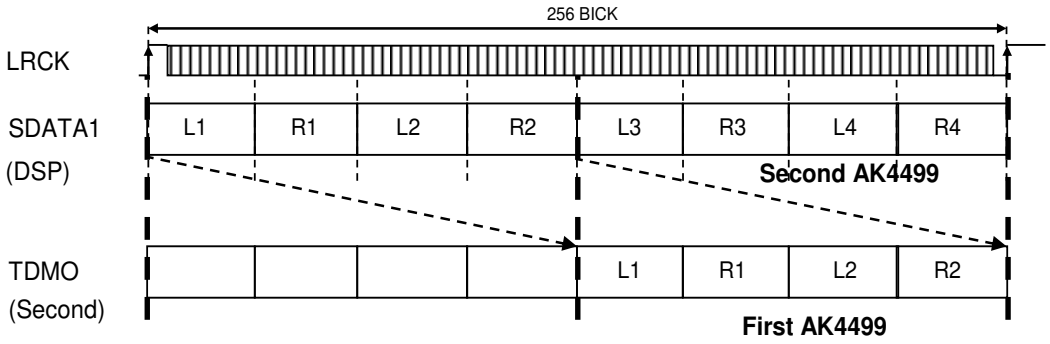


Figure 47. Daisy Chain (TDM256 Mode)

9.4.2. DSD Mode (Register Control Mode Only)

4ch Data is shifted in via the DSDL1/2 and DSDR1/2 pins using DCLK inputs (Figure 48). DSD data is supported by both Normal mode and Phase Modulation mode (Figure 49). The AK4499 does not support phase modulation when DCLK is 512fs (DSDSEL[1:0] bits = “11”).

Polarity of DCLK is possible to invert by DCKB bit. Input data is clocked in on a rising edge of DCLK when DCKB bit = “0” and it is clocked in on a falling edge of DCLK when DCKB bit = “1”.
In case of DSD mode, the setting of DIF[2:0] bits is ignored.

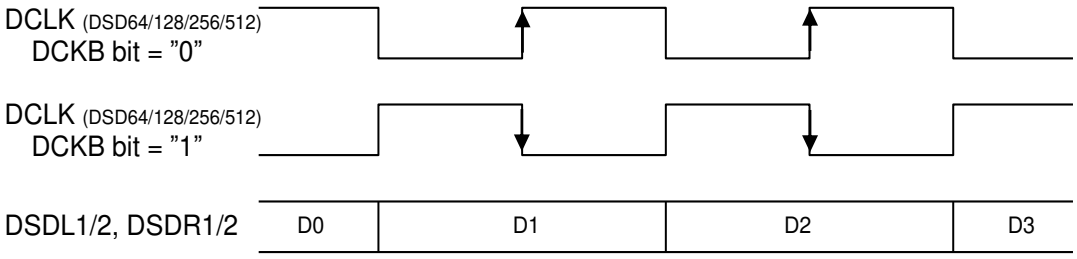


Figure 48. DSD Mode Timing

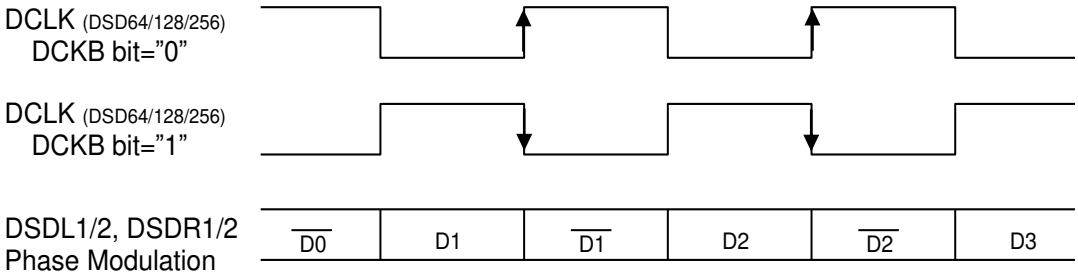


Figure 49. DSD Mode Timing (Phase Modulation Format)

9.4.3. External Digital Filter Mode (EXDF Mode; Register Control Mode Only)

The audio data is input by BCK and WCK from the DINL1/2 and DINR1/2 pins. Three formats are available (Table 24) by DIF[2:0] bits setting. The data is latched on the rising edge of BCK. The BCK and MCLK clocks must not burst.

Table 24. Audio Interface Format (EXDF Mode) (N/A: Not available)

Mode	DIF[2:0] bits	Input Format	
0	000	16-bit LSB justified	
-	001	N/A	
0	010	16-bit LSB justified	
-	011	N/A	
1	100	24-bit LSB justified	
2	101	32-bit LSB justified	
1	110	24-bit LSB justified	(default)
2	111	32-bit LSB justified	

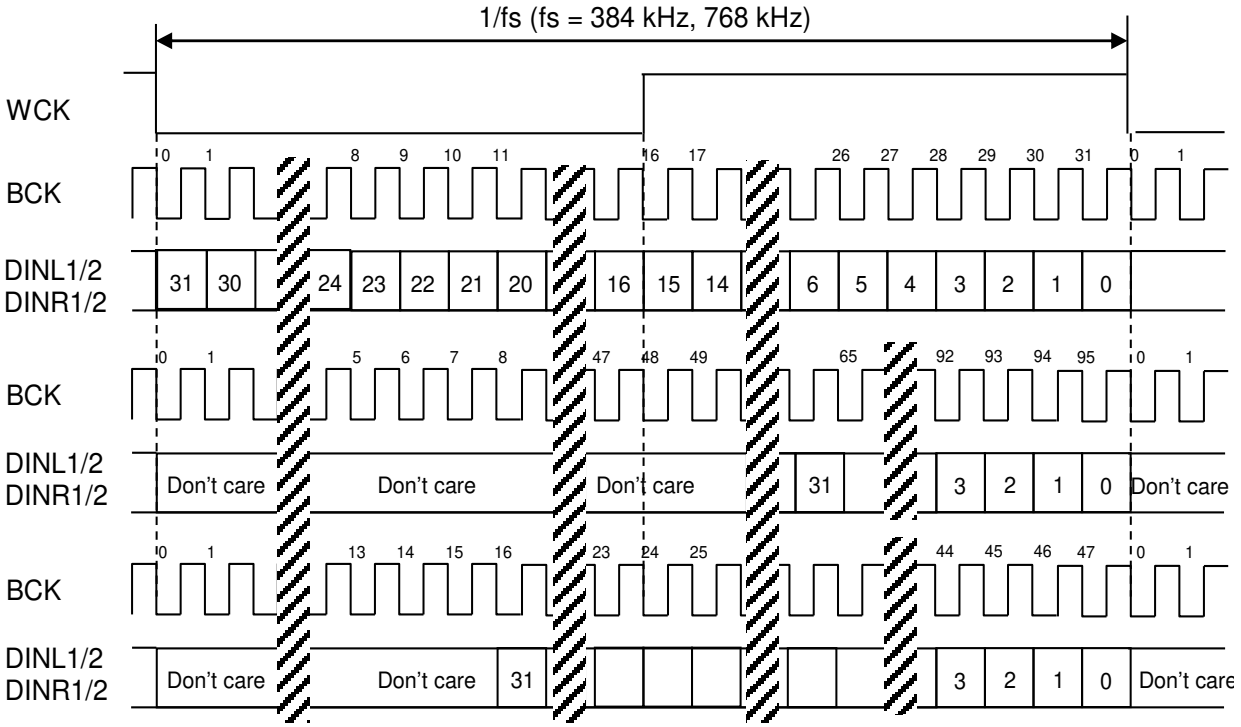


Figure 50. EXDF Mode Timing (32-bit LSB justified)

9.5. Digital Filter

Six types of digital filter in PCM mode and two types of digital filter in DSD mode are available in the AK4499 for sound color selection of music playback.

9.5.1. PCM Mode

In PCM mode, the digital filter can be selected by the SD, SLOW and SSLOW pins if the AK4499 is in Pin Control mode, and it can be selected by the SD, SLOW and SSLOW bits in Register Control mode (Table 25).

Table 25. Digital Filter Setting (N/A: not available)

SSLOW	SD	SLOW	Mode	
0	0	0	Sharp Roll-off filter	
0	0	1	Slow Roll-off filter	
0	1	0	Short Delay Sharp Roll-off filter	(default)
0	1	1	Short Delay Slow Roll-off filter	
1	0	0	Super Slow Roll-off filter	
1	0	1	Super Slow Roll-off filter	
1	1	0	Low Dispersion Short Delay filter	
1	1	1	N/A	

9.5.2. DSD Mode

In DSD64/128 mode, the cutoff frequency of digital filter can be switched by the DSDF bit. Table 26 shows the cutoff frequency @fs = 44.1 kHz.

Table 26. DSD Filter Select (×: Do Not Care)

DSD rate	DSDF bit	Internal DSD Filter Cut Off Frequency @fs = 44.1 kHz
DSD64@DSDF bit = ”0”	0	37 kHz
DSD64@DSDF bit = ”1”	1	65 kHz
DSD128@DSDF bit = ”0”	0	74 kHz
DSD128@DSDF bit = ”1”	1	131 kHz
DSD256	×	238 kHz
DSD512	×	476 kHz

However, GC[1:0] bits must not be set to “00” when DSDD bit = “0” and DSDF bit = “1” in DSD64/128 mode, or when DSDD bit = “0” in DSD256/512 mode. Otherwise a pop noise may occur.

9.6. De-emphasis Filter (PCM Mode)

The AK4499 has a de-emphasis function by IIR filter (50/15 μs). This function is only valid in PCM Normal Speed mode.

In Register Control mode, a digital de-emphasis filter is available for 32kHz*, 44.1kHz or 48kHz* sampling rates (tc = 50/15μs) and is enabled or disabled by DEM1/2[1:0] bits independently for DAC1 and DAC2 (Table 27). DEM1/2[1:0] bits setting value is held even if the data mode is switched among PCM, DSD and EXDF modes.

Table 27. De-emphasis Control in Register Control Mode

DEM1/2[1:0] bits	Mode	
00	44.1 kHz	
01	OFF	(default)
10	48 kHz	
11	32 kHz	

In Pin Control mode, a digital de-emphasis filter is available for 44.1kHz sampling rates (tc = 50/15μs) and is enabled or disabled by DEM pin (Table 28).

Table 28. De-emphasis Control in Pin Control Mode

DEM pin	Mode
L	44.1 kHz
H	OFF

9.7. Digital Attenuator

The AK4499 includes a channel independent digital attenuator for output volumes (ATT) with 256 levels at 0.5dB step including MUTE (Table 29). When changing output levels, it is executed in soft transition, thus no switching noise occurs during these transitions. It can attenuate the input data from 0dB to -127dB and MUTE when assuming the output signal level is 0dB when ATTL1/2 [7:0] bits and ATTR1/2[7:0] bits = "FFH".

The digital attenuator is disabled in volume bypass mode (DSDD bit = "1") at DSD mode. Digital attenuation is fixed to 0 dB in pin control mode.

Table 29. Attenuation Level of Digital Attenuator

ATTL1/R1/L2/R2[7:0] bits	ATT Code	Attenuation Level	
FFH	255	0dB	(default)
FEH	254	-0.5dB	
FDH	253	-1.0dB	
:	:	:	
:	:	:	
02H	2	-126.5dB	
01H	1	-127.0dB	
00H	0	MUTE (-∞)	

The transition time of when changing digital output volume is defined as (Transition time of 1 code shift) x (previous ATT level – changed ATT level). The transition time of 1 code shift is set by ATS[1:0] bits (Table 30). Register setting values will be kept even switching the PCM and DSD modes.

Table 30. Transition Time between Set Values of ATT[7:0] bits

ATS[1:0] bits	Transition Time of 1 Code Shift			
	PCM Mode	EXDF Mode	DSD Mode	
00	4080/fs	4080 WCK Cycle	4080/(2fs)	(default)
01	2040/fs	2040 WCK Cycle	2040/(2fs)	
10	510/fs	510 WCK Cycle	510/(2fs)	
11	255/fs	255 WCK Cycle	255/(2fs)	

It takes 4080/fs (92.5 ms @fs = 44.1 kHz) from "FFH" (0dB) to "00H" (MUTE) when ATS[1:0] bits "00" in PCM mode. ATTL1/2[7:0] bits and ATTR1/2[7:0] bits are initialized to "FFH" (0dB) by setting the PDN pin = "L".
If the digital volume attenuation level is changed during reset period, the output volume will become a setting value after releasing the reset. It will change to a setting value immediately if the volume is changed within 10/fs after releasing reset.

9.8. Gain Adjustment Function

The AK4499 has the gain adjustment function. The analog output amplitude can be adjusted by GC[1:0] bits. In Pin Control mode, the gain mode is fixed to 72.8 mApp output mode.

Table 31. Current Output Level between Set Values of GC[1:0] bits

GC[1:0] bits	Current Output Level			
	PCM/EXDF	DSD: Normal Path	DSD: Volume bypass	
00	72.8 mApp	72.8 mApp	45.5 mApp	(default)
01	72.8 mApp	45.5 mApp	45.5 mApp	
10	45.5 mApp	45.5 mApp	45.5 mApp	
11	45.5 mApp	45.5 mApp	45.5 mApp	

9.9. Zero Detection, DSD Full-scale Detection

The AK4499 has a zero detection function and a DSD full-scale detection function. These detection flags can be output from the DZFL/R pin. DDMOE bit selects the output detection flag of the DZFL/R pin (Table 32). The output polarity of the DZFL/R pin can be inverted by DZFB bit (Table 33).

Table 32. Output Select for DZFL/R Pins

DDMOE bit	DZFL/R Pin Output	
0	Zero Detection Flag	(default)
1	DSD Full-scale Detection Flag	

Table 33. Output Polarity Select for DZFL/R Pins

DZFB bit	DZFL/R Pin Output	
0	“H” when detect flag	(default)
1	“L” when detect flag	

9.9.1. Zero Detection

The AK4499 has a channel-independent zero detection function. As shown in Figure 51, DATT soft mute block outputs are the monitor nodes of zero detection. Zero detection flag is generated when the monitor node of each channel is continuously “0” for a detection time shown in Table 34.

Zero detection flag is generated immediately when the AK4499 is set to reset state (RSTN bit = “0”). Zero detection flag will be cleared in 4/fs-5/fs by releasing the reset (RSTN bit = “1”). The zero detection function is disabled if Volume Bypass is selected in DSD mode (Table 19).

Table 34. Zero Detection Time

Sampling Speed		Detection Time
PCM	Any Sampling Speed	8192 / fs
EXDF	Any Sampling Speed	8192 WCK cycle
DSD	DSD64/128/256	8192 / fs
	DSD512	16384 / fs

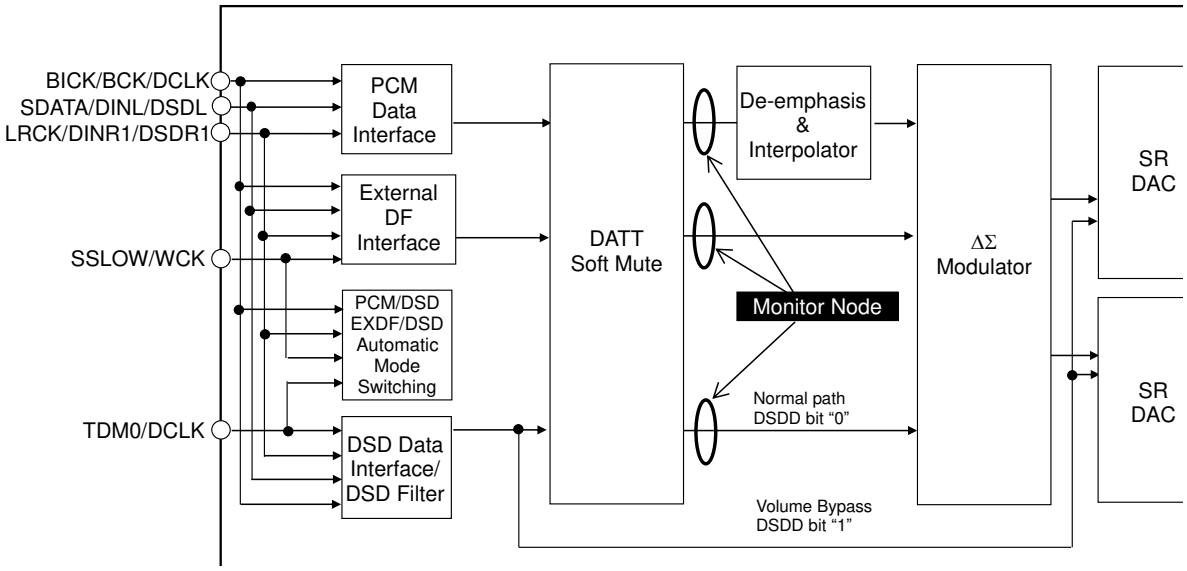


Figure 51. Zero Detection Monitor Node

Zero detection flag can be output from the DZFL/R pins by setting DZFE bit = "1" when DDMOE bit = "0". The output flag of the DZFL/R pins can be selected by DZFM bit and DZFSEL bit (Table 35).

Table 35. Output Signal Setting of DZFL/R Pins (DDMOE bit = "0") (×: Do Not Care)

DZFE bit	DZFM bit	DZFSEL bit	DZFL pin	DZFR pin	
0	×	×	"L"	"L"	(default)
1	0	0	L1ch Zero Detection Flag	R1ch Zero Detection Flag	
		1	L2ch Zero Detection Flag	R2ch Zero Detection Flag	
	1	×	AND Signal of Lch and Rch Zero Detection Flags	AND Signal of Lch and Rch Zero Detection Flags	

9.9.2. DSD Full-Scale Detection Function

The AK4499 has independent full-scale detection function for each channel in DSD mode. Mute function of analog output signal becomes enabled after detecting full-scale signal by setting DDM bit = "1". DDM bit setting should be made while PW bit = "0" or RSTN bit = "0".
Figure 52 shows a block diagram of DSD signal playback. Input data of each channel pin (DSDL1/2 or DSDR1/2) is received via the DSD_IF block and full-scale detection is executed at the DSD full-scale detection block. Full-scale detection is valid only the AK4499 is in power-on state.

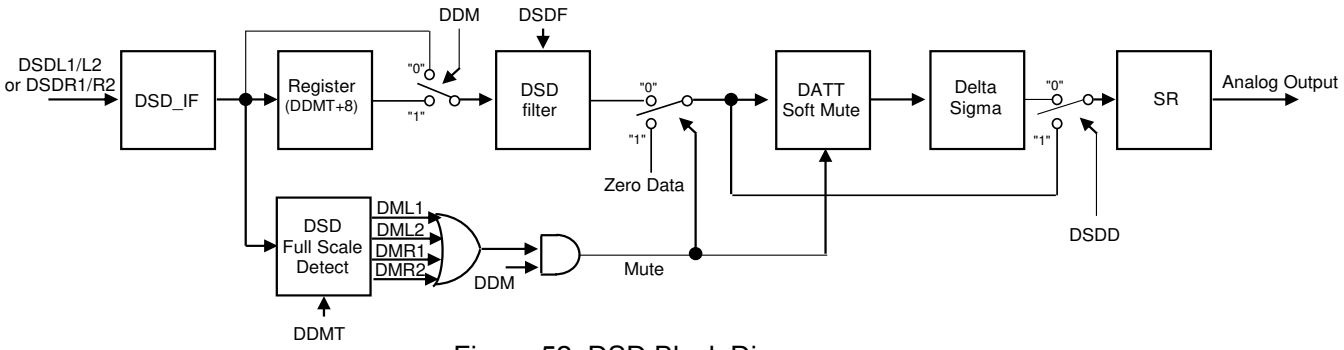


Figure 52. DSD Block Diagram

If the input data of any channel is continuously “H” or “L” for the time set by DDMT bit, the AK4499 is in full-scale detection state (Table 37) and corresponding DML1/2 or DMR1/2 bit becomes “1” independently. DML1/2 and DMR1/2 bits can be readout by register reading.

Full-scale detection signal can also be output from the DZFL/R pin by setting DDMOE bit = “1”. The output flag of the DZFL/R pin can be selected by DZFE, DZFM and DZFSEL bits (Table 36).

Table 36. Output Signal Setting of DZFL/R Pins (DDMOE bit = “1”) (×: Do Not Care)

DZFE bit	DZFM bit	DZFSEL bit	DZFL pin	DZFR pin
×	0	0	L1ch Full-scale Detection Flag	R1ch Full-scale Detection Flag
		1	L2ch Full-scale Detection Flag	R2ch Full-scale Detection Flag
0	1	×	“L”	OR Signal of L1/R1/L2/R2ch Full-scale Detection Flag
1	1	×	AND Signal of L1/R1/L2/R2ch Zero Detection Flag	

The AK4499 mutes the analog output when full-scale data is input to either L or R channel if DDM bit = "1". The output data of DSD_IF block is delayed by Register block for "Setting Time of DDMT bit + 8 DCLK cycles" to avoid clicking noise until the analog output is muted completely when DDM bit = "1". Therefore, the analog output delay becomes larger according to this delay time (Table 37). DDM bit setting should be made while PW1 bit = PW2 bit = "0" or RSTN bit = "0".

Full-scale detection state is released when the input data of the full-scale input channel is toggled. The operation after full-scale detection is released is according to DSDD bit setting that selects DSD playback path (Table 38).
When DSDD bit = "0" (Normal Path), the transition time until the output data returns to normal after releasing full-scale detection state is according to the setting of ATS[1:0] bits (Table 30).
If DSDD bit = "1" (Volume Bypass), the output data returns to normal immediately when the full-scale detection state is released.

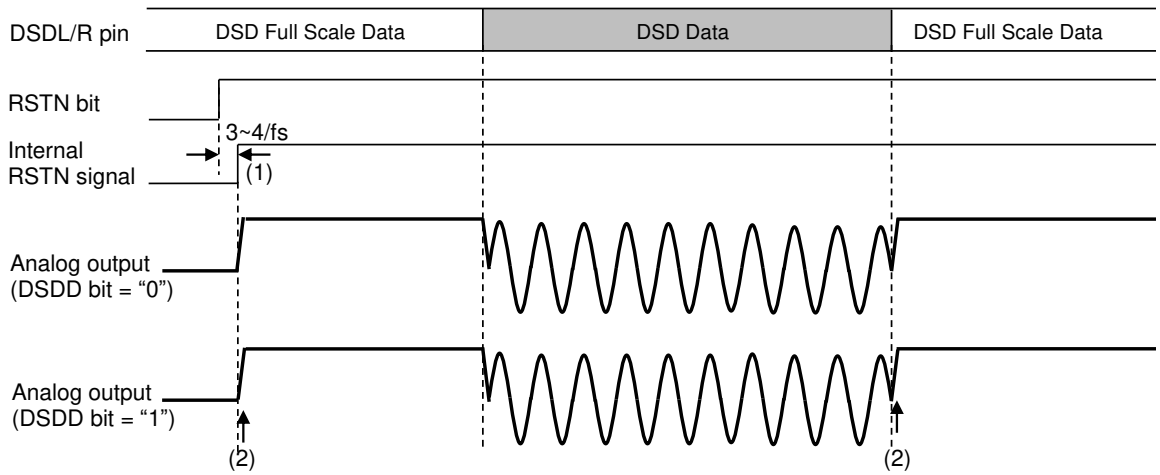
The full-scale detection function is assuming full-scale input that occurs when switching the data mode between PCM and DSD modes. Therefore, click noise will not occur when the input signal becomes full-scale from zero data and vice versa but there is a possibility that click noise occurs when the input signal becomes full-scale from the state there is an input signal and vice versa.

Table 37. DSD Full-scale Detection Time Setting

DDMT bit	Detection Time	Register Delay	
0	256 DCLK cycle	264 DCLK cycle	(default)
1	128 DCLK cycle	136 DCLK cycle	

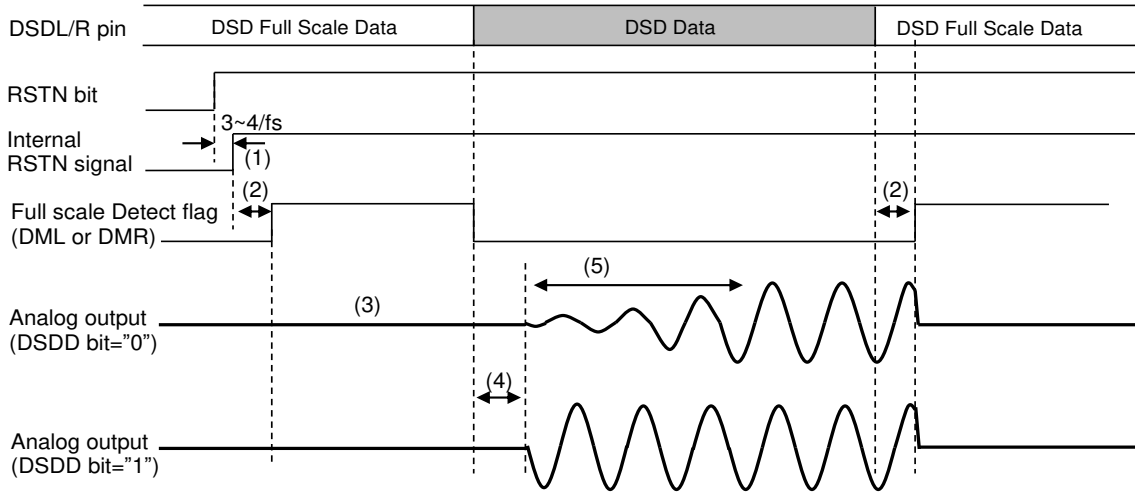
Table 38. Relationship between Output Signal Transition Time and DSDD Bit (DDM bit = "1")

DSDD bit	Mode	Mute Transition time	Mute Release time	
0	Normal Path	Rapidly	As ATS[1:0] bits	(default)
1	Volume Bypass	Rapidly		



Notes:
(1) Internal reset is released after 3-4/fs by setting RSTN bit = "1".
(2) Excessive signals will be output from the analog output if full-scale signal is input after releasing internal reset. This behavior does not depend on DSDD bit setting.

Figure 53. Analog Output Waveform with DSD Full-scale Input (DDM bit = "0")



Notes:
(1) Internal reset is released after 3-4/fs by setting RSTN bit = "1".
(2) The internal detection flag becomes "1" if the input data is full-scale for a period set by DDMT bit after releasing internal reset.
(3) Analog output is forced to zero output when full-scale signal is detected. No clicking noise occurs during a period from digital data input until full-scale detection since the analog output data delays for Register delay time (Table 37) if DDM bit is set to "1".
(4) Full-scale detection state is cleared when normal signal is input when the AK4499 is in full-scale detection state. Analog signal output starts after the Register delay time (Table 37) by clearing the full-scale detection state.
(5) Analog output transition time is different according to DSDD bit setting. When DSDD bit = "0", analog output transition time is set by ATS[1:0] bits (Table 30). When DSDD bit = "1", analog output recovers immediately.

Figure 54. Analog Output Waveform with DSD Full-scale Input (DDM bit = "1")

9.10. LR Channel Output Signal Select, Phase Inversion Function

In Register Control mode, input and output combination of the AK4499 can be changed by MONO1/2 bits and SELLR1/2 bits. In addition, the output signal phase can be inverted by INVL1/2 bits and INVR1/2 bits (Table 39). These functions are available on all audio formats. In Pin Control mode, Rch output signal phase of DAC1/2 can be inverted by the INVR pin (Table 40).

Table 39. Output Select for DAC1/2 (Register Control Mode)

MONO1 bit	SELLR1 bit	INVL1 bit	INVR1 bit	L1	R1
0	0	0	0	L1ch in	R1ch in
		1	0	L1ch in Invert	R1ch in
		0	1	L1ch in	R1ch in Invert
		1	1	L1ch in Invert	R1ch in Invert
0	1	0	0	R1ch in	L1ch in
		1	0	R1ch in Invert	L1ch in
		0	1	R1ch in	L1ch in Invert
		1	1	R1ch in Invert	L1ch in Invert
1	0	0	0	L1ch in	L1ch in
		1	0	L1ch in Invert	L1ch in
		0	1	L1ch in	L1ch in Invert
		1	1	L1ch in Invert	L1ch in Invert
1	1	0	0	R1ch in	R1ch in
		1	0	R1ch in Invert	R1ch in
		0	1	R1ch in	R1ch in Invert
		1	1	R1ch in Invert	R1ch in Invert

MONO2 bit	SELLR2 bit	INVL2 bit	INVR2 bit	L2	R2
0	0	0	0	L2ch in	R2ch in
		1	0	L2ch in Invert	R2ch in
		0	1	L2ch in	R2ch in Invert
		1	1	L2ch in Invert	R2ch in Invert
0	1	0	0	R2ch in	L2ch in
		1	0	R2ch in Invert	L2ch in
		0	1	R2ch in	L2ch in Invert
		1	1	R2ch in Invert	L2ch in Invert
1	0	0	0	L2ch in	L2ch in
		1	0	L2ch in Invert	L2ch in
		0	1	L2ch in	L2ch in Invert
		1	1	L2ch in Invert	L2ch in Invert
1	1	0	0	R2ch in	R2ch in
		1	0	R2ch in Invert	R2ch in
		0	1	R2ch in	R2ch in Invert
		1	1	R2ch in Invert	R2ch in Invert

Table 40. Output Select (Pin Control Mode)

INVR pin	L1	R1	L2	R2
L	L1ch in	R1ch in	L2ch in	R2ch in
H	L1ch in	R1ch in Invert	L2ch in	R2ch in Invert

9.11. PCM/DSD, EXDF/DSD Automatic Mode Switching Function

The AK4499 has automatic mode switching function that determines D/A conversion mode from the input clock and data. This function is available by setting ADPE bit = “1” when the PDN pin = “H” in register control mode. DP bit is for manual setting. It will be ignored when ADPE bit is “1”.

The automatic mode switching function is valid between PCM mode and DSD mode or EXDF mode and DSD mode. PCM/DSD automatic switching mode is enabled by setting ADPE bit = “1” when EXDF bit = “0”, EXDF/DSD automatic switching mode is enabled by setting ADPE bit = “1” when EXDF bit = “1”. EXDF bit setting should be made before changing ADPE bit = “0” → “1”. Note that automatic mode switching function is not available between PCM mode and EXDF mode.

The result of automatic mode detection can be readout by ADP bit. When ADPE bit = “1”, ADP bit outputs “0” if the detection result is PCM or EXDF mode and outputs “1” if it is DSD mode. This readout function of ADP bit is invalid and “0” data is readout when ADPE bit = “0”.

To prevent clicking noises on mode switching, the mute function of DSD full-scale detection should be enabled by setting DDM bit = “1” when using this automatic mode switching function. DDM bit must be set while PW bit or RSTN bit = “0”. By setting DDM bit = “1”, group delay will be 18/fs longer in PCM/EXDF mode and 136 to 264 DCLK cycle longer according to full-scale detection time setting by DDMT bit in DSD mode (Table 37). This function does not support DSD phase modulation format and edge inversion function of DSD receiving data (DCKB bit = “1”).

The automatic mode switching function supports both DSD data paths set by DSDPATH bit. The AK4499 determines mode from the clock input of the DCLK pin (#52) when DSDPATH bit = “0”, and it determines mode from clock and data inputs of the BICK/BCK/DCLK pin (#43), LRCK/DSDR1 pin (#45) and WCK pin (#48).

9.11.1. Automatic Mode Switching when DSDPATH bit = “0”

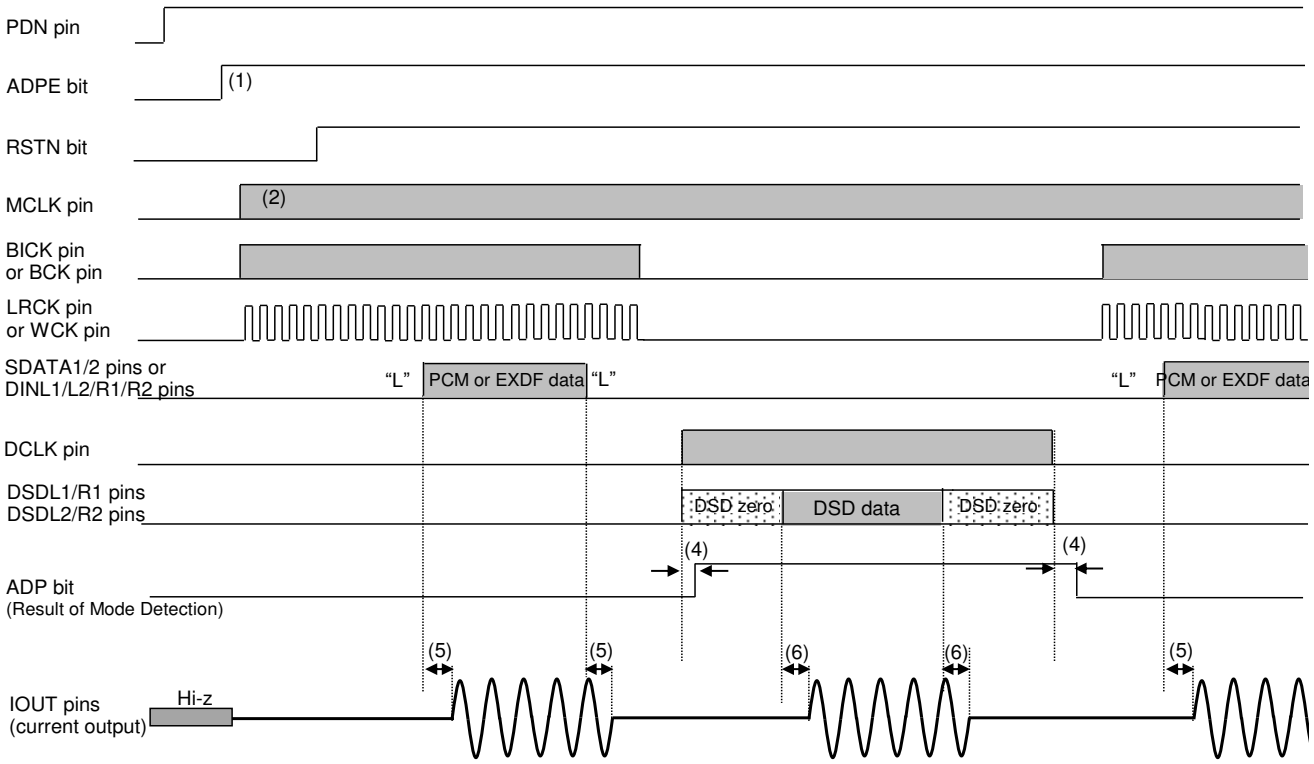
When DSDPATH bit = “0”, the AK4499 detects PCM (or EXDF) mode or DSD mode by counting a clock input to the DCLK pin (#52). MCLK should be input during mode detection.

Mode detection condition is different according to DSDSEL[1:0] bits setting. The AK4499 detects DSD mode if the number of clock pulse in 1/fs is in a range shown in Table 41 and PCM (or EXDF) mode is detected if not.

Table 41. Mode Detection Condition when DSDPATH = ”0”

DSD mode	DSDSEL[1:0] bits	Number of DCLK Pulse in 1/fs	Detection Result
DSD64	00	53 < pulse number < 77	DSD Mode
DSD128	01	106 < pulse number < 154	
DSD256	10	212 < pulse number < 308	
DSD512	11	424 < pulse number < 616	

When the mode is changed from PCM (or EXDF) to DSD, zero data should be input to both L and R channels in DSD mode after inputting zero data to both channels in PCM (or EXDF) mode. When the mode is changed from DSD mode to PCM (or EXDF), zero pattern data should be input to both L and R channels in DSD mode before inputting zero data to both channels in PCM (or EXDF) mode. In this case, 1024/fs of zero data input period is necessary. Refer to Figure 55 for operation sequence.



Notes:

(1) Automatic mode switching between PCM (or EXDF) and DSD modes is enabled by setting ADPE bit = "1".

(2) When DSDPATH bit = "0", MCLK input is necessary for mode detection.

(3) In PCM mode, analog output delay time becomes longer for about 18/fs comparing with when setting ADPE bit = "0".

(4) The AK4499 transitions to DSD mode if the number of DCLK input clock pulse in 1/fs satisfies the condition. The condition of DSD mode detection is set by DSDSEL[1:0] bits (Table 41).

(5) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT bit setting.

(6) The AK4499 transitions to PCM (or EXDF) mode if the number of DCLK input clock pulse does not satisfies the condition.

Figure 55. Mode Switching Sequence when DSDPATH bit = "0"

9.11.2. Automatic Mode Switching when DSDPATH bit = "1"

When the DSDPATH bit = "1", the AK4499 detects PCM (or EXDF) mode or DSD mode from a clock and data inputs of the BICK/BCK/DCLK pin (#43), LRCK/DSDR1 pin (#45) and WCK pin (#48).

9.11.2.1. Mode Detection Start Condition

If one of the five conditions shown below is satisfied, the AK4499 executes mode detection. The AK4499 keeps previous mode instead of executing mode detection if any condition is not satisfied. These start conditions of mode detection are common regardless of EXDF bit setting.

1. Input data of all channels are zero for a period set by ADPT[1:0] bits (Table 42).
2. Output data of all channels are zero for a period set by ADPT[1:0] bits (Table 42) because of the attenuation setting or SMUTE bit setting.
3. Input data of all channels are full-scale for a period set by DDMT bit in DSD mode (Table 37).
4. PW1 bit = PW2 bit = "0"
5. RSTN bit = "0"

Table 42. Time Until Mode Detection after Input Data Becomes Zero

ADPT[1:0] bits	Wait Time	
00	8192/fs+18/fs	(default)
01	4096/fs+18/fs	
10	2048/fs+18/fs	
11	1024/fs+18/fs	

9.11.2.2. Mode Detection

9.11.2.2.1. PCM/DSD Mode Automatic Switching (EXDF bit = "0")

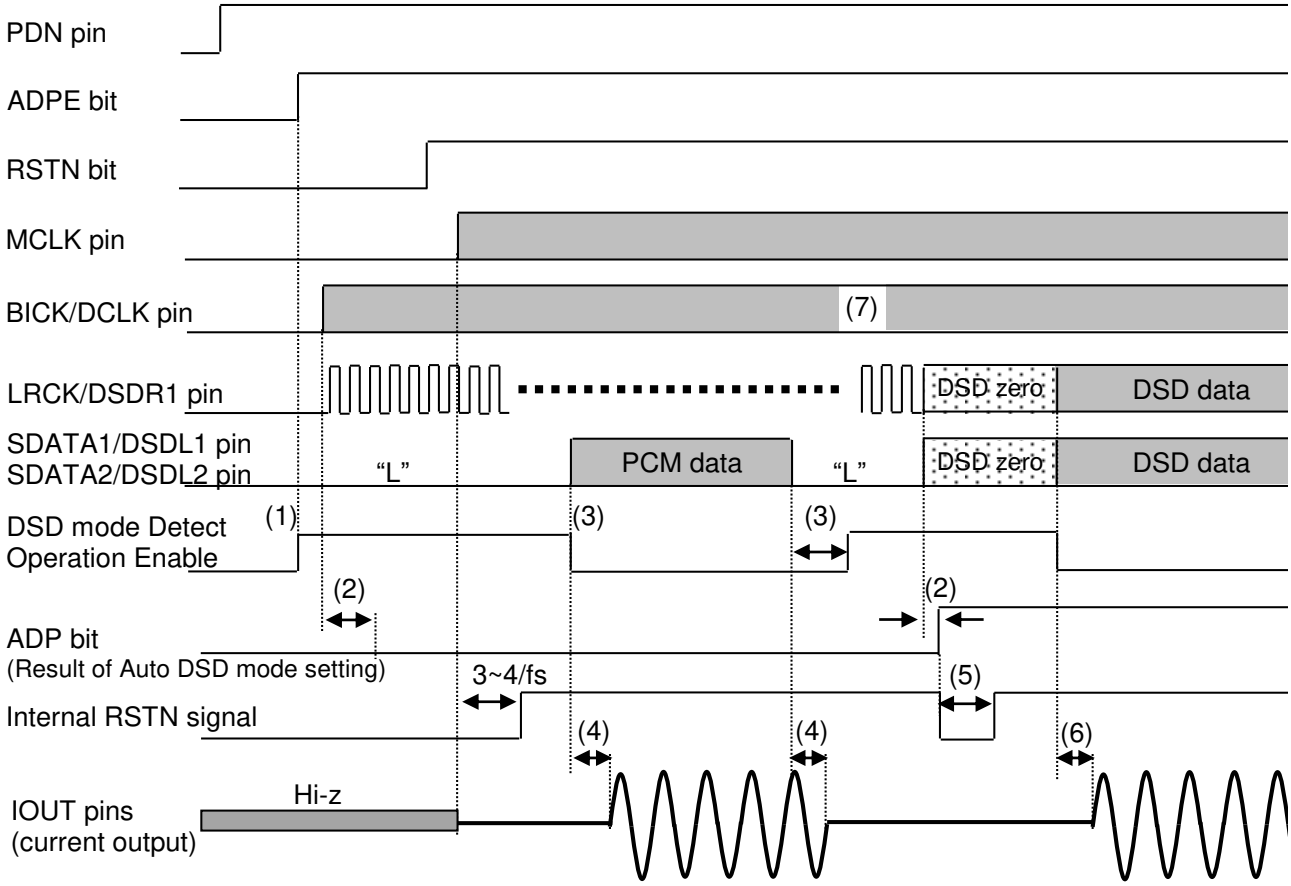
The AK4499 detects mode from the input signal to the LRCK/DSDR1 pin (#45). Input one of "01101001 01101001", "01010101 01010101", or "00110011 00110011" zero code pattern continuously to the LRCK/DSDR1 pin when changing to DSD mode from PCM mode (Table 43).

Input a clock that toggles in N times 16BICK cycle or a clock that is continuously "L" or "H" for 32BICK cycles or more to the LRCK/DSDL1 pin (#3) (Table 43). Refer to Figure 56 and Figure 57 for operation sequence.
The AK4499 keeps previous mode instead of executing mode switching if any condition is not satisfied.

Table 43. Input Signal when Switching PCM/DSD Mode

#45 LRCK/DSDR1 Pin Input Signal	Detection Result
One of zero code pattern below is input twice consecutively "01101001 01101001" or "01010101 01010101" or "00110011 00110011"	DSD Mode
Clock toggles in N times 16BICK cycles (N ≥ 1) or Clock that keeps "L" or "H" for 32BICK cycles	PCM Mode

The AK4499 executes data mode detection even if there is no MCLK input while PW bit = "0" or RSTN bit = "0". However, the analog output becomes Hi-Z and the AK4499 enters standby state when MCLK is stopped. The AK4499 resumes operation according to a data mode that is detected when MCLK is input again. The data mode will be maintained if the input clock to the BICK/BCK/DCLK pin (#43) is stopped.
The AK4499 executes internal reset for 3-4/fs automatically when switching the data mode and resumes operation.



Notes:

(1) Automatic mode switching between PCM and DSD modes is enabled by setting ADPE bit = "1" after setting PDN pin "L" → "H". If RSTN bit is in default value "0", mode detection operation will start.

(2) Mode detection is performed by monitoring input signal code pattern of the LRCK/DSDR1 pin. It is executed for 34 cycles of the BICK/DCLK pin input clock and then ADP bit is changed on a rising edge of input signal of the LRCK/DSDR1 pin. Mode detection is executed even when there is no MCLK input. The AK4499 starts data mode detection when input data of both channels are zero for a period set by ADPT[1:0] bits.

(3) The AK4499 finishes data mode detection when a data that is not zero is input.

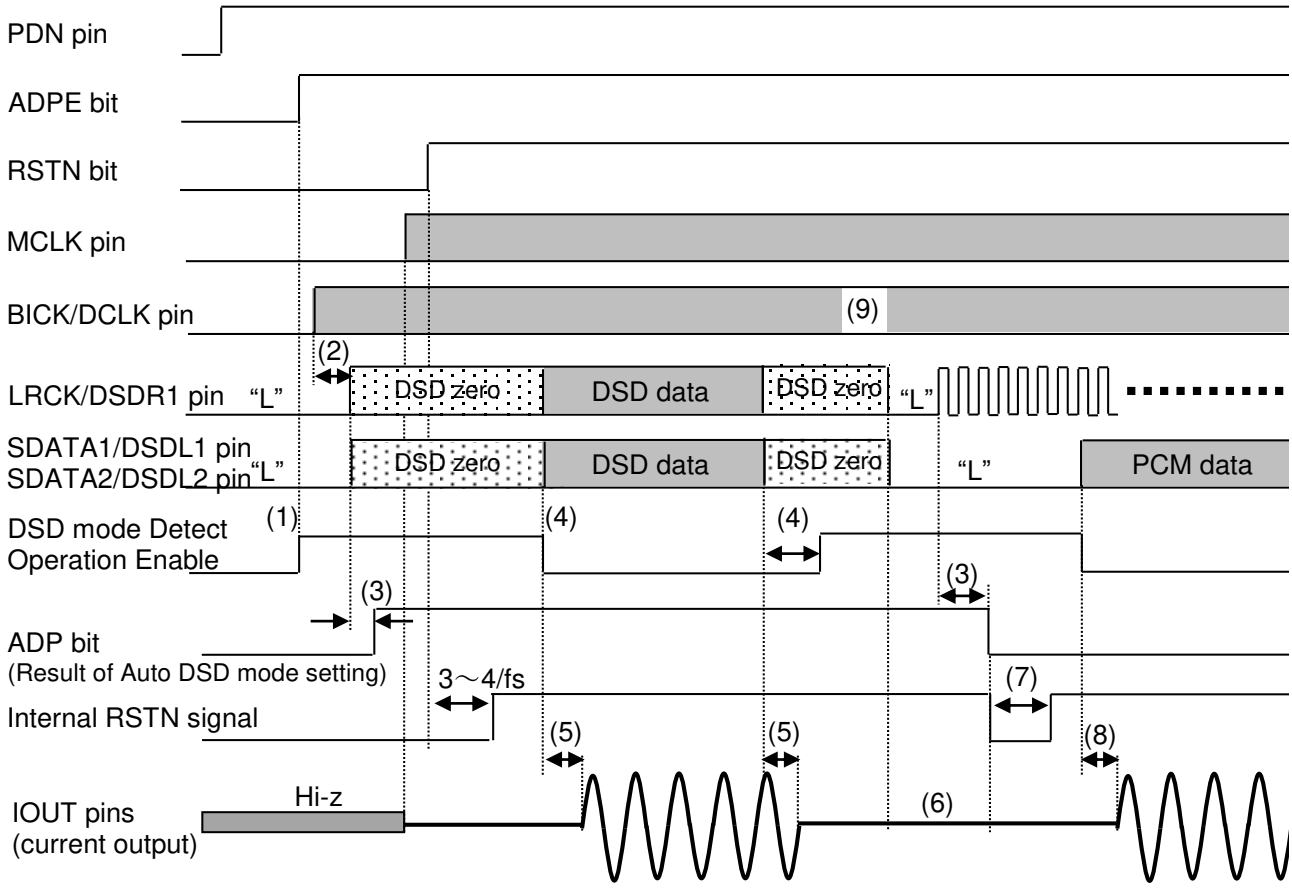
(4) In PCM mode, analog output delay time becomes 18/fs longer comparing with when setting ADPE bit = "0".

(5) When data mode is changed, the AK4499 executes internal reset for 3-4/fs automatically.

(6) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT bit setting.

(7) A clock input to the BICK/DCLK pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK pin is stopped.

Figure 56. Changing to DSD Mode after Power-up in PCM Mode (DSDPATH bit = "1", EXDF bit = "0")



Notes:

(1) Automatic mode switching between PCM and DSD modes is enabled by setting ADPE bit = "1" after setting the PDN pin "L" → "H". If RSTN bit is in default value "0", mode detection operation will start.

(2) Upon power up the AK4499, the AK4499 operates in PCM mode if DCLK is input and DSDL1 is not input.

(3) Mode detection is performed by monitoring input signal code pattern of the LRCK/DSDR1 pin. It is executed for 34 cycles of the BICK/DCLK pin input clock and then ADP bit is changed on a rising edge of input signal of the LRCK/DSDR1 pin. ADP bit outputs "0" in PCM mode and "1" in DSD mode. Mode detection is executed even when there is no MCLK input.

(4) The AK4499 finishes data mode detection when a data that is not zero is input. Then the AK4499 restarts the mode detection when input data of all channels are continuously zero for the period set by ADPT[1:0] bits.

(5) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT bit setting.

(6) If DSD data input is stopped in DSD mode, the AK4499 stays in DSD mode and continues operation. In this case, full-scale data is input to the AK4499. Excessive signal output can be avoided by setting DDM bit = "1" enabling automatic mute function works when detecting DSD full-scale input.

(7) When data mode is changed, the AK4499 executes internal reset for 3-4/fs automatically.

(8) In PCM mode, analog output delay time becomes 18/fs longer comparing with when setting ADPE bit = "0".

(9) A clock input to the BICK/DSLK pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK pin is stopped.

Figure 57. Changing to PCM Mode after Power-up in DSD Mode (DSDPATH bit = "1", EXDF bit = "0")

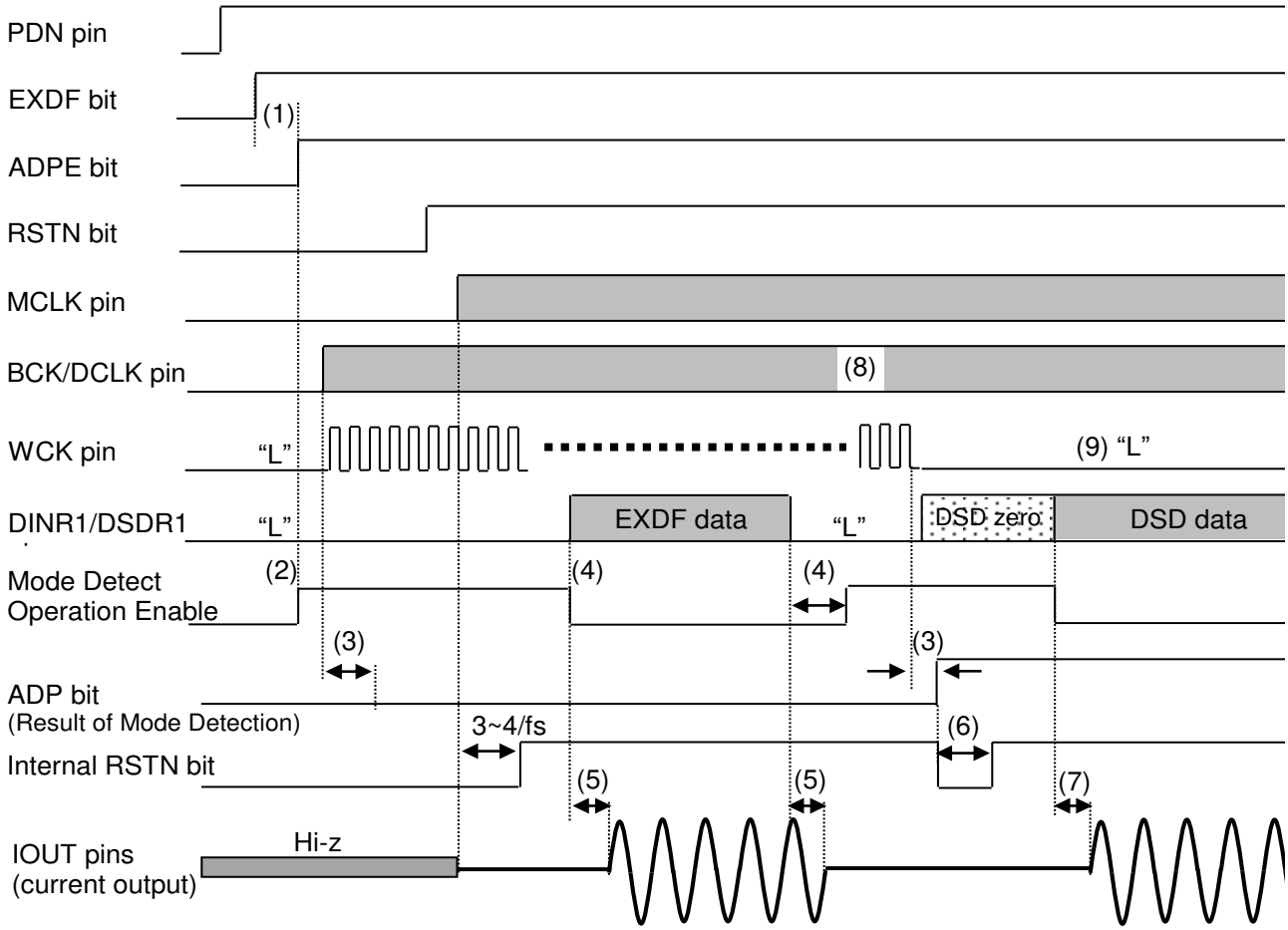
9.11.2.2.2. EXDF/DSD Automatic Mode Switching (EXDF bit = “1”)

The AK4499 detects mode from the input clocks to the WCK pin (#48) and the BCK/DCLK pin (#43). DSD mode is detected if the number of rising edge of the BCK/DCLK input clock exceeds 256 times in one cycle WCK input clock counting from a rising edge. EXDF mode is detected if the number of rising edge of the BCK/DCLK input clock does not reach 256 times in one cycle WCK input clock twice continuously (Table 44). Refer to Figure 58 and Figure 59 for the operation sequence.
The AK4499 keeps previous mode instead of executing mode switching if any condition is not satisfied.

Table 44. Mode Detection Conditions when Switching EXDF/DSD Mode

BCK/DCLK Pulse in One WCK Cycle	Detection Result
Once “256 < BCK/DCLK pulse number”	DSD Mode
Twice Continuously “BCK/DCLK pulse number ≤ 256”	EXDF Mode

The AK4499 executes data mode detection even if there is no MCLK input while PW bit = “0” or RSTN bit = “0”. However, the analog output becomes Hi-Z and the AK4499 enters standby state when MCLK is stopped. The AK4499 resumes operation according to a data mode that is detected when MCLK is input again. The data mode will be maintained if the input clock to the BICK/BCK/DCLK pin (#43) is stopped.
The AK4499 executes internal reset for 3-4/fs automatically when switching the data mode and resumes operation.



Notes:

(1) EXDF bit must be set before setting ADPE bit.

(2) Automatic mode switching between EXDF and DSD modes is enabled by setting ADPE bit = "1" after setting PDN pin "L" → "H". If RSTN bit is in default value "0", mode detection operation will start.

(3) Mode detection is performed by monitoring input clock of the WCK pin and the BCK/DCLK pin. It takes 256DCLK cycles for mode switching from EXDF to DSD mode, and takes 2WCK cycles for mode switching from DSD to EXDF mode. Mode detection is executed even when there is no MCLK input.

(4) The AK4499 finishes data mode detection when a data that is not zero is input. The AK4499 restarts data mode detection when input data of both channels are zero for a period set by ADPT[1:0] bits.

(5) In EXDF mode, analog output delay time becomes 18/fs longer comparing with when setting ADPE bit = "0".

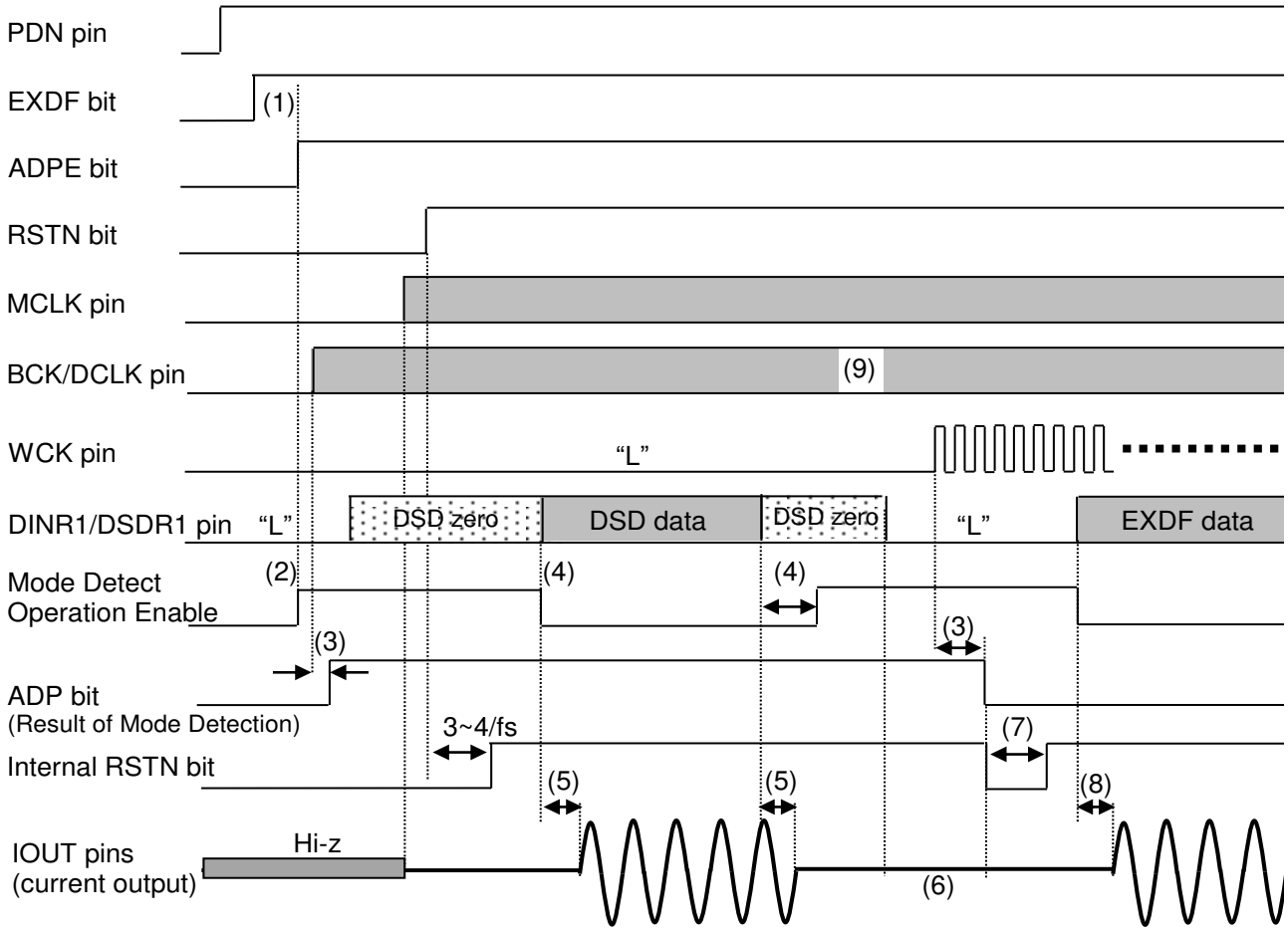
(6) When DSD mode is changed, the AK4499 executes internal reset for 3 to 4/fs automatically.

(7) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT bit setting.

(8) A clock input to the BICK/DCLK pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK pin is stopped.

(9) WCK input should be "L" when using DSD mode since DSD mode detection is performed by monitoring presence or absence of the WCK input clock when EXDF bit = "1".

Figure 58. Changing to DSD Mode after Power-up In EXDF Mode (DSDPATH bit = "1", EXDF bit = "1")



Notes:

(1) EXDF bit must be set before setting ADPE bit.

(2) Automatic mode switching between EXDF and DSD modes is enabled by setting ADPE bit = "1" after setting PDN pin "L" → "H". If RSTN bit is in default value "0", mode detection operation will start.

(3) Mode detection is performed by monitoring input clock of the WCK pin and the BCK/DCLK pin. It takes 256DCLK cycles for mode switching from EXDF to DSD mode, and takes 2WCK cycles for mode switching from DSD to EXDF mode. Mode detection is executed even when there is no MCLK input.

(4) The AK4499 finishes data mode detection when a data that is not zero is input. The AK4499 restarts data mode detection when input data of both channels are zero for a period set by ADPT[1:0] bits.

(5) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT bit setting.

(6) If DSDR input is stopped in DSD mode, the AK4499 stays in DSD mode and continues operation. In this case, full-scale data is input to the AK4499. Excessive signal output can be avoided by setting DDM bit = "1" enabling automatic mute function works when detecting DSD full-scale input.

(7) When data mode is changed, the AK4499 executes internal reset for 3 to 4/fs automatically.

(8) In EXDF mode, analog output delay time becomes 18/fs longer comparing with when setting ADPE bit = "0".

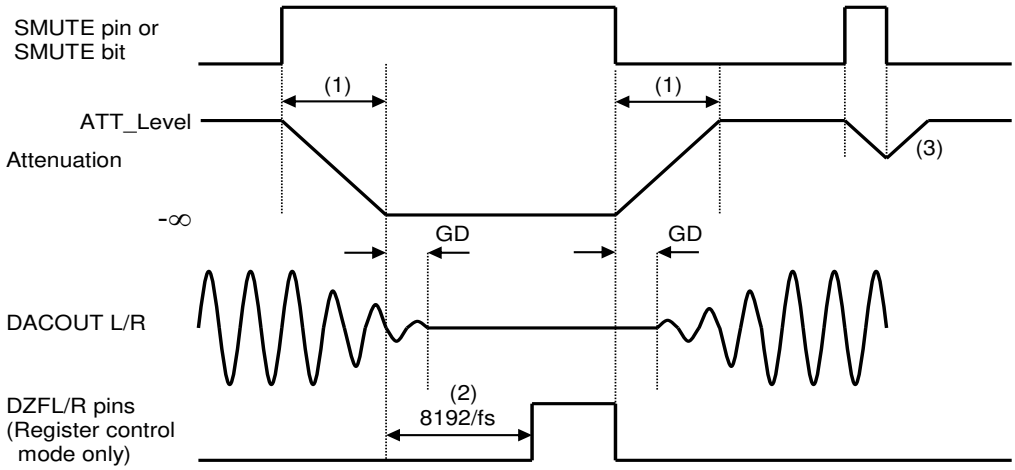
(9) A clock input to the BICK/DCLK pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK pin is stopped.

Figure 59. Changing to EXDF Mode after Power-up In DSD Mode (DSDPATH bit = "1", EXDF bit = "1")

Soft Mute Function

The AK4499 has soft mute function. The soft mute operation is performed at digital domain. When setting the SMUTE pin to “H” or SMUTE bit to “1”, the output signal is attenuated by −∞ during ATT_DATA × ATT transition time from the current ATT level.
When setting back the SMUTE pin to “L” or SMUTE bit to “0”, the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA × ATT transition time (Refer to Table 30 for ATT). If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

Soft mute function is not available when bypassing the volume (DSDD bit = “1”) in DSD mode.



Notes:
(1) ATT_DATA × ATT transition time. For example, this time is 4080LRCK cycles at ATS[1:0] bits = “00”, ATT_DATA = “FFH” in PCM Normal Speed mode.
(2) When the input data for each channel is continuously zeros for 8192 LRCK cycles (16384 cycles in DSD512 mode), the DZFL/R pin for each channel goes to “H”. The DZFL/R pin immediately returns to “L” if the input data is not zero.
(3) If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

Figure 60. Soft Mute Function

9.12. LDO

When TVDD = 3.0 to 3.6V, the power for digital core circuit (DVDD) is supplied by the internal LDO by setting the LDOE pin to “H”. Table 45 shows the DVDD pin statuses with the PDN and LDOE pins setting. The internal LDO is powered up by setting the PDN pin from “L” to “H” (power-down release) and it starts supplying 1.8V DVDD. Connect a 1µF capacitor to the DVDD pin when using the LDO. It takes 2ms (max.) to power-up the internal LDO.

Table 45. LDO Select Mode (×: Do Not Care)

PDN pin	LDOE pin	TVDD	DVDD
×	L	1.7 to 3.6 V	LDO OFF: Supply 1.7 to 1.98V to the DVDD pin externally
L	H	3.0 to 3.6 V	500 Ω Pull-down
H			LDO ON: LDO outputs 1.8V. (Do not connect DVDD with other device loads)

The AK4499 has error detect function, as shown in Table 46 for LDO operation (LDOE pin = “H”). The internal LDO will be powered down and stop supplying the power to the digital core when an error is detected. In this case, the analog signal output and the PDA pin becomes Hi-z state (In I^2C mode, ACK is not output). The AK4499 must be reset by setting the PDN pin = “L” → “H” to recover from the error detection status.

Table 46. Error Detection

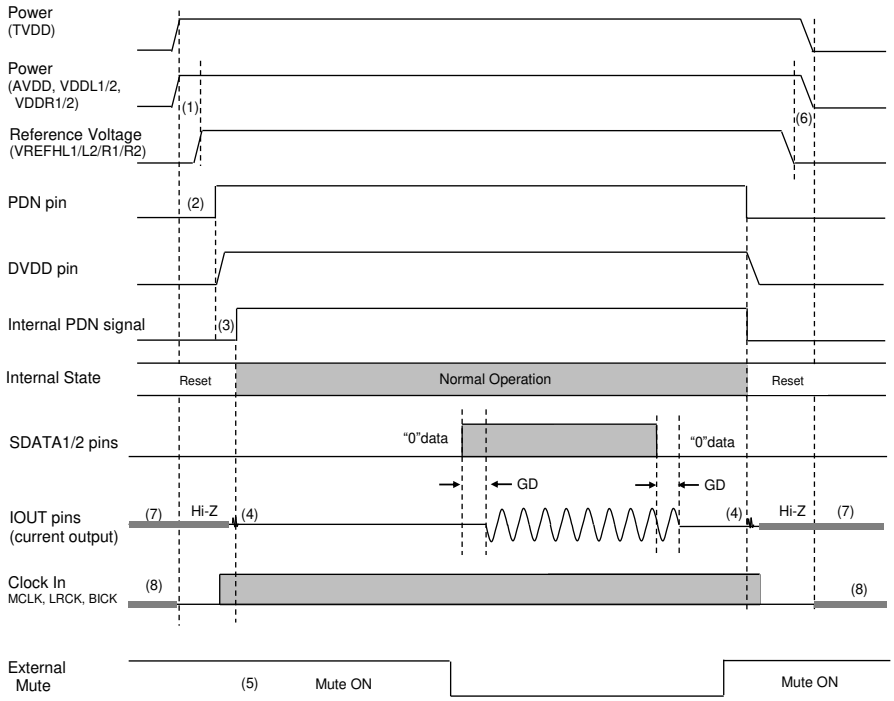
No	Error Correction	Error Detection Conditions
1	LDO Overvoltage Detection	The AK4499 detects an error when the output voltage of the LDO pin exceeds overvoltage threshold. Threshold: 2.35 V(typ) min: 2.2 V / max: 2.5 V
2	LDO Overcurrent Detection	The AK4499 detects an error when the current flows PMOS from LDO output exceeds overcurrent threshold. Threshold: 105 mA(typ) min: 80 mA / max: 130 mA

9.13. Power Up/Down Sequence

The AK4499 is powered down when the PDN pin is “L”. In power down state, all circuits stop operation and initialized, and the analog output becomes floating (Hi-z) state. The PDN pin must held “L” for more than 600 ns for a certain reset after all power supplies are on. There is a possibility of malfunctions with the “L” pulse less than 600 ns. Power down is released by setting the PDN pin to “H” from “L”. In this time Bias generating circuit and LDO (if LDOE pin = “H”) are powered up and the analog output becomes floating (Hi-z) state until all clocks are input.

9.13.1. Pin Control Mode (PSN pin = “H”)

All circuits will be powered up by inputting MCLK, LRCK and BICK clocks after the PDN pin = “H”. Figure 61 shows system timing example of power down/up when using the internal LDO (LDOE pin = “H”).

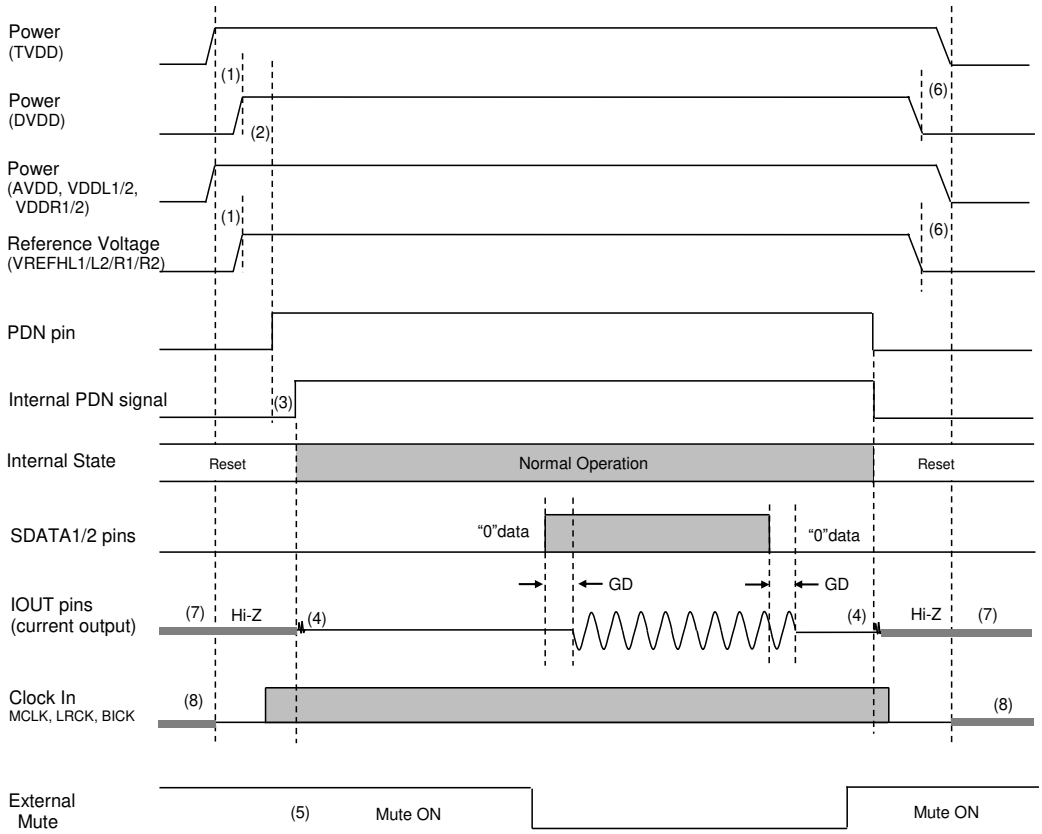


Notes:

(1) VREFHL1/L2/R1/R2 reference voltages should be input after AVDD is powered up or at the same time. Power up sequence between AVDD, TVDD and VDDL1/L2/R1/R2 are not critical.
(2) The PDN pin must be “L” when start supplying AVDD, TVDD and VDDL1/L2/R1/R2. It must be held “L” for more than 600 ns after AVDD, TVDD and VDDL1/L2/R1/R2 are powered up.
(3) The DVDD pin output voltage (generated by Internal LDO) is powered up by setting the PDN pin = “H” if the LDOE pin = “H”. The internal PDN signal will rise in 2 ms (max.) after the PDN pin = “H” and the internal circuit will start operation.
(4) Click noise occurs on an edge of PDN signal. This noise is output even if “0” data is input.
(5) Mute the analog output externally if click noise (4) adversely affect system performance.
(6) VREFHL1/L2/R1/R2 reference voltages should be stopped before AVDD is powered down or at the same time. Power down sequence between AVDD, TVDD and VDDL1/L2/R1/R2 are not critical.
(7) Analog outputs are floating (Hi-Z) in power down state.
(8) Do not input clocks (MCLK, BICK and LRCK) until after TVDD is turned on.

Figure 61. Power-down/up Sequence Example (Pin Control Mode, LDOE pin = “H”)

The timing example when not using the internal LDO (LDOE pin = “L”) is shown in Figure 62.



Notes:

(1) TVDD must be powered up before DVDD is powered up or at the same time. Power up sequence between other power supplies are not critical. VREFH L1/L2/R1/R2 reference voltages should be input after AVDD is powered up or at the same time.

(2) The PDN pin must be “L” when start supplying AVDD, TVDD, DVDD and VDDL1/L2/R1/R2. It must be held “L” for more than 600 ns after AVDD, TVDD, DVDD and VDDL1/L2/R1/R2 are powered up.

(3) When the LDOE pin = “L”, the internal PDN signal is on in 1 μs (max.) after the PDN pin is set to “H”, and the internal circuit will start operation.

(4) Click noise occurs on an edge of PDN signal. This noise is output even if “0” data is input.

(5) Mute the analog output externally if click noise (4) adversely affect system performance.

(6) TVDD must be powered down after or at the same time of DVDD. Power down sequence between other power supplies are not critical. VREFH L1/L2/R1/R2 reference voltages should be stopped before AVDD is powered down or at the same time.

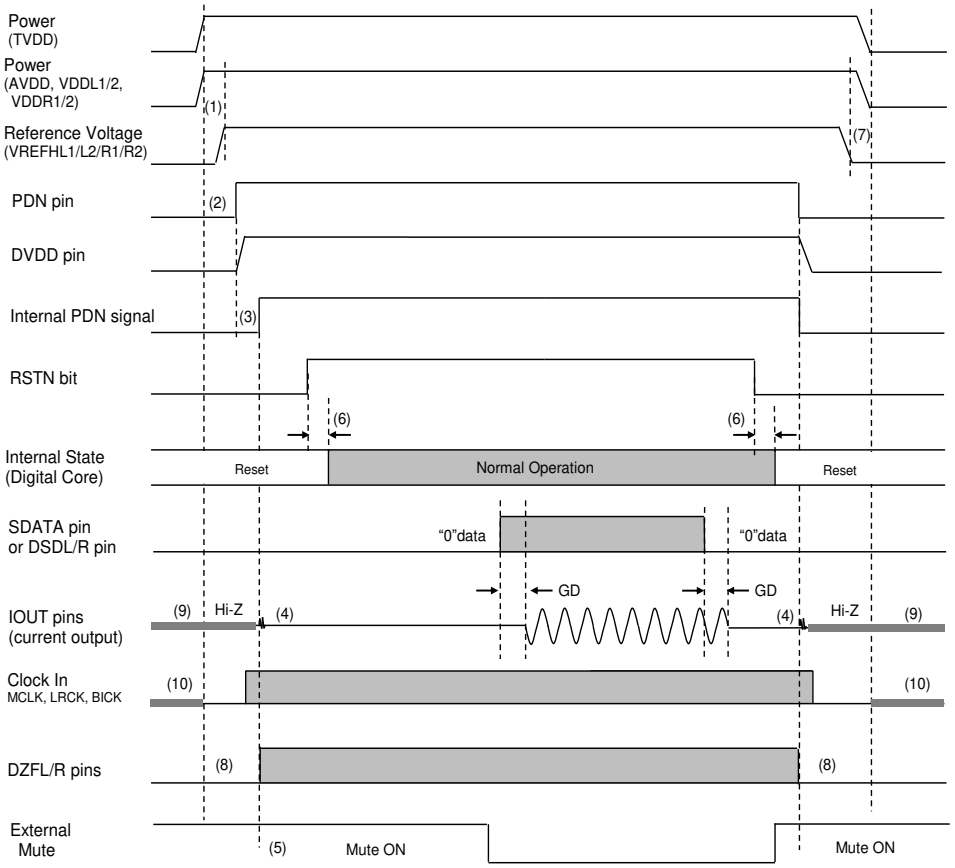
(7) Analog outputs are floating (Hi-Z) in power down state.

(8) Do not input clocks (MCLK, BICK and LRCK) until after TVDD is turned on.

Figure 62. Power-down/up Sequence Example (Pin Control Mode, LDOE pin = “L”)

9.13.2. Register Control Mode (PSN pin = “L”)

Figure 63 shows system timing example of power down/up when using the internal LDO (LDOE pin = “H”). Register access becomes available and internal LDO is powered up after setting the PDN pin = “H”. The analog circuit starts operation by supplying necessary clocks (MCLK, LRCK and BICK for PCM mode, MCLK, DCLK and EXDF for DSD mode, MCLK, BCK and WCK for EXDF mode), and the clock divider will start operation after about 3/fs. In this time, the analog output pins output zero signals. Then the AK4499 transitions to normal operation by setting RSTN bit = “1”.

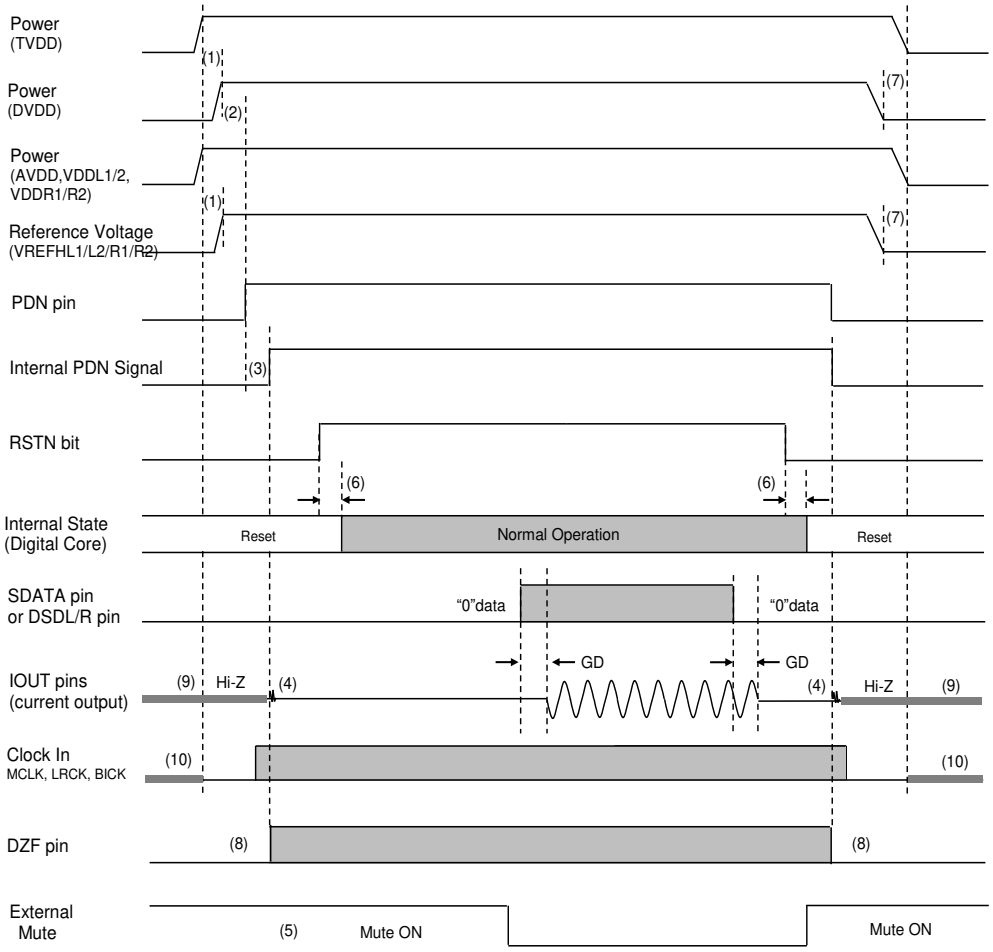


Notes:

(1) VREFHL1/L2/R1/R2 reference voltages should be input after AVDD is powered up or at the same time. Power up sequence between AVDD, TVDD and VDDL1/L2/R1/R2 are not critical.
(2) The PDN pin must be “L” when start supplying AVDD, TVDD and VDDL1/L2/R1/R2. It must be held “L” for more than 600 ns after AVDD, TVDD and VDDL1/L2/R1/R2 are powered up.
(3) The DVDD pin output voltage (generated by Internal LDO) is powered up by setting the PDN pin = “H” if the LDOE pin = “H”. The internal PDN signal will rise in 2 ms (max.) after the PDN pin = “H” and control register access becomes available.
(4) Click noise occurs on an edge of PDN signal. This noise is output even if “0” data is input.
(5) Mute the analog output externally if click noise (4) adversely affect system performance.
(6) It takes 3 to 4/fs until a reset instruction is valid when writing “0” to RSTN bit and it takes 3 to 4/fs when releasing the reset.
(7) VREFHL1/L2/R1/R2 reference voltages should be stopped before AVDD is powered down or at the same time. Power down sequence between AVDD, TVDD and VDDL1/L2/R1/R2 are not critical.
(8) The DZF pin outputs “L” in power down state.
(9) Analog outputs are floating (Hi-Z) in power down state.
(10) Do not input clocks (MCLK, BICK and LRCK) until after TVDD is turned on.

Figure 63. Power-down/up Sequence Example (Register Control Mode, LDOE pin = “H”)

The timing example of power up/down when not using LDO (LODE pin = “L”) is shown in Figure 64.



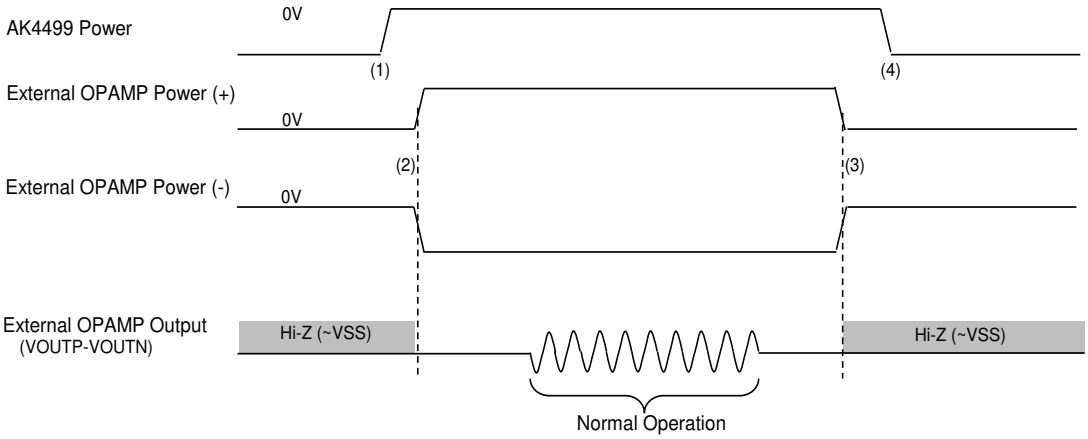
Notes:

(1) TVDD must be powered up before DVDD is powered up or at the same time. Power up sequence between other power supplies are not critical. VREFH L1/L2/R1/R2 reference voltages should be input after AVDD is powered up or at the same time.
(2) The PDN pin must be “L” when start supplying AVDD, TVDD, DVDD and VDDL1/L2/R1/R2. It must be held “L” for more than 600 ns after AVDD, TVDD, DVDD and VDDL1/L2/R1/R2 are powered up.
(3) When the LDOE pin = “L”, the internal PDN signal is on in 1 μs (max.) after the PDN pin is set to “H”, and the internal circuit will start operation.
(4) Click noise occurs on an edge of PDN signal. This noise is output even if “0” data is input.
(5) Mute the analog output externally if click noise (4) adversely affect system performance.
(6) It takes 3 to 4/fs until a reset instruction is valid when writing “0” to RSTN bit and it takes 3 to 4/fs when releasing the reset.
(7) TVDD must be powered down after or at the same time of DVDD. Power down sequence between other power supplies are not critical. VREFH L1/L2/R1/R2 reference voltages should be stopped before AVDD is powered down or at the same time.
(8) The DZFL/R pins output “L” in power down state.
(9) Analog outputs are floating (Hi-Z) in power down state.
(10) Do not input clocks (MCLK, BICK and LRCK) until after TVDD is turned on.

Figure 64. Power-down/up Sequence Example (Register Control Mode, LDOE pin = “L”)

9.13.3. Power Up Sequence of External Operational Amplifier for I-V Conversion

The output current of the AK4499 is converted voltage by external I-V conversion circuit. An operational amplifier used in this I-V conversion circuit must be powered up or stopped when the AK4499 is powered up. By doing this, a feedback path of the operational amplifier is maintained and DC offset (click noise) occurring at power-up of the operational amplifier can be suppressed.



(1) Power up the AK4499. Refer to "9.13.1. Power Up/Down Sequence" for power-up sequence.
(2) Power up an external operational amplifier after power up the AK4499.
(3) When power down the system, the external amplifier must be powered down before the AK4499.
(4) Power down the AK4499 after the external amplifier. Refer to "9.13.1.Power Up/Down Sequence" for power-down sequence of the AK4499.

Figure 65. Power Up Sequence of External Operational Amplifier for I-V Conversion

There is a possibility of IC destruction due to breakdown of the withstanding voltage of the analog output pins (IOUTLP/LN/RP/RN) if the power supply of the external operational amplifier is turned on before power up the AK4499. Therefore, connect a Zener diode (V_{RWM} = 6 to 7 V) between each VDDL1/R1/L2/R2 and VSSL1/R1/L2/R2 if the power up/down sequence shown in Figure 65 cannot be followed.

If the power supply of the external amplifier is turned on before power up the AK4499, there is a possibility that click noise occurs due to DC difference. Connect an external mute circuit to the analog signal line to prevent this click noise. Refer to "10.4.4. External Mute Circuit" for the external mute circuit.

9.14. Power Down, Standby and Reset Function

Power Down, Standby and Reset functions of the AK4499 are controlled by PDN pin, PW bit, MCLK, and RSTN bit (Table 47).

Table 47. Power Down, Standby, and Reset Function (×: Do Not Care)

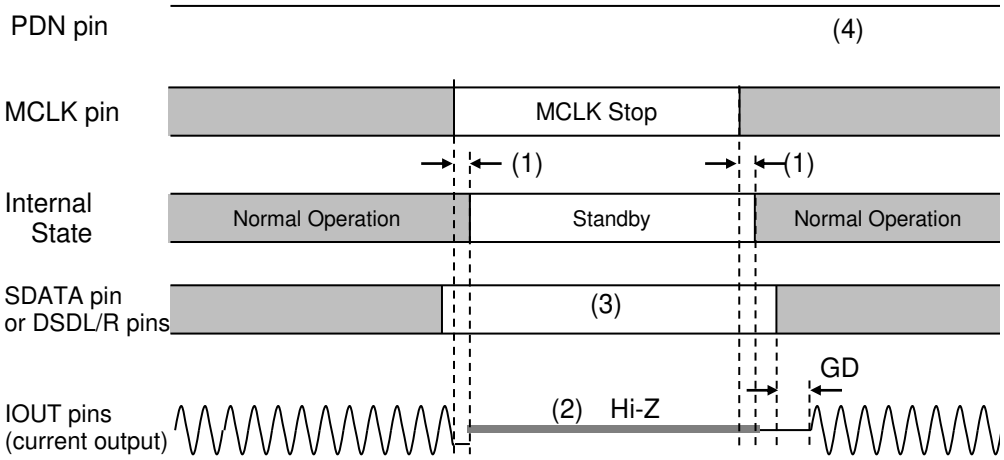
State	PDN pin	MCLK Input	PW1/2 bits	RSTN bit	DIGITAL Block	ANALOG Block	LDO / Register	Analog Output
Power Down	L	×	×	×	OFF	OFF	OFF	Hi-Z
Standby	H	No	×	×	OFF	OFF	ON	Hi-Z
	H	Yes	0	×	OFF	OFF	ON	Hi-Z
Reset	H	Yes	1	0	OFF	ON	ON	Zero output
Normal Operation	H	Yes	1	1	ON	ON	ON	Signal output

Table 48. Standby and Reset Function (detail)

PW1 bit	PW2 bit	RSTN bit	Analog Output	
			DAC1	DAC2
0	0	0	Hi-Z	Hi-Z
		1	Hi-Z	Hi-Z
1	0	0	Zero output	Hi-Z
		1	Signal output	Hi-Z
0	1	0	Hi-Z	Zero output
		1	Hi-Z	Signal output
1	1	0	Zero output	Zero output
		1	Signal output	Signal output

9.14.1. Standby Sequence by MCLK

The AK4499 detects a clock stop and all circuits except MCLK stop detection circuit, control register, IREF circuit and LDO (only when the LDOE pin = "H") stop operation if MCLK is not input for 1 μs (min.) during operation (PDN pin = "H"). In this case, the analog output goes floating state (Hi-Z). The AK4499 returns to normal operation if PW bit and RSTN bit are "1" and there are BCLK and LRCK inputs after starting to supply MCLK again. The zero detection function is disabled when MCLK is stopped. Figure 66 shows standby sequence example by MCLK.

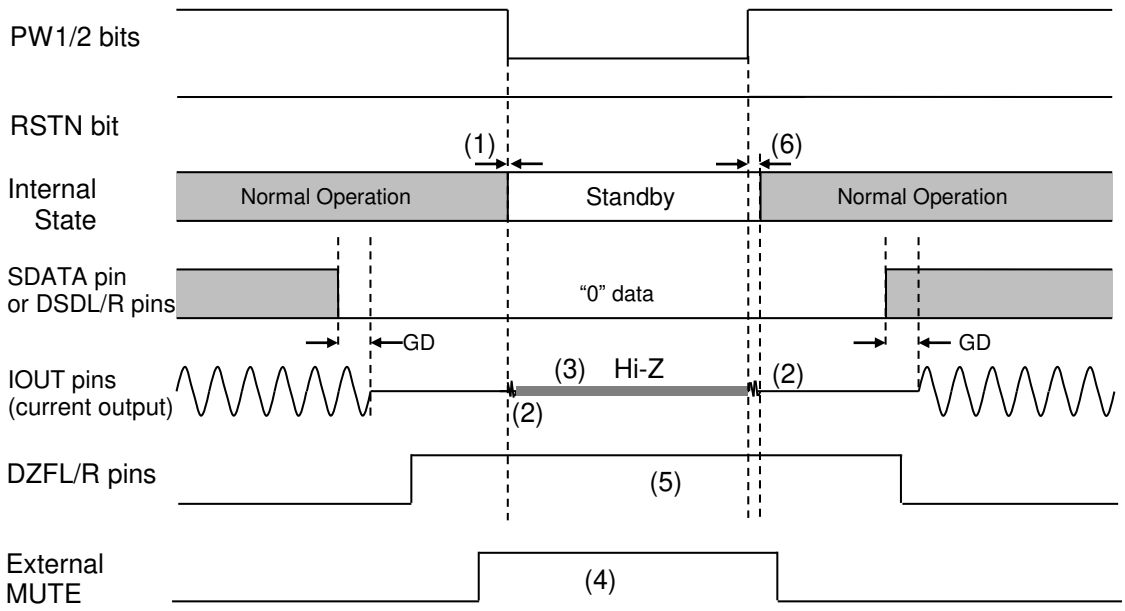


Notes:
(1) The AK4499 detects MCLK stop and becomes standby state when MCLK edge is not detected for 1 μs (min.) during operation.
(2) The analog output goes to floating state (Hi-Z) in standby state.
(3) Click noise can be reduced by inputting "0" data when stopping and resuming MCLK supply.
(4) Resume MCLK input to release the standby state. In this case, power-up sequence by the PDN pin is not necessary.

Figure 66. Standby Sequence Example by MCLK Stop

9.14.2. Standby Sequence by PW bits

All circuits except control register, IREF circuit and LDO (only when the LDOE pin = “H”) stop operation by setting PW1/2 bits to “0”. In this case, control register access is available. The analog output goes to floating state (Hi-Z). Figure 67 shows power ON/OFF sequence by PW1/2 bits.

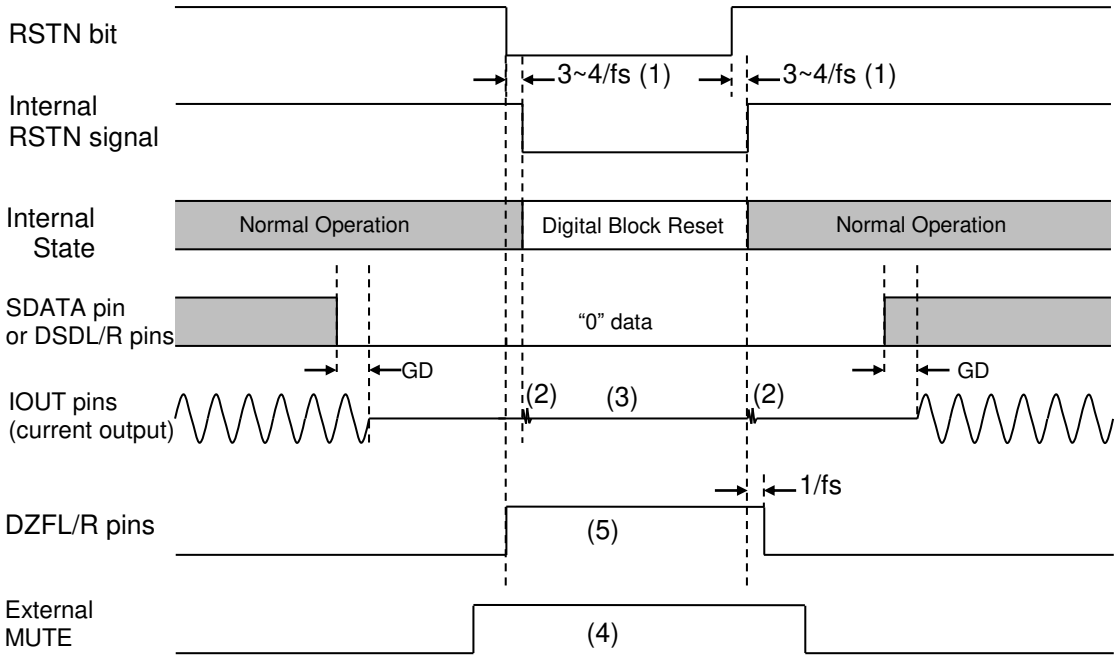


Notes:
(1) The corresponding channels become standby state immediately when writing “0” to PW1/2 bits.
(2) Click noise occurs on an edge of PW1/2 bits (“↓ ↑”). This noise is output even if “0” data is input.
(3) The analog output is floating (Hi-Z) state when PW1/2 bits = “0”.
(4) Mute the analog output externally if click noise (2) or Hi-z output (3) adversely affect system performance.
(5) The zero detection function is enable when the AK4499 is in standby state (PW1/2 bits = “0”). This figure shows the seuqnece when DZFE bit = “1” and DDMOE bit = “0”.
(6) It takes 2 to 3/fs until standby state is released when writing “1” to PW1/2 bits.

Figure 67. Standby Sequence by PW1/2 bit (Register Control Mode)

9.14.3. Reset by RSTN bit

Digital circuits except control registers, MCLK stop detection circuit, and clock divider are reset by setting RSTN bit to “0”. In this case, control register settings are held, the analog output becomes zero signal output and the DZFL/DZFR pin outputs “H”. Figure 68 shows reset sequence by RSTN bit.

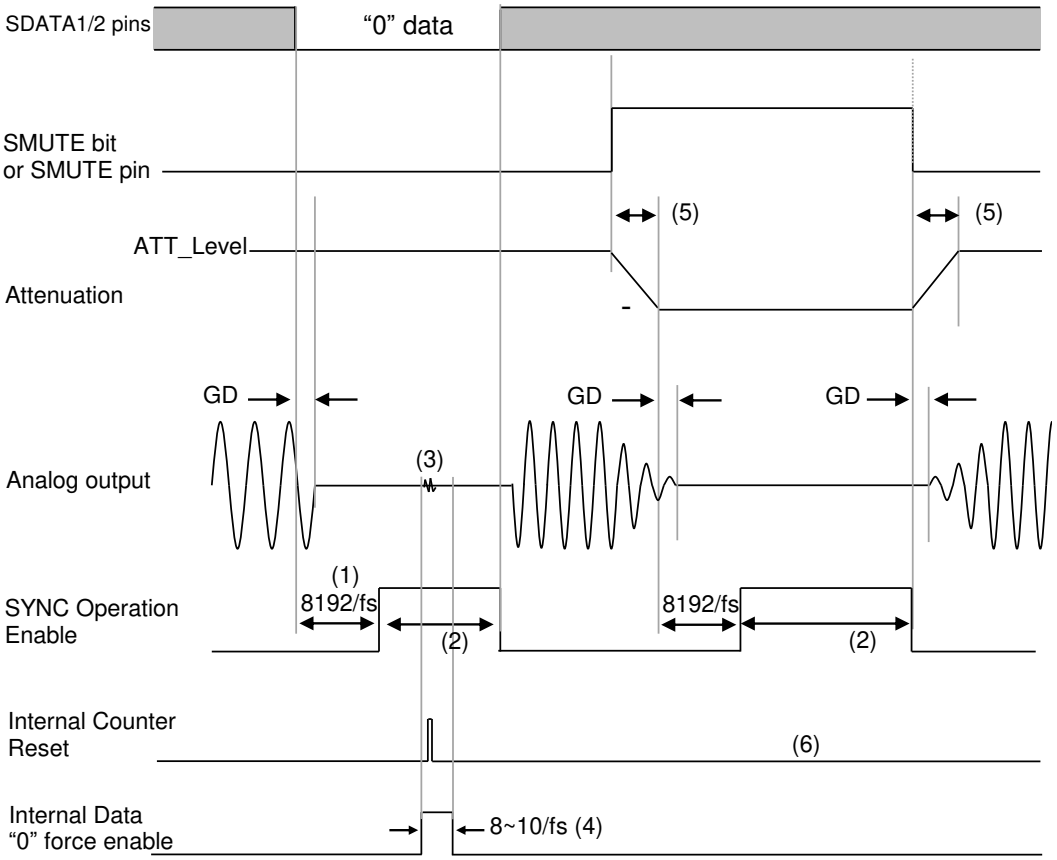


Notes:
(1) It takes 3 to 4/fs until a reset instruction is valid when changing RSTN bit to “0” and it takes 3 to 4/fs when releasing the reset.
(2) Click noise occurs on an edge of internal RSTN signal. This noise is output even if “0” data is input.
(3) Mute the analog output externally if click noise (2) adversely affect system performance.
(4) The analog output is zero signal when RSTN bit = “0”.
(5) This figure shows the seuqnece when DZFE bit = “1” and DDMOE bit = “0”. The DZF pin goes “H” on a falling edge of RSTN bit and goes “L” 1/fs after a rising edge of internal RSTN bit.

Figure 68 . Reset Timing Example (Register Control Mode)

9.15. Synchronize Function (PCM Mode, EXDF Mode)

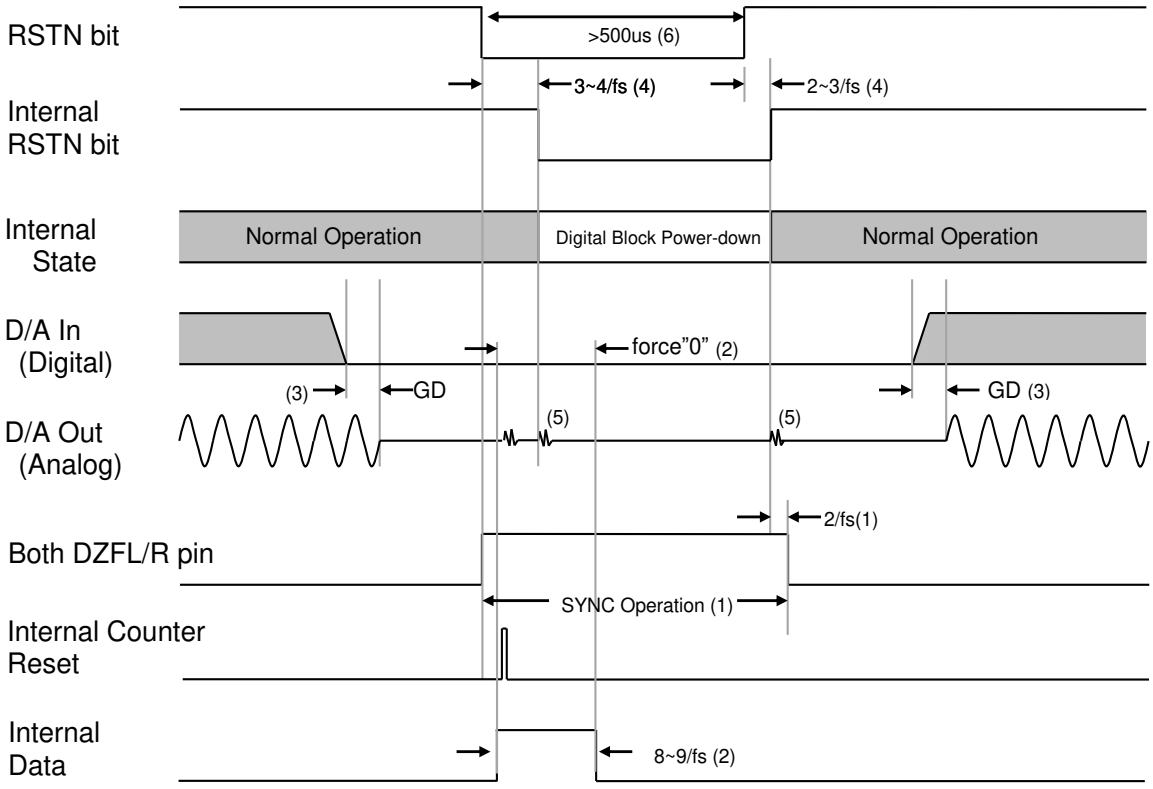
The AK4499 has a synchronize function. With this synchronize function, group delays between each device can be kept within 3/256 fs when using multiple AK4499's.
In PCM or EXDF mode, clock synchronize function becomes valid when input data of all channels are "0" for 8192 times continuously, when all channels data become "0" and kept for 8192 times continuously by attenuation, or when RSTN bit = "0". In PCM mode, the internal counter is synchronized with a rising edge of LRCK (falling edge of LRCK when the data format is I²S compatible). In EXDF mode, the internal counter is synchronized with a rising edge of WCK. In this case, the analog output becomes zero signal. This function is disabled by setting SYNCE bit = "0" in Register Control mode.
Figure 69 shows a synchronizing sequence when the input data is "0" for 8192 times continuously.
Figure 70 shows a synchronizing sequence by RSTN bit.



Notes:
(1) When all channels data are "0" for 8192 times continuously, the synchronize function is enabled.
(2) To ensure the synchronization, zero data input should be kept for 500 μs at least after the synchronize function is enabled.
(3) Input data of ΔΣ Modulator is fixed to "0" forcibly for 8 to 9/fs when internal counter is reset.
(4) Click noise may occur when the internal counter is reset. This noise is output even if "0" data is input. Mute the analog output externally if this click noise affects the system performance.
(5) Refer to "9.7. Digital Attenuator" for ATT transition time.
(6) When the internal clock and external input clock are in synchronization, the internal counter will not be reset even if the synchronize function is valid.

Figure 69. Synchronization Sequence by Continuous "0" Data Input for 8192 Times

If RSTN bit is set to “0”, digital circuit is reset in 3 to 4/fs and the synchronization function becomes valid.



Notes:

(1) Since the analog output corresponding to digital input has group delay (GD), it is recommended to have a no-input period longer than the group delay before writing “0” to RSTN bit.
(2) The synchronization function becomes valid on a falling edge of RSTN bit. It takes about 2/fs to become invalid after the internal RSTN is changed when changing RSTN bit to “1”.
(3) It takes 3 to 4/fs until the internal RSTN is changed when changing RSTN bit to “0” and it takes 3 to 4/fs when changing RSTN bit to “1”. The synchronization function becomes valid immediately when writing “0” to RSTN bit. Therefore, there is a case that the internal counter is reset before internal RSTN signal of the LSI is changed.
(4) Input data of ΔΣ Modulator is fixed to “0” forcibly for 2 to 3/fs when the internal counter is reset.
(5) Click noise occurs on rising and falling edges of the internal RSTN signal and when the internal counter is reset. This noise is output even if “0” data is input. Mute the analog output externally if this click noise affects the system performance.
(6) To ensure the synchronization, reset state should be kept for 500 μs at least after the synchronize function is enabled.

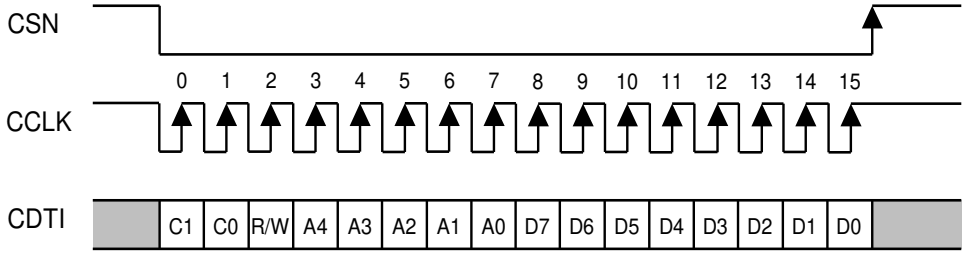
Figure 70. Synchronization Sequence by RSTN bit (Register Control Mode)

9.16. Register Control Interface

9.16.1. 3-wire Serial Control Mode (I2C pin = "L")

Internal registers may be written to through 3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2 bits, C1/0), Read/Write (1 bit; fixed to "1", write only), Register address (MSB first, 5 bits) and Control data (MSB first, 8 bits). The data is output on a falling edge of CCLK and the data is received on a rising edge of CCLK. The writing of data is valid when CSN "↑". The clock speed of CCLK is 5 MHz (max).

Setting the PDN pin to "L" resets the registers to their default values. In Register Control mode, the digital block except control registers and clock divider is reset by setting RSTN bit to "0". In this case, the register values are not initialized.



C1-0: Chip Address (C1 bit = CAD1 pin, C0 bit = CAD0 pin)
R/W: READ/WRITE (Fixed to "1", Write only)
A4-0: Register Address
D7-0: Control Data

Figure 71. Control I/F Timing

* The AK4499 does not support read commands in 3-wire serial control mode.
* When the PDN pin = "L", writing into control registers is prohibited.
* The control data cannot be written when the CCLK rising edge is 15 times or less, or 17 times or more during CSN is "L".

9.16.2. I²C Bus Control Mode (I2C pin = "H")

The AK4499 supports the fast-mode I²C-bus (max:400 kHz, Ver1.0).

9.16.2.1. WRITE Operation

Figure 72 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 78). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1 and CAD0 (device address bits). This bit identifies the specific device on the bus. The hard-wired input pin (CAD1 pin, CAD0 pin) sets these device address bits (Figure 73). If the slave address matches that of the AK4499, the AK4499 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 79). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4499 and the format is MSB first. The most significant three bits are fixed as "000" (Figure 74). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 75). The AK4499 generates an acknowledge after each byte is rece

ived. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 78).

The AK4499 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4499 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds "15H" prior to generating a stop condition, the address counter will "roll over" to "00H" and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 80) except for the START and STOP conditions.

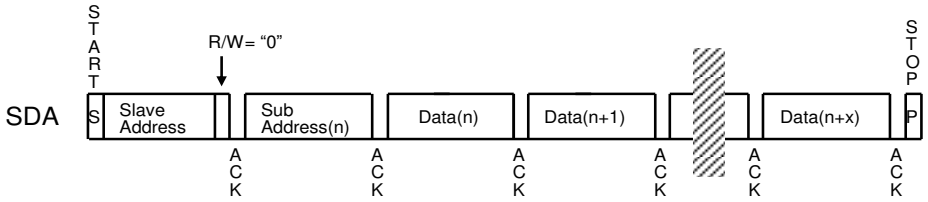


Figure 72. Data Transfer Sequence in I²C Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(CAD1 and CAD0 are set by pin)

Figure 73. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 74. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 75. Byte Structure after The Second Byte

9.16.2.2. READ Operation

Set the R/W bit = “1” for the READ operation of the AK4499. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “15H” prior to generating stop condition, the address counter will “roll over” to “00H” and the data of “00H” will be read out.

The AK4499 supports two basic read operations: Current Address Read and Random Address Read.

9.16.2.2.1. Current Address Read

The AK4499 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4499 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4499 ceases the transmission.

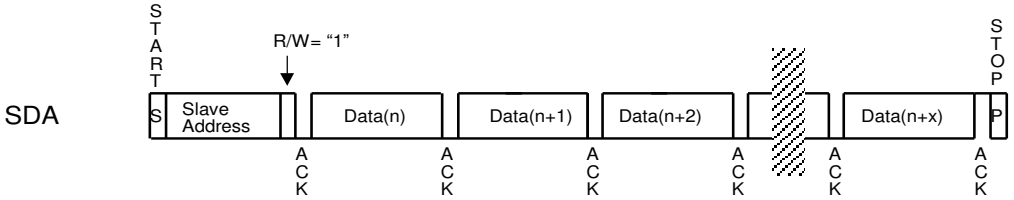


Figure 76. Current Address Read

9.16.2.2.2. Random Address Read

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK4499 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4499 ceases the transmission.

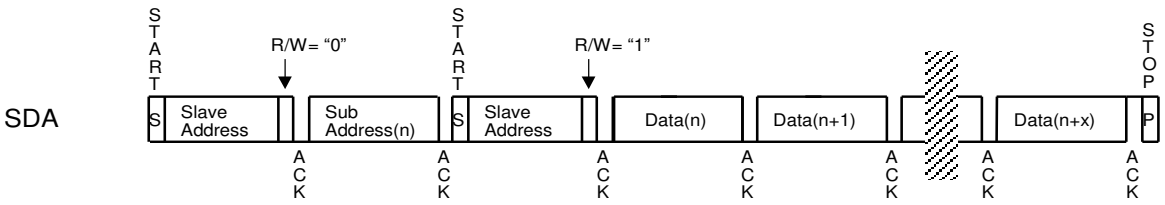


Figure 77. Random Address Read

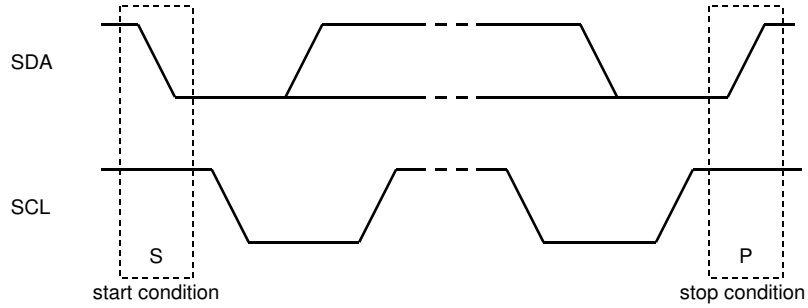


Figure 78. Start Condition and Stop Condition

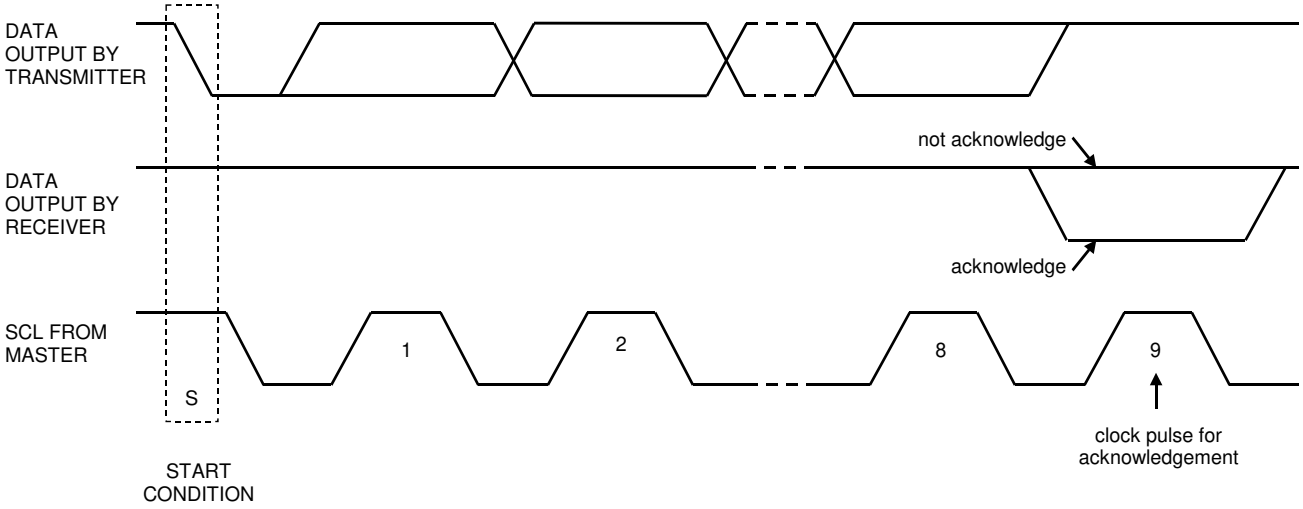


Figure 79. Acknowledge (I^2C Bus)

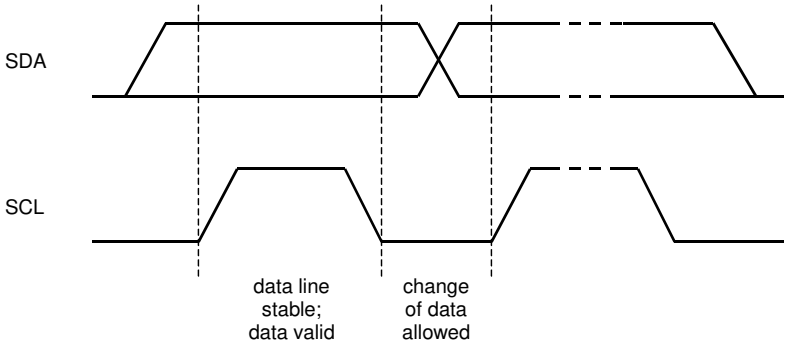


Figure 80. Bit Transfer (I^2C Bus)

9.17. Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
00H	Control 1	ACKS	EXDF	ECS	AFSD	DIF[2]	DIF[1]	DIF[0]	RSTN	0CH
01H	Control 2	DZFE	DZFM	SD	DFS[1]	DFS[0]	DEM1[1]	DEM1[0]	SMUTE	22H
02H	Control 3	DP	ADP	DCKS	DCKB	MONO1	DZFB	SELLR1	SLOW	00H
03H	L1ch ATT	ATTL1[7]	ATTL1[6]	ATTL1[5]	ATTL1[4]	ATTL1[3]	ATTL1[2]	ATTL1[1]	ATTL1[0]	FFH
04H	R1ch ATT	ATTR1[7]	ATTR1[6]	ATTR1[5]	ATTR1[4]	ATTR1[3]	ATTR1[2]	ATTR1[1]	ATTR1[0]	FFH
05H	Control 4	INVL1	INVR1	INVL2	INVR2	SELLR2	0	DFS[2]	SSLOW	00H
06H	DSD1	DDM	DML1	DMR1	DDMOE	0	DDMT	DSDD	DSDSEL[0]	00H
07H	Control 5	DZFSEL	0	0	0	0	GC[1]	GC[0]	SYNCE	01H
08H	Reserved	0	0	0	0	0	0	0	0	00H
09H	DSD2	DML2	DMR2	0	0	0	DSDPATH	DSDF	DSDSEL[1]	00H
0AH	Control 6	TDM[1]	TDM[0]	SDS[1]	SDS[2]	PW2	PW1	DEM2[1]	DEM2[0]	0DH
0BH	Control 7	ATS[1]	ATS[0]	MONO2	SDS[0]	0	0	DCHAIN	0	00H
0CH	L2ch ATT	ATTL2[7]	ATTL2[6]	ATTL2[5]	ATTL2[4]	ATTL2[3]	ATTL2[2]	ATTL2[1]	ATTL2[0]	FFH
0DH	R2ch ATT	ATTR2[7]	ATTR2[6]	ATTR2[5]	ATTR2[4]	ATTR2[3]	ATTR2[2]	ATTR2[1]	ATTR2[0]	FFH
0EH	Reserved	0	0	0	0	0	0	0	0	00H
0FH	Reserved	0	0	0	0	0	0	0	0	00H
10H	Reserved	0	0	0	0	0	0	0	0	00H
11H	Reserved	0	0	0	0	0	0	0	0	00H
12H	Reserved	0	0	0	0	0	0	0	0	00H
13H	Reserved	0	0	0	0	0	0	0	0	00H
14H	Reserved	0	0	0	0	0	0	0	0	00H
15H	Control 8	ADPE	ADPT[1]	ADPT[0]	0	0	ADFS[2]	ADFS[1]	ADFS[0]	00H

Notes:

(1) In 3-wire serial control mode, the AK4499 does not support read commands.
(2) The AK4499 supports read command in I2C-bus control mode.
(3) If the address exceeds “15H”, the address counter will “roll over” to “00H” and the next write/read address will be “00H” by automatic increment function in I²C-Bus mode.
(4) Bits indicated as 0 in each address must contain a “0” value. Malfunctions may occur if writing “1” value to these bits.
(5) Writing after 16H is forbidden. Malfunctions may also occur by this action.
(6) When the PDN pin goes to “L”, the registers are initialized to their default values.
(7) When RSTN bit is set to “0”, the digital block except control registers and clock divider is reset, and the registers are not initialized to their default values.
(8) When the PSN pin status is changed, the AK4499 should be reset by the PDN pin.
(9) The AK4499 is register compatible with the AK4490, AK4493, AK4495 and the AK4497.

9.18. Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	AFSD	DIF[2]	DIF[1]	DIF[0]	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

RSTN: Internal Timing Reset
0: Reset. All registers are not initialized. (default)
1: Normal Operation

DIF[2:0]: Audio Data Interface modes (Table 21)
Initial value is “110” (Mode 6: 32bit MSB justified)

AFSD: Sampling Frequency Auto Detect Mode Enable (PCM/EXDF modes only, Table 14, Table 15).
0: Disable: Manual or Auto Setting mode (default)
1: Enable: Auto Detect mode

ECS: EXDF mode clock setting (Table 20)
0: WCK = 705.6 kHz or 768 kHz mode (default)
1: WCK = 352.8 kHz or 384 kHz mode

EXDF: External Digital Filter I/F Mode (Register Control mode only)
0: Disable: Internal Digital Filter mode (default)
1: Enable: External Digital Filter mode

ACKS: Master Clock Frequency Auto Setting Mode Enable (PCM/EXDF modes only). (Table 6, Table 12, Table 13)
0: Disable: Manual Setting mode (default)
1: Enable: Auto Setting mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	DZFE	DZFM	SD	DFS[1]	DFS[0]	DEM1[1]	DEM1[0]	SMUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal Operation (default)
1: DAC outputs soft-muted.

DEM1[1:0]: DAC1 De-emphasis Filter Control (Table 27)
Initial value is “01” (OFF).

DFS[2:0]: Sampling Speed Control (Table 8)
Initial value is “000” (Normal Speed mode). A click noise occurs when changing DFS[2:0] bits setting.

SD: Short Delay Filter Enable (Table 25)
0: Traditional filter
1: Short Delay filter (default)

DZFM: Output select for DZFL/R pins (Table 35, Table 36)
DZFE: Output select for DZFL/R pins (Table 35, Table 36)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	DP	ADP	DCKS	DCKB	MONO1	DZFB	SELLR1	SLOW
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SLOW: Slow Roll-off Filter Enable (Table 25)
0: Sharp Roll-off filter (default)
1: Slow Roll-off filter

SELLR1: DAC1 data selection of L channel and R channel (Table 39)

DZFB: Inverting Enable of DZF (Table 33)
0: DZF pin goes “H” at Zero Detection (default)
1: DZF pin goes “L” at Zero Detection

MONO1: DAC1 Mono/Stereo mode select (Table 39)
0: Stereo mode (default)
1: Mono mode

DCKB: Polarity of DCLK (DSD Only)
0: DSD data is output from DCLK falling edge. (default)
1: DSD data is output from DCLK rising edge.

DCKS: Master Clock Frequency Select at DSD mode (DSD only)
0: 512fs (default)
1: 768fs

ADP: Read Back register for internal operation mode. This bit is valid when ADRE bit = “1”.
It is invalid when ADPE bit = “0” and readouts “0” when read.
0: PCM mode/EXDF mode
1: DSD Mode

DP: DSD/PCM Mode Select
0: PCM mode (default)
1: DSD mode
When DP bit is changed, the AK4499 should be reset by RSTN bit.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	L1ch ATT	ATTL1[7]	ATTL1[6]	ATTL1[5]	ATTL1[4]	ATTL1[3]	ATTL1[2]	ATTL1[1]	ATTL1[0]
04H	R1ch ATT	ATTR1[7]	ATTR1[6]	ATTR1[5]	ATTR1[4]	ATTR1[3]	ATTR1[2]	ATTR1[1]	ATTR1[0]
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATTL1[7:0]: DAC1 L channel Attenuation Level setting (Table 29)
ATTR1[7:0]: DAC1 R channel Attenuation Level setting (Table 29)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Control 4	INVL1	INVR1	INVL2	INVR2	SELLR2	0	DFS[2]	SSLOW
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SSLOW: Super Slow Roll-off (Digital Filter bypass mode) or Low Dispersion Filter Enable (Table 25)
0: Disable (default)
1: Enable

DFS[2]: Sampling Speed Control (Table 8)
Initial value is “000” (Normal Speed mode). A click noise occurs when changing DFS[2:0] bits setting.

SELLR2: DAC2 data selection of L channel and R channel (Table 39)

INVR2: DAC2 IOUTR Output Phase Inverting (Table 39)
0: Disable (default)
1: Enable

INVL2: DAC2 IOUTL Output Phase Inverting (Table 39)
0: Disable (default)
1: Enable

INVR1: DAC1 IOUTR Output Phase Inverting (Table 39)
0: Disable (default)
1: Enable

INVL1: DAC1 IOUTL Output Phase Inverting (Table 39)
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	DSD1	DDM	DML1	DMR1	DDMOE	0	DDMT	DSDD	DSDSEL[0]
R/W		R/W	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSDSEL[1:0]:DSD sampling speed control (Table 18)

DSDD: DSD Playback Path Control
0: Normal Path (default)
1: Volume Bypass

DDMT: DSD Signal Full-scale Detection Time Setting (Table 37)

DDMOE: Zero Detection/DSD Signal Full-scale Detection Flag Selection (Table 32)

DMR1/L1: This register outputs detection flag when a full-scale is detected at the DSDR1 pin /DSDL1 pin.

DDM: DSD data mute
The AK4499 has an internal mute function that mutes the output when DSD input data becomes all “1” or all “0” for 2048 samples (1/fs) continuously. DDM bit controls this function.
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Control 5	DZFSEL	0	0	0	0	GC[1]	GC[0]	SYNCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

SYNCE: SYNC Mode Enable
0: SYNC mode Disable
1: SYNC mode Enable (default)

GC[1:0]: Gain Control (Table 31)

DZFSEL: Output select for DZFL/R pins (Table 35, Table 36)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Reserved	0	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

08H: All Reserved

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	DSD2	DML2	DMR2	0	0	0	DSDPATH	DSDF	DSDSEL[1]
R/W		R	R	R	R	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSDSEL[1:0]: DSD sampling speed control (Table 18)

DSDF: Cut-off frequency of DSD Filter control (Table 26)

DSDPATH: DSD data input pin select (Table 4)

DMR2/L2: This register outputs detection flag when a full-scale signal is detected at the DSDR2 pin/ DSDL2 pin.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Control 6	TDM[1]	TDM[0]	SDS[1]	SDS[2]	PW2	PW1	DEM2[1]	DEM2[0]
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	1

DEM2[1:0]: DAC2 De-emphasis Filter Control (Table 27)
Initial value is “01” (OFF).

PW1: DAC1 Power Control (Table 47)

PW2: DAC2 Power Control (Table 47)

SDS[2:0]: Output Data Slot Selection of Each Channel (Table 22)

TDM[1:0]: TDM Mode Select
00: Normal (default)
01: TDM128
10: TDM256
11: TDM512

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Control 7	ATS[1]	ATS[0]	MONO2	SDS[0]	0	0	DCHAIN	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DCHAIN: Daisy Chain Mode Enable
0: Daisy Chain mode Disable (default)
1: Daisy Chain mode Enable

SDS[2:0]: Output Data Slot Selection of Each Channel (Table 22)

MONO2: DAC2 Mono/Stereo mode select (Table 39)
0: Stereo mode (default)
1: Mono mode

ATS[1:0]: Transition Time Between Set Values of ATT[7:0] bits (Table 30)
Initial value is “00”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	L2ch ATT	ATTL2[7]	ATTL2[6]	ATTL2[5]	ATTL2[4]	ATTL2[3]	ATTL2[2]	ATTL2[1]	ATTL2[0]
0DH	R2ch ATT	ATTR2[7]	ATTR2[6]	ATTR2[5]	ATTR2[4]	ATTR2[3]	ATTR2[2]	ATTR2[1]	ATTR2[0]
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATTL2[7:0]: DAC2 L channel Attenuation Level setting (Table 29)
ATTR2[7:0]: DAC2 R channel Attenuation Level setting (Table 29)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Reserved	0	0	0	0	0	0	0	0
0FH	Reserved	0	0	0	0	0	0	0	0
10H	Reserved	0	0	0	0	0	0	0	0
11H	Reserved	0	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

0EH: Reserved
0FH: Reserved
10H: Reserved
11H: Reserved

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	Reserved	0	0	0	0	0	0	0	0
13H	Reserved	0	0	0	0	0	0	0	0
14H	Reserved	0	0	0	0	0	0	0	0
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

12H: Reserved
13H: Reserved
14H: Reserved

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	Control 8	ADPE	ADPT[1]	ADPT[0]	0	0	ADFS[2]	ADFS[1]	ADFS[0]
R/W		R/W	R/W	R/W	R/W	R/W	R	R	R
Default		0	0	0	0	0	0	0	0

ADFS[2:0]: fs Auto Detect Mode Detection Result (Table 16)

ADPT[1:0]: Time until PCM/DSD mode detection when input data becomes zero (PCM/EXDF⇔DSD modes) (Table 42)

ADPE: Automatic Mode Switching Function Enable Bit for PCM/EXDF and DSD Modes
0: Disable (default)
1: Enable

10. Recommended External Circuits

10.1. External Connection Example

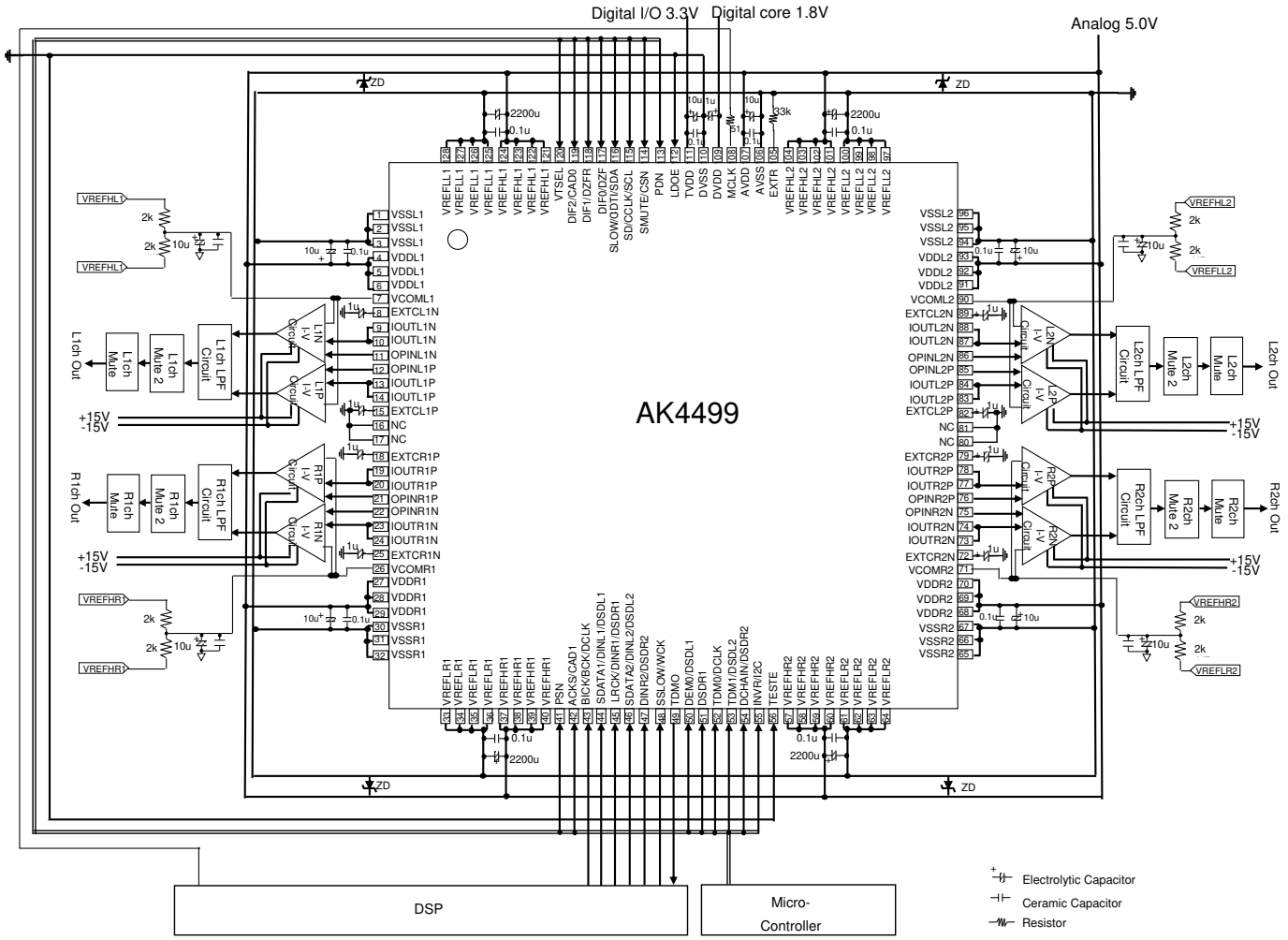


Figure 81. Typical Connection Diagram
(AVDD = VDDL1/R1/L2/R2 = 5.0 V, TVDD = 3.3 V, LDOE pin = "L", Register Control Mode)

Notes:
(1) Chip Address = "00".
(2) Power lines of AVDD, TVDD, VDDL1/R1 and VDDL2/R2 should be distributed separately, from the point with low impedance of regulators or other parts.
(3) AVSS, DVSS, VSSL1/R1 and VSSL2/R2 must be connected to the same analog ground plane. (Analog ground should have low impedance as a solid pattern. THD+N characteristics will degrade if there are impedances between each VSS.)
(4) When using LDO, the digital core circuit power supply (DVDD) is supplied from the built-in LDO. DVDD should not be used for any external circuit loads.
(5) Connect VCOML1/R1/L2/R2 and positive input pin of I-V conversion op-amp from the midpoint each four Voff circuits that connects VREFHL1/L2/R1/R2 and VREFLL1/L2/R1/R2 via the external voltage divider resistors. Four Voff circuits do not connect any other pins except VCOML1/R1/L2/R2 and positive input pins.
(6) It is recommended to input MCLK via a 51Ω damping resistor. Without the resistor, there is a possibility that THD+N characteristic degrades because of high-frequency noise of MCLK.
(7) All digital input pins except pull-down/pull-up pins should not be allowed to float.

(8) A 1 µF capacitor must be connected to the EXTCL1P/L1N, EXTCR1P/R1N, EXTCL2P/L2N, and EXTCR2P/R2N pins independently, even when only using one of DAC1 or DAC2.
(9) There is a possibility of IC destruction due to breakdown of the withstanding voltage of the analog output pins (IOUTLP/LN/RP/RN). Connect a Zener diode (V_{RWM} = 6 to 7 V) between each VDDL1/R1/L2/R2 and VSSL1/R1/L2/R2 if the power up/down sequence shown in Figure 65 cannot be followed.
(10) To avoid click noise, connect an external mute circuit if the power up/down sequence shown in Figure 65 cannot be followed. Refer to "10.4.4. External Mute Circuit" for details.

10.2. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD, TVDD, DVDD and VDDL1/R1/L2/R2. AVDD and VDDL1/R1/L2/R2 are supplied from analog supply in system, and TVDD and DVDD are supplied from digital supply in system. Power lines of VDDL1/R1/L2/R2 should be distributed separately, from the point with low impedance of regulators or other parts.
When not using LDO (LDOE pin = "L"), TVDD must be powered up before DVDD is powered up or at the same time. AVSS, DVSS, VSSL1/R1 and VSSL2/R2 must be connected to the same analog ground plane. Decoupling capacitors for high frequency should be placed as near as possible to the AK4499.

10.3. Reference Voltage

The differential voltage between the VREFHL1/R1/L2/R2 pin and the VREFLL1/R1/L2/R2 pin set the full-scale of the analog output range. The VREFHL1/R1/L2/R2 pin is normally connected to 5.0V reference voltage, and the VREFLL1/R1/L2/R2 pin is normally connected to the 0V reference voltage. Connect a 0.1μF ceramic capacitor and 2200 μF electrolytic capacitor between the VREFHL1/R1/L2/R2 pin and the VREFL L1/R1/L2/R2 pin.
The VREFHL1/R1/L2/R2 and VREFL L1/R1/L2/R2 pins should avoid noises from other power supplies. Connect the VREFHL1/R1/L2/R2 to the analog 5.0V via a 1Ω resistor, and the VREFL pin to the analog ground via a 1Ω resistor when it is difficult to obtain expected analog characteristics because of noises from other power supplies (A low pass filter of fc=36Hz will be composed with the 2200 μF capacitor and the 1Ω resistor. It removes signal frequency noise from other power supply lines). However, the direct voltage at the VREFHL1/R1/L2/R2 and VREFL L1/R1/L2/R2 pins drops ±23 mV since a current of ±23 mA flows at VREFH/L via 1 Ω resistor.
The ceramic capacitors should be connected as near as possible to the pins. All digital signals, especially clocks, should be kept away from the VREFHL1/R1/L2/R2 and VREFLL1/R1/L2/R2 pins in order to avoid unwanted coupling into the AK4499.

10.4. Analog Output

10.4.1. I-V Conversion Circuit Example

The analog outputs are full differential outputs. The full-scale output is 36.4 mApp Typ. The output current is converted to voltage by the I-V conversion circuit. Common voltage of the output signals is 2.5V but signal common of the I-V converted voltage can be adjusted with positive input of op-amp for I-V conversion, four Voff circuits, and VCOML1/R1/L2/R2, that is (VREFHL1/L2/R1/R2 + VREFLL1/L2/R1/R2)/2, since the output impedance is 110 Ω (typ.). For example, input Voff = 1.9V to obtain 0V signal common voltage at Rfb = 360Ω.
The output range of I-V conversion is 4.6 Vrms centered around signal common voltage, and 9.2 Vrms after differential summing. IOUTL1P/R1P/L2P/R2P current and IOUTL1N/R1N/L2N/R2N current cannot be summed. The differential outputs are summed externally after I-V conversion.

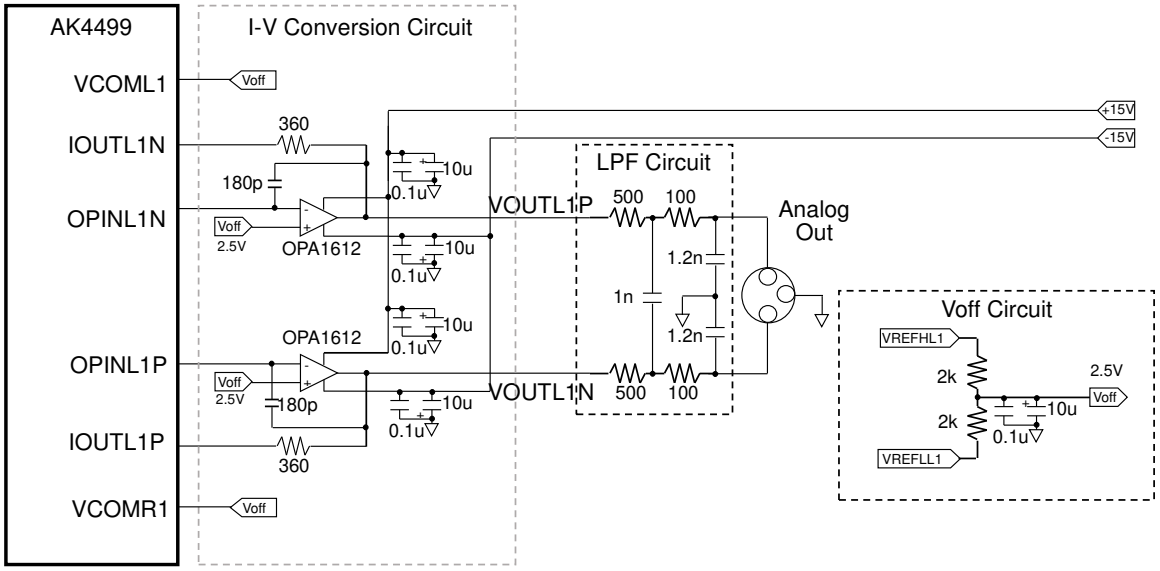


Figure 82. L1ch External I-V Conversion Circuit Example (same for R1ch, L2ch and R2ch)

Notes:

(1) Input voltage range of the operational amplifier for I-V conversion circuit is from 0.5 V (typ.) to 2.5 V (typ.). The signal common voltage (VOUTL1P and VOUTL1N) does not have to be 0V.

(2) Resistors used in the I-V conversion circuit are recommended to be within 0.1% of absolute error in order to meet specifications.

Table 49. Frequency Response of Differential Output Circuit

Gain (1 kHz, typ)		0.0 dB
Frequency Response (ref: 1 kHz, typ)	20 kHz	-0.18 dB
	40 kHz	-0.69 dB
	80 kHz	-2.28 dB

In mono mode, connect I-V conversion voltage output terminals with resistors and take differential output from the midpoint (Voff) of the connection as shown in Figure 83.

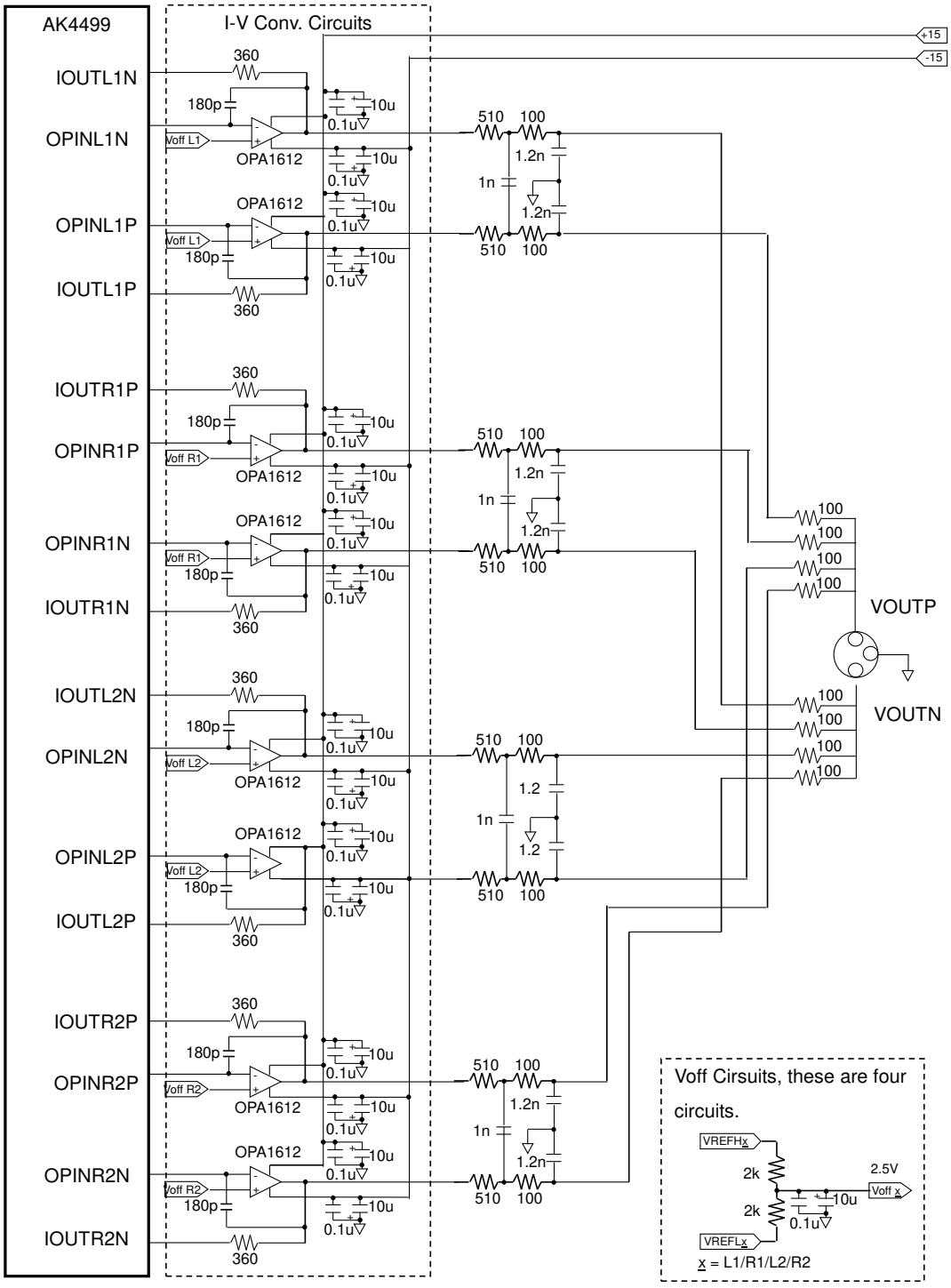


Figure 83. External I-V Conversion Circuit Example (Mono mode)

10.4.2. External Analog Low Pass Filter Example

Differential voltage signal after I-V conversion is summed by differential summing circuit (low pass filter). Figure 84 shows an example of differential summing circuit and Table 50 shows the frequency response.

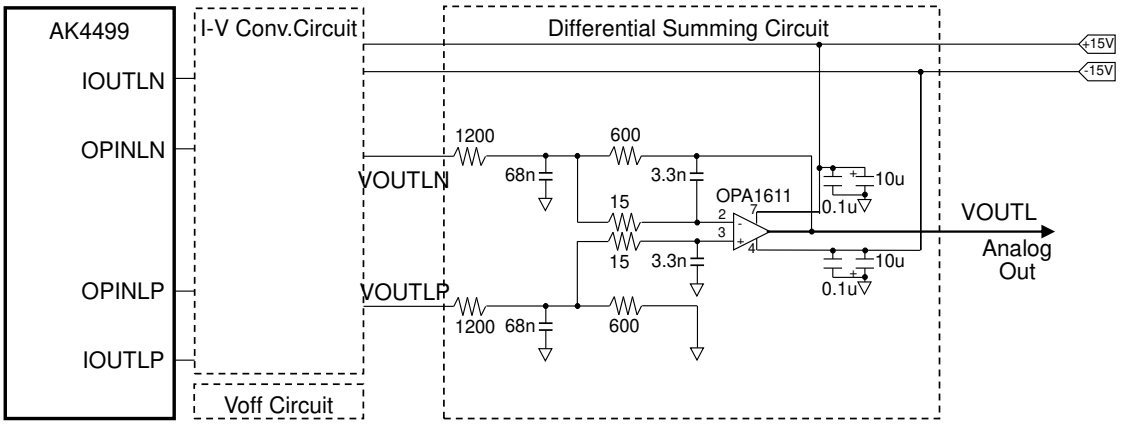


Figure 84. External 2nd Order LPF Circuit Example for PCM mode (fc = 112 kHz (typ), Q = 0.692 (typ))

Table 50. Frequency Response of External LPF Circuit Example

Gain (1 kHz, typ)		-6.02 dB
Frequency Response (ref:1 kHz, typ)	20 kHz	-6.04 dB
	40 kHz	-6.14 dB
	80 kHz	-7.19 dB

In DSD mode, signal pass out-of-band noise included in DSD data will be reduced by an internal digital filter of the AK4499 and an external analog low-pass filter (differential summing circuit). The cutoff frequency of the external analog low-pass filter can be changed by setting C1, C2, and C3 capacitance in Figure 85 according to the values shown in Table 51.

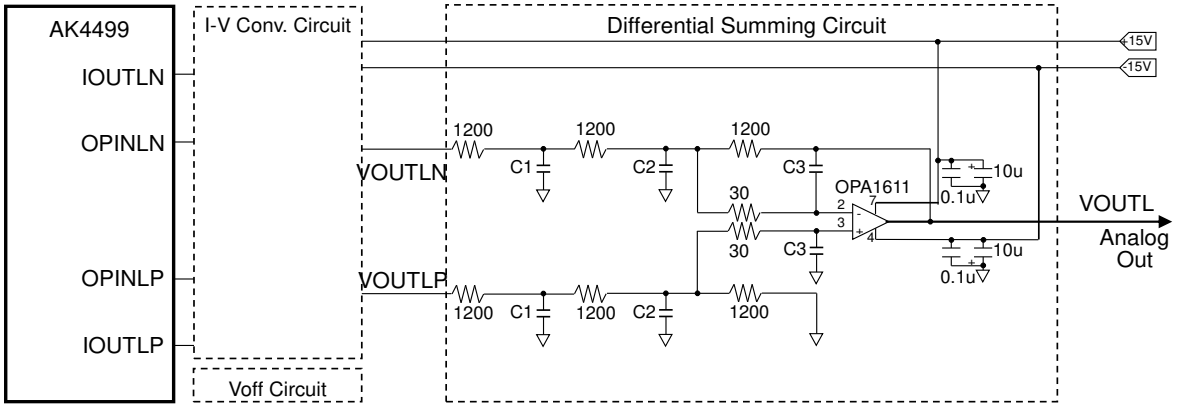


Figure 85. External 3rd Order LPF Circuit Example for DSD mode

Table 51. C1//2/3 Setting Value to Synchronize DSD Filter and fc of External 3rd LPF

DSD Rate	Internal DSD Filter Cut Off Frequency @fs = 44.1 kHz	C1, C2, C3 Setting Value [nF]		
		C1	C2	C3
DSD64@DSDF bit = ”0”	37 kHz	7.5	160	3.0
DSD64@DSDF bit = “1”	65 kHz	4.7	91	1.8
DSD128@DSDF bit = “0”	74 kHz	3.9	82	1.5
DSD128@DSDF bit =”1”	131 kHz	2.2	47	0.91
DSD256	238 kHz	1.2	27	0.47
DSD512	476 kHz	0.62	13	0.24

10.4.3. Feedback Loop of External Operational Amplifier

Figure 86 shows the internal status of the AK4499 when the analog output is Hi-Z (PDN = L, PW1/2 = L, or audio clocks stopped) and when the analog output is idle (reset state). Feedback loop of the external amplifier is always maintained while the power supply of the AK4499 is on.

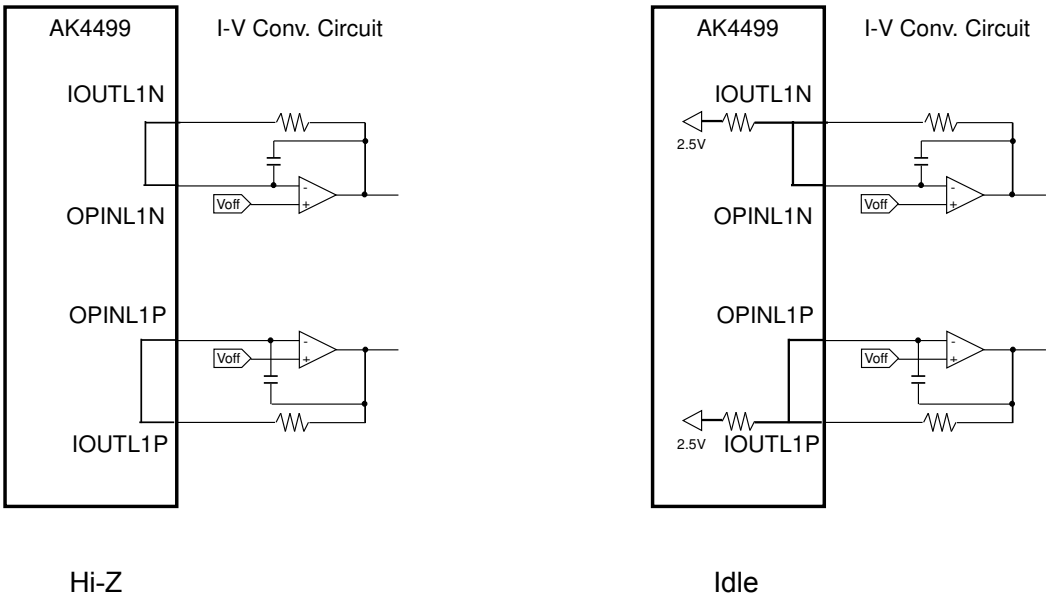


Figure 86. Internal Status of the AK4499 when Outputting Hi-Z or Idle

10.4.4. External Mute Circuit

Click noise may occur due to DC offset if the power up/down sequence shown in Figure 65 cannot be followed and external operational amplifier is powered up before the AK4499. Connect external mute circuits shown in Figure 87 to analog signal lines to prevent a click noise. The external mute circuit should be connected to the signal after I-V conversion (Figure 81). Base current will be input to the transistor RN2202 when the power (5.0V typ.) is not supplied to the VDDL1/R1/L2/R2 pins. In this case, emitter current flows to the 2SC3327 via 3.8kΩ resistance as base current and the analog signal line is short to the signal ground. Note that there is a possibility that THD+N performance degrades about 3dB by connecting an external mute circuit.

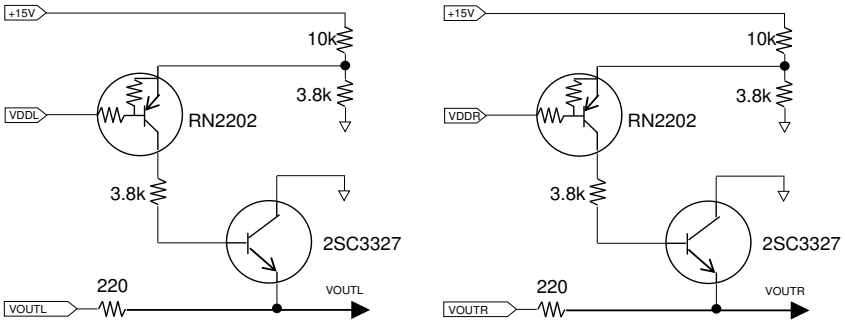
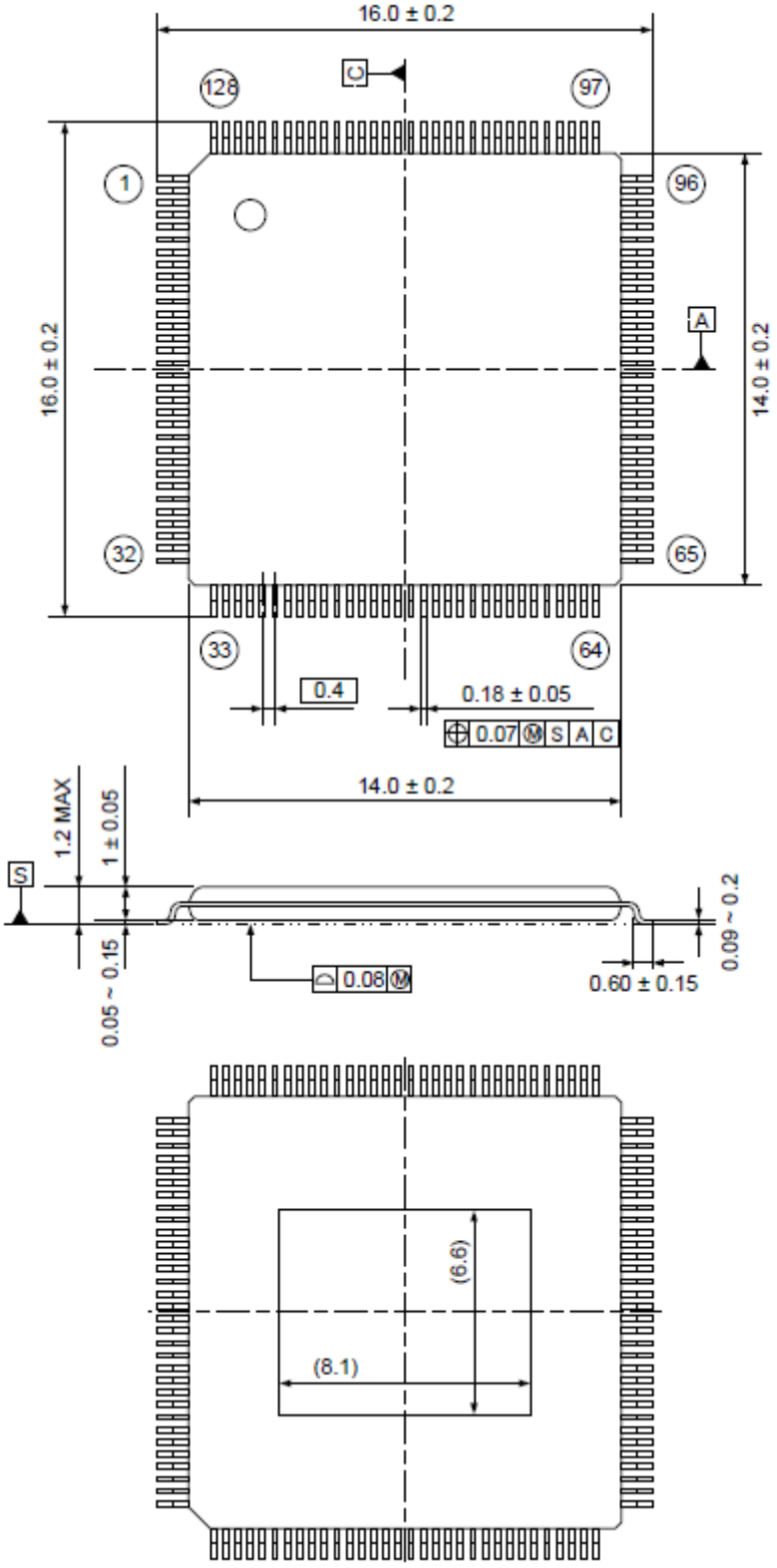


Figure 87. External Mute Circuit Example

11. Package

11.1. Outline Dimensions (HTQFP14 x 14-128, Unit: mm)



11.2. Material & Terminal Finish

Package molding compound:	Epoxy, Halogen (bromine and chlorine) free
Lead frame material:	EFTEC64
Pin surface treatment:	Solder (Pb free) plate

11.3. Marking

1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK4499EQ
4) AKM Logo

12. Ordering Guide

AK4499EQ	−40 to +85°C	128-pin HTQFP (0.4 mm pitch)
AKD4499	Evaluation Board for AK4499	

13. Revision Histroy

Date (Y/M/D)	Revision	Reason	Page	Contents
19/02/27	00	First Edition		

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