300MHz Wideband Receiver

FEATURES

- **Integrated I/Q Demodulator, IF Amplifier, and Dual 14-Bit, 310Msps High Speed ADC**
- **External Highpass Filter Allows Bandwidth Adjustment**
- **300MHz Lowpass Filter for Each Channel**
- **RF Input Frequency Range: 0.7GHz to 4GHz**
- **50Ω Single-Ended RF Port**
- **50Ω Differential LO Port**
- **Frequency Flatness: 1.3dB Typical**
- **66dBc IM3 Level at –7dBFS**
- **59dB SNR at –1dBFS**
- **Parallel DDR LVDS Outputs**
- Clock Duty Cycle Stabilizer
- Low Power: 2.6W
- Shutdown and Nap Modes
- 15mm × 15mm BGA Package

APPLICATIONS

- Telecommunications
- Wideband, Low IF Receivers
- Digital Predistortion Receivers
- Cellular Base Stations

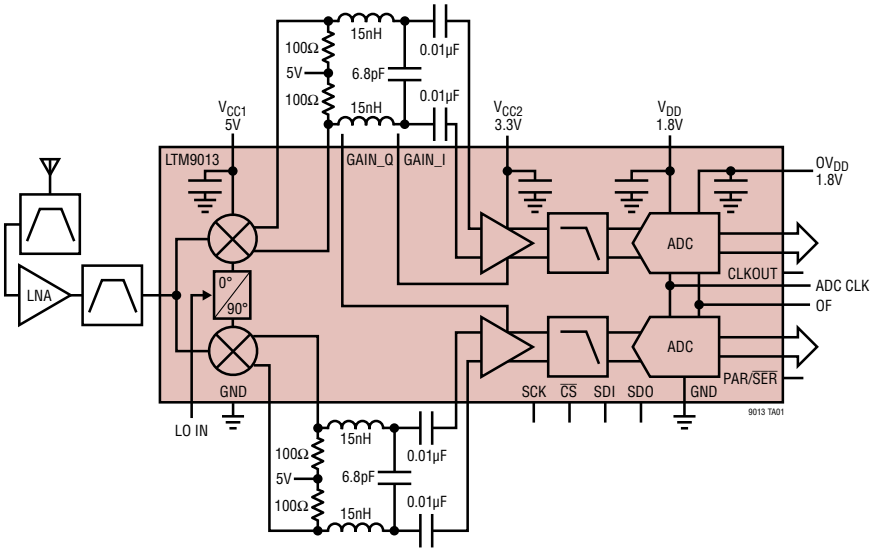
DESCRIPTION

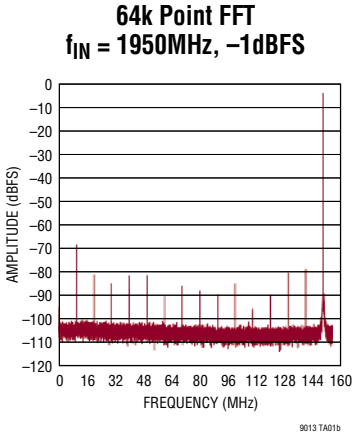
The LTM®9013 is a 300MHz wideband, low IF receiver. Utilizing an integrated system in a package (SiP) technology, it is a µModule® (micromodule) receiver that includes a dual high speed 14-bit A/D converter, lowpass filter, differential gain stages and a quadrature demodulator.

The LTM9013 is perfect for wideband I/Q receiver applications, with AC performance that includes 59dB SNR and 1.3dB frequency flatness from DC to 300MHz. A highpass filter or simple AC coupling are used external to the device for design flexiblity. The integrated on-chip broadband transformers provide a 50Ω single-ended interface at the RF input.

A 5V supply powers the demodulator and a 3.3V supply powers the IF amplifiers for minimal distortion. A 1.8V supply allows low power ADC operation. A separate output supply allows the DDR LVDS outputs to drive 1.8V logic. An optional multiplexer allows both channels to share a digital output bus. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

TYPICAL APPLICATION





ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage
- V_{CC1} ..... –0.3V to 5.5V
- V_{CC2} ..... –0.3V to 3.8V
- V_{DD}, OV_{DD} ..... –0.3V to 2.0V

Analog Input Voltage
- EN, EIP2, REF, IP2I, IP2Q ..... –0.3V to V_{CC1} + 0.3V
- PAR/$\overline{SER}$, SENSE ..... –0.3V to (V_{DD} + 0.2V)

Digital Input Voltage (Note 3)
- CLK^+, CLK^- ..... –0.3V to (V_{DD} + 0.3V)

Digital Input Voltage (Note 4)
- $\overline{CS}$, SDI, SCK ..... –0.3V to 3.9V

RF Input DC Voltage ..... ±0.1V

LO^+, LO^- Input DC Voltage ..... –0.3V to V_{CC1} + 0.3V

Analog Input Current
- +IN_I, –IN_I, +IN_Q, –IN_Q ..... ±20mA
- GAIN_I, GAIN_Q, $\overline{EN}$_I, $\overline{EN}$_Q, $\overline{SHDN}$_I, $\overline{SHDN}$_Q ..... ±10mA

LO^+, LO^- Input Power ..... +10dBm

RF Input Power ..... +20dBm

Analog Input Power, Continuous
- +IN_I, –IN_I, +IN_Q, –IN_Q ..... +15dBm

Analog Input Power, 100µs Pulse
- +IN_I, –IN_I, +IN_Q, –IN_Q ..... +20dBm

Analog Output Voltage
- +OUT_I, –OUT_I, +OUT_Q, –OUT_Q ..... 2.5V to V_{CC1} + 0.3V

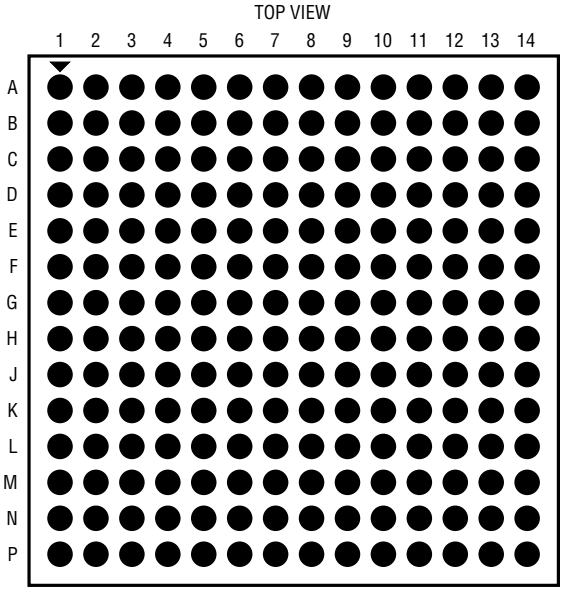
Digital Output Voltage
- SDO ..... –0.3V to 3.9V
- Except SDO ..... –0.3V to (OV_{DD} + 0.3V)

Operating Temperature Range
- LTM9013C ..... 0°C to 70°C
- LTM9013I ..... –40°C to 85°C

Storage Temperature Range ..... –55°C to 125°C

CAUTION: This part is sensitive to electrostatic discharge (ESD). It is very important that proper ESD precautions be observed when handling the RF and LO inputs of the LTM9013.

PIN CONFIGURATION



BGA PACKAGE
196-LEAD (15mm × 15mm × 2.82mm)

T_{JMAX} = 125°C, θ_{JA} = 20°C/W, $\theta_{JCbottom}$ = 6°C/W, θ_{JCtop} =19°C/W, θ_{JB} =9°C/W
θ VALUES DEFINED PER JESD 51-12
WEIGHT = 1.35g

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM9013CY-AA#PBF	LTM9013CY-AA#PBF	LTM9013Y-AA	196-Lead (15mm × 15mm × 2.8mm) BGA	0°C to 70°C
LTM9013IY-AA#PBF	LTM9013IY-AA#PBF	LTM9013Y-AA	196-Lead (15mm × 15mm × 2.8mm) BGA	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. P_{RF} = –5dBm, P_{LO} = 0dBm (Notes 5, 7) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	RF Input Frequency Range	No External Matching (Mid Band) with External Matching (Low Band, High Band)			1.5 to 2.7 0.7 to 4.0		GHz GHz
	LO Input Frequency Range	No External Matching (Mid Band) With External Matching (Low Band, High Band)			1.5 to 2.7 0.7 to 4.0		GHz GHz
	IF Frequency Range				0.5 to 300		MHz
	RF Input Return Loss	Z_O = 50Ω, 1.5GHz to 2.7GHz, Internally Matched			>10		dB
	LO Input Return Loss	Z_O = 50Ω, 1.5GHz to 2.7GHz, Internally Matched			>10		dB
	RF Input Power for –1dBFS	RF = 2140MHz, LO = 1990MHz (Figure 14)			–5		dBm
	LO Input Power				–6 to +6		dBm
	I/Q Gain Mismatch	RF = 2140MHz, LO = 1990MHz (Figure 14)			0.15		dB
	I/Q Phase Mismatch	RF = 2140MHz, LO = 1990MHz (Figure 14)			1		Deg
	LO to RF Leakage	LO = 1990MHz			–55		dBm
	RF to LO Isolation	RF = 2140MHz			58		dBm
	Gain Flatness (Notes 5, 6)	f_{IF} = 500kHz to 300MHz (Figure 14)			0.5		dB
	Lowpass Filter Cutoff Frequency	0.5dB Point			300		MHz
	Resolution (No Missing Codes)		●	14			Bits
	Integral Linearity Error (Note 8)	Differential Analog Input			±4.5		LSB
	Differential Linearity Error	Differential Analog Input		–1	±0.35	1	LSB
	Offset Error (Note 9)			–186	±62	186	LSB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. P_{RF} = –5dBm, P_{LO} = 0dBm (Notes 5, 7) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IIP3	Input 3rd Order Intercept, 1 Tone	RF = 2140MHz, LO = 1990MHz			30		dBm
IIP2	Input 2nd Order Intercept, 1 Tone	RF = 2140MHz, LO = 1990MHz			56		dBm
SNR	Signal-to-Noise Ratio at –1dBFS	RF = 2140MHz, LO = 1990MHz (Figure 14) f_{IF} = 150MHz (Note 6)	 ●	 59	59 62		dBFS dBFS
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	RF = 2140MHz, LO = 1990MHz (Figure 14) f_{IF} = 150MHz (Note 6)	 ●	 60	65 70		dB dB
	Spurious Free Dynamic Range 4th or Higher	RF = 2140MHz, LO = 1990MHz (Figure 14) f_{IF} = 150MHz (Note 6)			75 80		dB dB
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	RF = 2140MHz, LO = 1990MHz (Figure 14) f_{IF} = 150MHz (Note 6)	 ●	 58	58 61		dBFS dBFS
IMD3	Intermodulation Distortion at –7dBFS per Tone	RF = 2140MHz and 2141MHz, LO = 1990MHz (Figure 14)			66		dB

ANALOG INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 5, 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Demodulator Adjust Inputs (IP2I, IP2Q)							
	Input Voltage			0		1.3	V
	Input Impedance				2||1		kΩ||pF
	Settling Time	For Step Input; Output with 90% of Final Value			2		µs
Demodulator Adjust Input (REF)							
	Input Voltage			0.4	0.5	0.7	V
	Input Impedance				8||1		MΩ||pF
Amplifier Analog Inputs (+IN_I, –IN_I, +IN_Q, –IN_Q)							
	Differential Input Resistance	$V_{IN(DIFF)}$ = 100mV		49	57	65	Ω
	Input Common Mode Voltage				640		mV
	Minimum Input Frequency (3dB Corner)				500		kHz
Amplifier Gain Control Analog Inputs (GAIN_I, GAIN_Q)							
R_{IN}	Input Resistance	GAIN_I, GAIN_Q = 1.0V, $R_{IN} = 1V/\Delta I_{IL}$	 ●	7.8 7.2	9.2	10.6 12.8	kΩ kΩ
I_{IL}	Input Low Current	GAIN_I, GAIN_Q = 0V	 ●	–9 –10	–5	–1 –1	µA µA
	Gain Control Range	V_{GAIN} = 0.2V to 1.2V	●	27.5	29	30.5	dB
	Temperature Coefficient of Gain at Fixed Gain Control Voltage				–0.007		dB/°C
	Gain Control Slope	Gain Control Voltage = 0.2V to 1V, Slope of the Least-Square Fit Line	●	30.6	32.6	34.7	dB/V
	Average Conformance Error to Gain Slope Line	Gain Control Voltage = 0.2V to 1V, Standard Error to the Least-Square Fit Line			0.12		dB
	Maximum Conformance Error to Gain Slope Line	Gain Control Voltage = 0.2V to 1V, Maximum Error to the Least-Square Fit Line			0.2		dB

ANALOG INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 5, 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC Analog Inputs (SENSE)							
	Input Leakage Current	1.1V < SENSE < 1.2V		–1		1	µA
Demodulator Analog Outputs (+OUT_I, –OUT_I, +OUT_Q, –OUT_Q)							
	Common Mode Voltage				V_{CC1} – 1.5V		V
	Differential Output Impedance				50||6		Ω||pF

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 5, 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Demodulator Logic Inputs (EN, EIP2)							
V_{IH}	High Level Input Voltage	V_{CC} = 5V	●	2			V
V_{IL}	Low Level Input Voltage	V_{CC} = 5V	●			0.3	V
	Input Pull-Up Resistance	V_{CC} = 5V, V_{EN} = 4.4V to 2.6V			100		kΩ
	EIP2 Input Current	EIP2 = 5V			40		µA
	Turn-On Time				0.2		µs
	Turn-Off Time				0.8		µs
I and Q Channel Logic Inputs ($\overline{EN}$_I, $\overline{EN}$_Q, $\overline{SHDN}$_I, $\overline{SHDN}$_Q)							
V_{IH}	High Level Input Voltage	V_{CC} = 3.3V	●	2.2			V
V_{IL}	Low Level Input Voltage	V_{CC} = 3.3V	●			0.8	V
	Input Pull-Up Resistance	V_{CC} = 3.3V, V_{EN_I,EN_Q} = 0V to 0.5V			100		kΩ
	Input High Current	$\overline{EN}$_I, $\overline{EN}$_Q = 2.2V, $\overline{SHDN}$_I, $\overline{SHDN}$_Q = 2.2V		–30	–15	–1	µA
	Input Low Current	$\overline{EN}$_I, $\overline{EN}$_Q = 0.8V, $\overline{SHDN}$_I, $\overline{SHDN}$_Q = 0.8V		–60	–30	–1	µA
ADC Encode Clock Inputs (CLK^+, CLK^-)							
	Differential Input Voltage	V_{DD} = 1.8V	●	0.2			V
	Common Mode Input Voltage	Internally Set Externally Set	 ●	 1.1	1.2	 1.5	V V
	Input Resistance				10		kΩ
	Input Capacitance	(Note 10)			2		pF
ADC Logic Inputs (SDI, SCK, $\overline{CS}$)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.3			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
	Input Current	V_{IN} = 0V to 3.6V	●	–10		10	µA
	Input Capacitance	(Note 10)			3		pF
ADC Logic Inputs (PAR/$\overline{SER}$)							
	Input Leakage Current	0 < PAR/$\overline{SER}$ < V_{DD}		–1		1	µA
ADC Logic Output (SDO)							
	Logic Low Output Resistance to GND	V_{DD} = 1.8V, SDO = 0V			200		Ω
	Logic High Output Leakage Current	SDO = 0V to 3.6V	●	–10		10	µA
	Output Capacitance	(Note 10)			4		pF

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 5, 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Data Outputs (OV_{DD} = 1.8V)							
	Differential Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● ●	247 125	350 175	454 250	mV mV
	Common Mode Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● ●	1.125 1.125	1.250 1.250	1.375 1.375	V V
	On-Chip Termination Resistance	Termination Enabled, OV_{DD} = 1.8V			100		Ω

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 5, 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC1}	Demodulator and Amplifier Supply Voltage		●	4.75		5.25	V
V_{CC2}	Amplifier Analog Supply Voltage		●	2.7	3.3	3.6	V
V_{DD}	ADC Analog Supply Voltage		●	1.74	1.8	1.9	V
OV_{DD}	ADC Digital Output Supply Voltage		●	1.74	1.8	1.9	V
I_{CC1}	Demodulator and Amplifier Supply Current		●		285	330	mA
$I_{CC1(SHDN)}$	Demodulator and Amplifier Shutdown Current	$\overline{EN}$ = 0V, $\overline{EN}$_I, $\overline{EN}$_Q = 3.3V, $\overline{SHDN}$_I, $\overline{SHDN}$_Q = 0V	●		16	20	mA
I_{CC2}	Amplifier Supply Current		●		132	160	mA
I_{DD}	ADC Supply Current		●		335	385	mA
I_{OVDD}	Digital Supply Current	3.5mA Mode			80	90	mA
	ADC Sleep Power	ADC Programmed for Sleep Mode, No CLK			5		mW
	Total Power Dissipation				2.6		W

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 5, 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency		●	1		310	MHz
t_L	CLK Low Time	Duty Cycle Stabilizer Off (Note 10) Duty Cycle Stabilizer On (Note 10)	● ●	1.5 1.2	1.6 1.6	50 50	ns ns
t_H	CLK High Time	Duty Cycle Stabilizer Off (Note 10) Duty Cycle Stabilizer On (Note 10)	● ●	1.5 1.2	1.6 1.6	50 50	ns ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				0.15		ps_{RMS}
t_{AP}	Sample-and-Hold Acquisition Delay Time				1		ns
DATA Outputs (Note 10)							
t_D	CLK to DATA Delay	C_L = 5pF	●	1.7	2	2.3	ns
t_C	CLK to CLKOUT Delay	C_L = 5pF	●	1.3	1.6	2	ns
t_{SKEW}	DATA to CLKOUT Skew	$t_D - t_C$	●	0.3	0.4	0.55	ns

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 5, 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SPI Port Timing (Note 10)							
t_{SCK}	SCK Period	Write Mode Readback Mode C_{SDO} = 20pF, R_{PULLUP} = 2kΩ	● ●	40 250			ns ns
t_S	$\overline{CS}$ to SCK Set-up Time			5			ns
t_H	SCK to $\overline{CS}$ Hold Time			5			ns
t_{DS}	SDI Set-Up Time			5			ns
t_{DH}	SDI Hold Time			5			ns
t_{DO}	SCK Falling to SDO Valid	Readback Mode C_{SDO} = 20pF, R_{PULLUP} = 2kΩ				125	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below GND they will be clamped by internal diodes. When these pin voltages are taken above V_{DD}, they will not be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND without latchup.

Note 5: Using test circuit 1 (see Figure 14 Design Example in Applications Information section).

Note 6: Signal applied to the ±IN*n* pins and measures only the amplifier and ADC.

Note 7: V_{CC1} = 5V, V_{CC2} = 3.3V, V_{DD} = 1.8V, EN = 5V, $\overline{EN}$_I, $\overline{EN}$_Q = 0V, GAIN_I, GAIN_Q = 1.2V, $\overline{SHDN}$_I, $\overline{SHDN}$_Q = 3.3V, SENSE = 1.15V, f_S = 310MHz, unless otherwise noted.

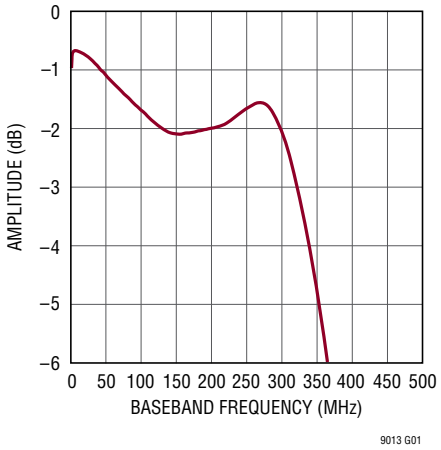
Note 8: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 9: DC offset is the ADC output code with no RF or LO input signal applied the module.

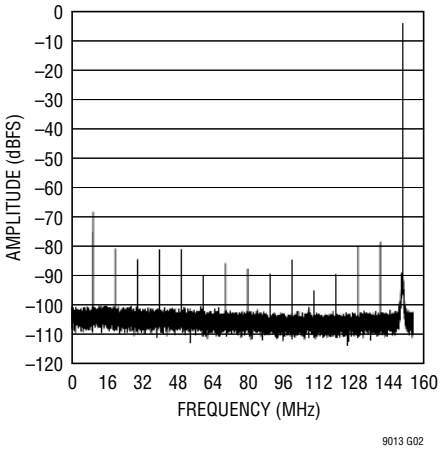
Note 10: Guaranteed by design, not subject to test

TYPICAL PERFORMANCE CHARACTERISTICS

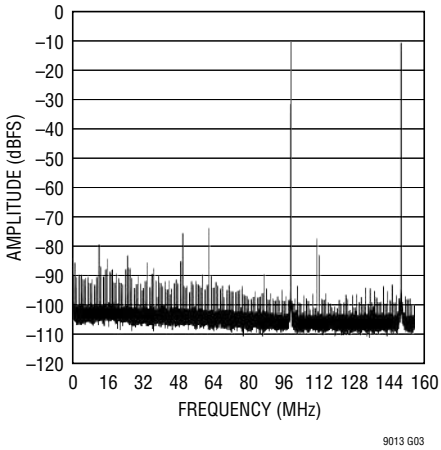
Baseband Frequency Response



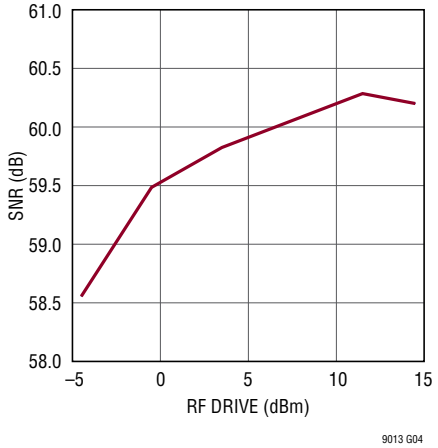
64k Point FFT, f_{IN} = 1950MHz, –1dBFS



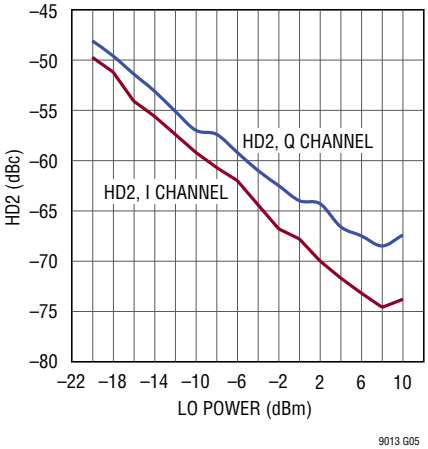
64K Point FFT, f_{IN} = 1925MHz, 1975MHz, –7dBFS per Tone



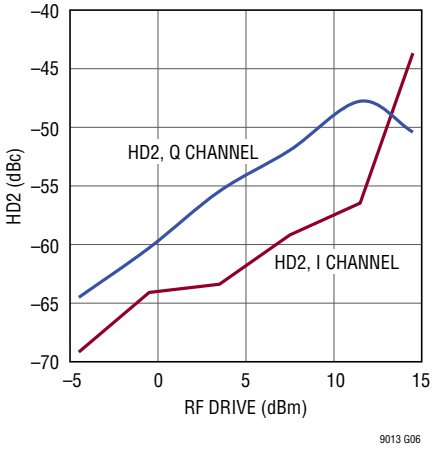
SNR at 150MHz IF vs RF Drive



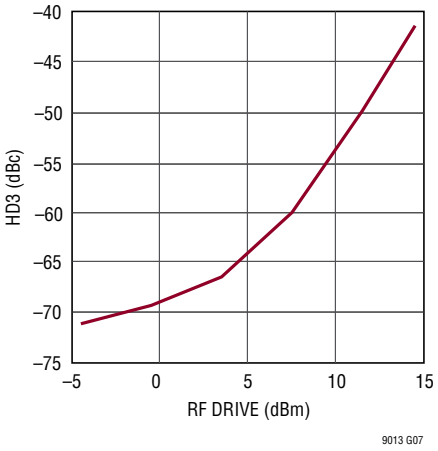
HD2 at 150MHz IF vs LO Power



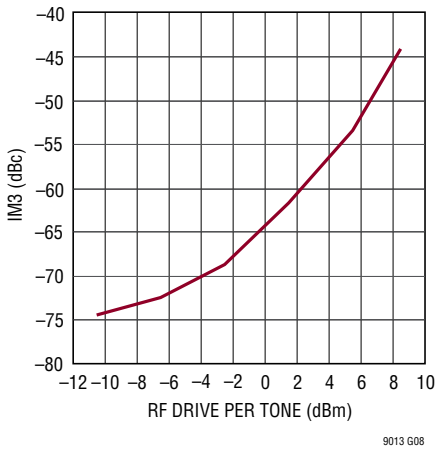
HD2 at 150MHz IF vs RF Drive



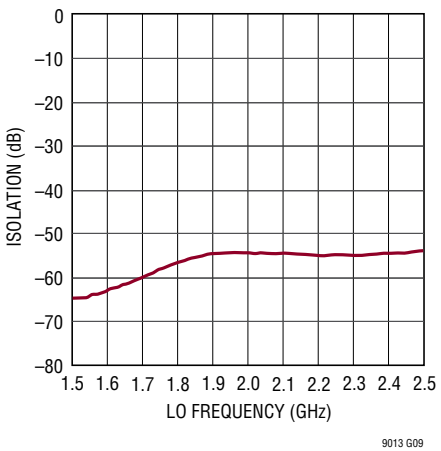
HD3 at 150MHz IF vs RF Drive



IM3 at 150MHz vs RF Drive



LO to RF Isolation



PIN FUNCTIONS

Supply Pins

V_{CC1} (Pin B7): Analog 5V Supply for Demodulator and Amplifiers. The specified operating range is 4.75V to 5.25V. The voltage on this pin provides power for the demodulator and amplifier stages only and is internally bypassed to GND.

V_{CC2} (Pins A2, A3, A12, A13, D1, D12): Analog 3.3V Supply for Amplifiers. The specified operating range is 2.7V to 3.6V. V_{CC2} is internally bypassed to GND.

V_{DD} (Pins J6, J9): Analog 1.8V Supply for ADC. The specified operating range is 1.74V to 1.9V. V_{DD} is internally bypassed to GND.

OV_{DD} (Pins N5, N10): Positive 1.8V Supply for the Digital Output Drivers. The specified operating range is 1.74V to 1.9V. OV_{DD} is internally bypassed to GND.

GND: Analog Ground. See Pin Configuration table for pin locations.

Analog Inputs

RF (Pin A10): RF Input Pin. This is a single-ended 50Ω terminated input. No external matching network is required for the 1.5GHz to 2.7GHz band. An external series inductor (and/or shunt capacitor) may be required for impedance transformation to 50Ω in the band from 700MHz to 1.5GHz, or for the band from 2.7GHz to 4GHz (see Figure 2). If the RF source is not DC blocked, a series blocking capacitor should be used. Otherwise, damage to the IC may result.

LO^+, LO^- (Pins A6, A5): Local Oscillator Input Pins. This is a differential 50Ω terminated input. An external series inductor (and/or shunt capacitor) may be required for impedance transformation to 50Ω in the band from 700MHz to 1.5GHz, or for the band from 2.7GHz to 4GHz (see Figure 4). If the LO source is not DC blocked, a series blocking capacitor must be used. Otherwise, damage to the IC may result.

+IN_I, –IN_I (Pins E10, E11): Channel I Signal Input. This is a differential input that drives the amplifier. It has an internally generated DC bias. Series blocking capacitors are required between these pins and +OUT_I, –OUT_I.

+IN_Q, –IN_Q (Pins E4, E5): Channel Q Signal Input. This is a differential input that drives the Amplifier. It has an internally generated DC bias. Series blocking capacitors are required between these pins and +OUT_Q, –OUT_Q.

GAIN_I (Pin C12): I Channel Gain Control Input. This is an input that controls the gain of the amplifier. This pin is internally pulled low with 10kΩ to GND. The gain control slope is approximately 32dB/V with a gain control range of 0.1V to 1.1V.

GAIN_Q (Pin C1): Q Channel Gain Control Input. This is an input that controls the gain of the amplifier. This pin is internally pulled low with 10kΩ to GND. The gain control slope is approximately 32dB/V with a gain control range of 0.1V to 1.1V.

CLK^+, CLK^- (Pins J5, K5): ADC Clock Input. Conversion starts on the rising edge of CLK^+.

IP2_I (Pin C10): IP2 Adjustment Pin for I Channel.

IP2_Q (Pin D10): IP2 Adjustment Pin for Q Channel.

REF (Pin D8): Voltage Reference Input for Analog Control Voltage Pins.

SENSE (Pin J8): ADC Reference Programming Pin. Connecting SENSE to V_{DD} selects the internal reference and a 1.32V input range.

Analog Outputs

+OUT_I, –OUT_I (Pins F10, F11): Channel I Signal Output. This is a differential output from the demodulator. The DC bias point is V_{CC1} – 1.5V for each pin. These pins must have an external 100Ω or inductor pull-up to V_{CC1}. Series blocking capacitors are required between these pins and +IN_I, –IN_I.

+OUT_Q, –OUT_Q (Pins F4, F5): Channel Q Signal Output. This is a differential output from the demodulator. The DC bias point is V_{CC1} – 1.5V for each pin. These pins must have an external 100Ω or inductor pull-up to V_{CC1}. Series blocking capacitors are required between these pins and +IN_Q, –IN_Q.

PIN FUNCTIONS

Control Pins

EN (Pin B8): Demodulator Enable Pin. If EN = high (the input voltage is higher than 2.0V), the demodulator is enabled. If EN = low (the input voltage is less than 1.0V), it is disabled. If the enable function is not needed, then this pin should be tied to V_{CC1}.

EIP2 (Pin D6): Demodulator IP2 Adjust Enable Pin. Pin is internally pulled low with 200kΩ to GND. If EIP2 = high (the input voltage is higher than 2.0V), the IP2 adjust circuit is enabled. If EIP2 = low (the input voltage is less than 1.0V), it is disabled.

NC1, NC2, NC3 (Pins C6, C9, D9): Do Not Connect.

$\overline{EN}$_I (Pin C14): First Amplifier I Channel Enable Pin. Pin is internally pulled high with 100kΩ to V_{CC2}. Assert pin to a low voltage to enable the amplifier. Connect pin to GND if enable function is not used.

$\overline{EN}$_Q (Pin C3): First Amplifier Q Channel Enable Pin. Pin is internally pulled high with 100kΩ to V_{CC2}. Assert pin to a low voltage to enable the amplifier. Connect pin to GND if enable function is not used.

$\overline{SHDN}$_I (Pin D14): Amplifier I Channel Shutdown Pin. Pin is internally pulled high with 100kΩ to V_{CC2}. Assert pin to a low voltage to shut down the amplifier. Proper sequencing of the $\overline{EN}$_I and $\overline{SHDN}$_I pins is required to avoid non-monotonic output signal behavior. Connect pin to V_{CC2} if shutdown function is not used.

$\overline{SHDN}$_Q (Pin D3): Amplifier Q Channel Shutdown Pin. Pin is internally pulled high with 100kΩ to V_{CC2}. Assert pin to a low voltage to shut down the amplifier. Proper sequencing of the EN_Q and $\overline{SHDN}$_Q pins is required to avoid non-monotonic output signal behavior. Connect pin to V_{CC2} if shutdown function is not used.

SDI (Pin K11): Serial Interface Data Input. In serial programming mode, (PAR/$\overline{SER}$ = GND), SDI is the serial interface data input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDI selects 3.5mA or a 7.5mA LVDS output current (see Table 4). SDI can be driven with 1.8V to 3.3V logic.

SCK (Pin J11): Serial Interface Clock Input. In serial programming mode (PAR/$\overline{SER}$ = GND), SCK is the serial interface clock input. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SCK can be used to place the part in the low power sleep mode (see Table 4). SCK can be driven with 1.8V to 3.3V logic.

$\overline{CS}$ (Pin K10): Serial Interface Chip Select Input. In serial programming mode (PAR/$\overline{SER}$ = GND), $\overline{CS}$ is the serial interface chip select input. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), $\overline{CS}$ controls the clock duty stabilizer (see Table 4). $\overline{CS}$ can be driven with 1.8V to 3.3V logic.

PAR/$\overline{SER}$ (Pin J10): Programming Mode Selection Pin. Connect to GND to enable the serial programming mode where $\overline{CS}$, SCK, SDI, SDO become a serial interface that controls the ADC operating modes. Connect to V_{DD} to enable the parallel programming mode where $\overline{CS}$, SCK, SDI, SDO become parallel logic inputs that control a reduced set of the ADC operating modes. PAR/$\overline{SER}$ should be connected directly to GND or V_{DD} and not be driven by a logic signal.

Digital Outputs

SDO (Pin L11): Serial Interface Data Output. In serial programming mode (PAR/$\overline{SER}$ = GND), SDO is the optional serial inter-face data output. Data on SDO is read back from the mode control registers and can be latched on the falling edge of SCK. SDO is an open-drain N-channel MOSFET output that requires an external 2kΩ pull-up resistor from 1.8V to 3.3V. If readback from the mode control registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected.

LVDS Digital Outputs

The following pins are differential LVDS outputs. The output current level is programmable. There is an optional internal 100Ω termination resistor between the pins of each LVDS output pair.

PIN FUNCTIONS

CLKOUT$^+$, CLKOUT$^-$ (Pins P8, P7): ADC Data Output Clock.

DB0_1$^-$/DB0_1$^+$ to DB12_13$^-$/DB12_13$^+$ (See Pin Configuration table for pin locations): Q Channel ADC Double Data Rate Digital Outputs. Two data bits are multiplexed onto each differential output pair. The even data bits (DB0, DB2, DB4, DB6, DB8, DB10, DB12) appear when CLKOUT$^+$ is low. The odd data bits (DB1, DB3, DB5, DB7, DB9, DB11, DB13) appear when CLKOUT$^+$ is high.

DA0_1$^-$/DA0_1$^+$ to DA12_13$^-$/DA12_13$^+$ (See Pin Configuration table for pin locations): Q Channel ADC Double Data Rate Digital Outputs. Two data bits are multiplexed onto each differential output pair. The even data bits (DA0, DA2, DA4, DA6, DA8, DA10, DA12) appear when CLKOUT$^+$ is low. The odd data bits (DA1, DA3, DA5, DA7, DA9, DA11, DA13) appear when CLKOUT$^+$ is high.

OF$^+$, OF$^-$ (Pins K2, K1): Overflow/Underflow Outputs. OF$^+$ is high when an overflow/underflow has occurred.

Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	GND	V_{CC2}	V_{CC2}	GND	LO^-	LO^+	GND	GND	GND	RF	GND	V_{CC2}	V_{CC2}	GND
B	GND	GND	GND	GND	GND	GND	V_{CC1}	EN	GND	GND	GND	GND	GND	GND
C	GAIN_Q	GND	$\overline{EN}$_Q	GND	GND	NC1	GND	GND	NC2	IP2_I	GND	GAIN_I	GND	$\overline{EN}$_I
D	V_{CC2}	GND	$\overline{SHDN}$_Q	GND	GND	EIP2	GND	REF	NC3	IP2_Q	GND	V_{CC2}	GND	$\overline{SHDN}$_I
E	GND	GND	GND	+IN_Q	–IN_Q	GND	GND	GND	GND	+IN_I	–IN_I	GND	GND	GND
F	GND	GND	GND	+OUT_Q	–OUT_Q	GND	GND	GND	GND	+OUT_I	–OUT_I	GND	GND	GND
G	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
H	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
J	GND	GND	GND	GND	CLK^+	V_{DD}	GND	SENSE	V_{DD}	PAR/$\overline{SER}$	SCK	GND	GND	GND
K	OF^-	OF^+	GND	GND	CLK^-	GND	GND	GND	GND	$\overline{CS}$	SDI	GND	GND	GND
L	$DB01^-$	DB01+	GND	GND	GND	GND	GND	GND	GND	GND	SDO	GND	$DA1213^-$	$DA1213^+$
M	$DB23^-$	$DB23^+$	$DB45^-$	$DB45^+$	GND	GND	GND	GND	GND	GND	$DA89^-$	$DA89^+$	$DA1011^-$	$DA1011^+$
N	$DB67^-$	$DB67^+$	$DB89^-$	$DB89^+$	OV_{DD}	GND	GND	GND	GND	OV_{DD}	$DA45^-$	$DA45^+$	$DA67^-$	$DA67^+$
P	GND	$DB1213^+$	$DB1213^-$	$DB1011^+$	$DB1011^-$	GND	$CLKOUT^-$	$CLKOUT^+$	GND	$DA23^+$	$DA23^-$	$DA01^+$	$DA01^-$	GND

Top View of BGA Package (Looking Through Component)

BLOCK DIAGRAM

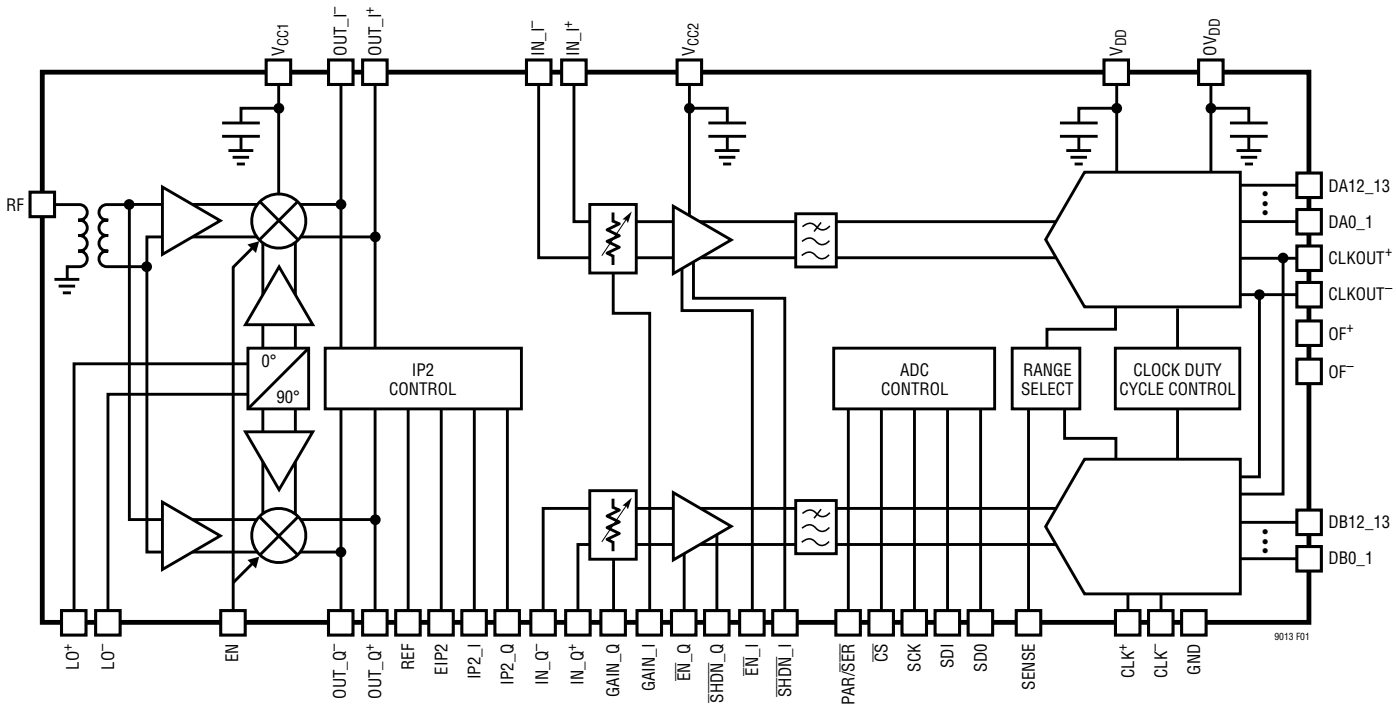
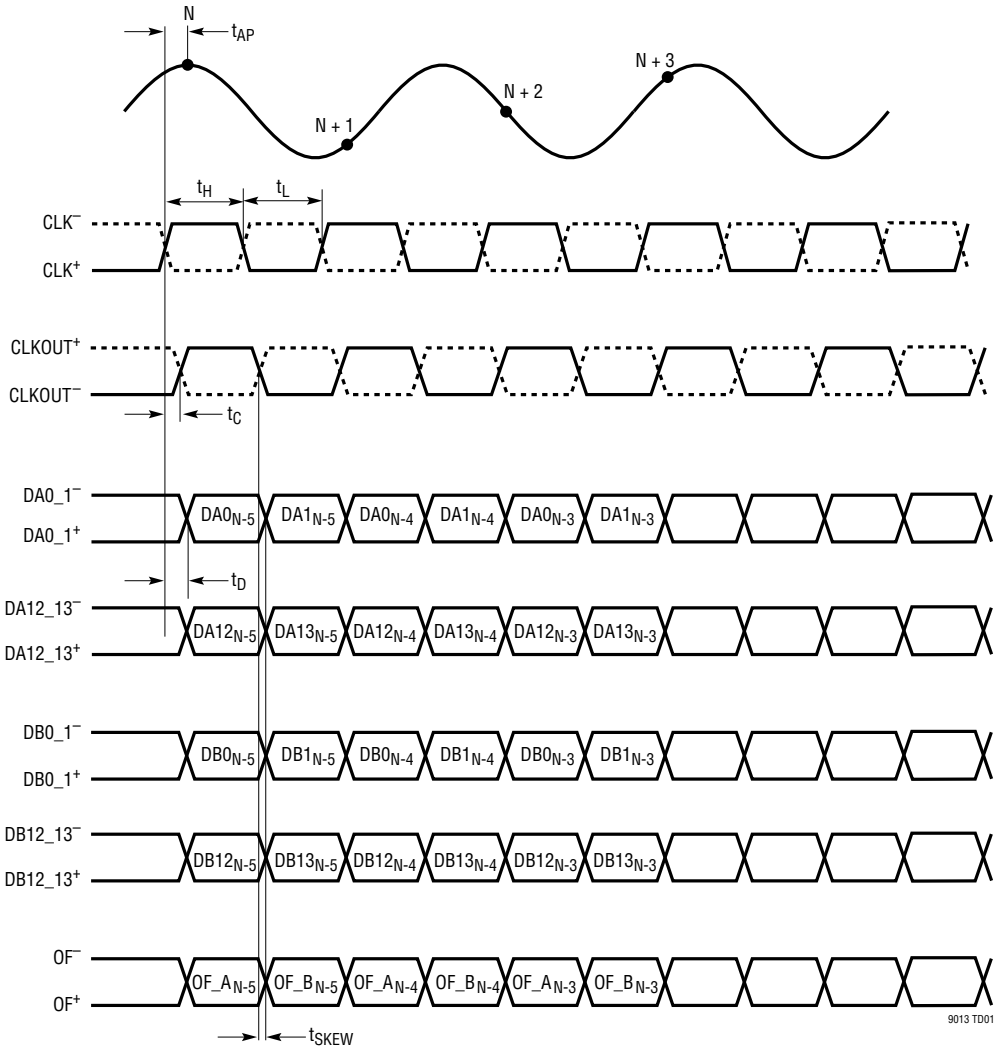


Figure 1. Functional Block Diagram

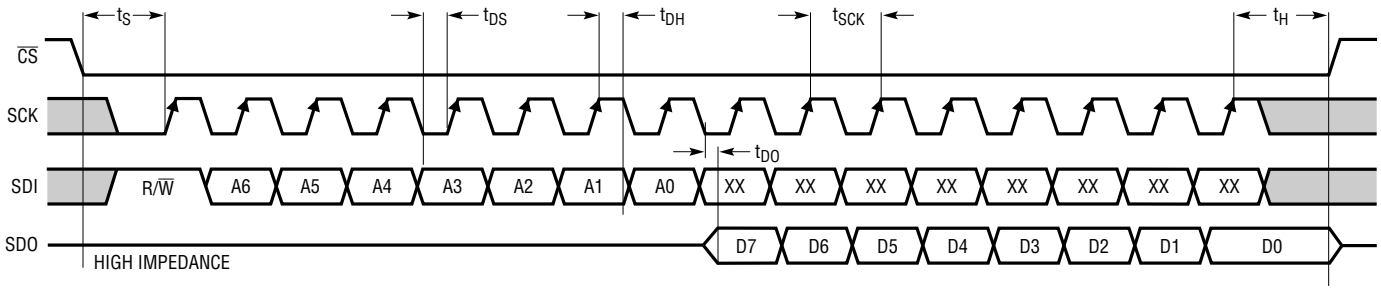
TIMING DIAGRAMS

Double-Data Rate Output Timing, All Data Are Differential LVDS

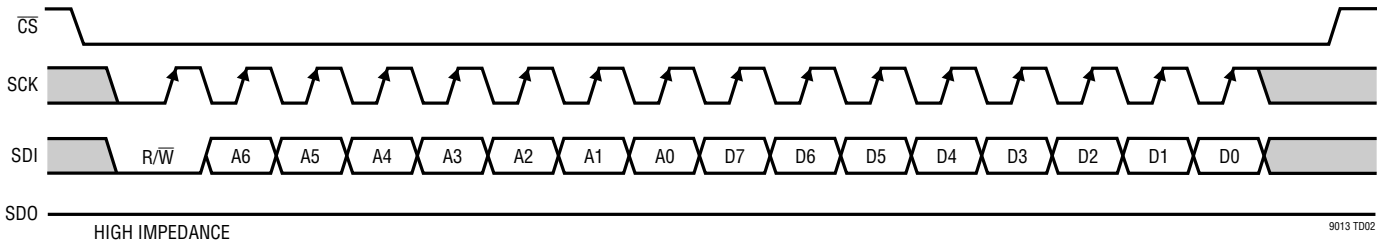


TIMING DIAGRAMS

SPI Port Timing (Readback Mode)



SPI Port Timing (Write Mode)



OPERATION

Description

The LTM9013 is a low IF receiver targeting wideband I/Q receiver and digital predistortion applications, such as wireless infrastructure with RF input frequencies up to 4GHz. It is an integrated µModule receiver utilizing system in a package (SiP) technology to combine a dual, high speed 14-bit A/D converter, 300MHz lowpass filters, one low noise, differential amplifier per channel with adjustable gain and an I/Q demodulator with IP2 adjustment.

The following sections describe in further detail the operation of each section.

Demodulator Operation

The RF signal is applied to the inputs of the RF transconductance amplifiers and is then demodulated into I/Q baseband signals using quadrature LO signals which are internally generated from an external LO source by precision 90° phase shifters.

Broadband transformers are integrated at the RF input to enable a single-ended RF interface. In the mid frequency band (1.5GHz to 2.7GHz), both RF and LO ports are internally matched to 50Ω. No external matching components are needed. For the low (700MHz to 1.5GHz), and high (2.7GHz to 4GHz) frequency bands a simple network with series inductors and/or shunt capacitors can be used as the impedance matching network.

Amplifier Operation

Each channel of the LTM9013 consists of a single stage of AC-coupled, low noise and low distortion fully differential op amp/ADC driver. Each stage is followed by a 4-pole lowpass filter using a high speed, high performance operational amplifier and precision passive components. The stage is designed to provide maximum gain and phase flatness.

The LTM9013 variable gain amplifier employs an interpolated, tapped attenuator circuit architecture to generate the variable-gain characteristic. The tapped attenuator is fed to a buffer and output amplifier to complete the differential signal path. This circuit architecture provides good RF input power handling capability along with a constant output noise and output IP3 characteristic that are desirable for most IF signal chain applications. The internal control circuitry takes the gain control signal from the GAIN terminals and converts this to an appropriate set of control signals to the attenuator ladder. The attenuator control circuit ensures that the linear-in-dB gain response is continuous and monotonic over the gain range for both slow and fast moving input control signals while exhibiting very little input impedance variation over gain. These design considerations result in a gain-vs-V_G characteristic with a ±0.1dB ripple and a 0.5µs gain response time that is slower than a similar digital step attenuator design.

An often overlooked characteristic of an analog-controlled VGA is upconverted amplitude modulation (AM) noise from the gain control terminals. The VGA behaves as a 2-quadrant multiplier, so some minimal care is required to avoid excessive AM sideband noise generation. The following table demonstrates the effect of the baseline 20nV/$\sqrt{\text{Hz}}$ equivalent input control noise from the LTM9013 circuit along with the effect of a higher combined input noise due to a noisy external control circuit.

CONTROL INPUT TOTAL NOISE VOLTAGE (nV/$\sqrt{\text{Hz}}$)	PEAK AM NOISE AT 10kHz OFFSET NEAR MAXIMUM GAIN (dBc/Hz)
20	–142
40	–136
70	–131
100	–128
200	–122

OPERATION

The baseline equivalent 20nV/√Hz input noise is seen to produce worst-case AM sidebands of –142dBc/Hz which is near the –147dBm/Hz output noise floor at maximum gain for a nominal 0dBm output signal. An input control noise voltage less than 80nV/√Hz is generally recommended to avoid measurable AM sideband noise. While op amp control circuit output noise voltage is usually below 80nV/√Hz, some low power DAC outputs exceed 150nV/√Hz. DACs with output noise in the range of 100nV/√Hz to 150nV/√Hz can usually be accommodated with a suitable 2:1 or 3:1 resistor divider network on the DAC output to suppress the noise amplitude by the same ratio. Noisy DACs in excess of 150nV/√Hz should be avoided if minimal AM noise is important in the application.

ADC Input Network

The passive network between the amplifier output and the ADC input stages provides a 0.1dB ripple, 4th order Chebyshev lowpass filter response.

Converter Operation

The LTM9013 includes a 2-channel, 14-bit 310Msps A/D converter powered by a single 1.8V supply. A sampled input will result in a digitized value six cycles later. The analog inputs are driven differentially by the VGA. The encode inputs should be driven differentially for optimal performance. The digital outputs are double data rate LVDS. Additional features can be chosen by programming the mode control registers through a serial SPI port.

APPLICATIONS INFORMATION

RF Input

Figure 2 shows the mixer's RF input which consists of an integrated transformer and high linearity transconductance amplifiers. The primary side of the transformer is connected to the RF input pin. The secondary side of the transformer is connected to the differential inputs of the transconductance amplifiers. Under no circumstances should an external DC voltage be applied to the RF input pin. DC current flowing into the primary side of the transformer may cause damage to the integrated transformer. A series blocking capacitor should be used to AC-couple the RF input port to the RF signal source.

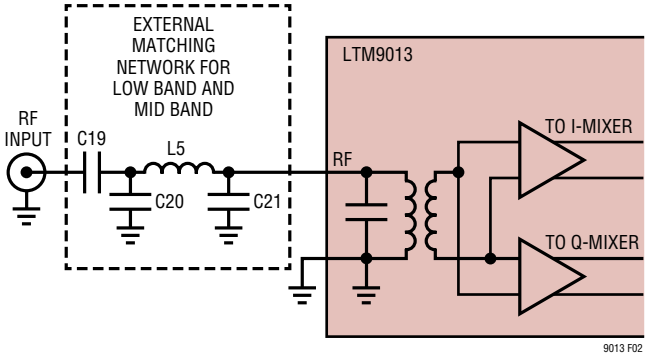


Figure 2. RF Input Interface

The RF input port is internally matched over a wide frequency range from 1.5GHz to 2.7GHz with input return loss typically better than 10dB. No external matching network is needed for this frequency range. When the part is operated at lower frequencies, however, the input return loss can be improved with the matching network shown in Figure 2. Shunt capacitors C20, C21 and series inductor L5 can be selected for optimum input impedance matching at the desired frequency as illustrated in Figure 3. C19 serves as a series DC blocking capacitor.

The RF input impedance and S11 parameters (without external matching components) are listed in Table 1.

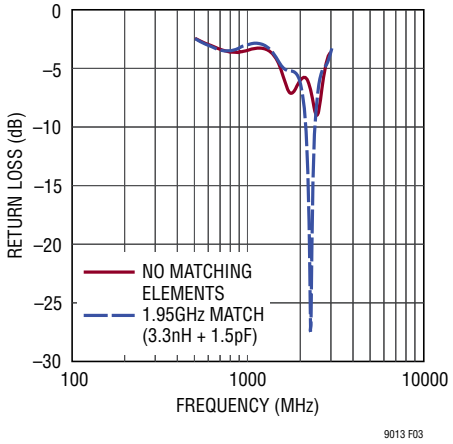


Figure 3. RF Input Return Loss with External Matching

Table 1. RF Input Impedance

FREQUENCY	MAGNITUDE	PHASE	R	X
500MHz	0.96	41.2	92.3Ω	–95.4Ω
600MHz	0.93	50.6	85.3Ω	–62.0Ω
700MHz	0.90	61.3	76.0Ω	–36.0Ω
800MHz	0.81	71.3	66.9Ω	–17.6Ω
900MHz	0.70	90.7	49.4Ω	0.4Ω
1000MHz	0.74	109.6	34.8Ω	8.5Ω
1100MHz	0.78	122.1	25.9Ω	11.2Ω
1200MHz	0.82	130.2	20.4Ω	12.1Ω
1300MHz	0.81	136.9	16.8Ω	11.6Ω
1400MHz	0.83	143.6	13.2Ω	10.9Ω
1500MHz	0.83	149.0	11.0Ω	9.7Ω
1600MHz	0.83	157.2	7.9Ω	7.7Ω
1700MHz	0.84	165.3	5.8Ω	5.2Ω
1800MHz	0.83	175.9	4.7Ω	1.5Ω
1900MHz	0.84	–173.1	4.8Ω	–2.5Ω
2000MHz	0.81	–161.6	7.3Ω	–6.2Ω
2100MHz	0.81	–150.2	10.9Ω	–9.2Ω
2200MHz	0.78	–141.5	15.2Ω	–10.5Ω
2300MHz	0.75	–132.7	20.2Ω	–10.9Ω
2400MHz	0.73	–129.9	22.2Ω	–10.6Ω
2500MHz	0.68	–126.8	24.9Ω	–9.7Ω
2600MHz	0.66	–128.6	24.3Ω	–9.4Ω
2700MHz	0.63	–129.1	24.8Ω	–8.8Ω
2800MHz	0.62	–126.9	26.0Ω	–8.6Ω
2900MHz	0.61	–124.9	27.2Ω	–8.5Ω
3000MHz	0.59	–117.7	31.5Ω	–7.6Ω

APPLICATIONS INFORMATION

LO Input Port

The mixer's LO input interface is shown in Figure 4. The input consists of a precision quadrature phase shifter which generates 0° and 90° phase-shifted LO signals for the LO buffer amplifiers driving the I/Q mixers. Under no circumstances should an external DC voltage be applied to the input pin. DC current flowing into the primary side of the transformer may damage the transformer.

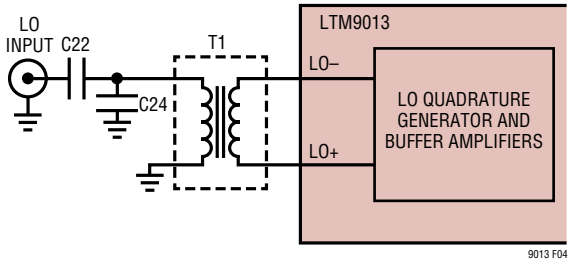


Figure 4. LO Input Interface

The LO input port is internally matched over a wide frequency range from 1.5GHz to 2.7GHz with input return loss typically better than 10dB. No external matching network is needed for this frequency range. The LO input impedance and S11 parameters (without external matching components) are listed in Table 2. Outside this frequency range, the impedance match can be improved using series capacitor C22 and shunt capacitor C24.

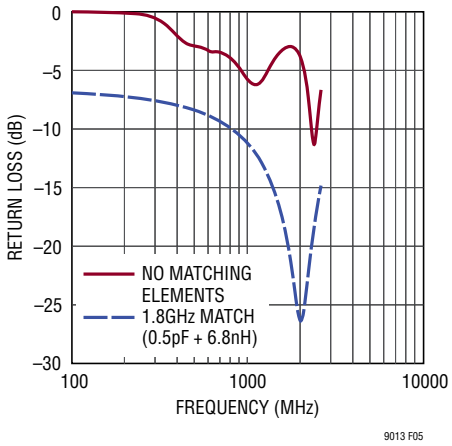


Figure 5. LO Input Return Loss with External Matching

Table 2. LO Input Impedance

FREQUENCY	MAGNITUDE	PHASE	R	X
500MHz	0.71	–70.3	67.7Ω	15.5Ω
600MHz	0.66	–83.9	55.0Ω	3.6Ω
700MHz	0.66	–97.1	44.5Ω	–3.3Ω
800MHz	0.62	–119.8	29.8Ω	–8.3Ω
900MHz	0.55	–144.9	20.2Ω	–6.5Ω
1000MHz	0.51	–177.8	16.1Ω	–0.4Ω
1100MHz	0.48	146.5	22.2Ω	5.3Ω
1200MHz	0.52	115.0	34.3Ω	6.1Ω
1300MHz	0.57	87.9	51.6Ω	–0.9Ω
1400MHz	0.62	70.5	66.9Ω	–12.4Ω
1500MHz	0.66	55.0	84.7Ω	–30.5Ω
1600MHz	0.67	44.0	101.4Ω	–46.6Ω
1700MHz	0.69	34.1	123.7Ω	–67.4Ω
1800MHz	0.67	24.3	154.8Ω	–75.6Ω
1900MHz	0.66	15.5	193.5Ω	–70.8Ω
2000MHz	0.61	2.5	206.9Ω	–10.8Ω
2100MHz	0.55	–10.2	163.1Ω	24.2Ω
2200MHz	0.46	–34.3	101.7Ω	21.3Ω
2300MHz	0.34	–63.8	65.5Ω	5.5Ω
2400MHz	0.30	–113.3	40.0Ω	–2.5Ω
2500MHz	0.33	–164.3	25.8Ω	–1.6Ω
2600MHz	0.42	164.8	21.4Ω	2.2Ω
2700MHz	0.51	140.5	23.1Ω	6.3Ω
2800MHz	0.53	120.3	31.4Ω	6.7Ω
2900MHz	0.52	101.7	42.2Ω	3.6Ω
3000MHz	0.33	98.1	45.9Ω	1.3Ω

APPLICATIONS INFORMATION

IM2 Adjustment Circuitry

The LTM9013 also contains circuitry for the independent adjustment of IM2 levels on the I and Q channels. When the EIP2 pin is a logic high, this circuitry is enabled and the IP2I and IP2Q analog control voltage inputs are able to adjust the IM2 level. The IM2 level can be effectively minimized over a large range of the baseband bandwidth. The circuitry has an effective baseband frequency upper limit of about 200MHz. Any IM2 component that falls in this frequency range can be minimized.

Variable Gain Amplifier

The LTM9013 includes a high linearity, fully-differential analog-controlled variable-gain amplifier (VGA) optimized for application frequencies in the range of 1MHz to 500MHz. The VGA architecture provides a constant OIP3 and constant output noise level (NF + Gain) over the 31dB gain-control range and thus exhibits a uniform spurious-free dynamic range (SFDR) over gain. This constant SFDR characteristic is ideal for use in receiver IF chains.

Gain Characteristics

The LTM9013 provides a continuously adjustable gain of 31dB that is linear-in-dB with respect to the control voltages applied to GAIN_I and GAIN_Q. In this way, a positive gain-control slope is easily achieved:

Apply gain control voltage to the GAIN_I/GAIN_Q pins. Gain increases with increasing GAIN_I/GAIN_Q voltage.

When connected in this typical single-ended configuration, the active control input range extends from 0.1V to 1.1V. This control input range can be extended using a resistor divider with a suitably low output resistance. For example, two series resistors of 1k each would extend the control input range from 0.2V to 2.2V while providing an effective 500Ω Thevinin equivalent source resistance, a relatively small loading effect compared to the 10k input resistance of the GAIN_I/GAIN_Q terminals.

IF Input Port Characteristics

The amplifier inputs provide a nominal 50Ω differential input impedance over the operating frequency range.

The input impedance characteristic derives from the differential attenuator ladder. The internal circuit controls the IF connections to this attenuator ladder and generates the appropriate common mode DC voltage.

Enable/Shutdown

Both the $\overline{EN}$ and $\overline{SHDN}$ pins are self-biased to V_{CC2} through their respective 100k pull-up resistors, so the default open-pin state is powered on with the output amplifier signal path disabled. Pulling the $\overline{EN}$ pin low completes the signal path from the attenuator ladder through the output amplifier. The $\overline{EN}$ pin essentially provides a fast muting function while the $\overline{SHDN}$ pin provides slower power on/off function.

For applications requiring the $\overline{SHDN}$ function, it is recommended that the output amplifier signal path be disabled with a high $\overline{EN}$ voltage before transitioning the $\overline{SHDN}$ signal. When enabling the amplifier, allow at least 5ms dwell time between the rising $\overline{SHDN}$ transition and the falling $\overline{EN}$ transition to avoid non-monotonic output signal behavior though the VGA. The opposite delay sequence is recommended for the falling $\overline{SHDN}$ transition, but this is less critical as the output signal amplitude will drop abruptly regardless of the $\overline{EN}$ pin.

Figure 6

APPLICATIONS INFORMATION

ESD

The amplifier inputs are protected with reverse-biased ESD diodes on all pins. If any pin is forced one diode drop above the positive supply or one diode drop below the negative supply, then large currents may flow through the diodes. No damage to the devices will occur if the current is kept below 10mA.

Reference

The LTM9013 has an internal 1.25V voltage reference for the ADC. For a 1.32V input range with internal reference, connect SENSE to V_{DD}. For a 1.32V input range with an external reference, apply a 1.25V reference voltage to SENSE (Figure 7). Apply a 1.15V reference voltage to SENSE to achieve specified performance.

Encode Input

The signal quality of the encode inputs strongly affects the A/D noise performance. The encode inputs should be treated as analog signals—do not route them next to digital traces on the circuit board.

The encode inputs are internally biased to 1.2V through 10k equivalent resistance (Figure 8). If the common mode of the driver is within 1.1V to 1.5V, it is possible to drive the encode inputs directly. Otherwise a transformer or coupling capacitors are needed (Figures 9 and 10). The maximum (peak) voltage of the input signal should never exceed V_{DD} + 0.1V or go below –0.1V.

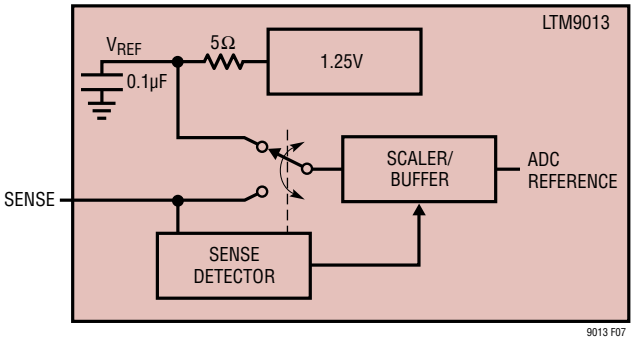


Figure 7. Reference Circuit

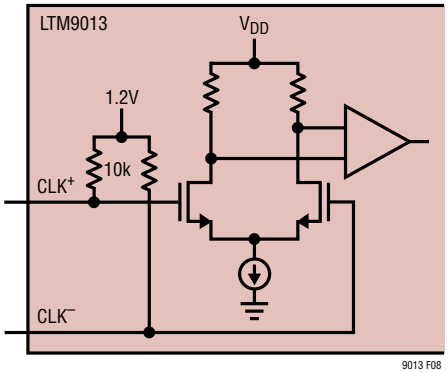


Figure 8. Equivalent Encode Input Circuit

APPLICATIONS INFORMATION

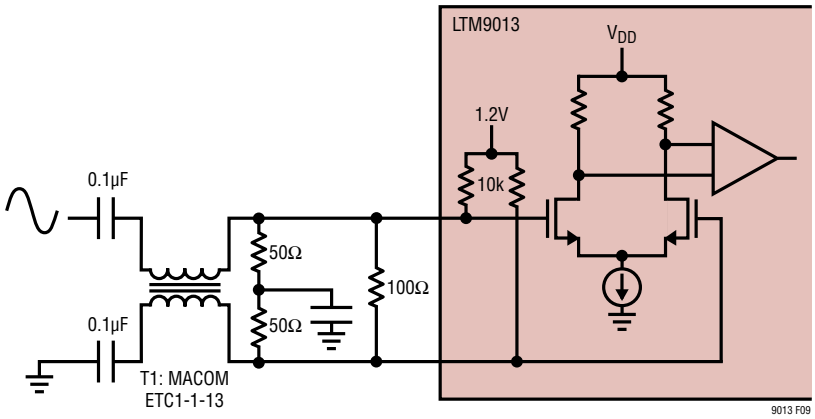


Figure 9. Sinusoidal Encode Circuit

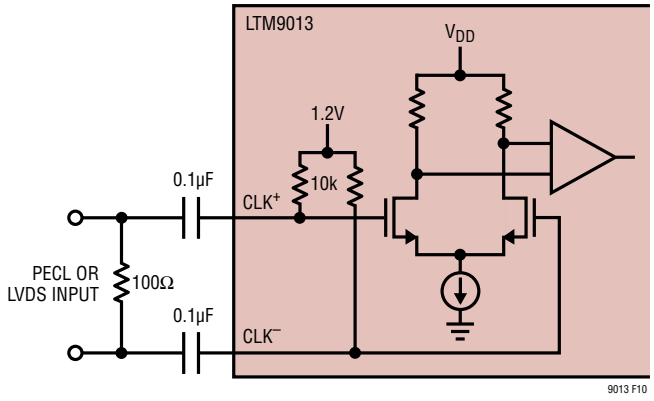


Figure 10. PECL or LVDS Encode Drive

Clock Duty Cycle Stabilizer

For good performance the encode signal should have a 50% (±5%) duty cycle. If the optional clock duty cycle stabilizer circuit is enabled, the encode duty cycle can vary from 30% to 70% and the duty cycle stabilizer will maintain a constant 50% internal duty cycle. The duty cycle stabilizer is enabled via SPI Register A2 (see Table 5) or by $\overline{CS}$ in parallel programming mode.

For applications where the sample rate needs to be changed quickly, the clock duty cycle stabilizer can be disabled. In this cases care should be taken to make the clock a 50% (± 5%) duty cycle.

DIGITAL OUTPUTS

The digital outputs are double data rate LVDS signals. Two data bits are multiplexed and output on each differential output pair. There are seven LVDS output pairs for channel A (DA0_1$^+$/DA0_1$^-$ through DA12_13$^-$/DA12_13$^+$) and seven pairs for channel B (DB0_1$^+$/DB0_1$^-$ through DB12_13$^-$/DB12_13$^+$). Overflow (OF$^+$/OF$^-$) and the data output clock (CLKOUT$^+$/CLKOUT$^-$) each have an LVDS output pair. Note that overflow for both channels is multiplexed onto the OF$^+$/OF$^-$ output pair.

By default the outputs are standard LVDS levels: 3.5mA output current and a 1.25V output common mode voltage. An external 100Ω differential termination resistor is required for each LVDS output pair. The termination resistors should be located as close as possible to the LVDS receiver.

Programmable LVDS Output Current

The default output driver current is 3.5mA. This current can be adjusted by serially programming mode control register A3 (see Table 5). Available current levels are 1.75mA, 2.1mA, 2.5mA, 3mA, 3.5mA, 4mA and 4.5mA.

APPLICATIONS INFORMATION

Optional LVDS Driver Internal Termination

In most cases, using just an external 100Ω termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100Ω termination resistor can be enabled by serially programming mode control register A3. The internal termination helps absorb any reflections caused by imperfect termination at the receiver. When the internal termination is enabled, the output driver current is doubled to maintain the same output voltage swing.

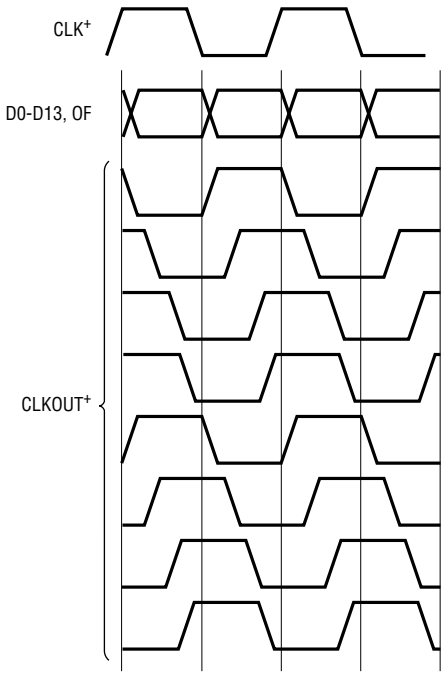
Overflow Bit

The overflow output bit (OF) outputs a logic high when the analog input is either overranged or underranged. The overflow bit has the same pipeline latency as the data bits. The OF output is double data rate; when CLKOUT+ is low, channel A's overflow is available; when CLKOUT+ is high, channel B's overflow is available.

Phase Shifting the Output Clock

To allow adequate set-up and hold time when latching the output data, the CLKOUT+ signal may need to be phase shifted relative to the data output bits. Most FPGAs have this feature; this is generally the best place to adjust the timing.

Alternatively, the ADC can also phase shift the CLKOUT+/CLKOUT– signals by serially programming mode control register A2. The output clock can be shifted by 0°, 45°, 90°, or 135°. To use the phase shifting feature the clock duty cycle stabilizer must be turned on. Another control register bit can invert the polarity of CLKOUT+ and CLKOUT–, independently of the phase shift. The combination of these two features enables phase shifts of 45° up to 315° (Figure 11).



PHASE SHIFT	MODE CONTROL BITS CLKINV	CLKPHASE1	CLKPHASE0
0°	0	0	0
45°	0	0	1
90°	0	1	0
135°	0	1	1
180°	1	0	0
225°	1	0	1
270°	1	1	0
315°	1	1	1

Figure 11. Phase Shifting CLKOUT

APPLICATIONS INFORMATION

DATA FORMAT

Table 3 shows the relationship between the analog input voltage, the digital data output bits and the overflow bit. By default the output data format is offset binary. The 2's complement format can be selected by serially programming mode control register A4.

Table 3. Output Codes vs Input Level

+IN – –IN	OF	D13-D0 (OFFSET BINARY)	D13-D0 (2's COMPLEMENT)
+Overflow	1	11 1111 1111 1111	01 1111 1111 1111
+Full Scale	0	11 1111 1111 1111	01 1111 1111 1111
	0	11 1111 1111 1110	01 1111 1111 1110
	0	10 0000 0000 0001	00 0000 0000 0001
Mid-Scale	0	10 0000 0000 0000	00 0000 0000 0000
	0	01 1111 1111 1111	11 1111 1111 1111
	0	01 1111 1111 1110	11 1111 1111 1110
–Full Scale	0	00 0000 0000 0001	10 0000 0000 0001
–Overflow	0	00 0000 0000 0000	10 0000 0000 0000
	1	00 0000 0000 0000	10 0000 0000 0000

Digital Output Randomizer

Interference from the A/D digital outputs is sometimes unavoidable. Digital interference may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can cause unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized which reduces the unwanted tone amplitude.

The digital output is randomized by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied—an exclusive-OR operation is applied between the LSB and all other bits. The LSB, OF and CLKOUT outputs are not affected. The output randomizer is enabled by serially programming mode control register A4.

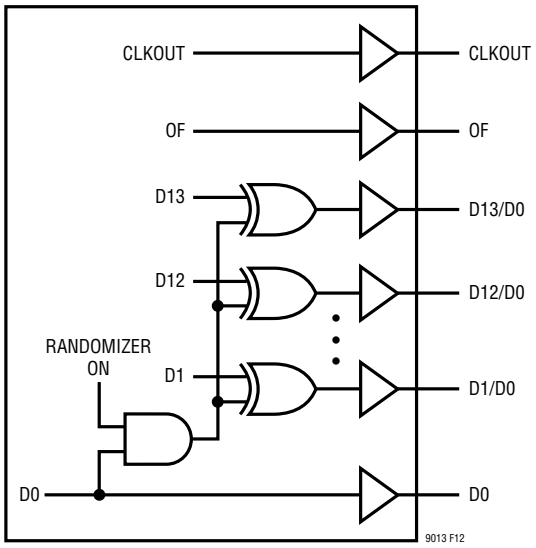


Figure 12. Functional Equivalent of Digital Output Randomizer

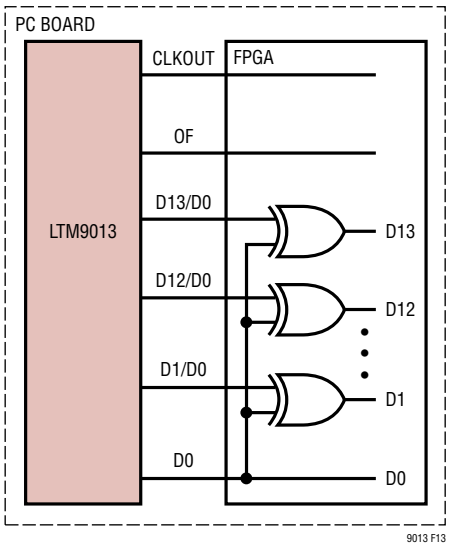


Figure 13. Decoding a Randomized Digital Output Signal

APPLICATIONS INFORMATION

Alternate Bit Polarity

Another feature that may reduce digital feedback on the circuit board is the alternate bit polarity mode. When this mode is enabled, all of the odd bits (D1, D3, D5, D7, D9, D11, D13) are inverted before the output buffers. The even bits (D0, D2, D4, D6, D8, D10, D12), OF and CLKOUT are not affected. This can reduce digital currents in the circuit board ground plane and reduce digital noise, particularly for very small analog input signals.

The digital output is decoded at the receiver by inverting the odd bits (D1, D3, D5, D7, D9, D11, D13.) The alternate bit polarity mode is independent of the digital output randomizer—either both or neither function can be on at the same time. The alternate bit polarity mode is enabled by serially programming mode control register A4.

Digital Output Test Patterns

To allow in-circuit testing of the digital interface to the A/D, there are several test modes that force the A/D data outputs (OF, D13 to D0) to known values:

All 1s: All outputs are 1

All 0s: All outputs are 0

Alternating: Outputs change from all 1s to all 0s on alternating samples

Checkerboard: Outputs change from 101010101010101 to 010101010101010 on alternating samples.

The digital output test patterns are enabled by serially programming mode control register A4. When enabled, the test patterns override all other formatting modes: 2's complement, randomizer, alternate-bit polarity.

Output Disable

The digital outputs may be disabled by serially programming mode control register A3. All digital outputs including OF and CLKOUT are disabled. The high impedance disabled state is intended for long periods of inactivity, it is not designed for multiplexing the data bus between multiple converters.

Sleep Mode

The A/D may be placed in sleep mode to conserve power. In sleep mode the entire A/D converter is powered down, resulting in <5mW power consumption. If the encode input signal is not disabled the power consumption will be higher (up to 5mW at 250Msps). Sleep mode is enabled by mode control register A1 (serial programming mode), or by SCK (parallel programming mode).

In the serial programming mode it is also possible to disable channel B while leaving channel A in normal operation.

The amount of time required to recover from sleep mode depends on the size of the bypass capacitor on V_{REF}. With the 2.2µF value used internally, the A/D will stabilize after 0.1ms + 2500 • t_p where t_p is the period of the sampling clock.

Nap Mode

In nap mode the A/D core is powered down while the internal reference circuits stay active, allowing faster wakeup. Recovering from nap mode requires at least 100 clock cycles. Nap mode is enabled by power-down register A1 in the serial programming mode.

Wake-up time from nap mode is guaranteed only if the clock is kept running, otherwise Power-Down Wake-up conditions apply.

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DEVICE PROGRAMMING MODES

The operating modes of the A/D can be programmed by either a parallel interface or a simple serial interface. The serial interface has more flexibility and can program all available modes. The parallel interface is more limited and can only program some of the more commonly used modes.

Parallel Programming Mode

To use the parallel programming mode, PAR/$\overline{SER}$ should be tied to V_{DD}. The $\overline{CS}$, SCK and SDI pins are binary logic inputs that set certain operating modes. These pins can be tied to V_{DD} or ground, or driven by 1.8V, 2.5V, or 3.3V CMOS logic. Table 4 shows the modes set by $\overline{CS}$, SCK and SDI.

Table 4. Parallel Programming Mode Control Bits (PAR/$\overline{SER}$ = V_{DD})

PIN	DESCRIPTION
$\overline{CS}$	Clock Duty Cycle Stabilizer Control Bit 0 = Clock Duty Cycle Stabilizer Off 1 = Clock Duty Cycle Stabilizer On
SCK	Power Down Control Bit 0 = Normal Operation 1 = Sleep Mode (entire ADC is powered down)
SDI	LVDS Current Selection Bit 0 = 3.5mA LVDS Current Mode 1 = 1.75mA LVDS Current Mode

Serial Programming Mode

To use the serial programming mode, PAR/$\overline{SER}$ should be tied to ground. The $\overline{CS}$, SCK, SDI and SDO pins become a serial interface that program the A/D control registers. Data is written to a register with a 16-bit serial word. Data can also be read back from a register to verify its contents.

Serial data transfer starts when $\overline{CS}$ is taken low. The data on the SDI pin is latched at the first sixteen rising edges of SCK. Any SCK rising edges after the first sixteen are ignored. The data transfer ends when $\overline{CS}$ is taken high again.

The first bit of the 16-bit input word is the R/$\overline{W}$ bit. The next seven bits are the address of the register (A6:A0). The final eight bits are the register data (D7:D0).

If the R/$\overline{W}$ bit is low, the serial data (D7:D0) will be written to the register set by the address bits (A6:A0). If the R/$\overline{W}$ bit is high, data in the register set by the address bits (A6:A0) will be read back on the SDO pin (see the Timing Diagrams). During a readback command the register is not updated and data on SDI is ignored.

The SDO pin is an open-drain output that pulls to ground with a 200Ω impedance. If register data is read back through SDO, an external 2k pull-up resistor is required. If serial data is only written and readback is not needed, then SDO can be left floating and no pull-up resistor is needed. Table 5 shows a map of the mode control registers.

Software Reset

If serial programming is used, the mode control registers should be programmed as soon as possible after the power supplies turn on and are stable. The first serial command must be a software reset which will reset all register data bits to logic 0. To perform a software reset it is necessary to write 1 in register A0 (Bit D7). After the reset is complete, Bit D7 is automatically set back to zero. This register is write-only.

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Table 5. Serial Programming Mode Register Map (PAR/$\overline{SER}$ = GND). X Indicates Unused Bit

REGISTER A0: RESET REGISTER (ADDRESS 00h) Write Only

D7	D6	D5	D4	D3	D2	D1	D0
RESET	X	X	X	X	X	X	X

Bit 7 **RESET** Software Reset Bit

0 = Reset Disabled
1 = Software Reset. All mode control registers are reset to 00h. This bit is automatically set back to zero after the reset is complete.

Bits 6-0 Unused Bits

REGISTER A1: POWER-DOWN REGISTER (ADDRESS 01h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	SLEEP	NAP	PDB	0

Bits 7-4 Unused, this bit read back as 0

Bit 3 **SLEEP**
0 = Normal Operation
1 = Power Down Entire ADC

Bit 2 **NAP**

0 = Normal Mode

1 = Low Power Mode for Both Channels

Bit 1 **PDB**

0 = Normal Operation

1 = Power Down Channel B. Channel A operates normally.

Bit 0 Must be set to 0

REGISTER A2: TIMING REGISTER (ADDRESS 02h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	CLKINV	CLKPHASE1	CLKPHASE0	DCS

Bits 7-4 Unused, This Bit Read Back as 0

Bit 3 **CLKINV** Output Clock Invert Bit
0 = Normal CLKOUT Polarity (as shown in the Timing Diagrams)
1 = Inverted CLKOUT Polarity

Bits 2-1 **CLKPHASE1:CLKPHASE0** Output Clock Phase Delay Bits
00 = No CLKOUT Delay (as shown in the Timing Diagrams)
01 = $CLKOUT^+/CLKOUT^-$ delayed by 45° (Clock Period • 1/8)
10 = $CLKOUT^+/CLKOUT^-$ delayed by 90° (Clock Period • 1/4)
11 = $CLKOUT^+/CLKOUT^-$ delayed by 135° (Clock Period • 3/8)
Note: If the CLKOUT phase delay feature is used, the clock duty cycle stabilizer must also be turned on.

Bit 0 **DCS** Clock Duty Cycle Stabilizer Bit
0 = Clock Duty Cycle Stabilizer Off
1 = Clock Duty Cycle Stabilizer On

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REGISTER A3: OUTPUT MODE REGISTER (ADDRESS 03h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	ILVDS2	ILVDS1	ILVDS0	TERMON	OUTOFF

Bits 7-5 Unused, This Bit Read Back as 0

Bits 4-2 **ILVDS2:ILVDS0** LVDS Output Current Bits
000 = 3.5mA LVDS Output Driver Current
001 = 4.0mA LVDS Output Driver Current
010 = 4.5mA LVDS Output Driver Current
011 = Not Used
100 = 3.0mA LVDS Output Driver Current
101 = 2.5mA LVDS Output Driver Current
110 = 2.1mA LVDS Output Driver Current
111 = 1.75mA LVDS Output Driver Current

Bit 1 **TERMON** LVDS Internal Termination Bit
0 = Internal Termination Off
1 = Internal Termination On. LVDS output driver current is 2× the current set by ILVDS2:ILVDS0

Bit 0 **OUTOFF** Digital Output Mode Control Bits
0 = Digital Outputs Are Enabled
1 = Digital Outputs Are Disabled (High Impedance)

REGISTER A4: DATA FORMAT REGISTER (ADDRESS 04h)

D7	D6	D5	D4	D3	D2	D1	D0
OUTTEST2	OUTTEST1	OUTTEST0	ABP	0	DTESTON	RAND	TWOSCOMP

Bits 7-5 **OUTTEST2:OUTTEST0** Digital Output Test Pattern Bits
000 = All Digital Outputs = 0
001 = All Digital Outputs = 1
010 = Alternating Output Pattern. OF, D13-D0 alternate between 000 0000 0000 0000 and 111 1111 1111 1111
100 = Checkerboard Output Pattern. OF, D13-D0 alternate between 101 0101 0101 0101 and 010 1010 1010 1010

Note 1: Other bit combinations are not used.

Note 2: Patterns from channel A and channel B may not be synchronous.

Bit 4 **ABP** Alternate Bit Polarity Mode Control Bit
0 = Alternate Bit Polarity Mode Off
1 = Alternate Bit Polarity Mode On

Bit 3 Must Be Set to 0

Bit 2 **DTESTON** Enable the digital output test patterns (set by Bits 7-5)
0 = Normal Mode
1 = Enable the Digital Output Test Patterns

Bit 1 **RAND** Data Output Randomizer Mode Control Bit
0 = Data Output Randomizer Mode Off
1 = Data Output Randomizer Mode On

Bit 0 **TWOSCOMP** Two's Complement Mode Control Bit
0 = Offset Binary Data Format
1 = Two's Complement Data Format

APPLICATIONS INFORMATION

Design Examples

The LTM9013 allows the user to tailor the highpass corner frequency to suit the application. The 0.5dB lowpass corner is set by the internal network at 300MHz. By cascading the external highpass and internal lowpass networks a bandpass characteristic is realized. An example of a very low frequency highpass corner is shown in Figure 14.

The typical performance for the overall module is shown below:

IF passband (1.5dB): 1MHz to 300MHz

RF input for –1dBFS: –5dBm at maximum gain

SNR at –1dBFS: 59.1dB

HD2 at –1dBFS: 74dBc

IMD3 at –7dBFS per tone: –72dBc

The frequency response is shown in Figure 15:

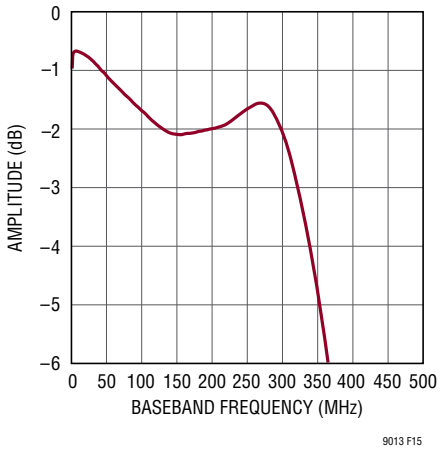


Figure 15. Baseband Frequency Response

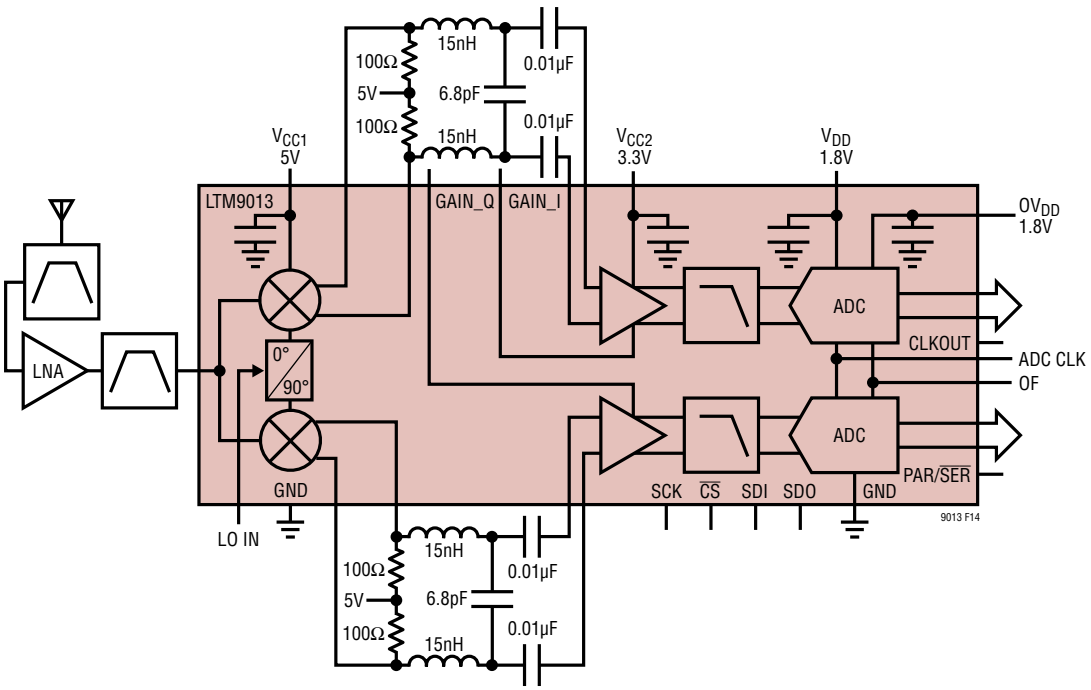


Figure 14. Highpass Filter Set for 1MHz

APPLICATIONS INFORMATION

For those applications that require a higher frequency corner at the highpass point, the network can be tailored, for example, as shown in Figure 16.

The typical performance for the overall module is shown below:

IF passband (1.0dB): 55MHz to 315MHz

RF input for –1dBFS: –5dBm at maximum gain

SNR at –1dBFS: 59.1dB

HD2 at –1dBFS: 74dBc

IMD3 at –7dBFS per tone: –72dBc

The frequency response is shown in Figure 17:

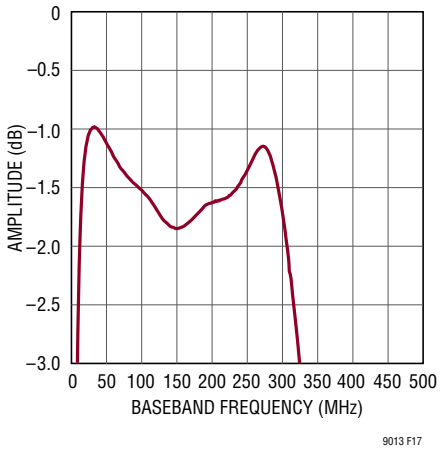


Figure 17. Baseband Frequency Response

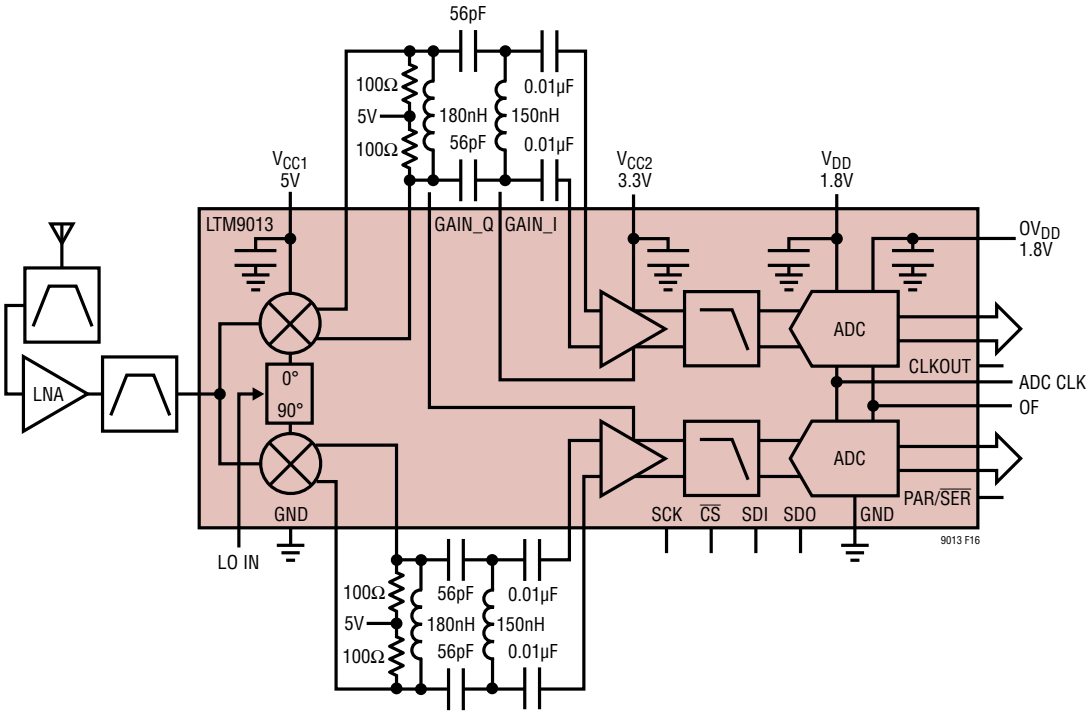


Figure 16. Highpass Filter Set for 55MHz

APPLICATIONS INFORMATION

Supply Sequencing

The V_{CC1} pins supply voltage to the demodulator. The V_{CC2} pins supply voltage to the amplifiers. The amplifier output stages are also fed by the V_{CC1} pins, so careful power supply sequencing is important. Power must be applied to the V_{CC2} pins before power is applied to the V_{CC1} pins to avoid damage to the amplifiers. Note also that the amplifiers must be enabled before voltage is applied to the V_{CC1} pins for the same reason.

Grounding and Bypassing

The LTM9013 requires a printed circuit board with a clean unbroken ground plane; a multilayer board with an internal ground plane is recommended. The pinout of the LTM9013 has been optimized for a flowthrough layout so that the interaction between inputs and digital outputs is minimized. A continuous row of ground pads facilitate a layout that ensures that digital and analog signal lines are separated as much as possible.

The LTM9013 is internally bypassed with the ADC (V_{DD}), mixer, amplifier (V_{CC}) digital (OV_{DD}) supplies returning to a common ground (GND). Additional bypass capacitance is optional and may be required if power supply noise is significant.

Heat Transfer

Most of the heat generated by the LTM9013 is transferred through the bottom-side ground pins. For good electrical and thermal performance, it is critical that all ground pins are connected to a ground plane of sufficient area with as many vias as possible.

Recommended Layout

The high integration of the LTM9013 makes the PCB board layout simple. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for ground. This helps to dissipate heat in the package through the board and also helps to shield sensitive on-board analog signals.
- Use multiple ground vias. Using as many vias as possible helps to improve the thermal performance of the board and creates necessary barriers separating analog and digital traces on the board at high frequencies.
- Separate analog and digital traces as much as possible, using vias to create high frequency barriers. This will reduce digital feedback that can reduce the signal-to-noise ratio (SNR) and dynamic range of the LTM9013.

Figures 18 through 25 give a good example of the recommended layout.

The quality of the paste print is an important factor in producing high yield assemblies. It is recommended to use a type 3 or 4 printing no-clean solder paste. The solder stencil design should follow the guidelines outlined in PCB Assembly and Manufacturing Guidelines

BGA Packages: Assembly Considerations for Linear Technology µModule BGA Packages.

TYPICAL APPLICATIONS

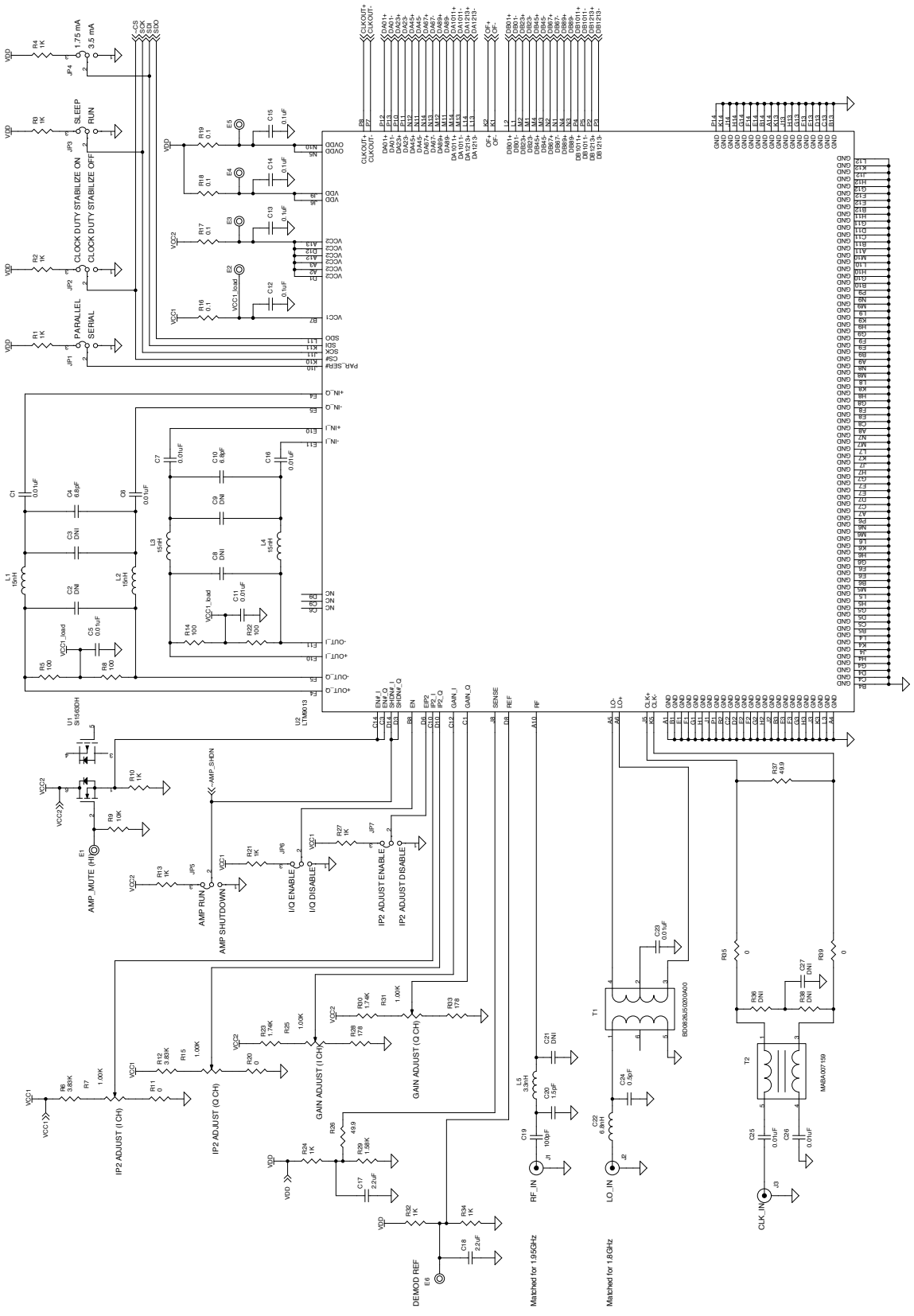


Figure 18. Schematic for Recommended Layout

TYPICAL APPLICATIONS

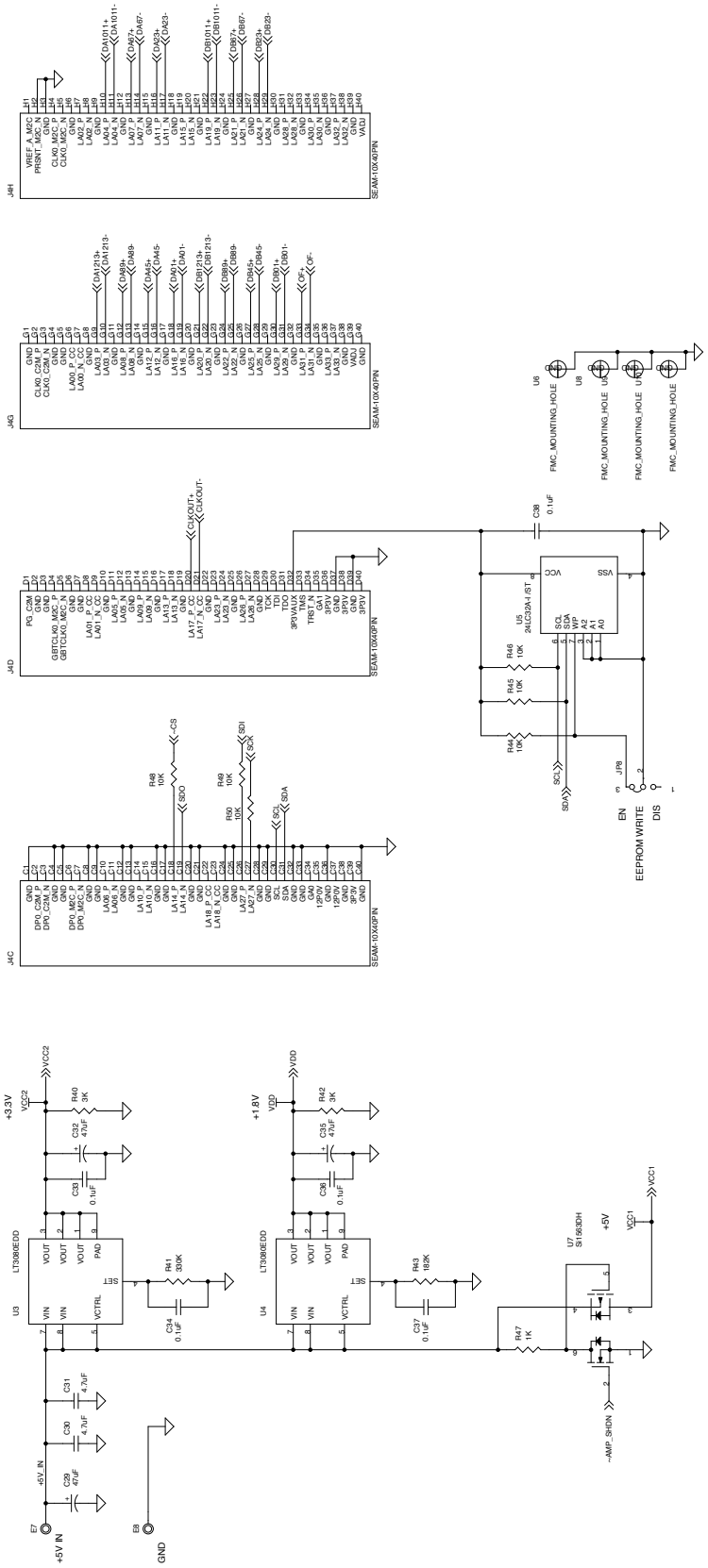


Figure 19. Additional Schematic Elements for Recommended Layout

TYPICAL APPLICATIONS

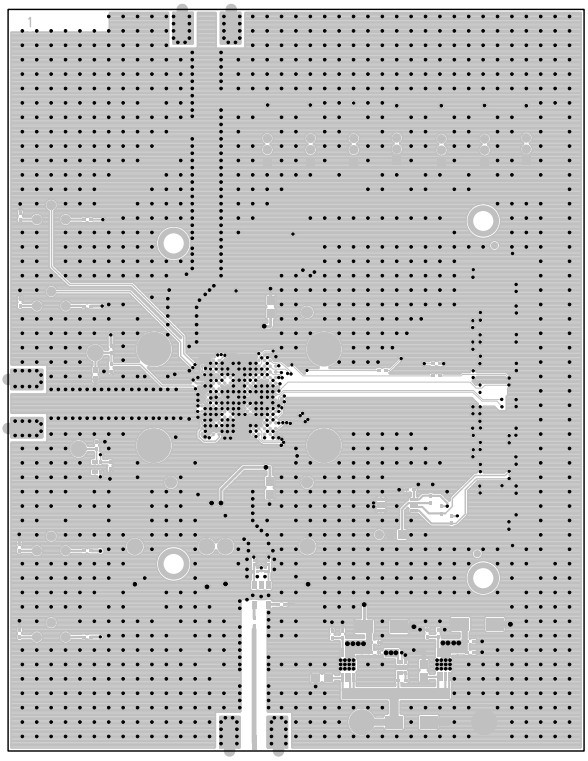


Figure 20. Layer 1

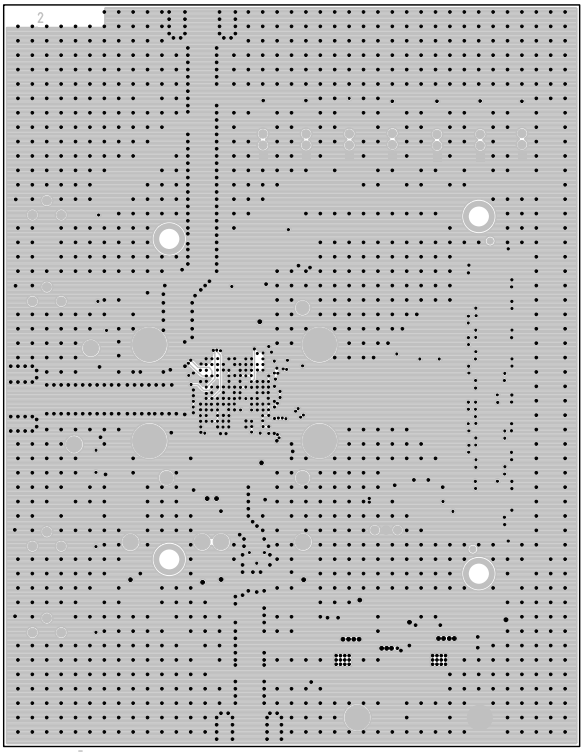


Figure 21. Layer 2

TYPICAL APPLICATIONS

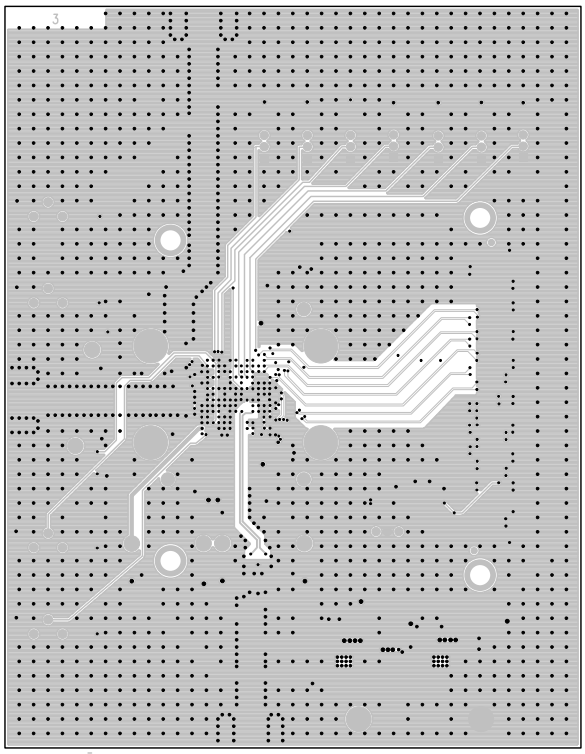


Figure 22. Layer 3

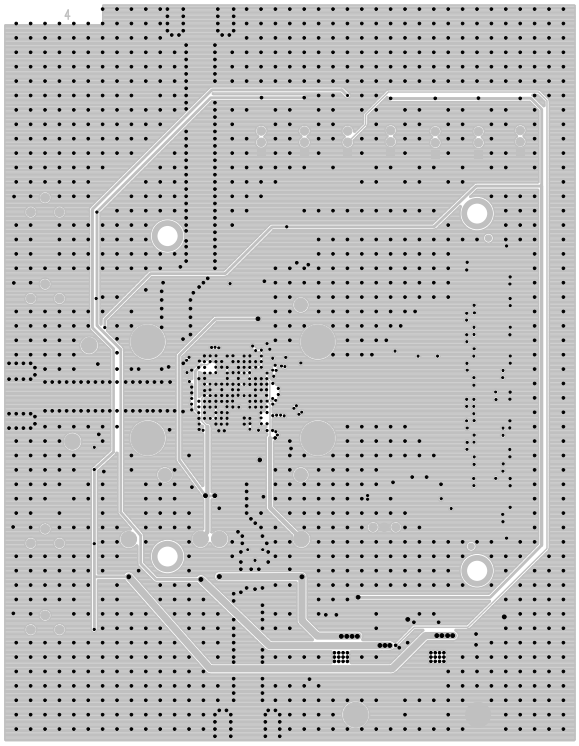


Figure 23. Layer 4

TYPICAL APPLICATIONS

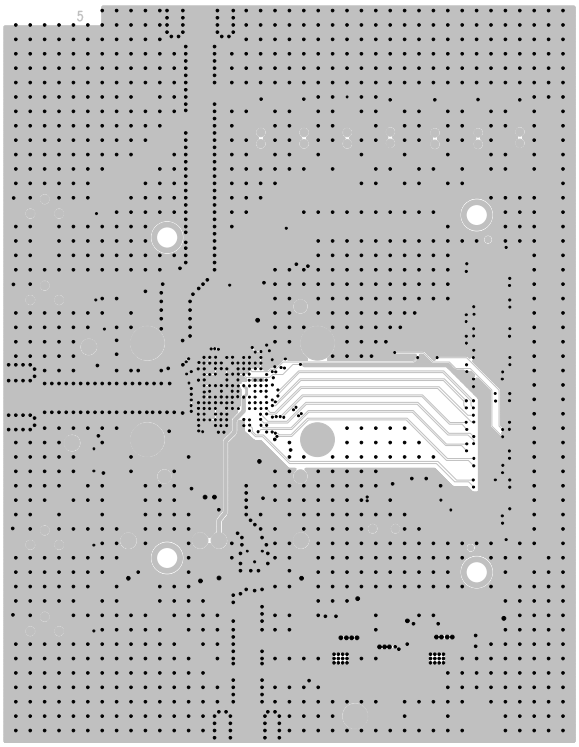


Figure 24. Layer 5

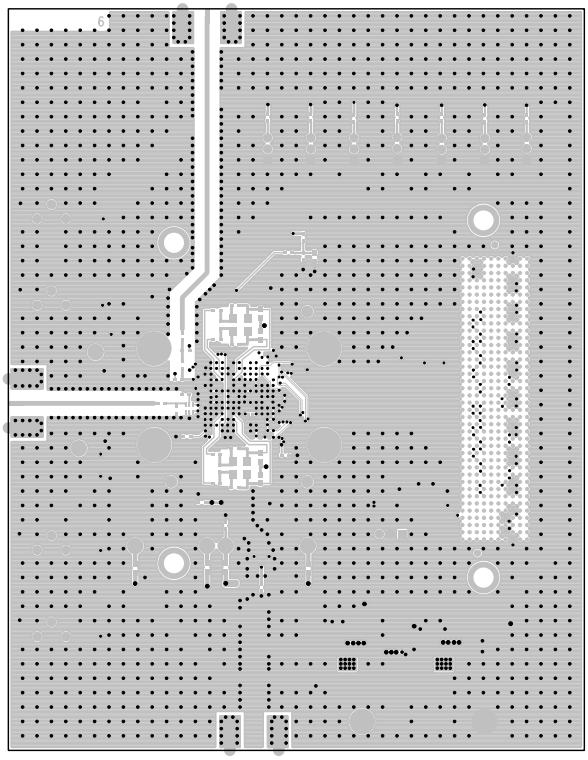
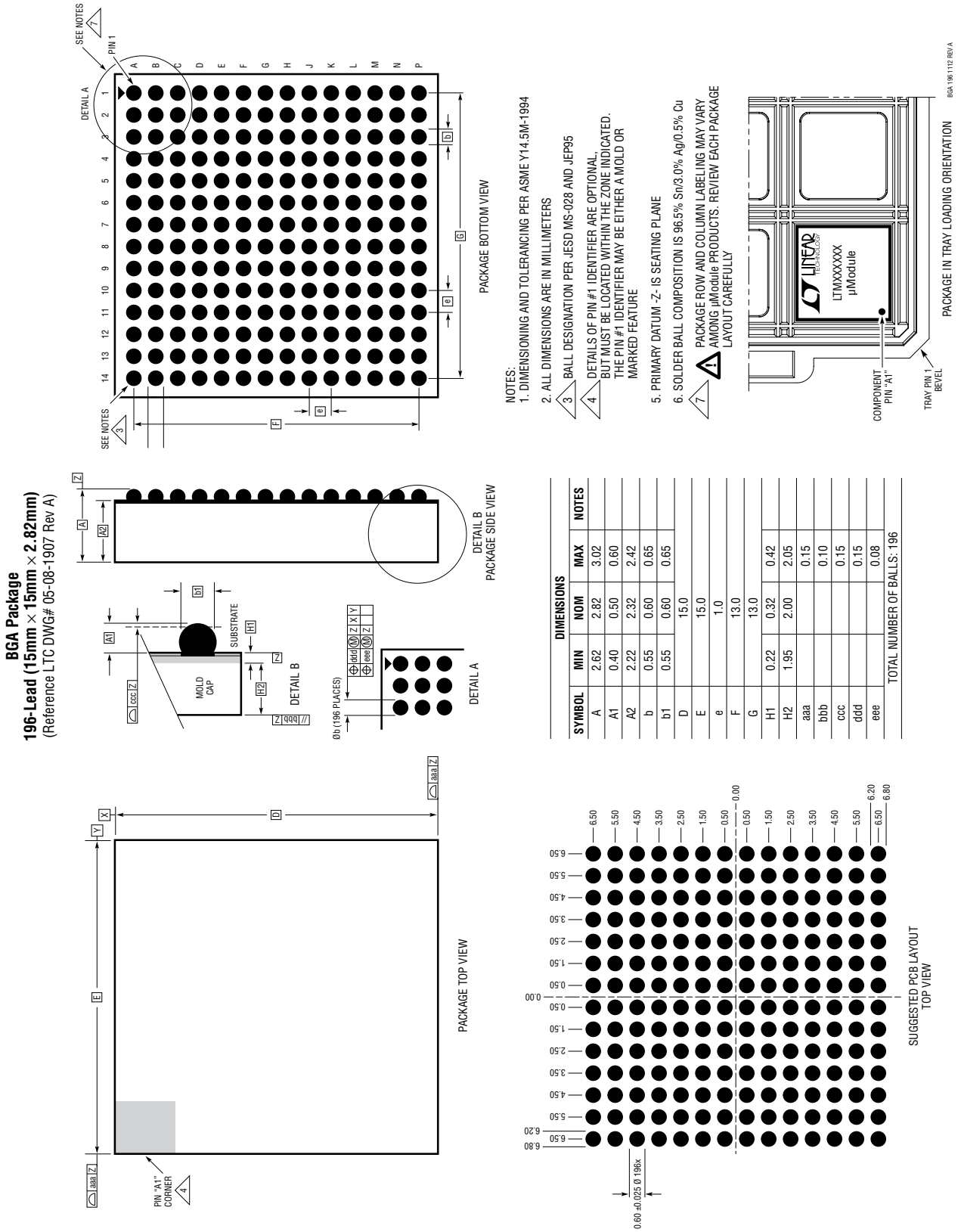


Figure 25. Layer 6

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.



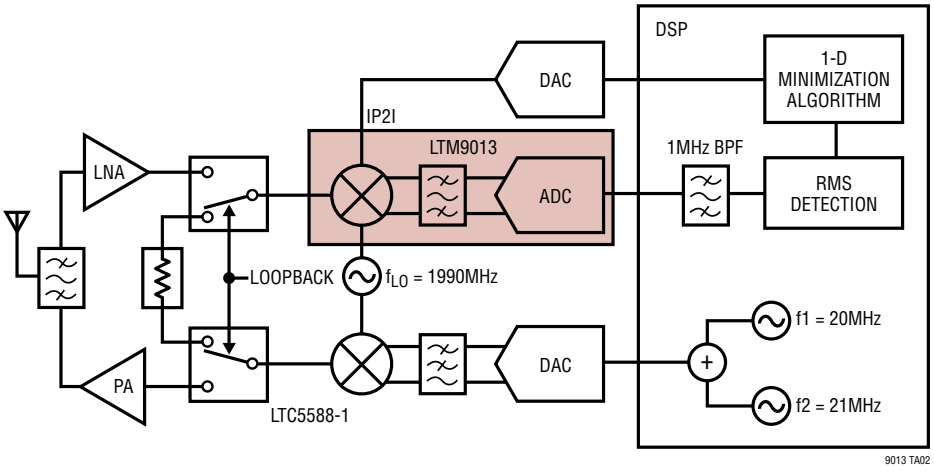
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.62	2.82	3.02	
A1	0.40	0.50	0.60	
A2	2.22	2.32	2.42	
b	0.55	0.60	0.65	
b1	0.55	0.60	0.65	
D		15.0		
E		15.0		
e		1.0		
F		13.0		
G		13.0		
H1	0.22	0.32	0.42	
H2	1.95	2.00	2.05	
aaa			0.15	
bbb			0.10	
ccc			0.15	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 196				

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/14	Changed product description to wideband receiver	1
		Changed latency to six cycles	16
		Updated demo board schematic to reflect pin out convention shown on page 11	31, 32

TYPICAL APPLICATION

Block Diagram for IM2 Adjustment. Only the I-Channel Is Shown



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2208	16-Bit, 130Msps, 3.3V ADC, LVDS Outputs	1250mW, 77.7dB SNR, 100dB SFDR, 64-Lead QFN Package
LTC2157-14/LTC2156-14/ LTC2155-14	14-Bit, 250Msps/210Msps/170Msps, 1.8V Dual ADC, DDR LVDS Outputs	605mW/565mW/511mW, 70dB SNR, 90dB SFDR, 9mm × 9mm 64-Lead QFN Package
LTC2152-14/LTC2151-14/ LTC2150-14	14-Bit, 250Msps/210Msps/170Msps, 1.8V Single ADC, DDR LVDS Outputs	338mW/316mW/290mW, 70dB SNR, 90dB SFDR, 6mm × 6mm 40-Lead QFN Package
LTC2158-14	14-Bit, 310Msps 1.8V Dual ADC, DDR LVDS Outputs, Low Power	724mW, 68.8dB SNR, 88dB SFDR, 9mm × 9mm 64-Lead QFN Package
RF Mixers/Demodulators		
LT5517	40MHz to 900MHz Direct Conversion Quadrature Demodulator	High IIP3: 21dBm at 800MHz, Integrated LO Quadrature Generator
LT5527	400MHz to 3.7GHz High Linearity Downconverting Mixer	24.5dBm IIP3 at 900MHz, 23.5dBm IIP3 at 3.5GHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LT5575	800MHz to 2.7GHz Direct Conversion Quadrature Demodulator	High IIP3: 28dBm at 900MHz, Integrated LO Quadrature Generator, Integrated RF and LO Transformer
Amplifiers/Filters		
LTC6409	10GHz GBW, 1.1nV/√Hz Differential Amplifier/ADC Driver	88dB SFDR at 100MHz, Input Range Includes Ground 52mA Supply Current, 3mm × 2mm QFN Package
LTC6412	800MHz, 31dB Range, Analog-Controlled Variable Gain Amplifier	Continuously Adjustable Gain Control, 35dBm OIP3 at 240MHz, 10dB Noise Figure, 4mm × 4mm QFN-24 Package
LTC6420-20	1.8GHz Dual Low Noise, Low Distortion Differential ADC Drivers for 300MHz IF	Fixed Gain 10V/V, 1nV/√Hz Total Input Noise, 80mA Supply Current per Amplifier, 3mm × 4mm QFN-20 Package
Receiver Subsystems		
LTM9002	14-Bit Dual Channel IF/Baseband Receiver Subsystem	Integrated High Speed ADC, Passive Filters and Fixed Gain Differential Amplifiers
LTM9003	12-Bit Digital Pre-Distortion Receiver	Integrated 12-Bit ADC Down-Converter Mixer with 0.4GHz to 3.8GHz Input Frequency Range

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