Title	***Reference Design Report for a 150 W LLC High-Voltage DC-DC Resonant Converter Using HiperLCS™ LCS702HG***
Specification	380 VDC Input; 24 V, 6.25 A Output
Application	HiperLCS Evaluation
Author	Applications Engineering Department
Document Number	RDR-239
Date	September 13, 2011
Revision	1.0

Summary and Features

- Low parts count, low cost, simple resonant (LLC) converter
  - Integration of controller, high-side and low-side MOSFETS and drivers reduces component count and design effort
- High operating frequency (250 kHz)
  - Reduces transformer core size (EEL25) and size of converter
  - Enables ceramic in place of electrolytic output capacitors
- High-efficiency
  - >95% efficiency at full load
  - >95% average efficiency (20%, 50%, 100% load points)
- Capacitive current sense for low power dissipation
- Burst mode ensures no-load regulation

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Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved.

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1 Introduction

This document is an engineering report describing a 24 V, 150 W LLC DC-DC converter utilizing a LCS702HG integrated LLC power stage IC. The report and board is intended as a general purpose test platform to demonstrate operation and capabilities of the HiperLCS family of devices.

The design operates from an input voltage range of 300 V to 420 V DC and requires an auxiliary supply of 12 V. The high-voltage DC input in a typical system would be supplied from a PFC stage and the 12 V from system bias or standby supply.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

1.1 Important Notes

For proper operation, the RD-239 must be used with a capacitor of at least 10 μF between the +380 V input and the input return placed directly across the terminals.

In most systems where this converter is used a secondary side supervisory circuit or output OV crowbar provides protection for output overvoltage. Therefore this design includes short-circuit protection, but no provisions for output overvoltage protection. Performing an overvoltage test by disabling the TL431 (U3) or optocoupler (U2) will cause the output voltage to rise, exceeding the voltage rating of the output Schottky rectifier (D2) and causing failure.

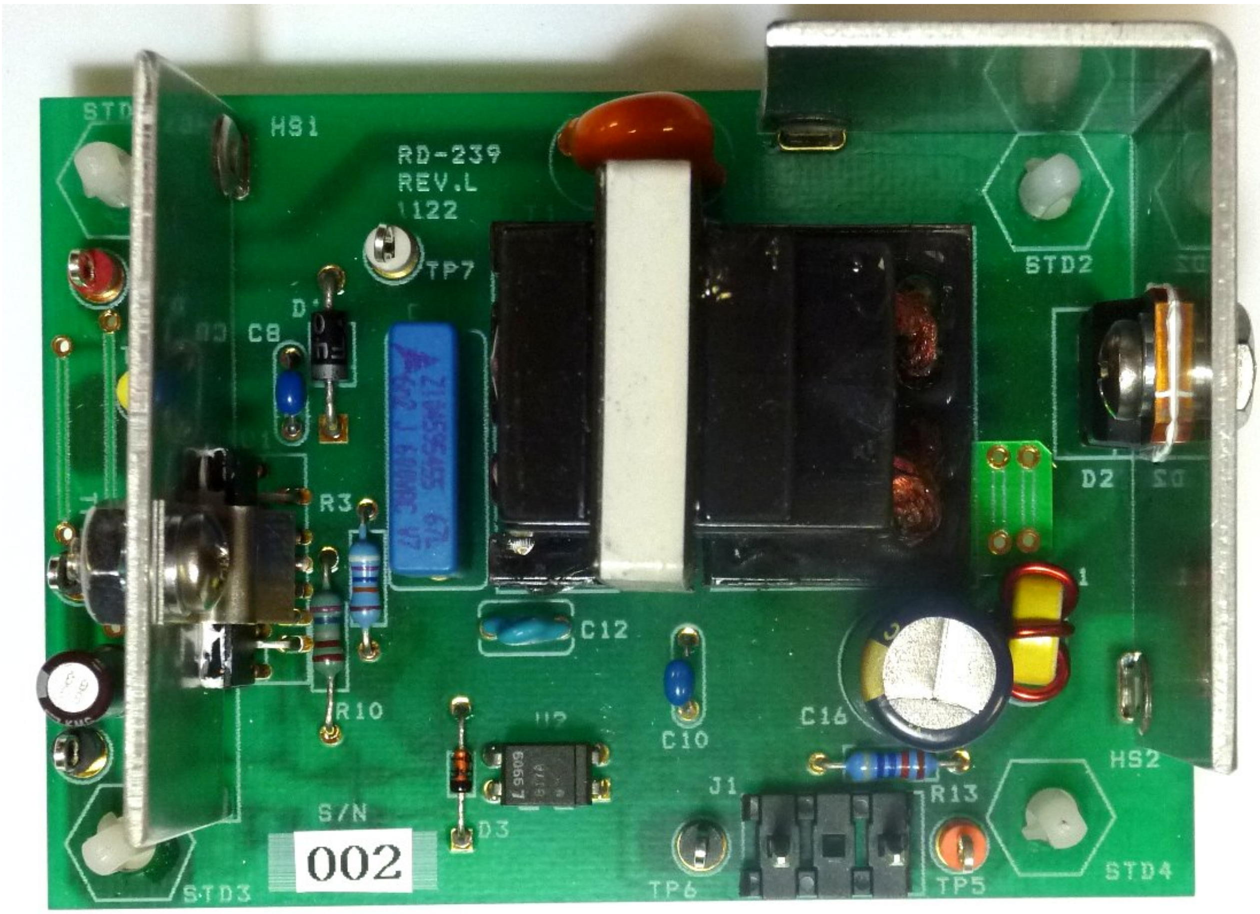

Figure 1 – Populated Circuit Board Photograph, Top View.

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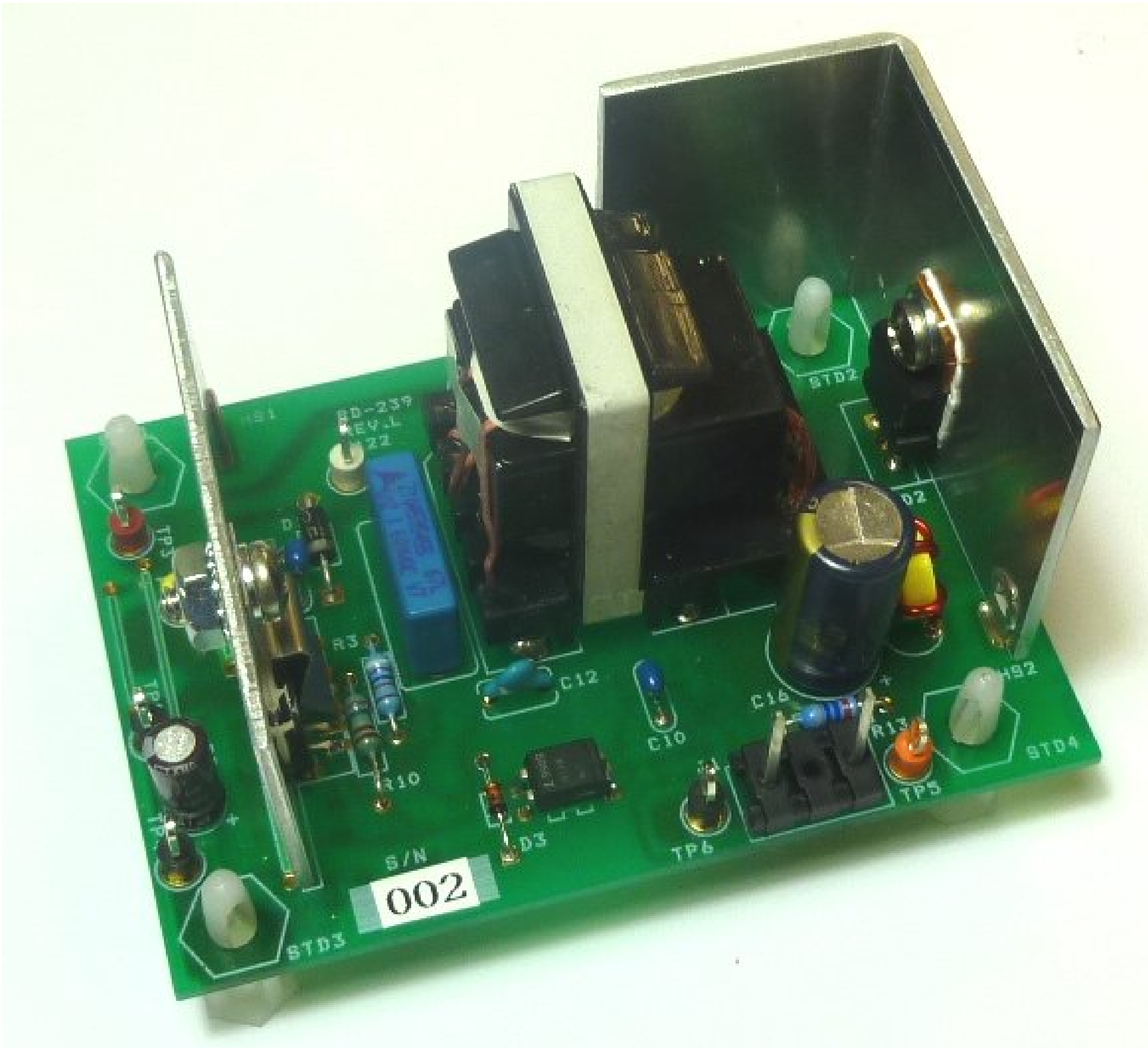

Figure 2 – Populated Circuit Board Photograph, Side View (1).

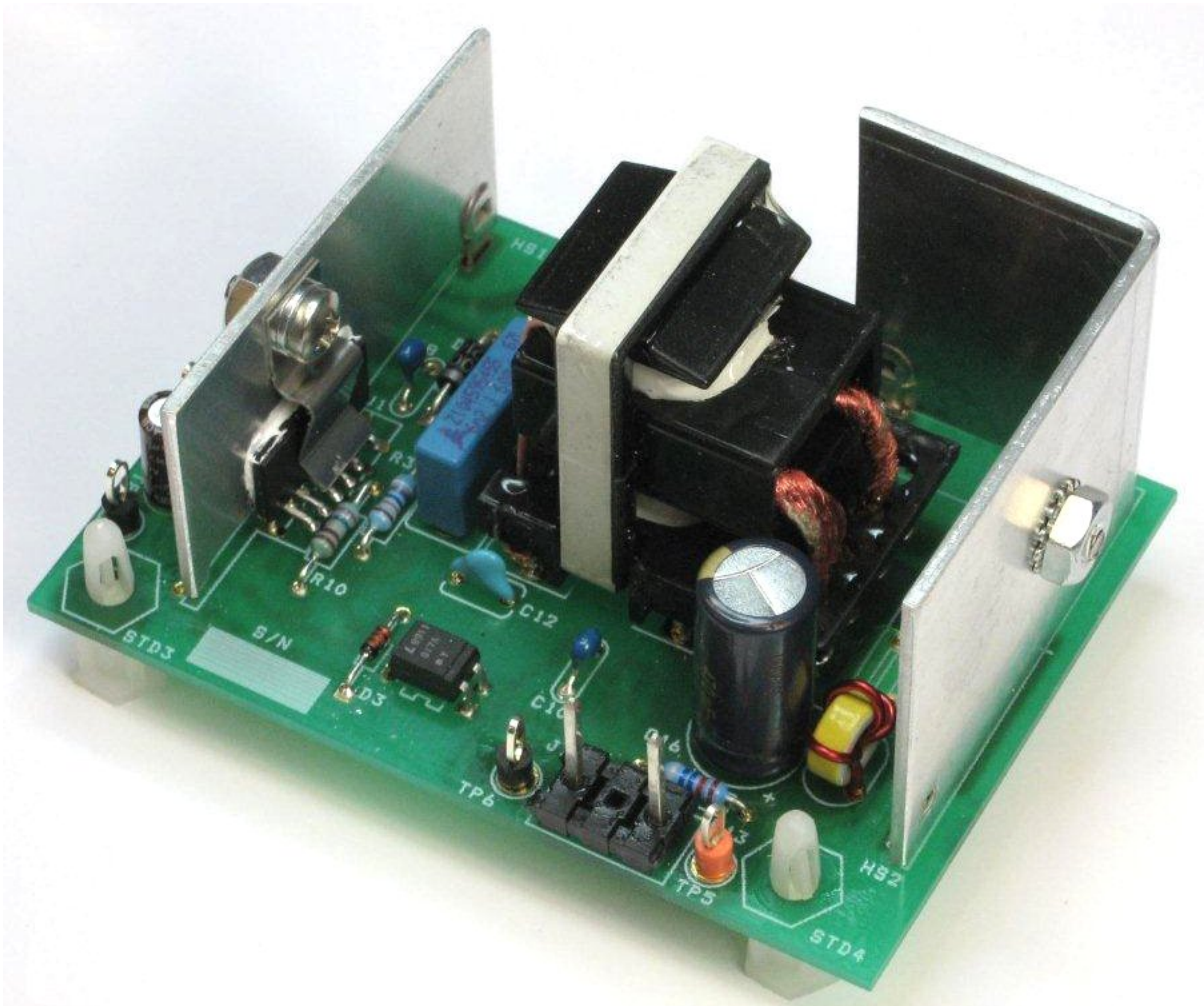

Figure 3 – Populated Circuit Board Photograph Side View (2)

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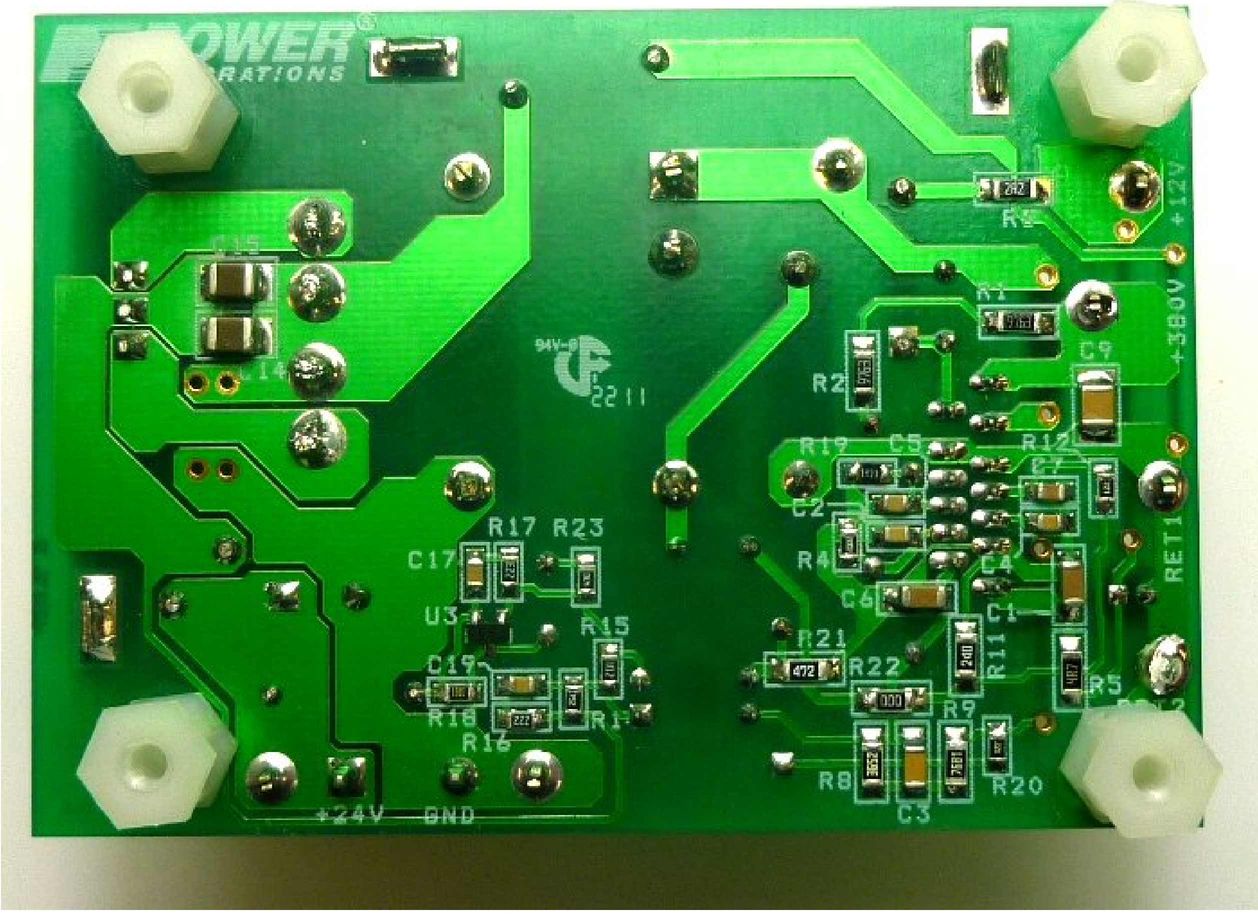

Figure 4 – Populated Circuit Board Photograph, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
DC Bus Voltage	V_{IN}	300	380	420	VDC	DC Input Only.
VCC Voltage	V_{CC}	11.4		14.5	VDC	>15 V may damage U1
No-load Input Power (380 VDC)			N/A		W	
Start-up Voltage	V_{START}		360		VDC	
Shutdown Voltage	V_{STOP}		285		VDC	
Output						
Output Voltage	V_{OUT}	22.8	24	25.2	V	$\pm$ 5%
Output P-P Ripple Voltage	V_{RIPPLE}			240	mV	20 MHz bandwidth
Output Current	I_{OUT}	0	6.25	6.25	A	
Total Output Power						
Continuous Output Power	P_{OUT}			150	W	
Peak Output Power	P_{OUT_PEAK}			150	W	
Efficiency						Measured at 25 °C, 380 VDC Input
20% Load	η	93.0	93.5		%	
50% Load	η	95.0	96		%	
100% Load	η	94.7	95.5		%	
Dimensions		82.5 x 58.4 x 34.8			mm	Length x Width x Height
Ambient Temperature	t_{AMB}	0		40	°C	Higher ambient operation requires lower thermal impedance heat sink for both IC1 and output diodes

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3 Schematic

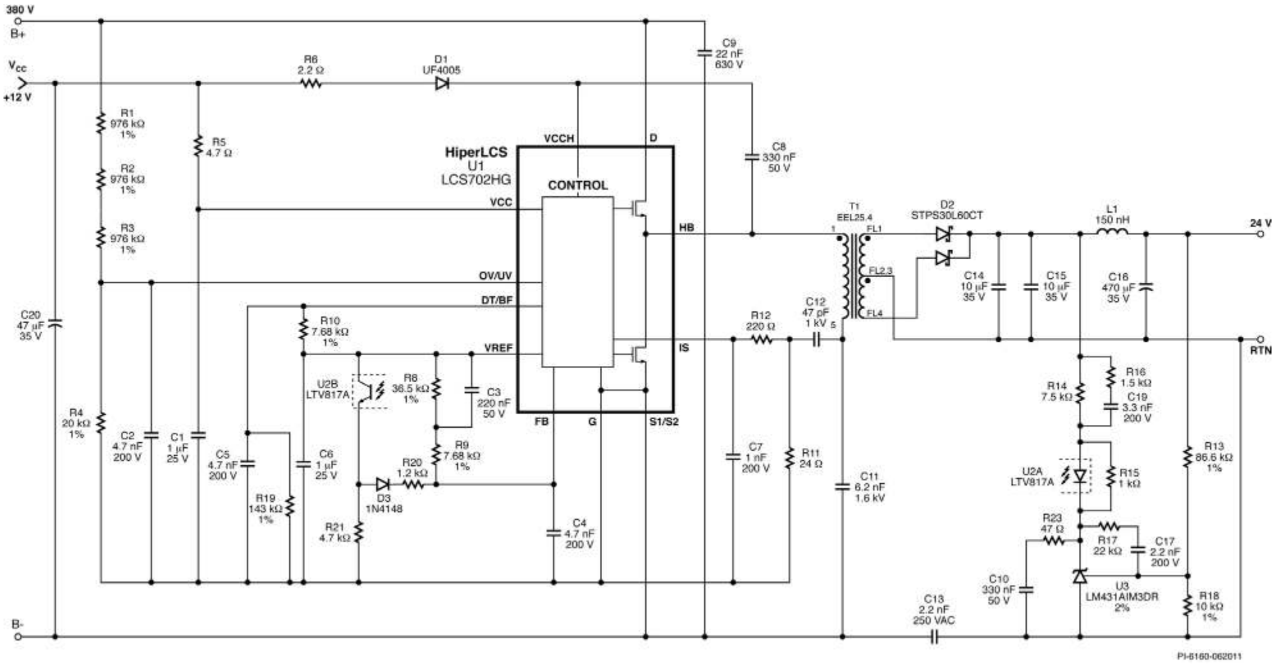

Figure 5 – Schematic.

4 Circuit Description

The schematic in Figures 5 depicts a 24 V, 150 W LLC DC-DC converter implemented using the LCS702HG, intended for demonstration of HiperLCS device operation. It is designed to be supplied from a nominal DC input voltage of 380 V and a 12 V bias supply.

For proper operation, the RD-239 must be used with a bulk capacitor of at least 10 μF placed directly between the +380 V input (B+) and the input return (0 V), placed directly across the terminals.

4.1 Primary

Integrated circuit U1 incorporates the control circuitry, drivers and output MOSFETs necessary for an LLC resonant half-bridge (HB) converter. The HB output of U1 drives output transformer T1 via a blocking/resonating capacitor (C11). This capacitor was rated for the operating ripple current and to withstand the high voltages present during fault conditions.

Transformer T1 was designed for a leakage inductance of 53 μH. This, along with resonating capacitor C11, sets the primary series resonant frequency at ~278 kHz according to the equation:

$$f_R = \frac{1}{6.28\sqrt{L_L \times C_R}}$$

Where f_R is the series resonant frequency in Hertz, L_L is the transformer leakage inductance in Henries, and C_R is the value of the resonating capacitor (C11) in Farads.

The transformer turns ratio was set by adjusting the primary turns such that the operating frequency at nominal input voltage and full load is close to, but slightly less than, the previously described resonant frequency.

An operating frequency of 250 kHz was found to be a good compromise between transformer size, output filter capacitance (enabling ceramic capacitors), and efficiency.

The number of secondary winding turns was chosen to provide a good compromise between core and copper losses. AWG #44 Litz wire was used for the primary and AWG #42 Litz wire, for the secondary, this combination providing high-efficiency at the operating frequency (~250 kHz). The number of strands within each gauge of Litz wire was chosen as a balance between winding fit and copper losses.

The core material selected was NC-2H (from Nicera). This material yielded acceptable (low loss) performance however selecting a material more suited for high-frequency operation, such as PC95 (from TDK), would further reduce core loss and increase efficiency.

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Components D1, R6, and C8 comprise the bootstrap circuit to supply the internal high-side driver of U1.

Components C20, R5, and C1 provide filtering and bypassing of the +12 V input which is the V_{CC} supply for U1. *Note: V_{CC} voltage of >15 V may damage U1.*

Voltage divider R1 to R4 sets the high-voltage turn-on, turn-off, and overvoltage thresholds of U1. The voltage divider values are chosen to set the LLC turn-on point at 360 VDC and the turn-off point at 285 VDC, with an input overvoltage turn-off point at 473 VDC. Built-in hysteresis sets the input undervoltage turn-off point at 280 VDC.

Capacitor C9 is a high-frequency bypass capacitor for the +380 V input, connected with short traces between the D and S1/S2 pins of U1.

Capacitor C12 forms a current divider with C11, and is used to sample a portion of the primary current. Resistor R11 senses this current, and the resulting signal is filtered by R12 and C7. Capacitor C12 should be rated for the peak voltage present during fault conditions, and should use a stable, low-loss dielectric such as metalized film, SL ceramic, or NPO/COG ceramic. The capacitor used in the RD-239 is a ceramic disc with "SL" temperature characteristic, commonly used in the drivers for CCFL tubes. The values chosen set the 1 cycle (fast) current limit at 5.5 A, and the 7-cycle (slow) current limit at 3 A, according to the equation:

$$I_{CL} = \frac{0.5}{\left(\frac{C12}{C11 + C12}\right) \times R11}$$

I_{CL} is the 7-cycle current limit in Amperes, R11 is the current limit resistor in Ohms, and C11 and C12 are the values of the resonating and current sampling capacitors in nanofarads, respectively. For the one-cycle current limit, substitute 0.9 V for 0.5 V in the above equation.

Resistor R12 and capacitor C7 filter primary current signal to the IS pin. Resistor R12 is set to 220 Ω, the minimum recommended value. The value of C7 is set to 1 nF to avoid nuisance tripping due to noise, but not so high as to substantially affect the current limit set values as calculated above. These components should be placed close to the IS pin for maximum effectiveness. The IS pin can tolerate negative currents, the current sense does not require a complicated rectification scheme.

Resistor R10 sets the dead time at 330 ns and maximum operating frequency for U1 at 773 kHz. The F_{MAX} input of U1 is filtered by C5. The combination of R10 and R19 also selects burst mode "1" for U1. This sets the lower and upper burst threshold frequencies at 338 kHz and 386 kHz, respectively.

The FEEDBACK pin has an approximate characteristic of 2.6 kHz per μA into the FEEDBACK pin. As the current into the FEEDBACK pin increases so does the operating frequency of U1, reducing the output voltage. The series combination of R8 and R9 sets the minimum operating frequency for U1, at ~115 kHz. This value was set to be slightly lower than the frequency required for regulation a full load and minimum bulk capacitor voltage. Resistor R8 is bypassed by C3 to provide output soft start during start-up by initially allowing a higher current to flow into the FEEDBACK pin when the feedback loop is open. This causes the switching frequency to start high and then decrease until the output voltage reaches regulation. Resistor R9 is typically set at the same value as R10 so that the initial frequency at soft-start is equal to the maximum switching frequency as set by R10. If the value of R9 is less than this, it will cause a delay before switching occurs when the input voltage is applied.

Optocoupler U2 drives the U1 FEEDBACK pin through R20 which limits the maximum optocoupler current into the FEEDBACK pin. Capacitor C4 filters the FEEDBACK pin. Resistor R21 loads the optocoupler output to force it to run at a relatively high quiescent current, increasing its gain. Resistors R20 and R21 also improve large signal step response and burst mode output ripple. Diode D3 isolates R21 from the F_{MAX}/soft start network.

4.2 Output Rectification

The output of transformer T1 is rectified and filtered by D2 and C14, C15. These capacitors are X5R dielectric, carefully chosen for output ripple current rating. Standard Z5U capacitors will *not* work in this application. Output Rectifier D2 is a 60 V Schottky rectifier chosen for high efficiency, Intertwining the transformer secondary halves (see transformer construction details in section 8) reduces leakage inductance between the two secondary halves, reducing the worst-case PIV to 57 V, allowing use of a 60 V Schottky diode with consequent higher efficiency. Additional output filtering is provided by L1 and C16. Capacitor C16 also damps the LLC output impedance peak at ~30 kHz caused by the LLC “virtual” output series R-L and ceramic output capacitors C14 and C15. It also improves the response to fast, high amplitude load steps. Resistors R13 and R18, along with the U3 reference voltage, set the output voltage of the supply. Error amplifier U3 drives the feedback optocoupler U2 via R14. Components C17, C19 and R14, R16, R17, and R21 determine the gain-phase characteristics of the supply. These values were chosen to provide stable operation at nominal and extreme load/input voltage combinations. Resistor R15 allows the minimum required operating current to flow in U3 when no current flow occurs in the LED of optocoupler U2. Components C10 and R23 are a soft finish network used to eliminate output overshoot at turn-on. Resistor R23 provides an artificially high ESR for C23, so that the output impedance of the TL431 (U3) dominates the gain-phase response.

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5 PCB Layout

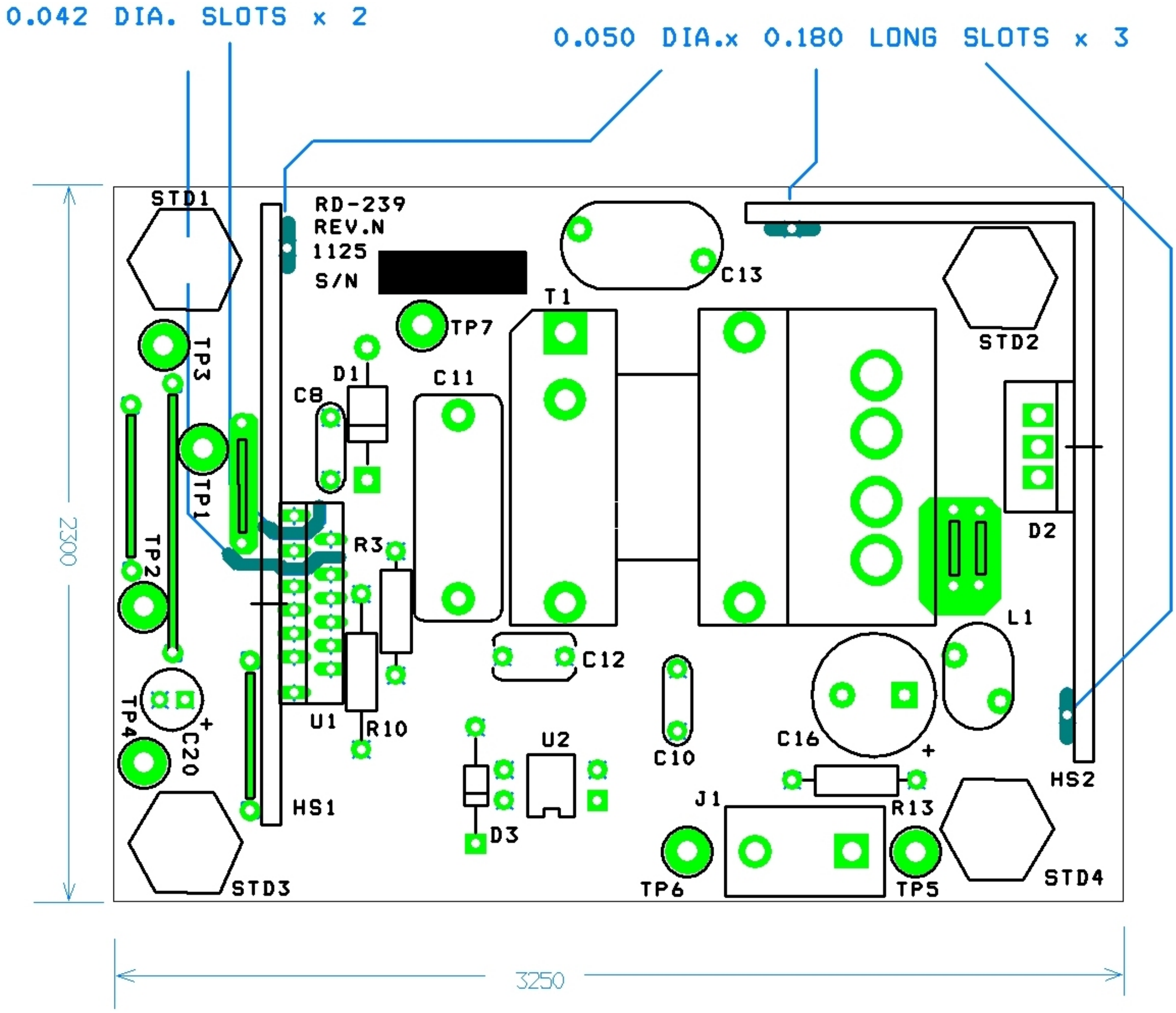

Figure 6 – Printed Circuit Layout, Top Side.

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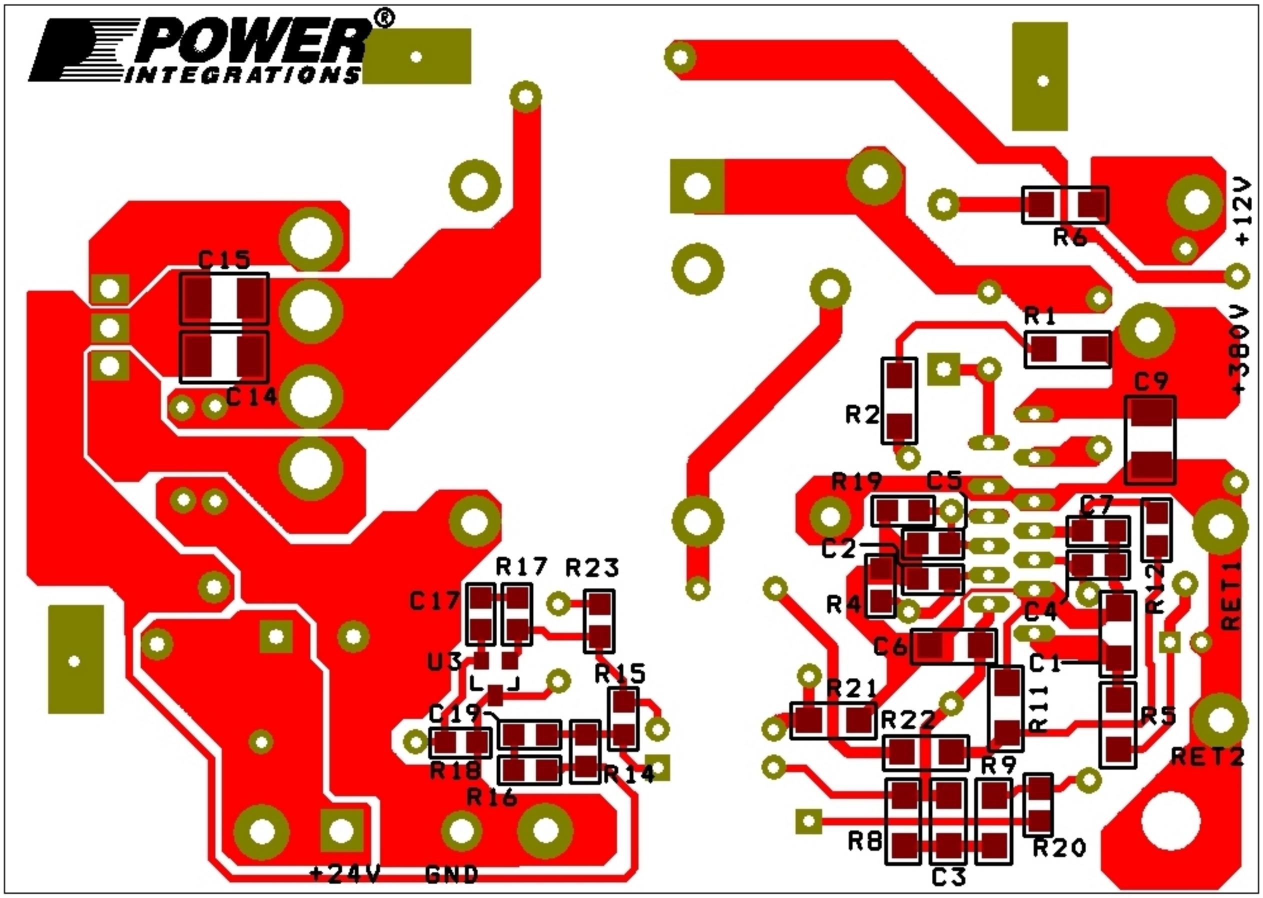

Figure 7 – Printed Circuit Layout, Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	C1 C6	1 μF, 25 V, Ceramic, X7R, 1206	C3216X7R1E105K	TDK
2	3	C2 C4 C5	4.7 nF, 200 V, Ceramic, X7R, 0805	08052C472KAT2A	AVX
3	1	C3	220 nF, 50 V, Ceramic, X7R, 1206	ECJ-3YB1H224K	Panasonic
4	1	C7	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
5	2	C8 C10	330 nF, 50 V, Ceramic, X7R	FK24X7R1H334K	TDK
6	1	C9	22 nF, 630 V, Ceramic, X7R, 1210	GRM32QR72J223KW01L	Murata
7	1	C11	6.2 nF, 1600 V, Film	B32672L1622J000	Epcos
8	1	C12	47 pF, 1 kV, Disc Ceramic	DEA1X3A470JC1B	Murata
9	1	C13	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
10	2	C14 C15	10 μF, 35 V, Ceramic, X5R, 1210	GMK325BJ106KN-T	Taiyo Yuden
11	1	C16	470 μF, 35 V, Electrolytic, Very Low ESR, 23 mΩ, (10 x 20)	EKZE350ELL471MJ20S	Nippon Chemi-Con
12	1	C17	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX
13	1	C19	3.3 nF, 200 V, Ceramic, X7R, 0805	08052C332KAT2A	AVX
14	1	C20	47 μF, 35 V, Electrolytic, Gen. Purpose, (5 x 11)	ECA-1VHG470	Panasonic
15	1	D1	600 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4005-E3	Vishay
16	1	D2	60 V, 30 A, Dual Schottky, TO-220AB	STPS30L60CT	ST Micro
17	1	D3	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
18	1	ESIPCLIP M4 METAL1	Heat sink Hardware, Edge Clip, 20.76 mm L x 8 mm W x 0.015 mm Thk	NP975864	Aavid Thermalloy
19	1	HS1	Heat sink, Diode, Custom, Al, 3003, 0.62Thk		Custom
20	1	HS2	Heat sink, Diode, Custom, Al, 3003, 0.062 Thk		Custom
21	1	J1	3 Position (1 x 3) header, 0.156 pitch, Vertical, Removed middle pin	26-48-1031	Molex
22	1	L1	Custom, 150nH, +/- 15%, constructed on Micrometals T30-26 toroidal core	SNX R1595	Santronics USA
23	2	NUT1 NUT2	Nut, Hex, Kep 6-32, Zinc Plate	6CKNTZR	Any RoHS Compliant Mfg.
24	2	R1 R2	976 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF9763V	Panasonic
25	1	R3	976 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-976K	Yageo
26	1	R4	20 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2002V	Panasonic
27	1	R5	4.7 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ4R7V	Panasonic
28	1	R6	2.2 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ2R2V	Panasonic
29	1	R8	36.5 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF3652V	Panasonic
30	1	R9	7.68 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7681V	Panasonic
31	1	R10	7.68 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-7K68	Yageo
32	1	R11	24 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ240V	Panasonic
33	1	R12	220 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ221V	Panasonic
34	1	R13	86.6 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-86K6	Yageo
35	1	R14	7.5 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ752V	Panasonic
36	1	R15	1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
37	1	R16	1.5 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ152V	Panasonic
38	1	R17	22 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ223V	Panasonic
39	1	R18	10 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
40	1	R19	143 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1433V	Panasonic
41	1	R20	1.2 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ122V	Panasonic
42	1	R21	4.7 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ472V	Panasonic
43	1	R22	0 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEY0R00V	Panasonic
44	1	R23	47 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ470V	Panasonic

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45	2	RTV1 RTV2	Thermally conductive Silicone Grease	120-SA	Wakefield
46	2	SCREW1 SCREW2	SCREW MACHINE PHIL 6-32 X 5/16 SS	PMSSS 632 0031 PH	Building Fasteners
47	4	STD1 STD2 STD3 STD4	Post, Circuit Board, Female, Hex, 6-32, snap, 0.375L, Nylon	561-0375A	Eagle Hardware
48	1	T1	Custom Transformer, Bobbin, EEL25.4, Vertical, 11 pins (2 mounting pins)	SNX R1545	Santronics USA
49	1	TP1	Test Point, YEL, THRU-HOLE MOUNT	5014	Keystone
50	3	TP2 TP4 TP6	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
51	1	TP3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
52	1	TP5	Test Point, ORG, THRU-HOLE MOUNT	5013	Keystone
53	1	TP7	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
54	1	U1	HiperLCS, ESIP16/13	LCS702HG	Power Integrations
55	1	U2	Optocoupler, 35 V, CTR 80-160%, 4-DIP	LTV-817A	Liteon
56	1	U3	IC, REG ZENER SHUNT ADJ SOT-23	LM431AIM3/NOPB	National Semr
57	2	WASHER1 WASHER2	Washer Flat #6, SS, Zinc Plate, 0.267 OD x 0.143 ID x 0.032 Thk	620-6Z	Olander

7 Transformer Design Spreadsheet

HiperLCS_041311; Rev.1.0; Copyright Power Integrations 2011	INPUTS	INFO	OUTPUTS	UNITS	HiperLCS_041311_Rev1-0.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
Enter Input Parameters					
VBULK_NOM			380	V	Nominal LLC input voltage
Vbrownout			280	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of VBULK_NOM. Set to 65% for max holdup time
Vbrownin			353	V	Startup threshold on bulk capacitor
VOV_shut			465	V	OV protection on bulk voltage
VOV_restart			448	V	Restart voltage after OV protection.
CBULK			103	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbulkmin to change bulk cap value
tHOLDUP			21.8	ms	Bulk capacitor hold up time
Enter LLC (secondary) outputs					**The spreadsheet assumes AC stacking of the secondaries**
VO1	24.00		24.0	V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
IO1	6.25		6.3	A	Main output maximum current
VD1	0.60		0.60	V	Forward voltage of diode in Main output
PO1			150	W	Output Power from first LLC output
VO2			0.0	V	Second Output Voltage
IO2			0.0	A	Second output current
VD2			0.70	V	Forward voltage of diode used in second output
PO2			0.00	W	Output Power from second LLC output
P_LLC			150	W	Specified LLC output power
LCS Device selection					
Device	**LCS702**		**LCS702**		LCS Device
RDSON (MAX)			1.39	ohms	RDSON (max) of selected device
Coss			250	pF	Equivalent Coss of selected device
Cpri			40	pF	Stray Capacitance at transformer primary
PCOND_LOSS			1.4	W	Conduction loss at nominal line and full load
TMAX_HS			90	deg C	Maximum heatsink temperature
Theta J-HS			9.1	deg C/W	Thermal resistance junction to heatsink (with grease and no insulator)
Expected Junction temperature			102	deg C	Expectd Junction temperature
Ta max			50	deg C	Expected max ambient temperature
Theta HS-A			29	deg C/W	Required thermal resistance heatsink to ambient
LLC Resonant Parameter and Transformer Calculations (generates red curve)					
Po			154	W	Output from LLC converter including diode loss
Vo			24.60	V	Main Output at transformer windings (includes diode drop)
f_target			250	kHz	Desired full load switching frequency of PFC and LLC. 66 kHz to 300 kHz, recommended 250 kHz
Lpar			287	uH	Parallel inductance. (Lpar = Lopen - Lres for integrated transformer; Lpar = Lmag for non-integrated low-leakage transformer)

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Lpri			340	uH	Primary open circuit inductance for integrated transformer; for low-leakage transformer it is sum of primary inductance and series inductor. If left blank, auto-calculation shows value necessary for loss of ZVS at 80% of Vnom
Lres	53.00		53.0	uH	Series inductance or primary leakage inductance of integrated transformer; if left blank auto-calculation is for K=4
Kratio			5.4		Ratio of Lpar to Lres. Maintain value of K such that 2.1 < K < 11. Preferred Lres is such that K<7.
Cres	6.20		6.2	nF	Series resonant capacitor. Red background cells produce red graph. If Lpar, Lres, Cres, and n_RATIO_red_graph are left blank, they will be auto-calculated
Lsec			5.098	uH	Secondary side inductance of one phase of main output; measure and enter value, or adjust value until f_predicted matches what is measured ;
m			50	%	Leakage distribution factor (primary to secondary). 99% signifies most of the leakage is in primary side
n_eq			7.50		Turns ratio of LLC equivalent circuit ideal transformer
Npri	49.0		49.0		Primary number of turns; if input is blank, default value is auto-calculation so that f_predicted = f_target
Nsec	6.0		6.0		Secondary number of turns (each phase of Main output). Default value is estimate to maintain BAC<=2000 Gauss
f_predicted			280	kHz	Expected frequency at nominal input voltage and full load; Heavily influenced by n_Ratio and primary turns
f_res			278	kHz	Series resonant frequency (defined by series inductance Lres and C)
f_brownout			180	kHz	Switching frequency at VBULK_MIN, full load
f_par			110	kHz	Parallel resonant frequency (defined by Lpar + Lres and C)
f_inversion			164	kHz	Min frequency, at Vbrownout and full load. Set HiperLCS minimum frequency to this value. Operation below this frequency results inoperation in gain inversion region
Vinversion			256	V	Minimum input voltage of LLC power train before low freq gain inversion point. Optimum value is equal Vbrownout
RMS CURRENTS AND VOLTAGES					
IRMS_LLC_Primary			0.99	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and fnominal_actual
Winding 1 (Lower secondary Voltage) RMS current			4.8	A	Winding 1 (Lower secondary Voltage) RMS current
Lower Secondary Voltage Capacitor RMS current			2.8	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			0.0	A	Winding 2 (Higher secondary Voltage) RMS current
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Cres_Vrms			91	V	Resonant capacitor AC RMS Voltage at full load and nominal input voltage
Virtual Transformer Trial - (generates blue curve)					
New primary turns			49.0		Trial transformer primary turns; default value is from resonant section
New secondary turns			6.0		Trial transformer secondary turns; default value is from resonant section
New Lpri			340	uH	Trial transformer open circuit inductance; default value is from resonant section
New Cres			7.6	nF	Trial value of series capacitor (if left blank calculated value chosen so f_res = f_target

New estimated Lres			53.0	uH	Trial transformer estimated Lres
New estimated Lpar			287	uH	Estimated value of Lpar for trial transformer
New estimated Lsec			5.098	uH	Estimated value of secondary leakahe inductance
New Kratio			5.4		Ratio of Lpar to Lres for trial transformer
New equivalent circuit transformer turns ratio			7.50		Estimated effective transformer turns ratio
V powertrain inversion new			246	V	Voltage on Bulk Capacitor below which ZVS is lost
f_res_trial			250	kHz	New Series resonant frequency
f_predicted_trial			252	kHz	New nominal operating frequency
IRMS_LLC_Primary			1.01	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and f_predicted_trial
Winding 1 (Lower secondary Voltage) RMS current			5.0	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Lower Secondary Voltage Capacitor RMS current			3.2	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			5.0	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
TRANSFORMER CORE CALCULATIONS (calculates from resonant parameter section)					
Transformer Core	**EEL25**		**EEL25**		**Transformer Core**
Ae			0.4	cm^2	Enter transformer core cross-sectional area
Ve			3.0	cm^3	Enter the volume of core
Aw			107.9	mm^2	Area of window
Bw			22.0	mm	Total Width of Bobbin
Loss density			200.0	mW/cm^3	Enter the loss per unit volume at the switching frequency and BAC (Units same as kW/m^3)
MLT			3.1	cm	Mean length per turn
N_CHAMBERS			2.0		Number of Bobbin chambers
W_SEP			3.0	mm	Winding separator distance (will result in loss of winding area)
Ploss			0.6	W	Estimated core loss
Bpkfmin			141	mT	First Quadrant peak flux density at minimum frequency.
BAC			181	mT	AC peak to peak flux density (calculated at f_predicted, Vbulk at full load)
PRIMARY WINDING					
Npri			49.0		Number of primary turns; determined in LLC resonant section
Primary gauge			44	AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge			0.050	mm	Equivalent diameter of wire in metric units
Primary litz strands	125		125		Number of strands in Litz wire; for non-litz primary winding, set to 1
Primary Winding Allocation Factor			50	%	Primary window allocation factor - percentage of winding space allocated to primary
AW_P			47	mm^2	Winding window area for primary
Fill Factor			43%	%	% Fill factor for primary winding (typical max fill is 60%)
Resistivity_25 C_Primary			75.42	m-ohm/m	Resistivity in milli-ohms per meter
Primary DCR 25 C			114.42	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C			153.32	m-ohm	Estimated resistance at 100 C (approximately 33% higher

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					than at 25 C)
Primary RMS current			0.99	A	Measured RMS current through the primary winding
ACR_Trf_Primary			245.31	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss			0.24	W	Total primary winding copper loss at 85 C
Secondary winding 1 (Lower secondary voltage OR Single output)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			24.00	V	Output Voltage (assumes AC stacked windings)
Sec 1 Turns			6.00		Secondary winding turns (each phase)
Sec 1 RMS current (total, AC+DC)			4.8	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Winding current (DC component)			3.13	A	DC component of winding current
Winding current (AC RMS component)			3.68	A	AC component of winding current
Sec 1 Wire gauge			42	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge			0.060	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands	270		270		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec1			21.96	m-ohm/m	Resistivity in milli-ohms per meter
DCR_25C_Sec1			4.08	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec1			5.47	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.43	W	Estimated Power loss due to DC resistance (both secondary phases)
ACR_Sec1			8.75	m-ohm	Measured AC resistance per phase(at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature . Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1			0.24	W	Estimated AC copper loss (both secondary phases)
Total winding 1 Copper Losses			0.66	W	Total (AC + DC) winding copper loss for both secondary phases
Capacitor RMS current			2.8	A	Output capacitor RMS current
Co1			4.8	uF	Secondary 1 output capacitor
Capacitor ripple voltage			3.0	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Secondary winding 2 (Higher secondary voltage)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			0.00	V	Output Voltage (assumes AC stacked windings)
Sec 2 Turns			0.00		Secondary winding turns (each phase) AC stacked on top of secondary winding 1
Sec 2 RMS current (total, AC+DC)			4.8	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Winding current (DC component)			0.0	A	DC component of winding current
Winding current (AC RMS component)			0.0	A	AC component of winding current
Sec 2 Wire gauge			42	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge			0.060	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands			0		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25			59292.53	m-ohm/m	Resistivity in milli-ohms per meter

C_sec2					
Transformer Secondary MLT			3.10	cm	Mean length per turn
DCR_25C_Sec2			0.00	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec2			0.00	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.00	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2			0.00	m-ohm	Measured AC resistance per phase(at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature . Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2			0.00	W	Estimated AC copper loss (both secondary halves)
Total winding 2 Copper Losses			0.00	W	Total (AC + DC) winding copper loss for both secondary halves
Capacitor RMS current			0.0	A	Output capacitor RMS current
Co2			N/A	uF	Secondary 2 output capacitor
Capacitor ripple voltage			N/A	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Transformer Loss Calculations					**Does not include fringing flux loss from gap**
Primary copper loss (from Primary section)			0.24	W	Total primary winding copper loss at 85 C
Secondary copper Loss			0.66	W	Total copper loss in secondary winding
Transformer total copper loss			0.91	W	Total copper loss in transformer (primary + secondary)
AW_S			46.59	mm^2	Area of window for secondary winding
Secondary Fill Factor			33%	%	% Fill factor for secondary windings; typical max fill is 60% for served and 75% for unserved Litz
Signal pins resistor values					
Dead Time	330		330	ns	Dead time
Burst Mode	**1**		**1**		Select Burst Mode: 1, 2, and 3 have hysteresis and have different frequency thresholds
f_max			773	kHz	Max internal clock frequency, dependent on dead-time setting
f_burst_start			338	kHz	Lower threshold frequency of burst mode, provides hysteresis. This is switching frequency at restart after a bursting off-period
f_burst_stop			386	kHz	Upper threshold frequency of burst mode; This is switching frequency at which a bursting off-period stops
DT/BF pin upper divider resistor			7.62	k-ohms	Resistor from DT/BF pin to VREF pin
DT/BF pin lower divider resistor			145	k-ohms	Resistor from DT/BF pin to G pin
Rstart			7.62	k-ohms	Start-up resistor - resistor in series with soft-start capacitor; equivalent resistance from FB to VREF pins at startup
Start up delay			0.0	ms	Start-up delay; delay before switching begins. Reduce R_START to increase delay
Rfmin			34.7	k-ohms	Resistor from VREF pin to FB pin, to set min operating frquency; This resistor plus Rstart determine f_MIN
C_softstart	0		0.2	uF	Softstart capacitor. Recommended values are between 0.1 uF and 10 uF
Ropto			3.9	k-ohms	Resistor in series with opto emitter
OV/UV pin lower resistor	20.00		20.0	k-ohm	Lower resistor in OV/UV pin divider
OV/UV pin upper resistor			2.92	M-ohm	Total upper resistance in OV/UV pin divider

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LLC capacitive divider current sense circuit					
slow current limit			2.78	A	8-cycle current limit - check postivie half-cycles during brownout and startup
fast current limit			5.00	A	1-cycle current limit - check positive half-cycles during startup
LLC sense capacitor			47	pF	HV sense capacitor, forms current divider with main resonant capacitor
RLLC sense resistor			23.9	ohms	LLC current sense resistor, senses current in sense capacitor
IS pin current limit resistor			220	ohms	Limits current from sense resistor into IS pin when voltage on sense R is < -0.5V
IS pin noise filter capacitor			1.0	nF	IS pin bypass capacitor; forms a pole with IS pin current limit capacitor
IS pin noise filter pole frequency			724	kHz	This pole attenuates IS pin signal
LOSS BUDGET					
LCS device Conduction loss			1.4	W	Conduction loss at nominal line and full load
Output diode Loss			3.8	W	Estimated diode losses
Transformer estimated total copper loss			0.91	W	Total copper loss in transformer (primary + secondary)
Transformer estimated total core loss			0.6	W	Estimated core loss
Total transformer losses			1.5	W	Total transformer losses
Total estimated losses			6.6	W	Total losses in LLC stage
Estimated Efficiency			96%	%	Estimated efficiency
PIN			157	W	LLC input power
SECONDARY TURNS AND VOLTAGE CENTERING CALCULATOR					**This is to help you choose the secondary turns - Outputs not connected to any other part of spreadsheet**
V1			24.00	V	Target regulated output voltage Vo1. Change to see effect on slave output
V1d1			0.60	V	Diode drop voltage for Vo1
N1			6.00		Total number of turns for Vo1
V1_Actaul			24.00	V	Expected output
V2			0.00	V	Target output voltage Vo2
V2d2			0.70	V	Diode drop voltage for Vo2
N2			0.00		Total number of turns for Vo2
V2_Actual			-0.70	V	Expected output voltage
Separate Series Inductor (For non-integrated transformer only)					**Not applicable if using integrated magnetics - not connected to any other part of spreadsheet**
Lsep			53.00	uH	Desired inductance of separate inductor
Ae_Ind			0.53	cm^2	Inductor core cross-sectional area
Inductor turns			10		Number of primary turns
BP_fnom			1502	Gauss	AC flux for core loss calculations (at f_predicted and full load)
Expected peak primary current			2.8	A	Expected peak primary current
BP_fmin			2804	Gauss	Peak flux density, calculated at minimum frequency fmin
Inductor gauge			44	AWG	Individual wire strand gauge used for primary winding
Equivalent Inductor Metric Wire gauge			0.050	mm	Equivalent diameter of wire in metric units
Inductor litz strands			125.00		Number of strands used in Litz wire
Inductor parallel			1		Number of parallel individual wires to make up Litz wire

wires					
Resistivity_25 C_Sep_Ind			75.4	m-ohm/m	Resistivity in milli-ohms per meter
Inductor MLT			7.00	cm	Mean length per turn
Inductor DCR 25 C			52.8	m-ohm	Estimated resistance at 25 C (for reference)
Inductor DCR 100 C			70.7	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
ACR_Sep_Inductor			113.2	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Inductor copper loss			0.11	W	Total primary winding copper loss at 85 C

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8 Transformer Specification

8.1 Electrical Diagram

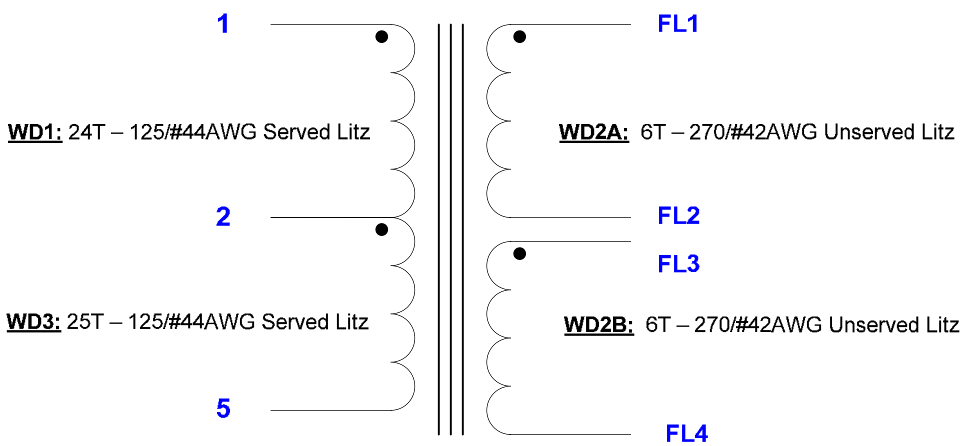

Figure 8 –Transformer Electrical Diagram.

8.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-5 to FL1, FL2, FL3, FL4.	3000 VAC
Primary Inductance	Pins 1-5, all other windings open, measured at 300 kHz, 0.4 V_{RMS}	350 μH, ±10%
Resonant Frequency	Pins 1-5, all other windings open	1400 kHz (Min)
Primary Leakage Inductance	Pins 1-5, with FL1, FL2, FL3, FL4 shorted, measured at 300 kHz, 0.4 V_{RMS}	53 μH ±7%

8.3 Materials

Item	Description
[1]	Core Pair: EEL25.4 Nippon Ceramic FEEL25.4-NC-2H, ungapped.
[2]	Bobbin: EEL25 Vertical, 3 chamber, 5 pins. PI P/N 25-00960-05
[3]	Bobbin Cover, PI P/N 25-00961-00.
[4]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 7.0mm wide.
[5]	Litz wire: 270/#42 Single Coated, Unserved.
[6]	Litz wire: 125/#44 Single Coated, Served.
[7]	Transformer Varnish: Dolph BC-359 or equivalent.

8.4 Transformer Build Diagram

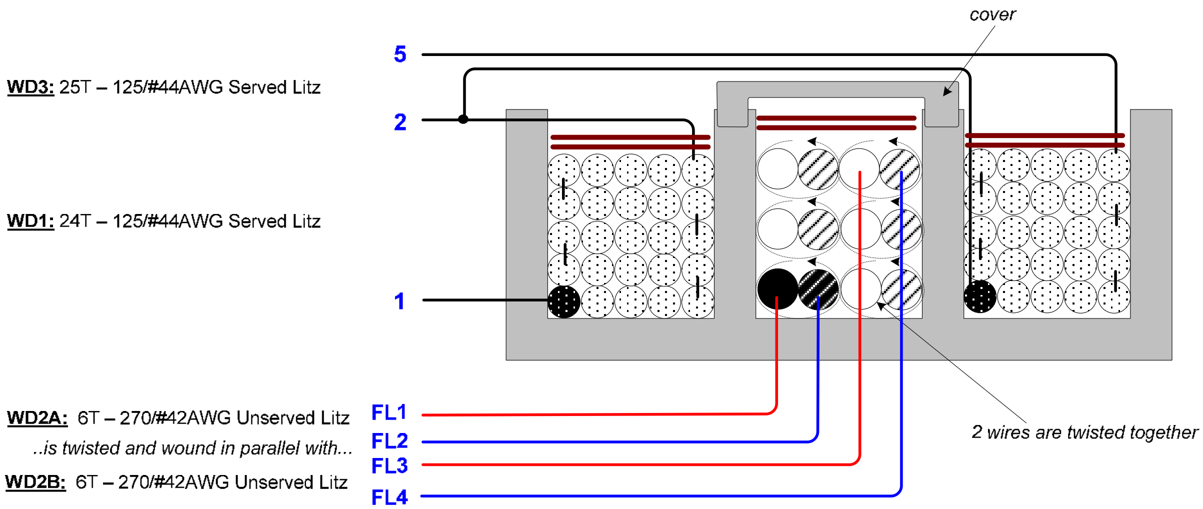

Figure 9 – Transformer Build Diagram.

8.5 Transformer Construction

Secondary Wire Preparation	Prepare 2 strands of wire item [5] 13" length, tin ends, and label one strand to distinguish from other and designate it as FL1, FL2. Other strand will be designated as FL3 and FL4. Twist these 2 strands together ~30 twists evenly along length leaving 1" free at each end. See pictures below.
WD1 (Primary)	Place the bobbin item [2] on the mandrel with pin side on the left side. Starting on pin 1, wind 24 turns of served Litz wire [6] in 5 layers, and finish on pin 2. Secure winding with one turn of tape [4].
WD2A and WD2B (Secondary)	Using unserved Litz assembly prepared in step 1, start with FL1 and FL3 inserted into hole 1 and hole 2 of bobbin [2] bottom flange (see illustration). Tightly wind 6 turns in bobbin center chamber. Finish with FL2 in Hole 3 of bobbin bottom flange, and FL4 in hole 4. Secure winding with one turn of tape [4].
Bobbin Cover	Slide bobbin cover [3] into grooves in bobbin flanges as shown, with closed end of cover pointed to pin 1-5 side of bobbin see illustration. Make sure cover is securely seated.
WD 3 (Primary)	Start on pin 2 of bobbin [2], wind 25 turns of served Litz wire [6], finishing on pin 5. Secure and insulate winding start lead using tape [4] per illustration. Secure winding with one turn of tape [4].
Finish	Grind core halves [1] for inductance of 350 µH ±10%. Assemble and secure core halves. Tin all secondary wires to ~ ¼" from bobbin holes per illustration, and trim to ½". Dip varnish [7].

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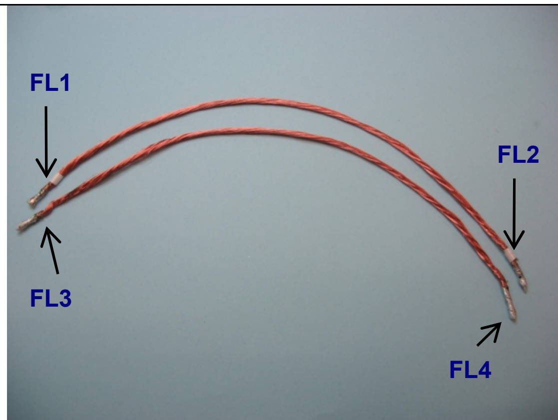
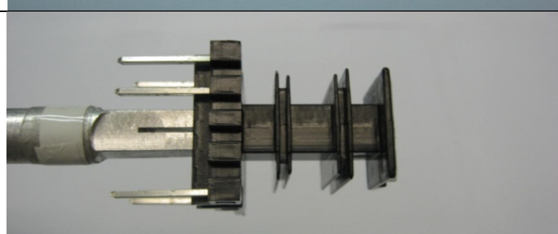
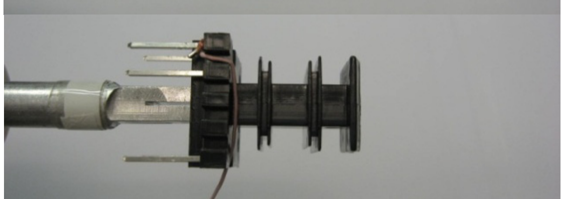
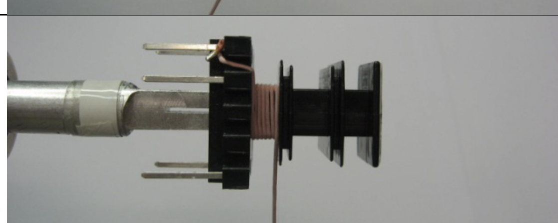
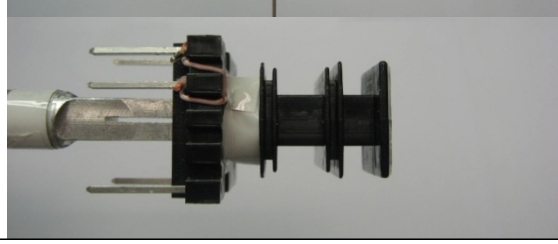
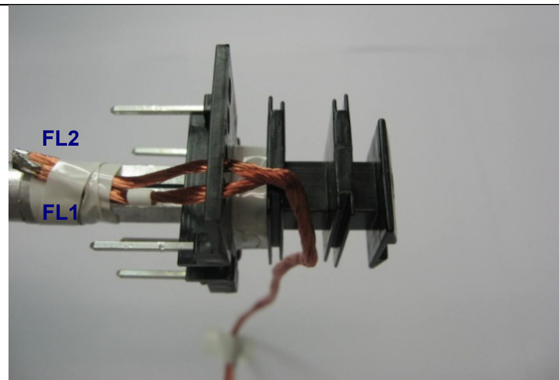
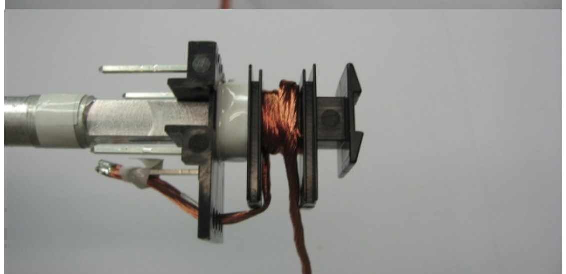
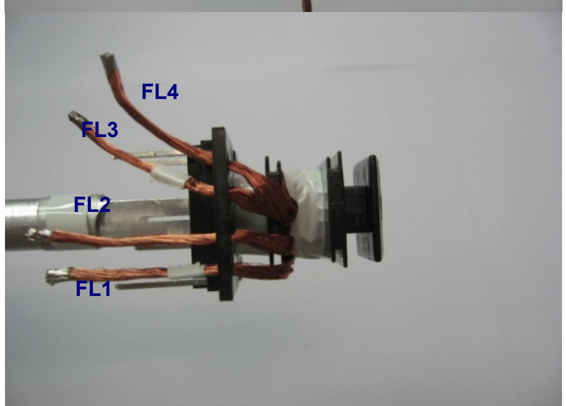
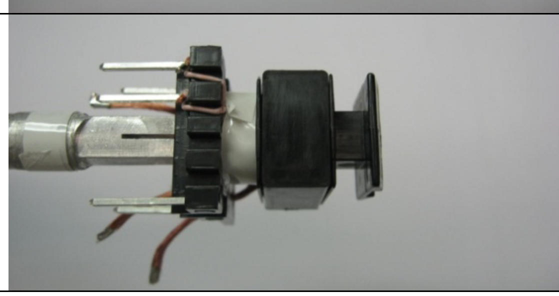
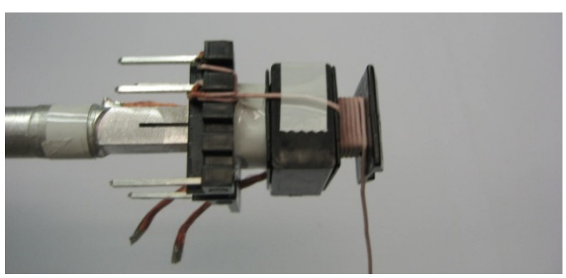
8.6 Winding Illustrations

Secondary Wire Preparation		Make 2 cables of wire item [5] 13” length, tin ends, label one cable to distinguish from other and designate it as FL1, FL2. Other cable will be designated as FL3 and FL4. Twist these 2 cables together ~15 twists evenly along length leaving 1” free at each end. See pictures below.
WD1 (Primary)		Place the bobbin item [2] on the mandrel with pin side on the left side.
WD1 (Primary) (Cont’d)		Starting on pin 1, wind 24 turns of served Litz wire [6] in 5 layers, and finish on pin 2. Secure winding with one turn of tape [4].

WD2A and WD2B (Secondary)	  	Using unserved Litz assembly prepared in step 1, start with FL1 and FL3 inserted into hole 1 and hole 2 of bobbin [2] bottom flange (see illustration). Tightly wind 6 turns in bobbin center chamber. Finish with FL2 in hole 3 of bobbin bottom flange, and FL4 in hole 4. Secure winding with one turn of tape [4].
Bobbin Cover		Slide bobbin cover [3] into grooves in bobbin flanges as shown, with closed end of cover pointed to pin 1-5 side of bobbin, see illustration. Make sure cover is securely seated.
WD 3 (Primary)		Start on pin 2 of bobbin [2], wind 25 turns of served Litz wire [6] in 5 layers, finish on pin 5. Secure and insulate winding start lead using tape [4] per illustration. Secure winding with one turn of tape [4].

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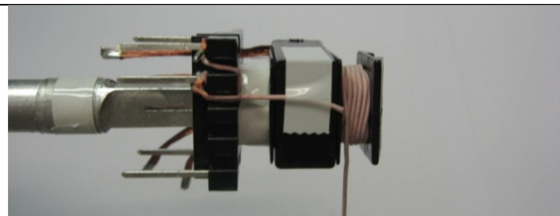
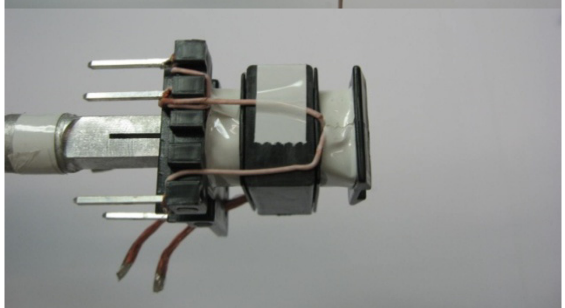
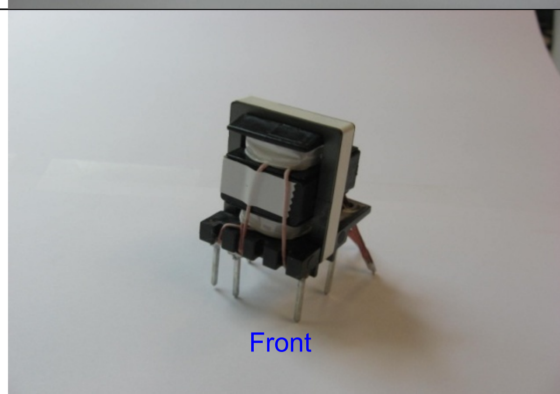
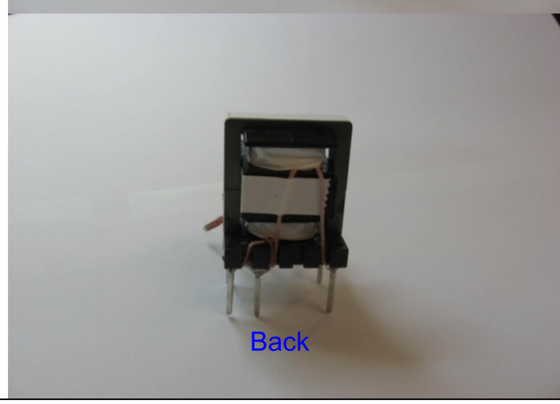
	 	
Finish	 	Grind core halves [1] for inductance of 350 µH ±10%. Assemble and secure core halves. Tin all secondary wires to ~ ¼” from bobbin holes per illustration, and trim to ½”. Dip varnish [7].

9 Output Inductor Specification

9.1 *Electrical Diagram*

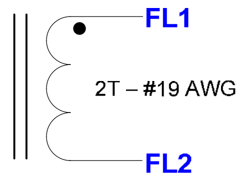


Figure 10 – Inductor Electrical Diagram.

9.2 *Electrical Specifications*

Inductance	Pins FL1-FL2, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	150 nH, ±15%

9.3 *Material List*

Item	Description
[1]	Powdered Iron Toroidal Core: Micrometals T30-26
[2]	Magnet wire: #19 AWG Solderable Double Coated

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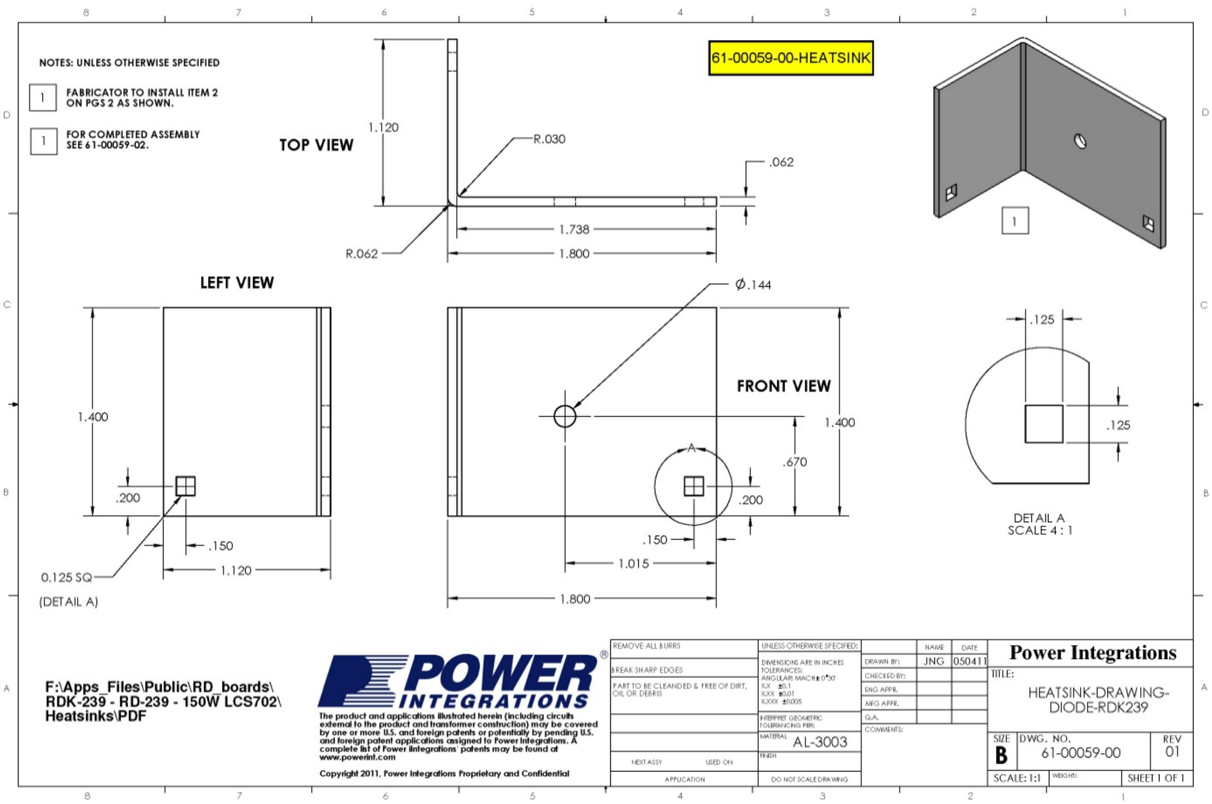
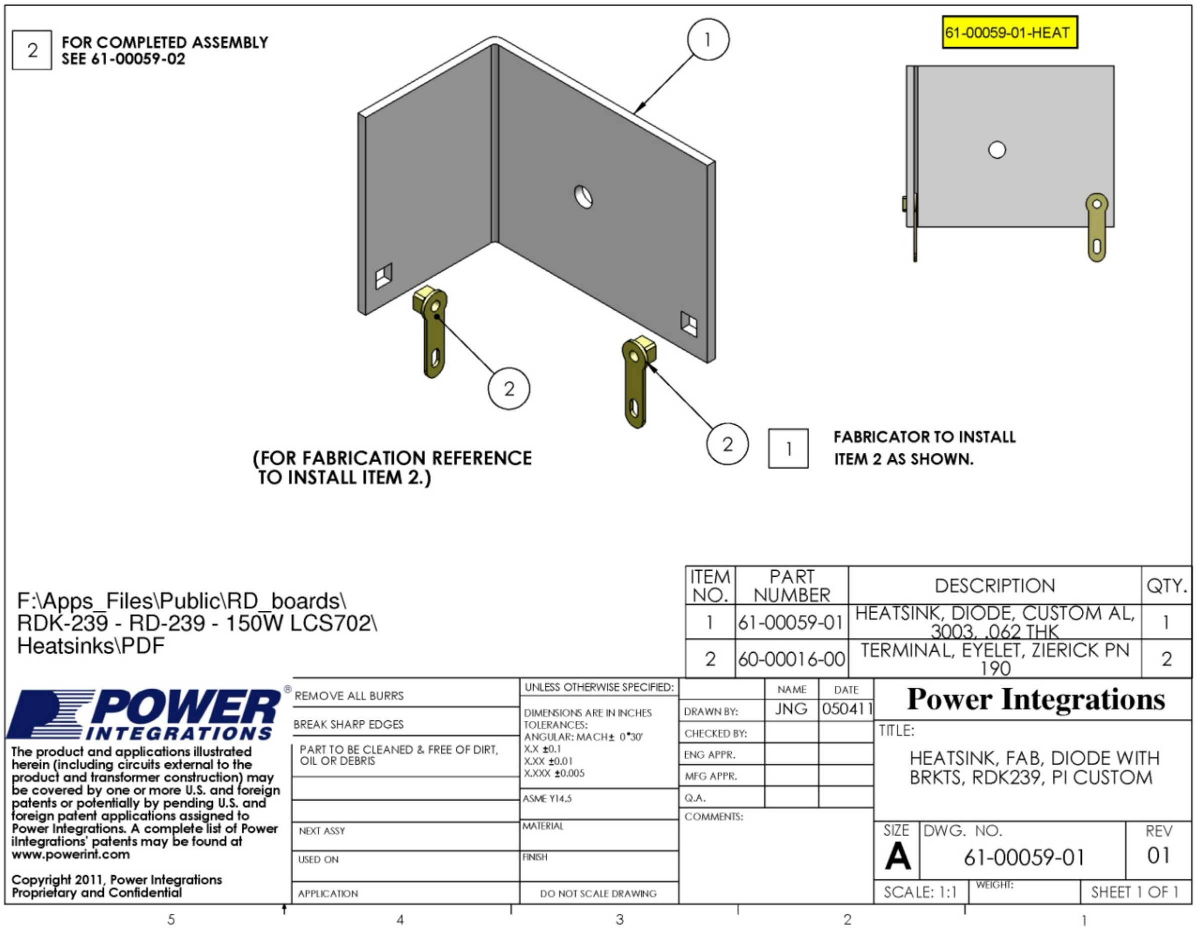
10 Heat Sink Assemblies

10.1 Diode Heat Sink

10.1.1 Diode Heat Sink Drawing



10.1.2 Diode Heat Sink Fabrication Assembly Drawing



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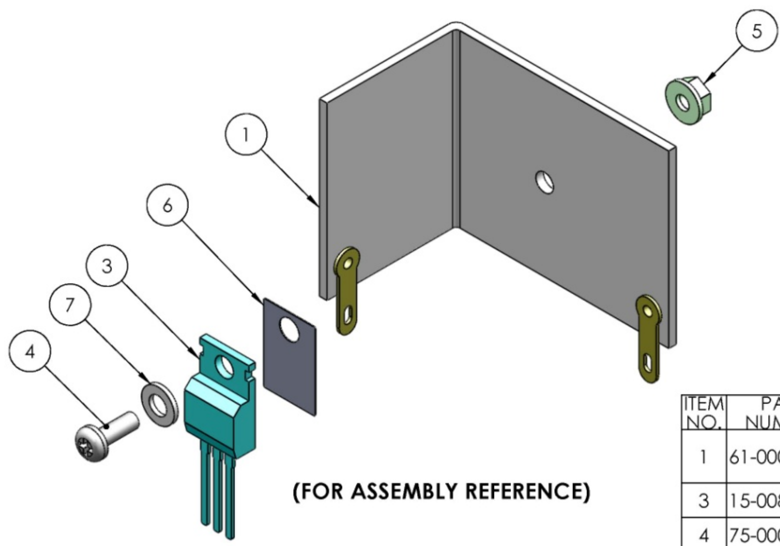
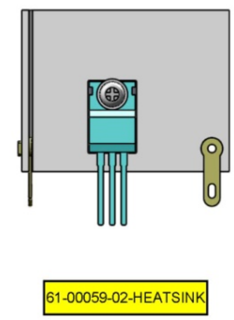
10.1.3 Diode and Heat Sink Assembly Drawing





ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00059-01	HEATSINK, DIODE, CUSTOM AL, 3003, .062 THK	1
3	15-00820-00	60V, 30 A, DUAL SCHOTTKY,TO-220AB	1
4	75-00002-00	SCREW MACHINE PHIL 6-32 X 5/16 SS	1
5	75-00069-00	NUT,HEX,KEP 6-32, ZINC PLATE	1
6	66-00084-00	THERMAL CONDUCTIVE SILICONE GREASE	1
7	75-00167-00	WASHER FLAT #6, SS, ZINC PLATE	1

F:\Apps_Files\Public\RD_boards\
RDK-239 - RD-239 - 150W LCS702\
Heatsinks\PDF

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REMOVE ALL BURRS
BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS
NEXT ASSY
USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGULAR: MACH± 0°30'
X.X ±0.1
X.XX ±0.01
X.XXX ±0.005
ASME Y14.5
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	JNG	050411
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

Power Integrations

TITLE:
HEATSINK, ASSY, DIODE WITH BRKTS, RDK239, PI CUSTOM

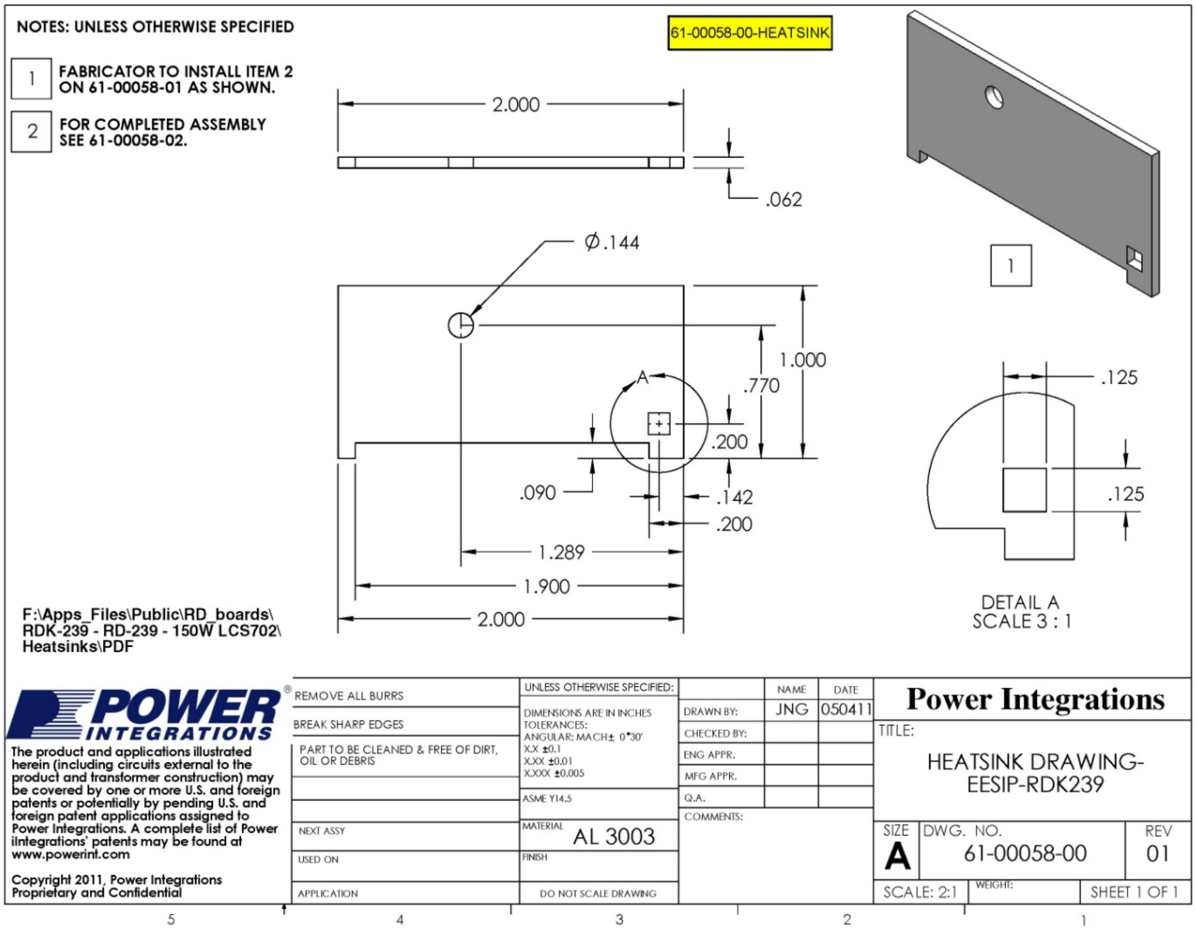
SIZE	DWG. NO.	REV
A	61-00059-02	01

SCALE: 1:2 WEIGHT: SHEET 1 OF 1

5 4 3 2 1

10.2 HiperLCS Heat Sink

10.2.1 HiperLCS Heat Sink Drawing



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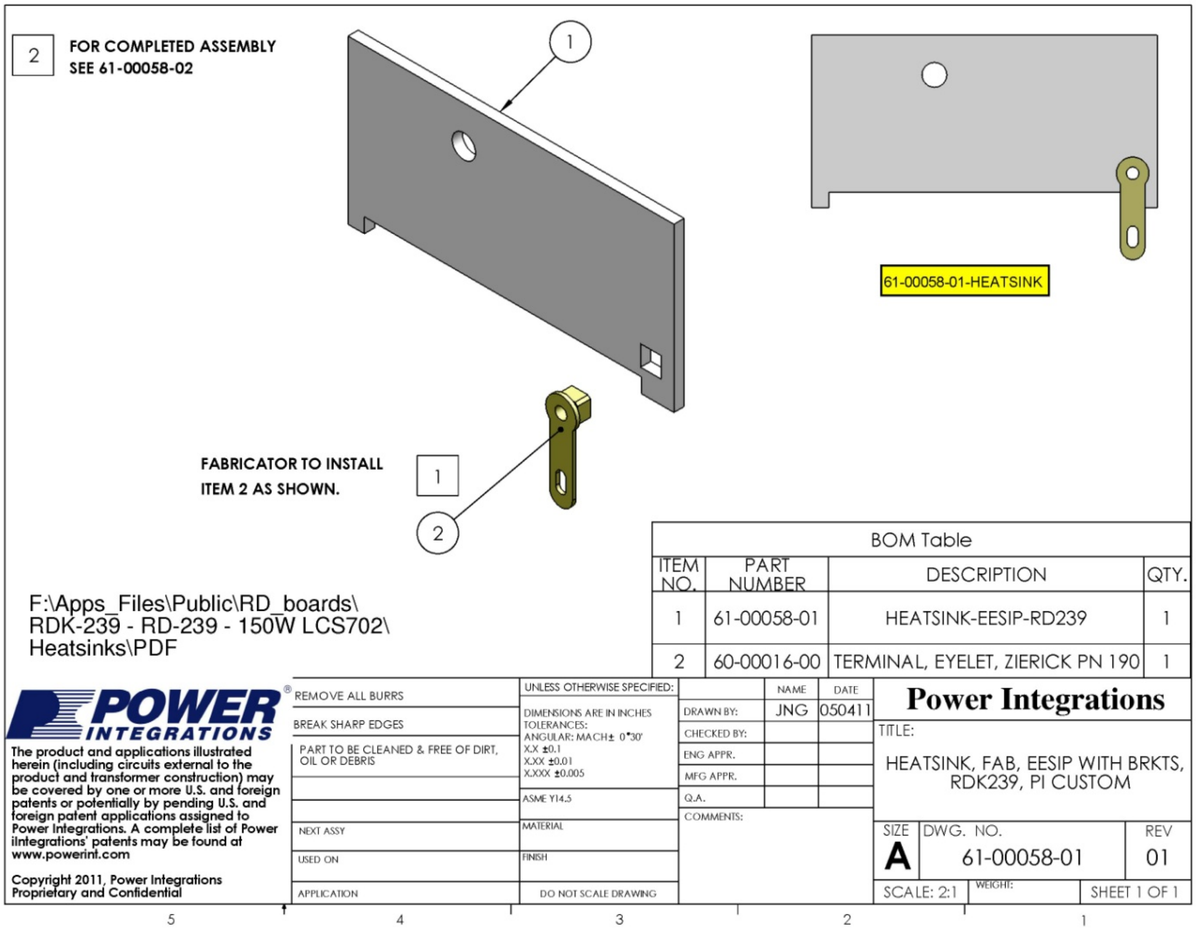
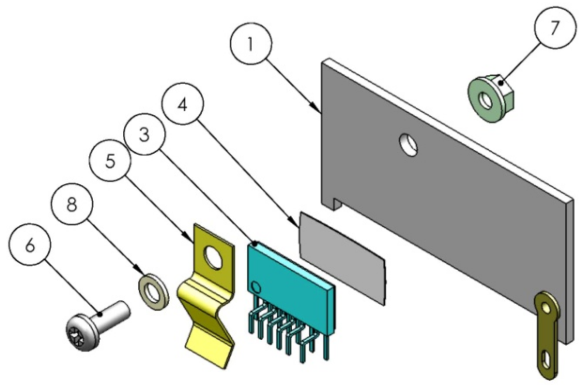
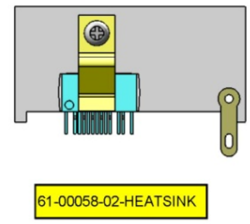
10.2.2 HiperLCS Heat Sink Fabrication Assembly Drawing



10.2.3 HiperLCS and Heat Sink Assembly Drawing





(FOR ASSEMBLY REFERENCE)

ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00058-01	HEATSINK-EESIP-RD239	1
3	10-00342-00	LCSwitch, LCS702HG,ESIP16/13	1
4	66-00084-00	THERMALLY CONDUCTIVE SILICONE GREASE	1
5	60-00042-00	EDGE CLIP, 20.76mm L x 8 mm WX 0.015mm THK	1
6	75-00002-00	SCREW MACHINE PHIL 6-32 X 5/16 SS	1
7	75-00069-00	NUT,HEX,KEP 6-32, ZINC PLATE	1
8	75-00167-00	WASHER FLAT #6, SS, 0.267 OD x 0.143 ID x 0.032 Thk	1

F:\Apps_Files\Public\RD_boards\
RDK-239 - RD-239 - 150W LCS702\
Heatsinks\PDF

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The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power iIntegrations' patents may be found at www.powerint.com

REMOVE ALL BURRS
BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS
NEXT ASSY
USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGULAR: MACH± 0°30'
X.X ±0.1
X.XX ±0.01
X.XXX ±0.005
ASME Y14.5
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	JNG	050411
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

Power Integrations

TITLE:
HEATSINK, ASSY, EESIP WITH BRKTS, RDK239, PI CUSTOM

SIZE	DWG. NO.	REV
A	61-00058-02	01

SCALE: 1:1 WEIGHT: SHEET 1 OF 1

5 4 3 2 1

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11 Performance Data

11.1 Efficiency Curve – 100%, 50%, 20% and 10% Load

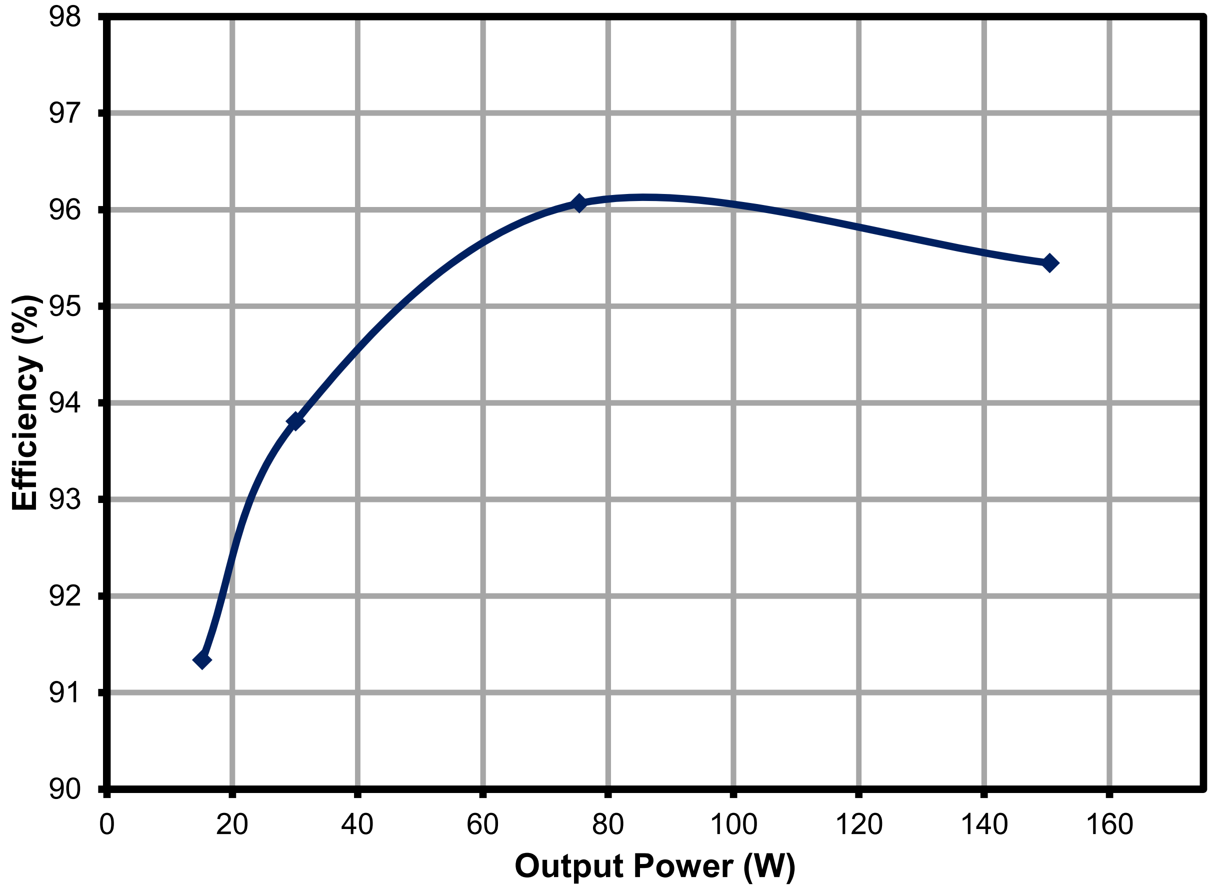

Figure 11 – Efficiency Data.

11.2 Load Regulation Curve – 100%, 50%, 20%, 10% and 0 Load

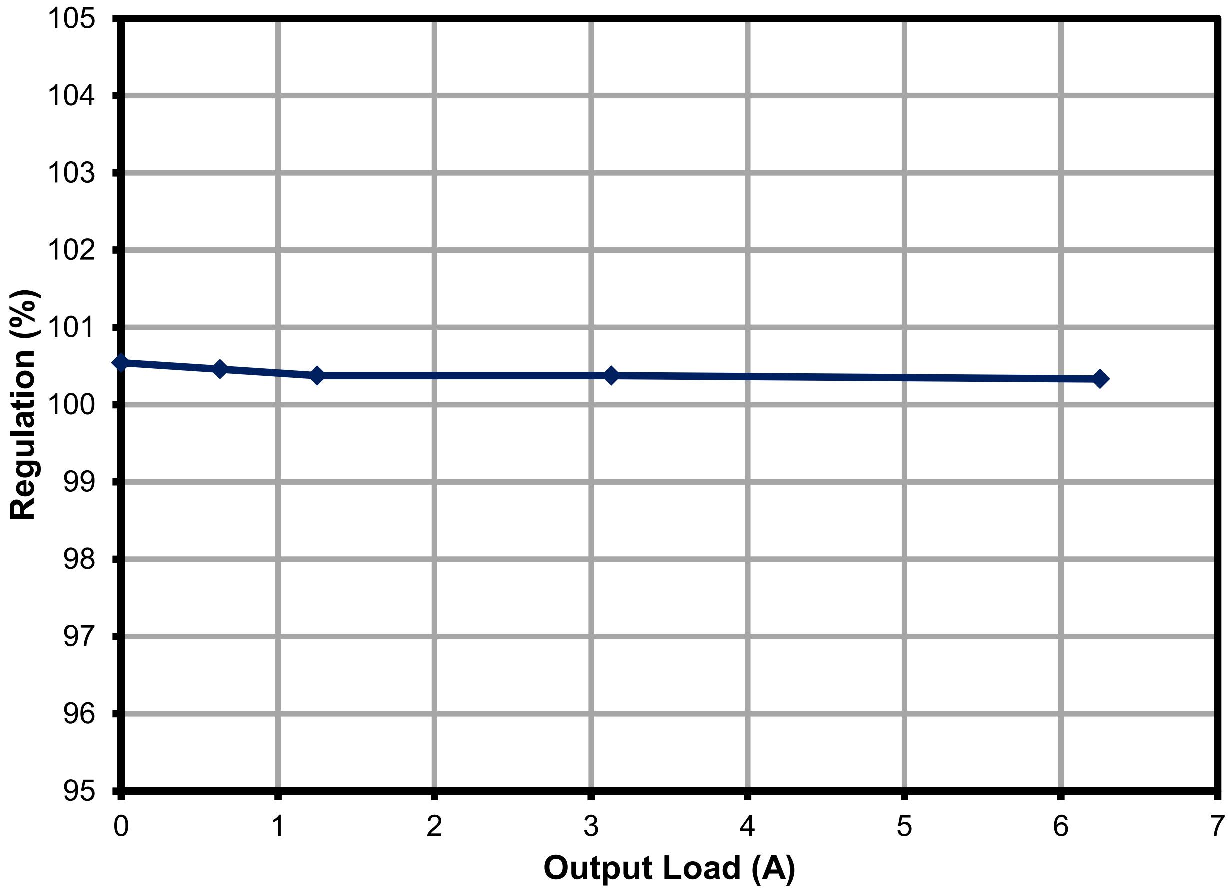

Figure 12 – Output Load Regulation.

11.3 Tabulated Data

V_{IN} (V)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	f_{OP} (kHz)	P_{OUT} (W)	Efficiency (%)	Regulation (%)	V_{TON} (V)	V_{TOFF} (V)
380	157.68	24.08	6.25	245.1	150.500	95.45	100.333	357	283
380	78.49	24.09	3.13	255.1	75.402	96.07	100.375		
380	32.1	24.09	1.25	257.1	30.113	93.81	100.375		
380	16.63	24.11	0.63	260.4	15.189	91.34	100.458		
380	0.42	24.13	0	BM	0.000	0.00	100.542		

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12 Waveforms

12.1 Half-Bridge Voltage and Current, Normal Operation

Measured at 380 VDC input

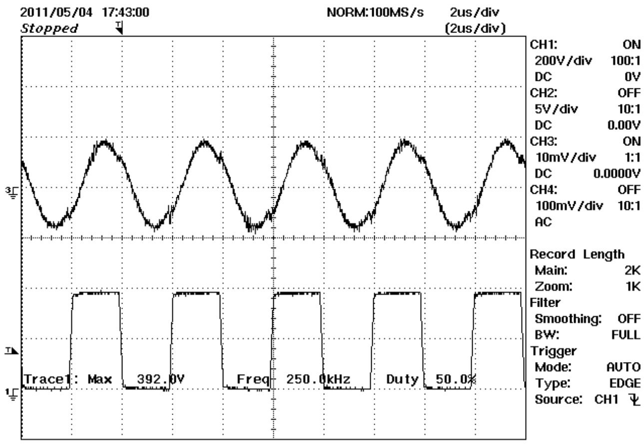

Figure 13 − Primary V-I, Half Load.
Upper: Primary Current, 1 A / div.
Lower: Primary Voltage, 100 V, 2 μs / div.

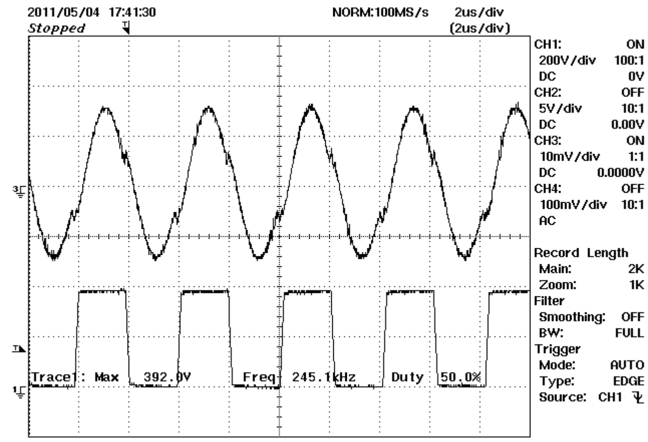

Figure 14 − Primary V-I, Full Load.
Upper: Primary Current, 1 A / div.
Lower: Primary Voltage, 100 V, 2 μs / div.

12.2 Output Voltage Start-Up Profile

Figures 15 and 16 were taken using a passive resistor load.

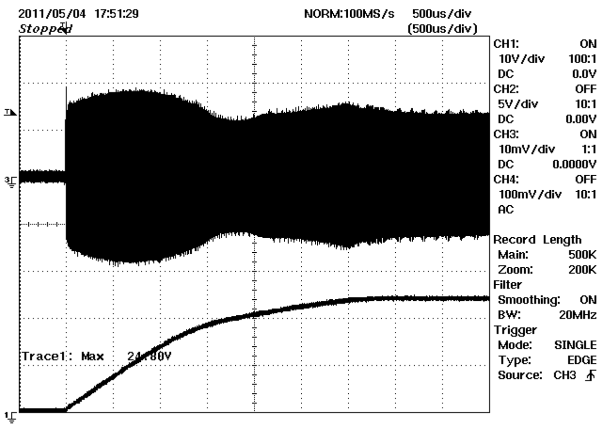

Figure 15 − Full Load Start-up, Resistive Load.
Upper: Primary Current, 2 A / div.
Lower: V_{OUT}, 10 V, 500 µs / div.

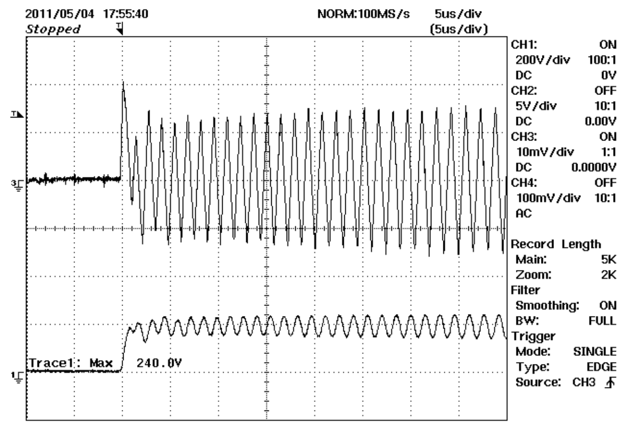

Figure 16 − Full Load Start-up, Resistive Load.
Upper: Primary Current, 2 A / div.
Lower: Resonating Capacitor (C11) Voltage, 200 V, 5 µs / div.

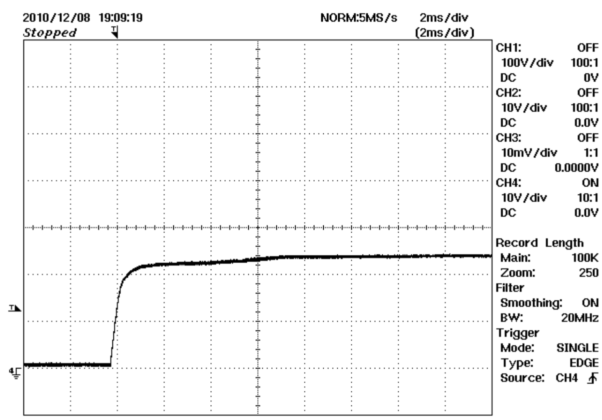

Figure 17 – No-Load Output Voltage at Start-up,
10 V, 2 ms / div.

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12.3 Output Brown-Out

Figures 18 and 19 taken by switching off input voltage supply and triggering oscilloscope on rise of primary current.

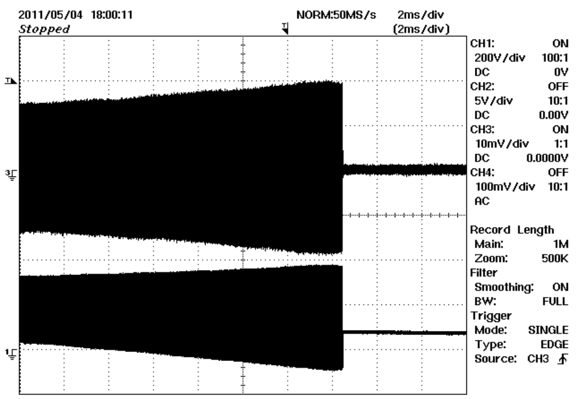

Figure 18 − Output Brown-Out.
Upper: Primary Current, 2 A / div.
Lower: Primary Voltage,
200 V, 2 ms / div.

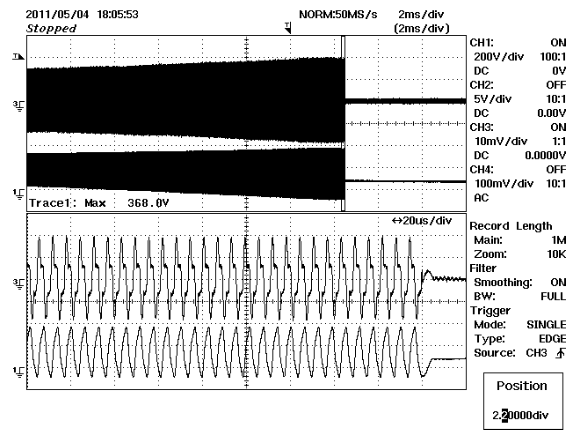

Figure 19 − Output Brown-Out, Magnified View.
Upper: Primary Current, 2 A / div.
Lower: Resonating Capacitor Voltage,
200 V, 20 μs / div.

12.4 Output Overload

Figure 20 obtained by increasing output load up until primary overcurrent is triggered and supply goes into auto restart.

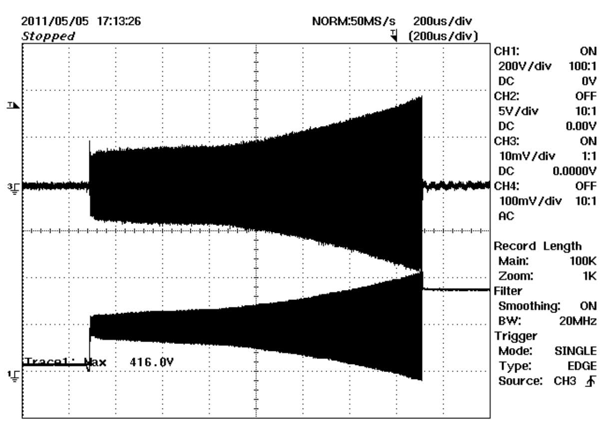

Figure 20 − Output Overload.
Upper: Primary Current, 2 A / div.
Lower: Resonating Capacitor Voltage,
200 V, 200 μs / div.

12.5 Output Diode Peak Reverse Voltage

The following waveforms were measured at full load and 380/420 VDC input.

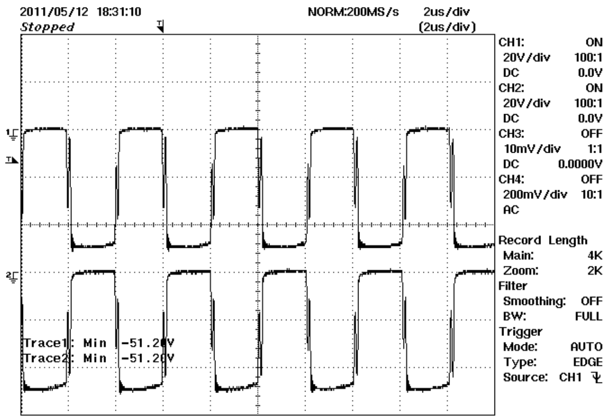

Figure 21 – Output Diode Peak Reverse Voltage, 380 VDC Input, 20 V, 2 μs / div.

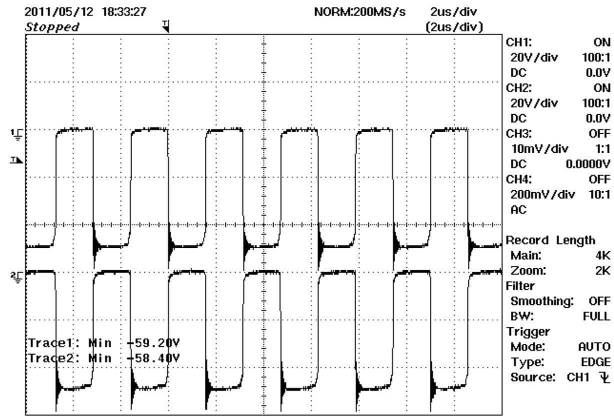

Figure 22 – Output Diode Peak Reverse Voltage, 420 VDC Input, 20 V, 2 μs / div.

12.6 Short-Circuit

For tests shown below, the supply output was shorted with a mercury displacement relay (no contact bounce and very low impedance) at 150 W load, 380 VDC input. The oscilloscope was set to trigger on current rise.

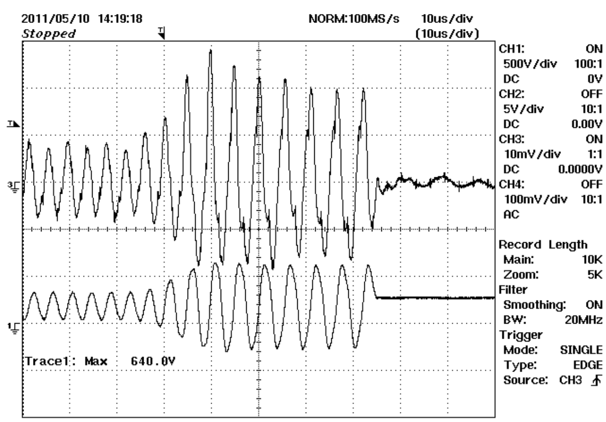

Figure 23 − Primary Waveforms During Output Short-Circuit.
Upper: Primary Current, 2 A / div.
Lower: Resonating Cap Voltage, 500 V, 10 μs / div.

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12.7 Load Step Response, 380 VDC Input

In the figures shown below, the oscilloscope was triggered using the load current step as a trigger source. In Figure 24, signal averaging mode was used to separate the power supply step response signal from the output ripple.

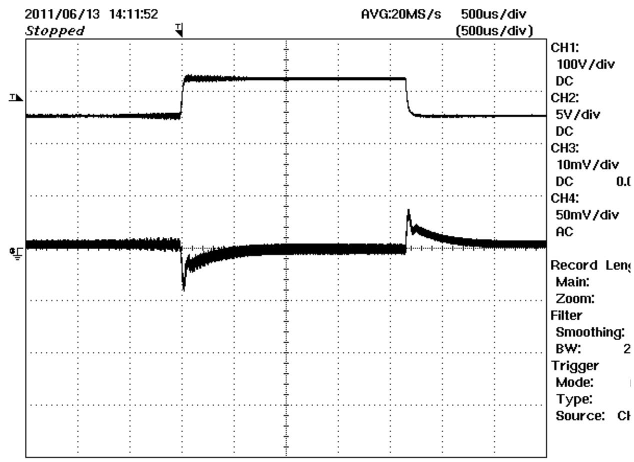

Figure 24 − Transient Response, 75%-100%-75% Load Step.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 50 mV, 500 μs / div.

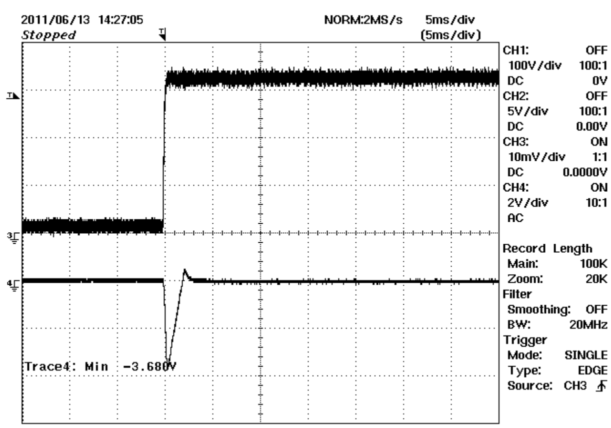

Figure 25 − Load Step, 0-100% Load, 380 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 2 V, 5 ms / div.

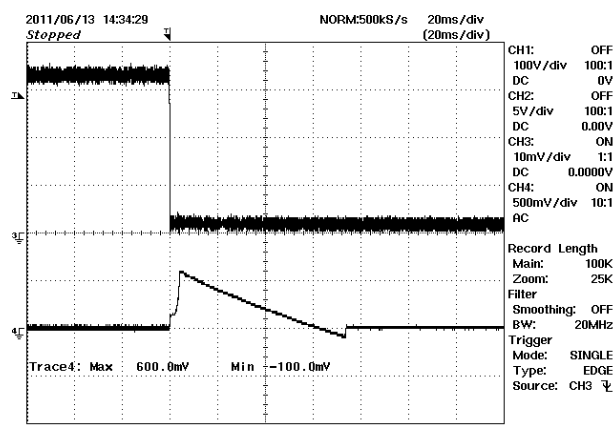

Figure 26 − Load Step, 100%-0 Load, 380 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 500 mV, 20 ms / div.

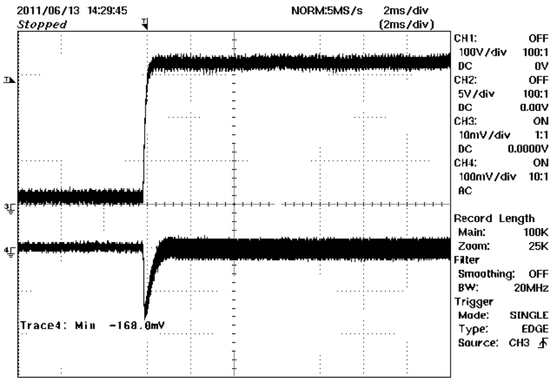

Figure 27 – Load Step, 20 mA-100% Load, 380 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

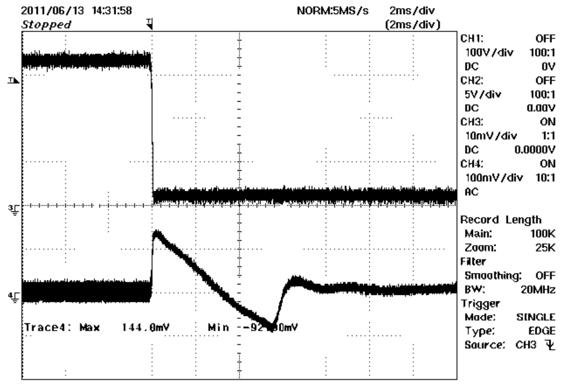

Figure 28 – Load Step, 100%-20 mA Load, 380 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

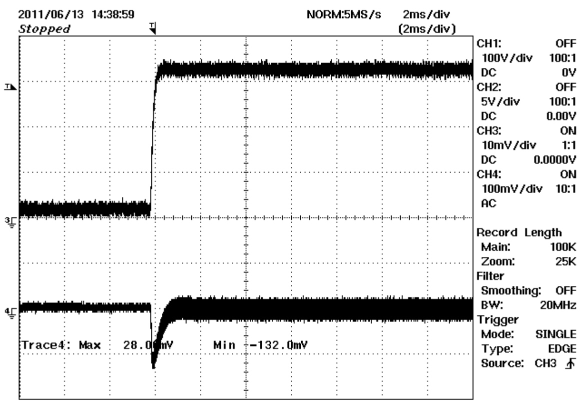

Figure 29 – Load Step, 1%-100% Load, 380 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

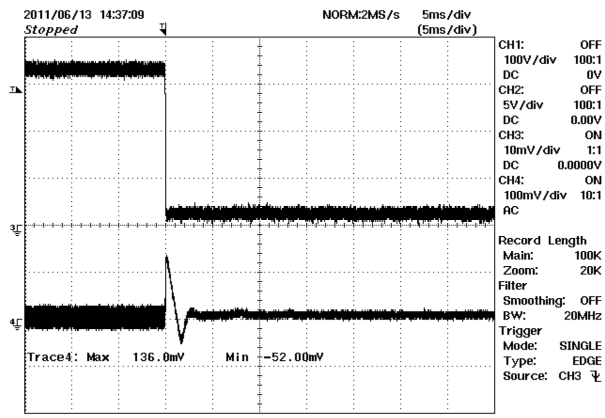

Figure 30 – Load Step, 100%-1% Load, 380 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 5 ms / div.

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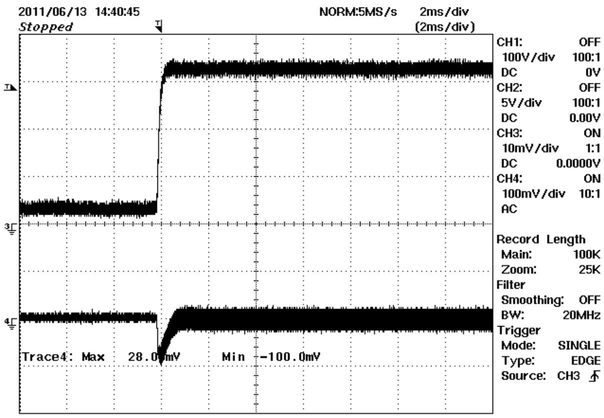

Figure 31 − Load Step, 5%-100% Load, 380 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

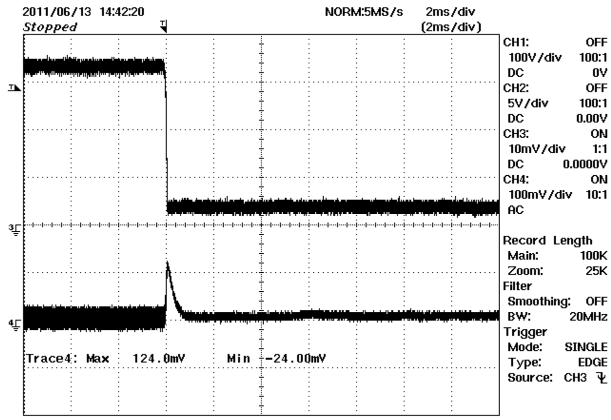

Figure 32 − Load Step, 100%-5% Load, 380 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

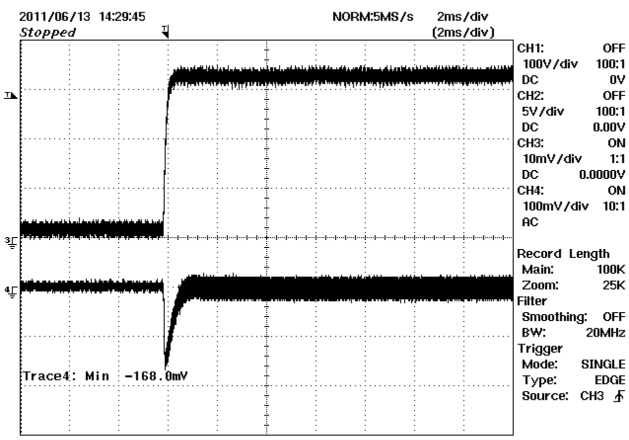

Figure 33 − Load Step, 10%-100% Load, 380 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

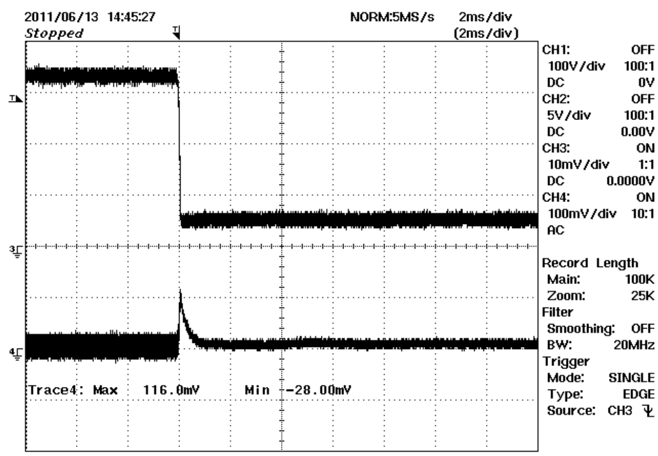

Figure 34 − Load Step, 100%-10% Load, 380 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

12.8 Load Step Response, 400 VDC Input

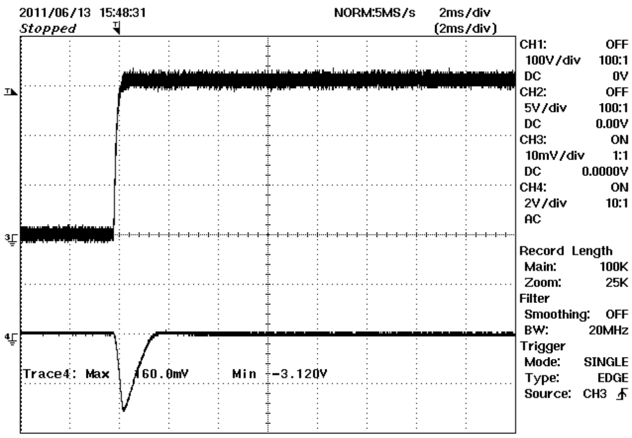

Figure 35 − Load Step, 0-100% Load, 400 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 2 V, 2 ms / div.

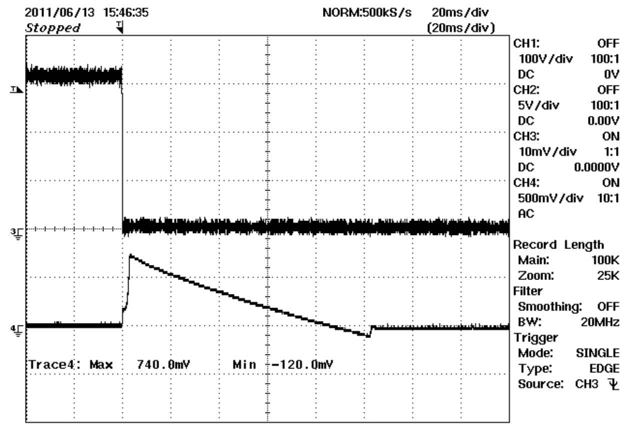

Figure 36 − Load Step, 100%-0 Load, 400 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 500 mV, 20 ms / div.

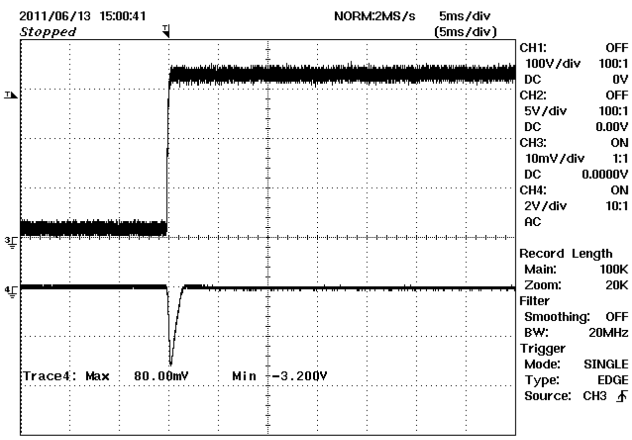

Figure 37 − Load Step, 20 mA-100% Load, 400 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 2 V, 5 ms / div.

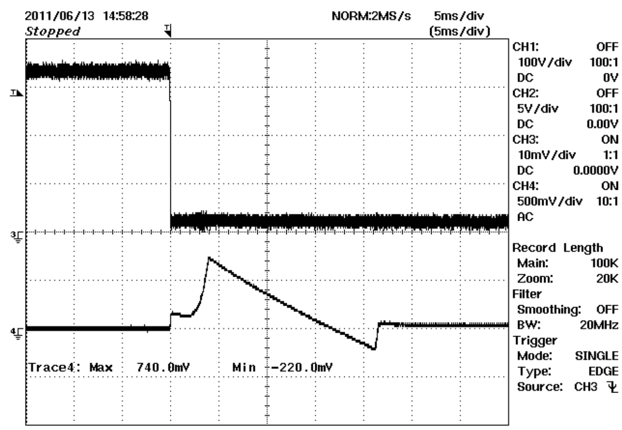

Figure 38 − Load Step, 100%-20 mA Load, 400 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 500 mV, 5 ms / div.

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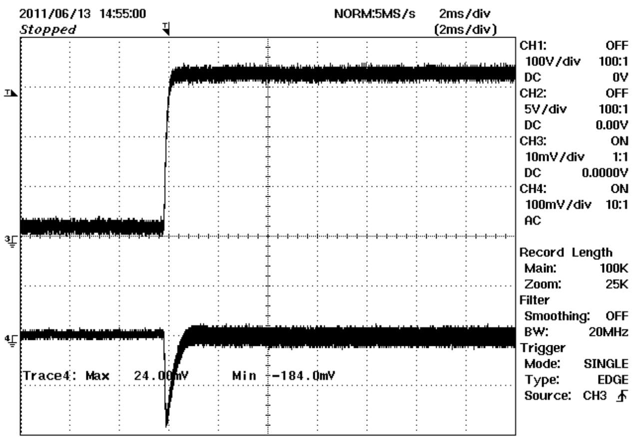

Figure 39 − Load Step, 1%-100% Load, 400 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

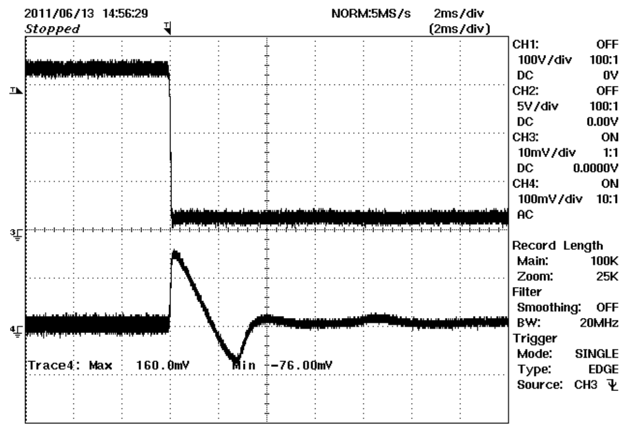

Figure 40 − Load Step, 100%-1% Load, 400 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

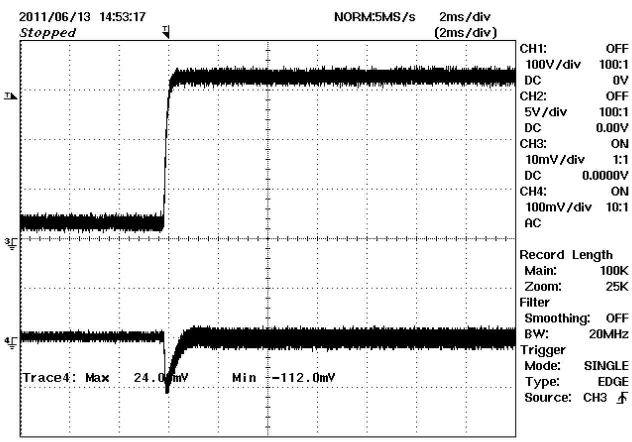

Figure 41 − Load Step, 5%-100% Load, 400 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

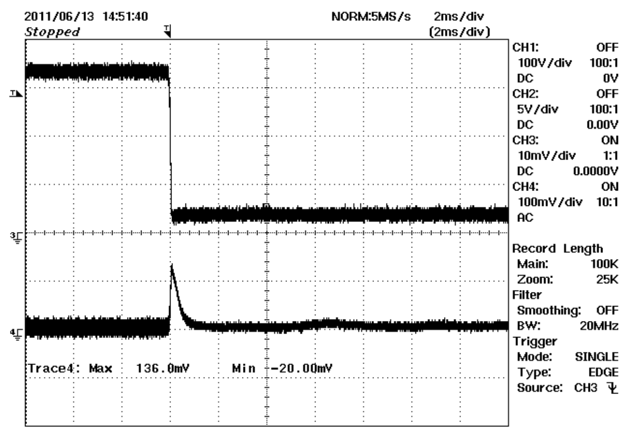

Figure 42 − Load Step, 100%-5% Load, 400 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

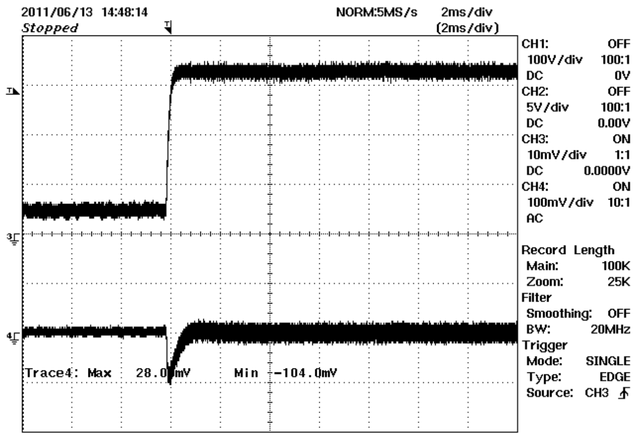

Figure 43 − Load Step, 10%-100% Load, 400 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

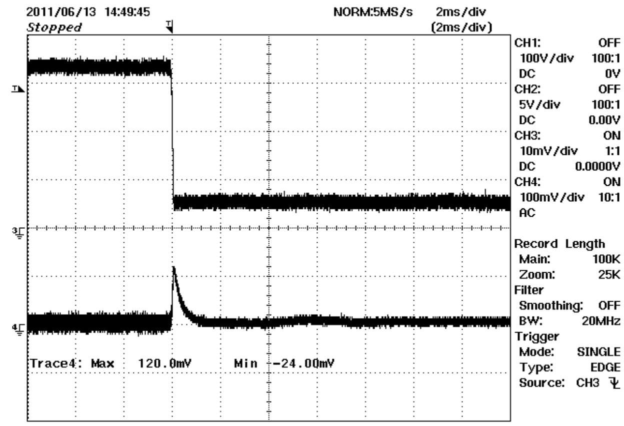

Figure 44 − Load Step, 100%-10% Load, 400 V Input.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT}, 100 mV, 2 ms / div.

12.9 Output Ripple Measurements

12.9.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to noise pickup. Details of the probe modification are provided in the figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

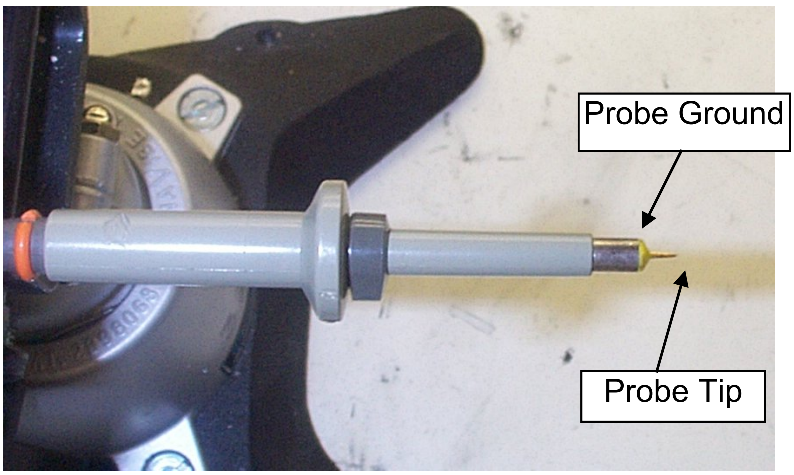

Figure 45 − Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

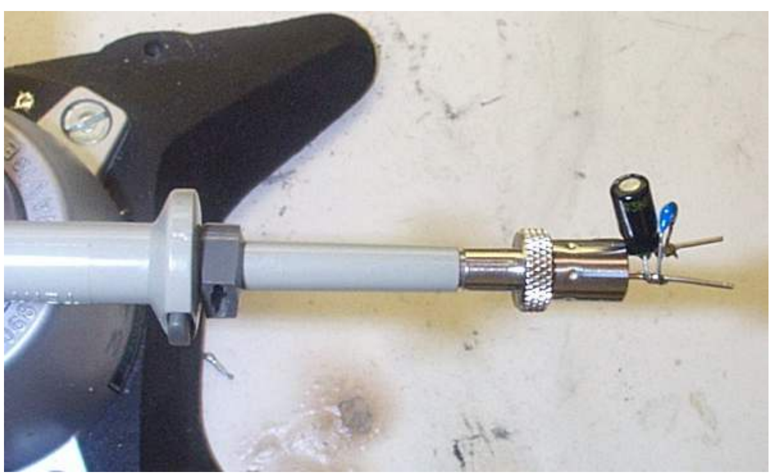

Figure 46 − Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with Wires for Ripple Measurement, and Two Parallel Decoupling Capacitors added)

12.9.2 Output Ripple Measurement Results

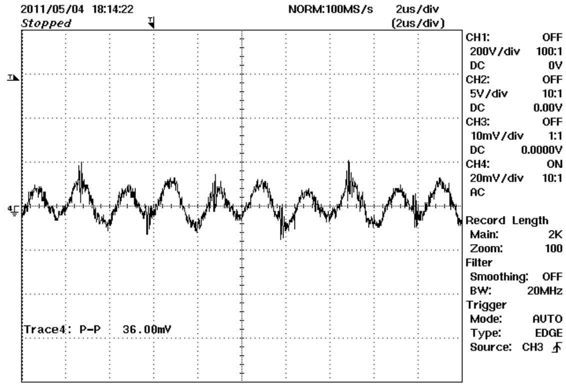

Figure 47 − Ripple, 380 VDC Input, 100% Load.
Upper: Output Ripple Voltage,
20 mV / div, 2 μs / div.

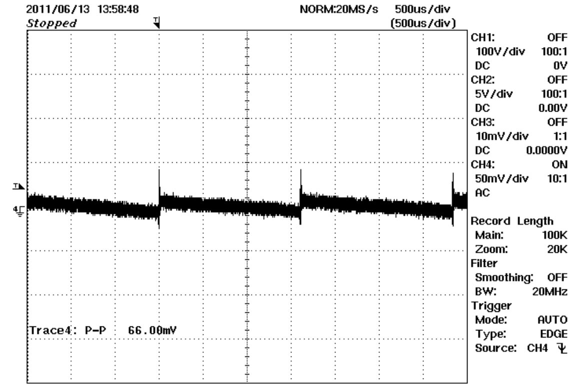

Figure 48 − Ripple, 400 VDC Input, No Load.
Upper: Output Ripple Voltage,
50 mV / div. 500 μs / div.
Power Supply is in Burst Mode.

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13 Temperature Measurements

13.1 Conditions: 380 VDC, Full Load, 1 Hour Soak

Figure 49 – Visible Light Transformer Front View.

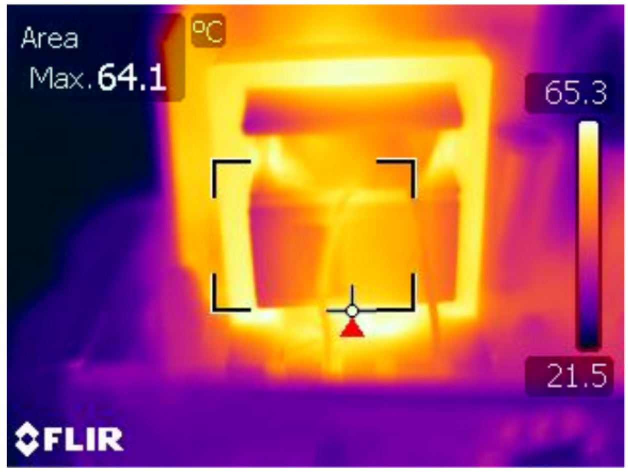

Figure 50 – Full Load Transformer Thermal Front View, Room Temperature.

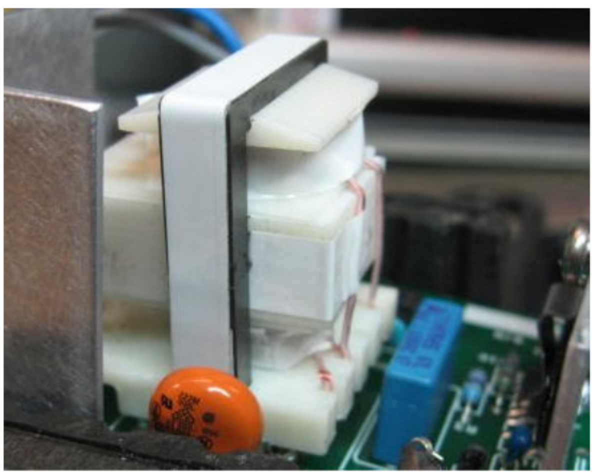

Figure 51 – Visible Light Transformer Side View.

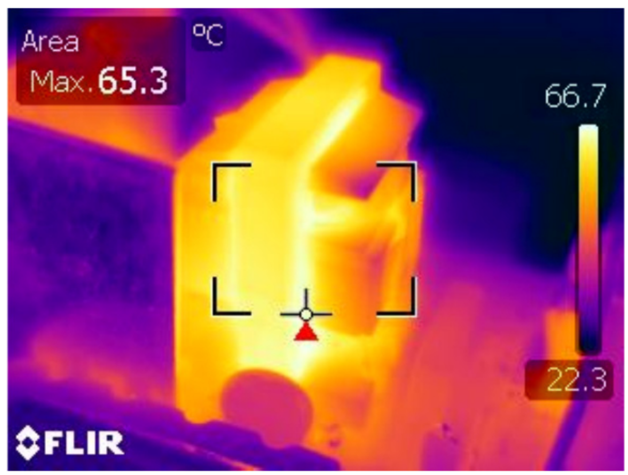

Figure 52 – Full load Transformer Thermal Side View, Room Temperature.

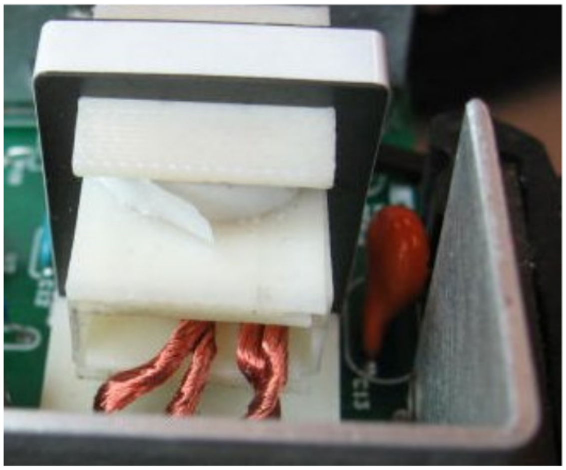

Figure 53 – Visible Light Transformer Back View.

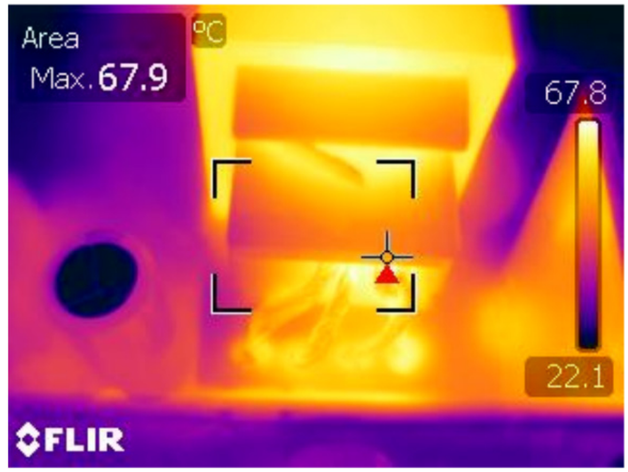

Figure 54 – Full Load Transformer Thermal Back View, Room Temperature.

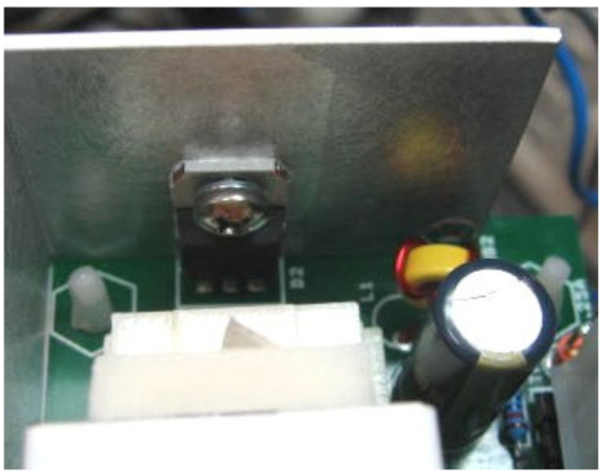

Figure 55 – Visible Light Output Rectifier Front View.

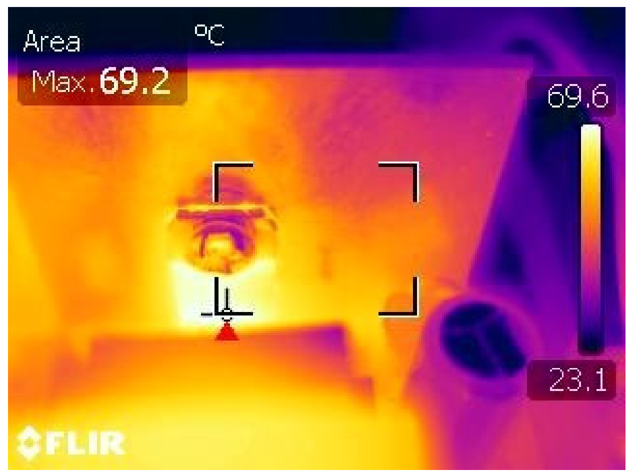

Figure 56 – Full Load Output Rectifier Thermal View, Room Temperature.

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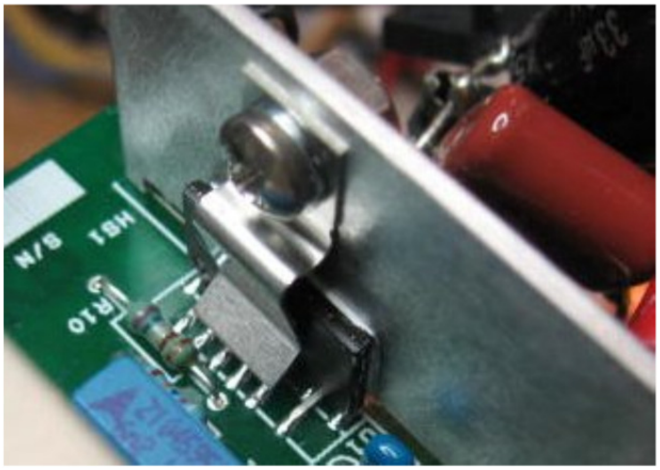

Figure 57 – Visible Light HiperLCS Front View.

Figure 58 – Full Load HiperLCS Thermal View, Room Temperature.

14 Gain-Phase Plot

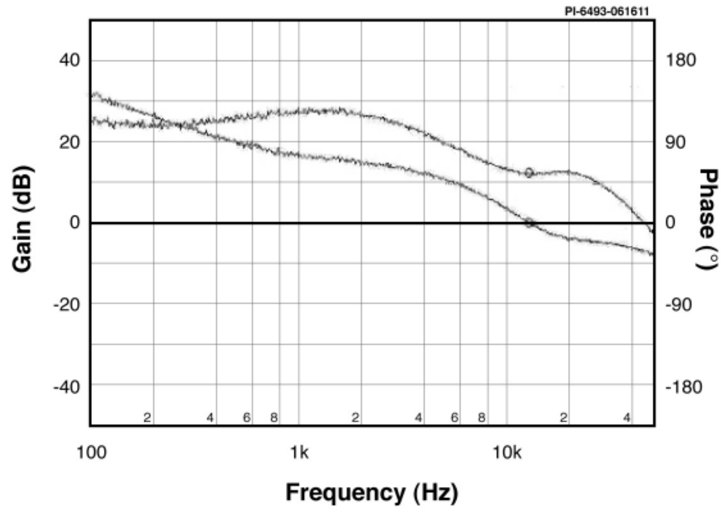

Figure 59 – Gain-Phase, 0.06 V Excitation. Gain Crossover 12.9 kHz, Phase Margin 57 Degrees**.**

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15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
13-Sep-11	RH	1.0	Initial Release	Apps & Mktg

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