Adjustable Frequency Buck or Buck-Boost Pre-Regulator with Synchronous Buck, 3 Internal LDOs, Watchdog Timer, NPOR, and FF0/FF1

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- 2.8 to 36 V_{IN} operating range, 40 V_{IN} maximum
- Buck or buck-boost pre-regulator (VREG)
- Adjustable PWM switching frequency: 250 kHz to 2.4 MHz
- PWM frequency can be synchronized to external clock
- Adjustable synchronous buck regulator (1.25 V_{NOM})
- 3.3V (3V3) and 5V (V5) internal LDO regulators with foldback short-circuit protections
- 5V (V5P) internal tracking LDO regulator with foldback short-circuit and short-to-battery protections
- TRACK sets either 3V3 or V5 as the reference for V5P
- Power-on reset (NPOR) with fixed delay of 15 ms
- Programmable watchdog timer with activation delay
- Active-low watchdog timer enable pin (WD_{ENn})
- Dual bandgaps for increased reliability: BG_{VREF}, BG_{FAULT}
- MODE pin sets the NPOR undervoltage threshold for V5 and V5P
- Fixed POK5V undervoltage threshold for V5 and V5P
- Logic enable input (ENB) for microprocessor control
- Two ignition enable inputs (ENBAT1 and ENBAT2)

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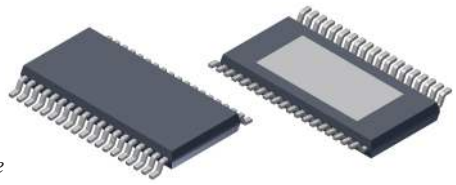
APPLICATIONS

- □ Electronic Power Steering (EPS)
- □ Transmission Control Units (TCU)
- □ Advanced Braking Systems (ABS)
- □ Emissions Control Modules
- □ Other automotive applications

PACKAGE: 38-Pin eTSSOP (suffix LV)



Not to scale

DESCRIPTION

The A4408 is power management IC that uses a buck or buck-boost pre-regulator to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage, complete with control, diagnostics, and protections. The output of the pre-regulator supplies a 5 V / 115 mA_{MAX} tracking/protected LDO, a 3.3 V / 165 mA_{MAX} LDO, a 5 V / 325 mA_{MAX} LDO, and an adjustable output synchronous buck regulator (1.25 V_{TYP} / 700 mA_{DC}). Designed to supply CAN or microprocessor power supplies in high-temperature environments, the A4408 is ideal for underhood applications.

Enable inputs to the A4408 include a logic-level (ENB) and two high-voltage (ENBAT1 and ENBAT2) inputs. The A4408 provides flexibility by including a TRACK pin to set the reference of the tracking regulator to either the 5 V or the 3.3 V output, so the A4408 can be adapted across multiple platforms with different sensors and supply rails. The MODE pin selects the NPOR undervoltage threshold for the V5 and V5P outputs.

Diagnostic outputs from the A4408 include a power-on-reset output (NPOR). POK5V indicates the status of the 5 V and 5 V protected LDOs. Fault Flag 0 (FF0) and Fault Flag 1 (FF1) retain the last fault to reset the microcontroller. Dual bandgaps, one for regulation and one for fault checking, improve long-term reliability of the A4408.

The A4408 contains a watchdog timer that can be programmed to accept a wide range of clock frequencies (WD_{ADJ}). The watchdog timer has a fixed activation delay to accommodate processor startup. The watchdog timer has an enable/disable pin (active low, WD_{ENn}) to facilitate initial factory programming or field reflash programming.

Protection features include under- and overvoltage lockout on all four CPU supply rails. In case of a shorted output, all linear regulators feature foldback overcurrent protection. In addition,

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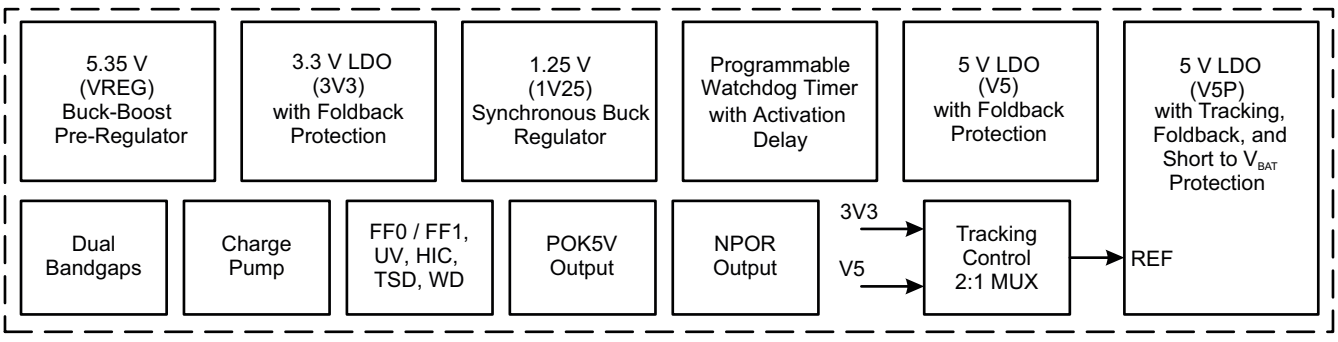


Figure 1: A4408 Simplified Block Diagram

FEATURES AND BENEFITS (continued)

- FF0, FF1 Fault Flags—last microcontroller RESET indicators
- Slew rate control pin helps reduce EMI/EMC
- Frequency dithering helps reduce EMI/EMC
- Overvoltage and undervoltage protection for all four CPU supply rails
- Pin-to-pin and pin-to-ground tolerant at every pin
- Thermal shutdown protection
- −40°C to 150°C junction temperature range

DESCRIPTION (continued)

the V5P output is protected from a short-to-battery event. Both switching regulators include pulse-by-pulse current limit, hiccup mode short-circuit protection, LX short-circuit protection, missing asynchronous diode protection (VREG), and thermal shutdown.

The A4408 is supplied in a low profile (1.2 mm maximum height) 38-lead eTSSOP package (suffix “LV”) with exposed thermal pad.

SELECTION GUIDE

Part Number	Package	Packing [1]	Lead Frame
A4408KLVTR-T	38-pin eTSSOP with thermal pad	4000 pieces per 7-inch reel	100% matte tin

[1] Contact Allegro for additional packing options.

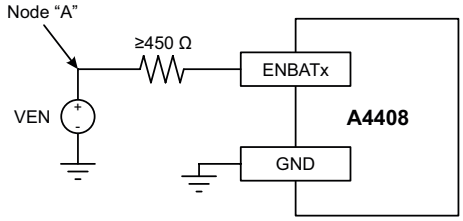
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN	V_{VIN}		−0.3 to 40	V
ENBAT1, ENBAT2	V_{ENBATx}	With current limiting resistor [3]	−13 to 40	V
			−0.3 to 8	V
	I_{ENBATx}		±75	mA
LX1, SLEW			−0.3 to V_{VIN} + 0.3	V
		t < 250 ns	−1.5	V
		t < 50 ns	V_{VIN} + 3 V	V
VCP, CP1, CP2			−0.3 to 50	V
V5P	V_{V5P}	Independent of V_{VIN}	−1 to 40	V
All other pins			−0.3 to 7	V
Junction Temperature	T_J		−40 to 150	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

[3] The higher ENBAT1 and ENBAT2 ratings (–13 V and 40 V) are measured at node “A” in the following circuit configuration:



THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [4]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	eTSSOP-38 (LV) Package	30	°C/W

[4] Additional thermal information available on the Allegro website.

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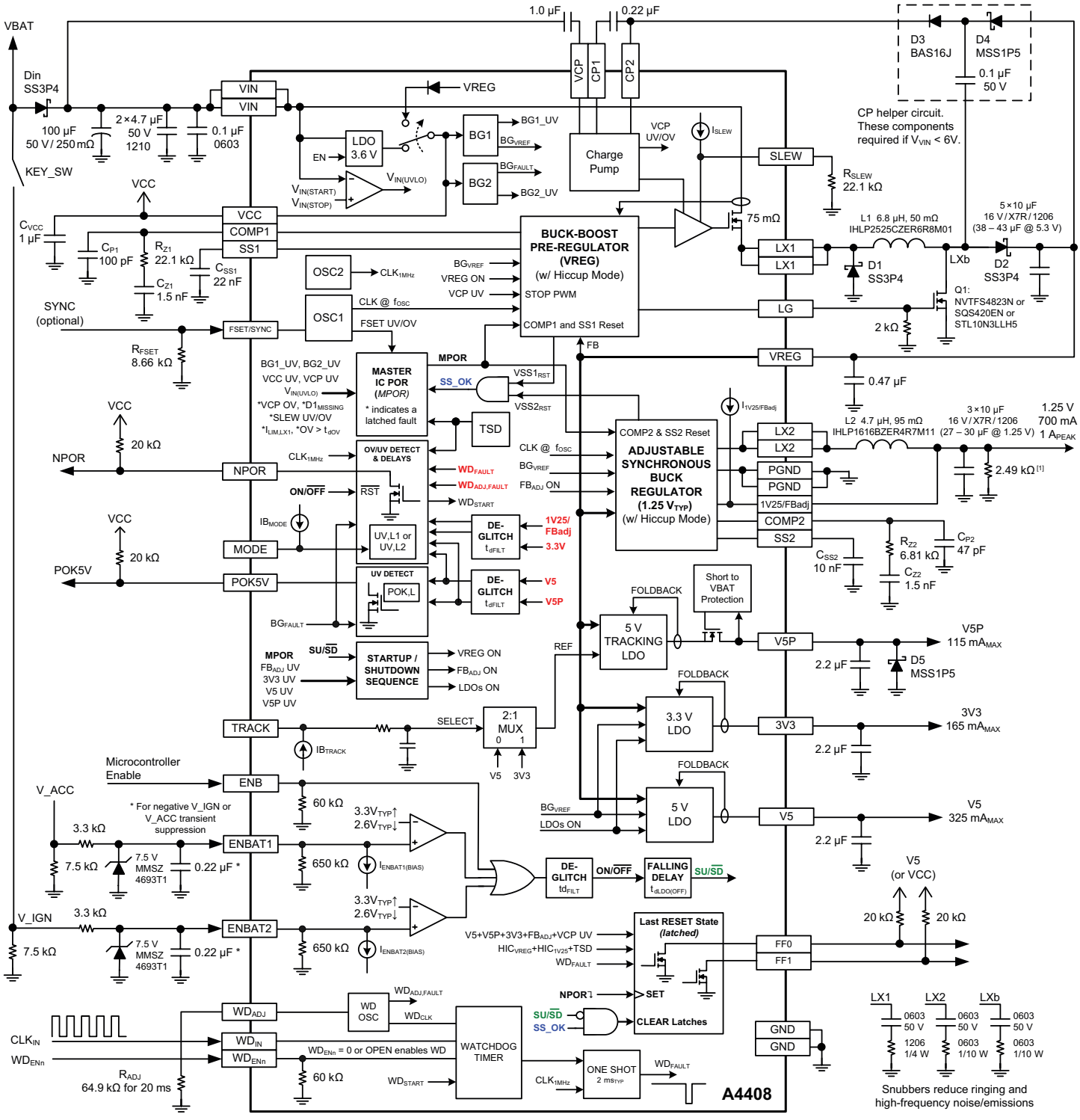

Figure 2: Functional Block Diagram/Typical Schematic

Buck-Boost Mode (f_{OSC} = 2 MHz)

[1] For optimal no-load operation.

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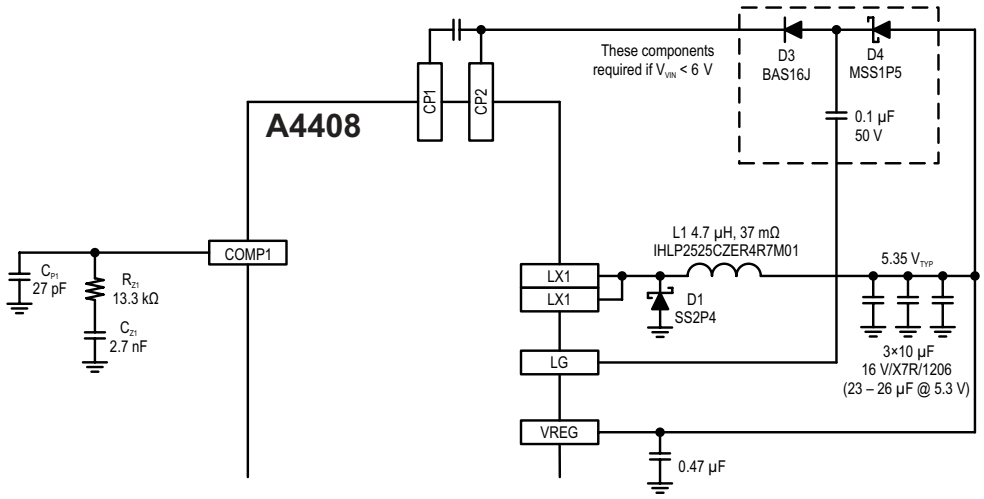

Figure 3: Functional Block Diagram Modifications for Buck Only Mode, f_{OSC} = 2 MHz

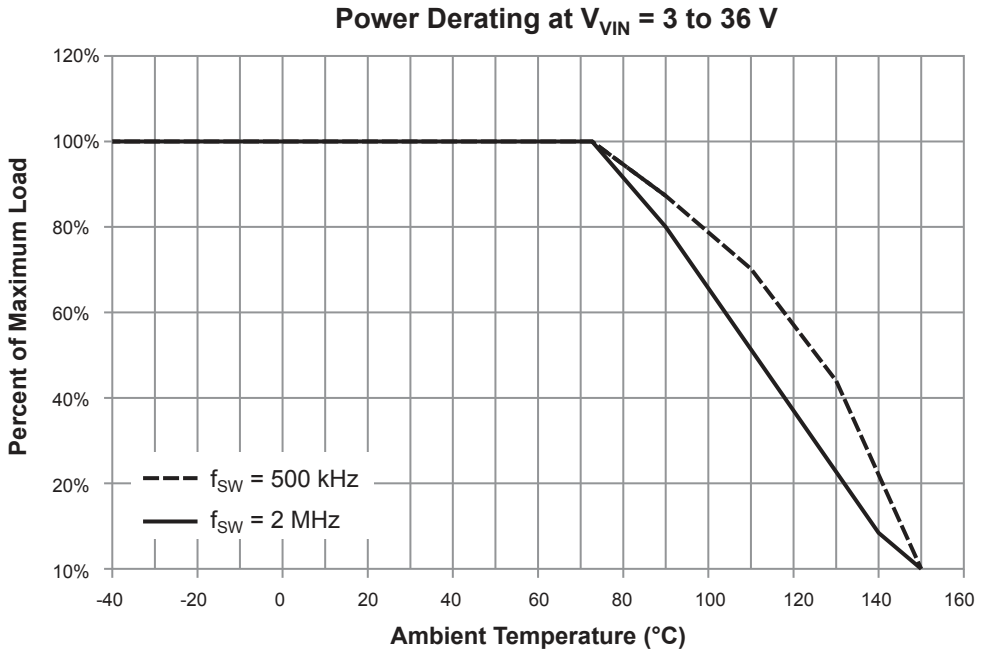

Figure 4: Thermal Derating for Buck-Boost Operation Down to 3 V

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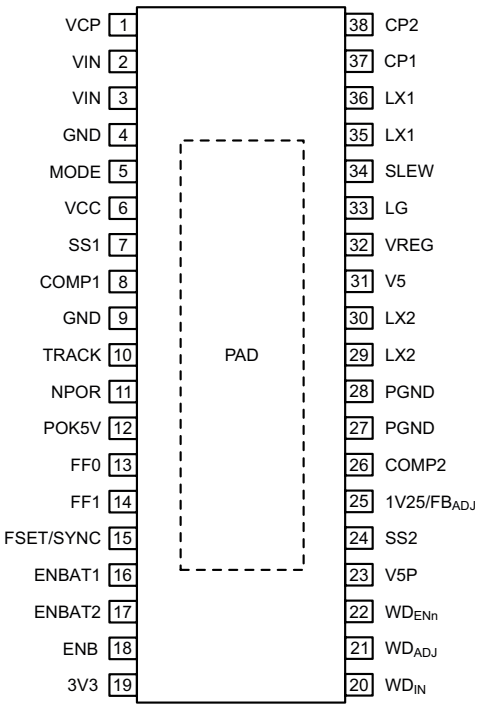

Package LV, 38-Pin eTSSOP Pinout Diagram

Terminal List Table

Number	Name	Function
1	VCP	Charge pump reservoir capacitor
2, 3	VIN	Input voltage
4, 9	GND	Ground
5	MODE	Sets UV threshold for V5/V5P in NPOR logic. MODE pin does not affect POK5V threshold. GND/low–$NPOR_{UV}$ is set high at $V_{V5x(UV,L1)}$. Open/high–$NPOR_{UV}$ is set low at $V_{V5x(UV,L2)}$.
6	VCC	Internal voltage regulator bypass capacitor pin
7	SS1	Soft-start programming pin for buck-boost pre-regulator
8	COMP1	Error amplifier compensation network pin for buck-boost pre-regulator
10	TRACK	Tracking control: Open/High – V5P tracks 3V3, GND/Low – V5P tracks V5
11	NPOR	Active-low, open-drain regulator fault detection output
12	POK5V	Power OK output indicating when either V5 or V5P rail is undervoltage (UV). $POK5V_{UV}$ threshold is always at $V_{V5x(POK,L)}$.
13, 14	FF0, FF1	Open-drain, latched Fault Flag (FFx) outputs indicate last type of fault to reset microcontroller. FF0 and FF1 bits are only valid if NPOR has first transitioned high. FF0 and FF1 latches are reset when all A4408 enable inputs are low and soft-start voltages have decayed below reset thresholds. See Table 2 for more details.
15	FSET/ SYNC	Frequency setting and synchronization input
16	ENBAT1	Ignition enable input from key/switch via 1 kΩ of resistance
17	ENBAT2	Ignition enable input from key/switch via 1 kΩ of resistance
18	ENB	Logic enable input from microcontroller
19	3V3	3.3 V regulator output
20	WDIN	Watchdog refresh input (rising edge triggered) from microcontroller or DSP
21	WDADJ	Watchdog wait/delay time is programmed by connecting R_{ADJ} from this pin to ground
22	WDENn	Watchdog enable pin: Open/Low – WD is enabled, High – WD is disabled
23	V5P	5 V tracking/protected regulator output
24	SS2	Soft-start programming pin for adjustable synchronous buck regulator
25	1V25/ FBadj	Feedback pin for 1.25 V (or adjustable) synchronous buck regulator
26	COMP2	Error amplifier compensation network pin for 1.25 V synchronous regulator
27, 28	PGND	Power ground for adjustable synchronous regulator and its gate driver
29, 30	LX2	Switching node for adjustable synchronous buck regulator
31	V5	5 V regulator output
32	VREG	Output of buck-boost and input for LDOs and adjustable synchronous buck regulator
33	LG	Boost gate drive output for buck-boost pre-regulator
34	SLEW	Slew rate adjustment for rise time of LX1
35, 36	LX1	Switching node for buck-boost pre-regulator
37, 38	CP1, CP2	Charge pump capacitor connections
–	PAD	Exposed thermal pad

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Valid at 3.6 V [2] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage	V_{VIN}	After V_{VIN} > $V_{VIN(START)}$, and V_{ENB} > 2 V or V_{ENBATx} > 3.5 V, Buck-Boost Mode	2.8	13.5	36	V
		After V_{VIN} > $V_{VIN(START)}$, and V_{ENB} > 2 V or V_{ENBATx} > 3.5 V, Buck Mode	5.7	13.5	36	V
VIN UVLO START Voltage	$V_{VIN(START)}$	V_{VIN} rising	5.1	5.4	5.7	V
VIN UVLO STOP Voltage	$V_{VIN(STOP)}$	V_{VIN} falling	2.53	2.64	2.78	V
VIN UVLO Hysteresis	$V_{VIN(HYS)}$	$V_{VIN(START)}$ – $V_{VIN(STOP)}$	–	2.7	–	V
Supply Quiescent Current [1]	I_Q	V_{VIN} = 13.5 V, V_{ENBATx} ≥ 3.6 V or V_{ENB} ≥ 2 V, V_{VREG} = 5.6 V (no PWM)	–	13	–	mA
	$I_{Q(SLEEP)}$	V_{VIN} = 13.5 V, V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V	–	–	10	µA
PWM SWITCHING FREQUENCY AND DITHERING						
Oscillator Frequency	f_{OSC}	R_{FSET} = 8.66 kΩ	1.8	2.0	2.2	MHz
		R_{FSET} = 19.1 kΩ [3]	–	1.0	–	MHz
		R_{FSET} = 52.3 kΩ [3]	343	400	457	kHz
PWM Switching Frequency Foldback Thresholds	f_{SW}	V_{VREG} > 2.7 V, V_{VIN} rising, f_{OSC} → f_{OSC}/2	18.7	19.5	20.3	V
		V_{REG} > 2.7 V, V_{VIN} falling, f_{OSC}/2 → f_{OSC}	–	18.5	–	V
		V_{REG} > 2.7 V, V_{VIN} rising, f_{OSC}/2 → f_{OSC}	–	7.5	–	V
		V_{REG} > 2.7 V, V_{VIN} falling, f_{OSC} → f_{OSC}/2	6.7	7.0	7.4	V
Frequency Dithering	Δf_{OSC}	As a percent of f_{OSC}	–	±12	–	%
Dither/Slew Start Threshold	$V_{IN(DS,ON)}$		8.5	9.0	9.5	V
Dither/Slew Stop Threshold	$V_{IN(DS,OFF)}$		7.8	8.3	8.8	V
VIN Dithering/Slew Hysteresis	$V_{IN(DS,HYS)}$		–	700	–	mV
CHARGE PUMP (VCP)						
Output Voltage	V_{VCP}	V_{VCP} – V_{VIN}, V_{VIN} = 13.5 V, V_{VREG} = 5.5 V, I_{VCP} = 6.5 mA, V_{COMP1} = V_{COMP2} = 0 V, V_{ENB} = 3.3 V	4.1	6.6	–	V
		V_{VCP} – V_{VIN}, V_{VIN} = 6.5 V, V_{VREG} = 5.5 V, I_{VCP} = 6.5 mA, V_{COMP1} = V_{COMP2} = 0 V, V_{ENB} = 3.3 V	3.6	4.4	–	V
Switching Frequency	$f_{SW(CP)}$		–	65	–	kHz
VCC PIN VOLTAGE						
Output Voltage	V_{VCC}	V_{VREG} = 5.35 V	–	4.65	–	V
THERMAL PROTECTION						
Thermal Shutdown Threshold [3]	T_{TSD}	T_J rising	155	170	185	°C
Thermal Shutdown Hysteresis [3]	T_{HYS}		–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{CP(UV,H)}$ and V_{VREG} > $V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.
[3] Ensured by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS – BUCK AND BUCK-BOOST PRE-REGULATOR (continued) [1]:

Valid at 3.6 V [2] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE SPECIFICATIONS						
Buck Output Voltage – Regulating	V_{VREG}	V_{VIN} = 13.5 V, ENB = 1, 0.1 A < I_{VREG} < 1.25 A	5.25	5.35	5.45	V
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWM1OFFS}$	V_{COMP1} for 0% duty cycle	–	400	–	mV
LX1 Rising Slew Rate Control [3]	$LX1_{RISE}$	V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A, R_{SLEW} = 22.1 kΩ	–	0.9	–	V/ns
		V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A, R_{SLEW} = 150 kΩ	–	0.3	–	V/ns
LX1 Falling Slew Rate [3]	$LX1_{FALL}$	V_{VIN} = 13.5 V, 90% to 10%, I_{VREG} = 1 A	–	1.5	–	V/ns
Buck Minimum On-Time	$t_{ON(MIN,BUCK)}$		–	85	160	ns
Buck Maximum Duty Cycle	$D_{MAX(BUCK)}$		–	100	–	%
Boost Duty Cycle (LG Pin)	$D_{MIN(BST)}$ [3]	After V_{VIN} > $V_{VIN(START)}$, V_{VIN} = 6.5 V	–	20	–	%
	$D_{MAX(BST)}$	After V_{VIN} > $V_{VIN(START)}$, V_{VIN} = 3.5 V	53	61	66	%
COMP1 to LX1 Current Gain	gm_{POWER1}		–	4.5	–	A/V
Slope Compensation [3]	S_{E1}	f_{OSC} = 2 MHz	1.04	1.48	1.92	A/µs
		f_{OSC} = 400 kHz	0.22	0.33	0.44	A/µs
INTERNAL MOSFET						
MOSFET On-Resistance	R_{DSon}	V_{VIN} = 13.5 V, T_J = –40°C [3], I_{DS} = 0.1 A	–	50	65	mΩ
		V_{VIN} = 13.5 V, T_J = 25°C [4], I_{DS} = 0.1 A	–	75	90	mΩ
		V_{VIN} = 13.5 V, T_J = 150°C, I_{DS} = 0.1 A	–	150	180	mΩ
MOSFET Leakage	$I_{FET(LKG)}$	V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, V_{LX1} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 85°C [4]	–	–	10	µA
		V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, V_{LX1} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 150°C	–	50	150	µA
ERROR AMPLIFIER						
Open-Loop Voltage Gain [3]	A_{VOL1}		–	60	–	dB
Transconductance	gm_{EA1}	V_{SS1} = 750 mV	550	750	950	µA/V
		V_{SS1} = 500 mV	275	375	500	µA/V
Output Current	I_{EA1}		–	±75	–	µA
Maximum Output Voltage	$V_{EA1VO(max)}$		1.3	1.7	2.1	V
Minimum Output Voltage	$V_{EA1VO(min)}$		–	–	300	mV
COMP1 Pull-Down Resistance	R_{COMP1}	HICCUP1 = 1 or FAULT1 = 1 or V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, latched until V_{SS1} < $V_{SS1(RST)}$	–	1	–	kΩ

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{CP(UV,H)}$ and V_{VREG} > $V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.
[3] Ensured by design and characterization, not production tested.
[4] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

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Valid at 3.6V < V_{VIN} < 36 V [2], –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
BOOST MOSFET (LG) GATE DRIVER						
LG High Output Voltage	$V_{LG(ON)}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V	4.6	–	5.5	V
LG Low Output Voltage	$V_{LG(OFF)}$	V_{VIN} = 13.5 V, V_{VREG} = 5.35 V	–	0.2	0.4	V
LG Source Current [1]	$I_{LG(ON)}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	–	−300	–	mA
LG Sink Current [1]	$I_{LG(OFF)}$	V_{VIN} = 13.5 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	–	150	–	mA
SOFT-START						
SS1 Offset Voltage	$V_{SS1(OFFS)}$	V_{SS1} rising due to $I_{SS1(SU)}$	–	400	–	mV
SS1 Fault/Hiccup Reset Voltage	$V_{SS1(RST)}$	V_{SS1} falling due to HICCUP1 = 1 or FAULT1 = 1 or V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V	140	200	275	mV
SS1 Startup (Source) Current	$I_{SS1(SU)}$	V_{SS1} = 1 V, HICCUP1 = FAULT1 = 0	−10	−20	−30	µA
SS1 Hiccup (Sink) Current	$I_{SS1(HIC)}$	V_{SS1} = 0.5 V, HICCUP1 = 1	5	10	15	µA
SS1 Delay Time [3]	$t_{SS1(DLY)}$	C_{SS1} = 22 nF	–	440	–	µs
SS1 Ramp Time [3]	t_{SS1}	C_{SS1} = 22 nF	–	880	–	µs
SS1 Pull-Down Resistance	$R_{PD(SS1)}$	FAULT1 = 1 or IC disabled, latched until V_{SS1} < $V_{SS1(RST)}$	–	3	–	kΩ
SS1 PWM Frequency Foldback	$f_{SW1(SS)}$	0 V < V_{VREG} < 1.3 V_{TYP}, V_{COMP1} = $V_{EA1VO(max)}$	–	f_{OSC}/8	–	–
		0 V < V_{VREG} < 1.3 V_{TYP}, V_{COMP1} < $V_{EA1VO(max)}$	–	f_{OSC}/4	–	–
		1.3 V_{TYP} < V_{VREG} < 2.7 V_{TYP}	–	f_{OSC}/2	–	–
		V_{VREG} > 2.7 V_{TYP}	–	f_{OSC}	–	–
HICCUP MODE						
Hiccup1 OCP PWM Counts	$t_{HIC1(OCP)}$	V_{SS1} > $V_{HIC1(EN)}$, V_{VREG} < 1.3 V_{TYP}, V_{COMP1} = $V_{EA1VO(max)}$	–	30	–	PWM cycles
		V_{SS1} > $V_{HIC1(EN)}$, V_{VREG} > 1.3 V_{TYP}, V_{COMP1} = $V_{EA1VO(max)}$	–	120	–	PWM cycles
CURRENT PROTECTIONS						
Pulse-by-Pulse Current Limit	$I_{LIM1(ton,min)}$	V_{VIN} < 7.0 V, t_{ON} = $t_{ON(MIN)}$	4.1	4.6	5.1	A
		V_{VIN} > 7.0 V, t_{ON} = $t_{ON(MIN)}$	2.5	2.8	3.3	A
LX1 Short-Circuit Current Limit	$I_{LIM(LX1)}$	Latched fault	6.0	7.0	–	A
MISSING ASYNCHRONOUS DIODE (D1) PROTECTION						
Detection Level	$V_{D(OPEN)}$		−1.9	−1.5	−1.0	V
Time Filtering [3]	$t_{D(OPEN)}$		50	–	250	ns

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{CP(UV,H)}$ and V_{VREG} > $V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.
[3] Ensured by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS – ADJUSTABLE SYNCHRONOUS BUCK REGULATOR [1]:

Valid at 3.6 V [2] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
FEEDBACK REFERENCE VOLTAGE						
Feedback Voltage Accuracy	$V_{1V25/FBadj}$	50 mA < I_{1V25} < 700 mA	1.23	1.25	1.27	V
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWM2(OFFS)}$	V_{COMP2} for 0% duty cycle	–	350	–	mV
High-Side MOSFET Minimum On-Time	$t_{ON(MIN)}$		–	65	105	ns
High-Side MOSFET Minimum Off-Time	$t_{OFF(MIN)}$	Does not include total gate driver non-overlap time, t_{NO}	–	100	125	ns
Gate Driver Non-Overlap Time [3]	t_{NO}		–	15	–	ns
COMP2 to LX2 Current Gain	gm_{POWER2}		–	3.7	–	A/V
Slope Compensation [3]	S_{E2}	f_{OSC} = 2 MHz	0.45	0.63	0.81	A/µs
		f_{OSC} = 400 kHz	0.12	0.14	0.19	A/µs
INTERNAL MOSFETS						
High-Side MOSFET On-Resistance	$R_{DSon(HS)}$	T_A = 25°C [4], I_{DS} = 100 mA	–	200	235	mΩ
		I_{DS} = 100 mA	–	–	400	mΩ
LX2 Node Rise/Fall Time [3]	$t_{R/F(LX2)}$	V_{VREG} = 5.5 V	–	12	–	ns
High-Side MOSFET Leakage [2]	$I_{DSS(HS)}$	V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, V_{LX2} = 0 V, V_{VREG} = 5.5 V, –40˚C < T_J < 85˚C [4]	–	–	2	µA
		V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, V_{LX2} = 0 V, V_{VREG} = 5.5 V, −40°C < T_J < 150°C	–	3	15	µA
Low-Side MOSFET On-Resistance	$R_{DSon(LS)}$	T_A = 25°C [4], I_{DS} = 100 mA	–	55	65	mΩ
		I_{DS} = 100 mA	–	–	110	mΩ
Low-Side MOSFET Leakage [2]	$I_{DSS\ (LS)}$	V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, V_{LX2} = 5.5 V, –40˚C < T_J < 85˚C [4]	–	–	1	µA
		V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, V_{LX2} = 5.5 V, −40°C <T_J < 150°C	–	8	25	µA
ERROR AMPLIFIER						
Feedback Input Bias Current [2]	$I_{1V25/FBAdj}$	V_{COMP2} = 0.8 V, $V_{FB(ADJ)}$ regulated so that I_{COMP2} = 0 A	–	–150	−350	nA
Open-Loop Voltage Gain [3]	A_{VOL2}		–	60	–	dB
Transconductance	gm_{EA2}	I_{COMP2} = 0 µA, V_{SS2} > 500 mV	515	900	1350	µA/V
		0 V < V_{SS2} < 500 mV	–	250	–	µA/V
Source and Sink Current	I_{EA2}	V_{COMP2} = 1.5 V	–	±50	–	µA
Maximum Output Voltage	$V_{EA2VO(max)}$		1.00	1.25	1.50	V
Minimum Output Voltage	$V_{EA2VO(min)}$		–	–	150	mV
COMP2 Pull-Down Resistance	R_{COMP2}	HICCUP2 = 1 or FAULT2 = 1 or V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, latched until V_{SS2} < $V_{SS2(RST)}$	–	1.5	–	kΩ

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{CP(UV,H)}$ and V_{VREG} > $V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.
[3] Ensured by design and characterization, not production tested.
[4] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS – ADJUSTABLE SYNCHRONOUS BUCK REGULATOR [1] (continued):

Valid at 3.6 V [2] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SOFT-START						
SS2 Offset Voltage	$V_{SS2(OFFS)}$	V_{SS2} rising due to $I_{SS2(SU)}$	120	200	270	mV
SS2 Fault/Hiccup Reset Voltage	$V_{SS2(RST)}$	V_{SS2} falling due to HICCUP2 = 1 or FAULT2 = 1 or V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V	–	100	120	mV
SS2 Startup (Source) Current	$I_{SS2(SU)}$	V_{SS2} = 1 V, HICCUP2 = FAULT2 = 0	−10	−20	−30	µA
SS2 Hiccup (Sink) Current	$I_{SS2(HIC)}$	V_{SS2} = 0.5 V, HICCUP2 = 1	5	10	20	µA
SS2 to V_{1V25} Delay Time [3]	$t_{SS2(DLY)}$	C_{SS2} = 10 nF	–	100	–	µs
V_{1V25} Ramp Time [3]	t_{SS2}	C_{SS2} = 10 nF	–	625	–	µs
SS2 Pull-Down Resistance	$R_{PD(SS2)}$	FAULT2 = 1 or V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, latched until V_{SS2} < $V_{SS2(RST)}$	–	2	–	kΩ
SS2 PWM Frequency Foldback	$f_{SW2(SS)}$	$V_{1V25/FBadj}$ < 450 mV_{TYP}	–	f_{OSC}/4	–	–
		450 mV_{TYP} < $V_{1V25/FBadj}$ < 780 mV_{TYP}	–	f_{OSC}/2	–	–
		$V_{1V25/FBadj}$ > 780 mV_{TYP}	–	f_{OSC}	–	–
HICCUP MODE						
Hiccup2 OCP Enable Threshold	$V_{HIC2(EN)}$	V_{SS2} rising	–	2.3	–	V
Hiccup2 OCP Counts	$t_{HIC2(OCP)}$	V_{SS2} > $V_{HIC2(EN)}$, $V_{1V25/FBadj}$ < 450 mV_{TYP}	–	30	–	PWM cycles
		V_{SS2} > $V_{HIC2(EN)}$, $V_{1V25/FBadj}$ > 450 mV_{TYP}	–	120	–	PWM cycles
CURRENT PROTECTIONS						
High-Side MOSFET Pulse-by-Pulse Current Limit	$I_{LIM2(5\%)}$	Duty cycle = 5%	1.8	2.1	2.7	A
Low-Side MOSFET Reverse Current Limit	$I_{LIM2(LS)}$		–	500	–	mA

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[2] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{CP(UV,H)}$ and V_{VREG} > $V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.
[3] Ensured by design and characterization, not production tested.
[4] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS – V5 and V5P LINEAR REGULATOR (LDO) [1]:

Valid at 3.6 V [2] < V_{VIN} < 36 V, −40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V5 AND V5P LINEAR REGULATORS						
V5 Accuracy and Load Regulation	V_{V5}	10 mA < I_{V5} < 325 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5 Output Capacitance [3]	$C_{OUT(V5)}$		1.0	–	22	µF
V5P Accuracy and Load Regulation	V_{V5P}	10 mA < I_{V5P} < 115 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5P Output Capacitance [3]	$C_{OUT(V5P)}$		1.5	2.2	4.1	µF
V5 and V5P Minimum Output Voltage, Buck Only Mode [3]	$V_{V5x(MIN1)}$ (5.5 V_{BAT})	V_{VCP} = 8.60 V, TRACK = 1, I_{V5} = 265 mA, I_{V5P} = 35 mA, I_{3V3} = 75 mA, I_{1V25} = 250 mA 1) T_A = 150°C, V_{VIN} = 5.26 V, V_{VREG} = 5.14 V 2) T_A = –40°C [3], V_{VIN} = 5.04 V, V_{VREG} = 4.97 V	4.82	–	–	V
	$V_{V5x(MIN2)}$ (4.5 V_{BAT})	V_{VCP} = 7.70 V, TRACK = 1, I_{V5} = 265 mA, I_{V5P} = 35 mA, I_{3V3} = 75 mA, I_{1V25} = 250 mA 1) T_A = 150°C, V_{VIN} = 4.26 V, V_{VREG} = 4.14 V 2) T_A = –40°C [3], V_{VIN} = 4.04 V, V_{VREG} = 3.97 V	3.65	–	–	V
V5 and V5P Minimum Output Voltage, Buck-Boost Mode [3][4]	$V_{V5x(MIN3)}$	V_{VIN} = 2.8 V, V_{VREG} = 5.25 V, V_{VCP} ≥ 7.5 V, TRACK = 1, I_{V5} = 310 mA, I_{V5P} = 110 mA, I_{3V3} = 100 mA, I_{1V25} = 500 mA	4.82	4.90	–	V
V5P TRACKING						
V5P/3V3 Tracking Ratio		V_{V5P} ÷ V_{3V3}	1.508	1.515	1.523	–
V5P/3V3 Tracking Accuracy	$TRACK_{3V3}$	3 V < V_{3V3} < 3.3 V, TRACK = 1, I_{3V3} = I_{V5P} = 75 mA	−0.5	–	+0.5	%
V5P/V5 Tracking Accuracy	$TRACK_{V5}$	3.5 V < V_{V5} < 5.0 V, TRACK = 0, I_{V5P} = I_{V5} = 75 mA	−25	–	+25	mV
V5P OVERCURRENT PROTECTION						
V5P Current Limit [1]	$I_{LIM(V5P)}$	V_{V5P} = 5 V	−210	−285	–	mA
V5P Foldback Current [1]	$I_{FBK(V5P)}$	V_{V5P} = 0 V	−30	−60	−90	mA
V5 OVERCURRENT PROTECTION						
V5 Current Limit [1]	$I_{LIM(V5)}$	V_{V5} = 5 V	−350	−500	–	mA
V5 Foldback Current [1]	$I_{FBK(V5)}$	V_{V5} = 0 V	−40	−75	−180	mA
V5P AND V5 STARTUP TIMING						
V5P Startup Time [3]	$t_{SU(V5P)}$	C_{V5P} ≤ 2.9 µF, Load = 45 Ω ±5% (110 mA)	–	175	565	µs
V5 Startup Time [3]	$t_{SU(V5)}$	C_{V5} ≤ 2.9 µF, Load = 16 Ω ±5% (310 mA)	–	150	530	µs

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{CP(UV,H)}$ and V_{VREG} > $V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.
[3] Ensured by design and characterization, not production tested.
[4] See B/B schematic, CP helper circuit required when V_{VIN} < 6 V.

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ELECTRICAL CHARACTERISTICS – 3V3 LDO and CONTROL INPUTS [1]:

Valid at 3.6 V [2] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
3V3 LINEAR REGULATORS						
3V3 Accuracy and Load Regulation	V_{3V3}	10 mA < I_{3V3} < 165 mA, V_{VREG} = 5.25 V	3.23	3.30	3.37	V
3V3 Output Capacitance [3]	$C_{OUT(3V3)}$		1.0	–	22	µF
3V3 Minimum Output Voltage, Buck Only Mode [3]	$V_{3V3(MIN1)}$ (5.5 V_{BAT})	V_{VCP} = 8.80 V, TRACK = 1, I_{V5} = 265 mA, I_{V5P} = 35 mA, I_{3V3} = 75 mA, I_{1V25} = 250 mA 1) T_A = 150°C, V_{VIN} = 5.26 V, V_{VREG} = 5.14 V 2) T_A = –40°C [3], V_{VIN} = 5.04 V, V_{VREG} = 4.97 V	3.23	3.30	–	V
	$V_{3V3(MIN2)}$ (4.5 V_{BAT})	V_{VCP} = 6.80 V, TRACK = 1, I_{V5} = 265 mA, I_{V5P} = 35 mA, I_{3V3} = 75 mA, I_{1V25} = 250 mA 1) T_A = 150°C, V_{VIN} = 4.26 V, V_{VREG} = 4.14 V 2) T_A = –40°C [3], V_{VIN} = 4.04 V, V_{VREG} = 3.97 V	3.20	–	–	V
3V3 OVERCURRENT PROTECTION						
3V3 Current Limit [1]	$I_{LIM(3V3)}$	V_{3V3} = 3.3 V	−185	−260	–	mA
3V3 Foldback Current [1]	$I_{FBK(3V3)}$	V_{3V3} = 0 V	−15	−40	−65	mA
3V3 STARTUP TIMING						
3V3 Startup Time [3]	$t_{SU(3V3)}$	C_{3V3} ≤ 2.9 µF, Load = 33 Ω ±5% (100 mA)	–	170	550	µs
IGNITION ENABLE (ENBAT1 AND ENBAT2) INPUTS						
ENBAT1, ENBAT2 Thresholds	$V_{ENBATx(H)}$	V_{ENBATx} rising	2.9	3.3	3.5	V
	$V_{ENBATx(L)}$	V_{ENBATx} falling	2.2	2.6	2.9	V
ENBAT1, ENBAT2 Hysteresis	$V_{ENBATx(HYS)}$	$V_{ENBATx(H)}$ – $V_{ENBATx(L)}$	–	700	–	mV
ENBAT1, ENBAT2 Bias Current [2]	$I_{ENBATx(BIAS)}$	T_J = 25°C [4], V_{ENBATx} = 3.51 V	–	28	45	µA
		T_J = 150°C, V_{ENBATx} = 3.51 V	–	35	55	µA
ENBAT1, ENBAT2 Resistance	R_{ENBATx}	V_{ENBATx} < 1.2 V	–	650	–	kΩ
LOGIC ENABLE (ENB) INPUT						
ENB Thresholds	$V_{ENB(H)}$	V_{ENB} rising	–	–	2.0	V
	$V_{ENB(L)}$	V_{ENB} falling	0.8	–	–	V
ENB Bias Current [1]	$I_{ENB(IN)}$	V_{ENB} = 3.3 V	–	–	175	µA
ENB Resistance	R_{ENB}	V_{ENB} = 0.8 V	–	60	–	kΩ
ENB/ENBATX FILTER/DEGLITCH						
Enable Filter/Deglitch Time	$t_{dEN(FILT)}$		10	15	20	µs
ENB/ENBATX SHUTDOWN DELAY						
LDO Shutdown Delay	$t_{dLDO(OFF)}$	Measure $t_{dLDO(OFF)}$ from the falling edge of ENB and ENBAT1 and ENBAT2 to time when all LDOs begin to decay	15	50	100	µs

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{CP(UV,H)}$ and V_{VREG} > $V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.
[3] Ensured by design and characterization, not production tested.
[4] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS – 3V3 LDO and CONTROL INPUTS [1] (continued):

Valid at 3.6 V [2] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
TRACK AND MODE INPUTS						
TRACK and MODE Thresholds	V_{TH}, V_{MH}	V_{TRACK} or V_{MODE} rising	–	–	2.0	V
	V_{TL}, V_{ML}	V_{TRACK} or V_{MODE} falling	0.8	–	–	V
TRACK and MODE Bias Current [1]	I_{BTRACK}, I_{BMODE}		–	–50	–	µA
FSET/SYNC INPUT						
FSET/SYNC Pin Voltage	$V_{FSET/SYNC}$	No external SYNC signal	–	800	–	mV
FSET/SYNC Open Circuit (Undercurrent) Detection Time	$t_{FSET/SYNC(UC)}$	PWM switching disabled upon detection	–	3	–	µs
FSET/SYNC Short Circuit (Overcurrent) Detection Time	$t_{FSET/SYNC(OC)}$	PWM switching disabled upon detection	–	3	–	µs
Sync. Minimum Frequency	$f_{SYNC(MIN)}$		250	–	–	kHz
Sync. High Threshold	$V_{SYNC(IH)}$	V_{SYNC} rising	–	–	2.0	V
Sync. Low Threshold	$V_{SYNC(IL)}$	V_{SYNC} falling	0.5	–	–	V
Sync. Input Duty Cycle	DC_{SYNC}		–	–	80	%
Sync. Input Pulse Width	t_{wSYNC}		200	–	–	ns
Sync. Input Transition Times [3]	t_{tSYNC}		–	10	15	ns
SLEW INPUT						
SLEW Pin Operating Voltage	V_{SLEW}		–	800	–	mV
SLEW Open Circuit (Undercurrent) Detection Time	$t_{SLEW(UC)}$	PWM latched off if open	–	3	–	µs
SLEW Short Circuit (Overcurrent) Detection Time	$t_{SLEW(OC)}$	PWM latched off if shorted	–	3	–	µs
SLEW Bias Current [1]	I_{SLEW}		–	−100	–	nA

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] The lowest operating voltage is only valid if the conditions $V_{VIN} > V_{VIN(START)}$ and $V_{VCP} – V_{VIN} > V_{CP(UV,H)}$ and $V_{VREG} > V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.
[3] Ensured by design and characterization, not production tested.
[4] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS [1]: Valid at 3.6 V [2] < V_{IN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NPOR OV/UV PROTECTION THRESHOLDS						
V5 OV Thresholds	$V_{V5(OV,H)}$	V_{V5} rising	5.15	5.33	5.50	V
	$V_{V5(OV,L)}$	V_{V5} falling	–	5.30	–	V
V5 OV Hysteresis	$V_{V5(OV,HYS)}$	$V_{V5(OV,H)} – V_{V5(OV,L)}$	15	30	50	mV
V5 UV Thresholds	$V_{V5(UV,H)}$	V_{V5} rising, independent of the MODE pin	–	4.68	–	V
	$V_{V5(UV,L1)}$	V_{V5} falling, V_{MODE} = 0 V or GND	4.50	4.65	4.80	V
	$V_{V5(UV,L2)}$	V_{V5} falling, V_{MODE} = 5 V or open	3.00	3.13	3.27	V
V5P Output Disconnect Threshold	$V_{V5P(DISC)}$	V_{V5P} rising	–	7.2	–	V
V5P OV Thresholds	$V_{V5P(OV,H)}$	V_{V5P} rising	5.15	5.35	5.50	V
	$V_{V5P(OV,L)}$	V_{V5P} falling	–	5.29	–	V
V5P OV Hysteresis	$V_{V5P(OV,HYS)}$	$V_{V5P(OV,H)} – V_{V5P(OV,L)}$	45	60	75	mV
V5P UV Thresholds	$V_{V5P(UV,H)}$	V_{V5} rising, independent of the MODE pin	–	4.68	–	V
	$V_{VP5(UV,L1)}$	V_{V5P} falling, V_{MODE} = 0 V or GND	4.50	4.65	4.80	V
	$V_{V5P(UV,L2)}$	V_{V5P} falling, V_{MODE} = 5 V or open	3.00	3.13	3.27	V
3V3 OV Thresholds	$V_{3V3(OV,H)}$	V_{3V3} rising	3.41	3.52	3.60	V
	$V_{3V3(OV,L)}$	V_{3V3} falling	–	3.48	–	V
3V3 OV Hysteresis	$V_{3V3(OV,HYS)}$	$V_{3V3(OV,H)} – V_{3V3(OV,L)}$	25	35	50	mV
3V3 UV Thresholds	$V_{3V3(UV,H)}$	V_{3V3} rising	–	3.12	–	V
	$V_{3V3(UV,L)}$	V_{3V3} falling	2.97	3.07	3.17	V
3V3 UV Hysteresis	$V_{3V3(UV,HYS)}$	$V_{3V3(UV,H)} – V_{3V3(UV,L)}$	40	50	60	mV
1V25/FBadj OV Thresholds	$V_{1V25(OV,H)}$	$V_{1V25/FBadj}$ rising	1.29	1.32	1.35	V
	$V_{1V25(OV,L)}$	$V_{1V25/FBadj}$ falling	–	1.30	–	V
1V25/FBadj OV Hysteresis	$V_{3V3(OV,HYS)}$	$V_{1V25(OV,H)} – V_{1V25(OV,L)}$	15	22	30	mV
1V25/FBadj UV Thresholds	$V_{1V25(UV,H)}$	V_{1V25} rising, triggers LDOs on	–	1.20	–	V
	$V_{1V25(UV,L)}$	V_{1V25} falling	1.15	1.18	1.21	V
1V25/FBadj UV Hysteresis	$V_{1V25(UV,HYS)}$	$V_{1V25(UV,H)} – V_{1V25(UV,L)}$	10	17	25	mV

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and $V_{VCP} – V_{VIN}$ > $V_{CP(UV,H)}$ and V_{VREG} > $V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.

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ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS (continued) [1]:

Valid at 3.6 V [2] < V_{IN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NPOR OV DELAY TIME (First silicon will shut down if an OV is detected)						
Overvoltage Detection Delay	t_{dOV}	V5P, V5, 3V3, and 1V25/FBadj over voltage detection delay time	6.40	8.00	9.60	ms
NPOR TURN-ON AND TURN-OFF DELAYS						
NPOR Turn-On Delay	$t_{dNPOR(ON)}$		12	15	18	ms
NPOR Turn-Off Propagation Delay	$t_{dNPOR(OFF)}$	ENB and ENBAT1 and ENBAT2 low to NPOR low	–	15	23	µs
NPOR OUTPUT VOLTAGES						
NPOR Output Low Voltage	$V_{NPOR(L)}$	ENB or ENBAT1 or ENBAT2 high, V_{VIN} ≥ 2.5 V, I_{NPOR} = 4 mA	–	150	400	mV
		ENB or ENBAT1 or ENBAT2 high, V_{VIN} = 1.5 V, I_{NPOR} = 2 mA	–	–	800	mV
NPOR Leakage Current [1]	$I_{NPOR(LKG)}$	V_{NPOR} = 3.3 V	–	–	2	µA
NPOR AND POK5V UV FILTERING/DEGLITCH						
UV Filter/Deglitch Times	t_{dFILT}	Applies to undervoltage of 3V3, 1V25/FBadj, V5, and V5P voltages	10	15	20	µs
POK5V UV PROTECTION THRESHOLDS						
V5 and V5P Rising Thresholds	$V_{V5x(POK,H)}$	V_{V5} or V_{V5P} rising, independent of the MODE pin	–	4.68	–	V
V5 and V5P Falling Thresholds	$V_{V5x(POK,L)}$	V_{V5} or V_{V5P} falling, independent of the MODE pin	4.50	4.65	4.80	V
POK5V OUTPUT VOLTAGES						
POK5V Output Voltage	$V_{POK5V(L)}$	ENB = 1 or ENBAT1 = 1 or ENBAT2 = 1, V_{VIN} ≥ 2.5 V, I_{POK5V} = 4 mA	–	150	400	mV
		ENB = 1 or ENBAT1 = 1, ENBAT2 = 1, V_{VIN} = 1.5 V, I_{POK5V} = 2 mA	–	–	800	mV
POK5V Leakage Current	$I_{POK5V(LKG)}$	V_{POK5V} = 3.3 V	–	–	2	µA

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{CP(UV,H)}$ and V_{VREG} > $V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.

Continued on next page...

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ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS (continued) [1]:

Valid at 3.6 V [2] < V_{IN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VREG, VCP, AND BG THRESHOLDS						
VREG OV Thresholds	$V_{VREG(OV,H)}$	V_{VREG} rising, LX1 PWM disabled	5.50	5.65	5.90	V
	$V_{VREG(OV,L)}$	V_{VREG} falling, LX1 PWM enabled	–	5.55	–	V
VREG OV Hysteresis	$V_{REG(OV,HYS)}$	$V_{VREG(OV,H)} – V_{VREG(OV,L)}$	–	100	–	mV
VREG UV Thresholds	$V_{VREG(UV,H)}$	V_{VREG} rising, triggers rise of SS2	4.14	4.38	4.62	V
	$V_{VREG(UV,L)}$	V_{VREG} falling	–	4.28	–	V
VREG UV Hysteresis	$V_{VREG(UV,HYS)}$	$V_{VREG(UV,H)} – V_{VREG(UV,L)}$	–	100	–	mV
VCP OV Thresholds	$V_{VCP(OV,H)}$	V_{VCP} rising, latches all regulators off	11.0	12.5	14.0	V
VCP UV Thresholds	$V_{VCP(UV,H)}$	V_{VCP} rising, PWM enabled	–	3.2	–	V
	$V_{VCP(UV,L)}$	V_{VCP} falling, PWM disabled	–	2.8	–	V
VCP UV Hysteresis	$V_{VCP(UV,HYS)}$	$V_{VCP(UV,H)} – V_{VCP(UV,L)}$	–	400	–	mV
BGREF and BGFAULT UV Thresholds [3]	$V_{BGx(UV)}$	V_{BGVREF} or $V_{BGFAULT}$ rising	1.00	1.05	1.10	V
LAST MICROCONTROLLER (OR DSP) RESET STATE INDICATORS (FF0 AND FF1)						
FF0, FF1 UV Detection Delay	$t_{dFFx(UV)}$	NPOR↓ due to UV to FF0/FF1 latching	0.8	1.0	1.2	ms
FF0, FF1 Output Voltage	$V_{FFx(LO)}$	I_{FFx} = 4 mA	–	–	400	mV
FF0, FF1 Leakage Current [1]	I_{FFx}	V_{FFx} = 3.3 V	–	–	1	µA

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] The lowest operating voltage is only valid if the conditions $V_{VIN} > V_{VIN(START)}$ and $V_{VCP} – V_{VIN} > V_{CP(UV,H)}$ and $V_{VREG} > V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.
[3] Ensured by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS – WATCHDOG TIMER (WDT) [1]:

Valid at 3.6 V [2] < V_{VIN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
WD ENABLE / INPUT (WD_{ENn})						
WD_{ENn} Voltage Thresholds	$V_{WDENn(LO)}$	V_{WDENn} falling, WDT enabled	0.8	–	–	V
	$V_{WDENn(HI)}$	V_{WDENn} rising, WDT disabled	–	–	2.0	V
WD_{ENn} Input Resistance	$R_{WD(ENn)}$		–	60	–	kΩ
WD_{IN} VOLTAGE THRESHOLDS AND CURRENT						
WD_{IN} Input Voltage Thresholds	$V_{WDIN(LO)}$	V_{WDIN} falling, WD_{ADJ} pulled low by R_{ADJ}	0.8	–	–	V
	$V_{WDIN(HI)}$	V_{WDIN} rising, WD_{ADJ} charging	–	–	2.0	V
WD_{IN} Input Current [1]	I_{WDIN}	V_{WDIN} = 5 V	−10	±1	10	µA
WD_{IN} TIMING SPECIFICATIONS						
WD_{IN} Duty Cycle	D_{WDIN}		20	50	80	%
Watchdog Activation Delay	$t_{dWD(START)}$	Default	120	140	160	ms
		Metal Option	24	30	36	ms
WD PROGRAMMING (WD_{ADJ})						
WD Timeout, Slow Clock	$t_{WD(TO,SLOW)}$	R_{ADJ} = 32.4 kΩ	8.0	10	12	ms
		R_{ADJ} = 324 kΩ	80	100	120	ms
WD ONE-SHOT TIME						
WD Pulse Time after WD Fault	$t_{WD(FAULT)}$		1.6	2.0	2.4	ms

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

[2] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{CP(UV,H)}$ and V_{VREG} > $V_{VREG(UV,H)}$ are satisfied before V_{VIN} is reduced.

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FUNCTIONAL DESCRIPTION

Overview

The A4408 is a power management IC designed for automotive applications. It contains a pre-regulator plus four DC post-regulators to create the voltages necessary for typical automotive applications such as electrical power steering and automatic transmission control.

The pre-regulator can be configured as a buck or buck-boost regulator. Buck-boost is required for applications that must work at extremely low battery voltages. This pre-regulator generates a fixed 5.35 V and can deliver up to 1 A to power the internal or external post-regulators. These post-regulators generate the various voltage levels for the end system.

The A4408 includes four internal post-regulators: three linear regulators and one adjustable output synchronous buck regulator. The synchronous buck regulator was designed to deliver 1.25 V / 700 mA but will produce higher voltages if a feedback resistor divider is used.

Buck-Boost Pre-Regulator (VREG)

The pre-regulator incorporates an internal high-side buck switch and a boost switch gate driver. An external freewheeling Schottky diode and an LC filter are required to complete the buck converter. By adding a MOSFET and a Schottky diode, the boost configuration can maintain all outputs with input voltages as low as 2.8 V. The A4408 includes a compensation pin (COMP1) and a soft-start pin (SS1) for the pre-regulator.

The A4408 can maintain its outputs over a wide range of input voltages and slew rates. Actual boost performance is shown in Figure 5 and Figure 6 with voltages swinging between 2.9 and 18 V, and V_{VIN} slew rates ranging from 0.3 to 100V/ms.

The buck-boost pre-regulator provides protection and diagnostic functions.

1. Overvoltage protection
2. High voltage rating for load dump
3. Switch-node-to-ground short-circuit protection
4. Open freewheeling diode protection
5. Pulse-by-pulse current limit
6. Hiccup short circuit protection – lab measurement shown in Figure 7 and detailed timing diagram shown in Figure 5

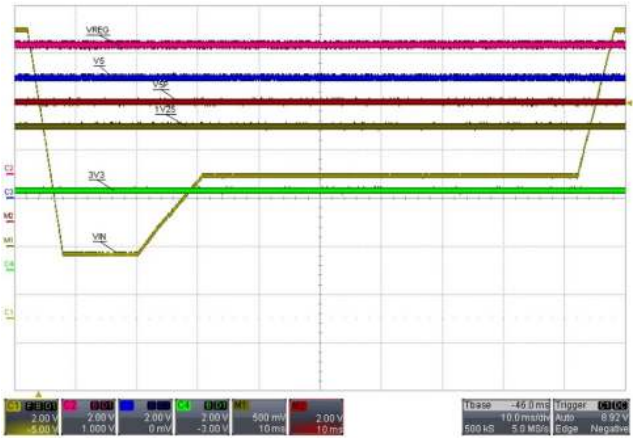

Figure 5: A4408 Buck-Boost operation at full load V_{VIN} slew rates ranging from 0.3 V/ms to 1.6 V/ms Typical of an automotive START/STOP waveform

$V_{VIN(TYP)}$ = 12 V, $V_{VIN(MIN)}$ = 2.9 V, 10 ms/DIV

CH1=VIN, CH2=VREG, CH3=V5, CH4=3V3, M1=1V25, M2=V5P

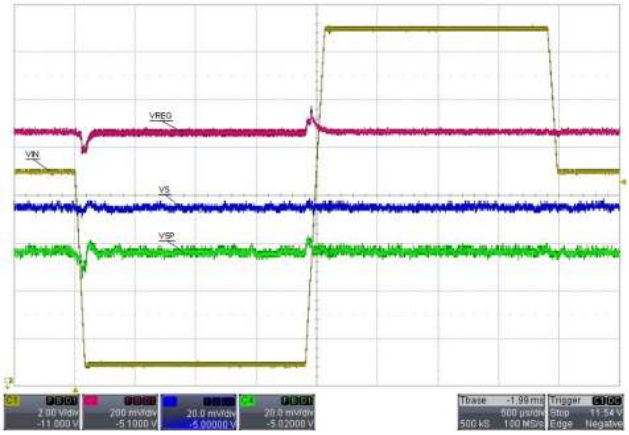

Figure 6: A4408 Buck-Boost operation at full load V_{VIN} slew rates of 100 V/ms – V5P deviates less than 0.2%

$V_{VIN(TYP)}$ = 12 V, $V_{VIN(MIN)}$ = 4 V, $V_{VIN(MAX)}$ = 18 V

CH1=VIN, CH2=VREG, CH3=V5, CH4=V5P, 500 µs/DIV

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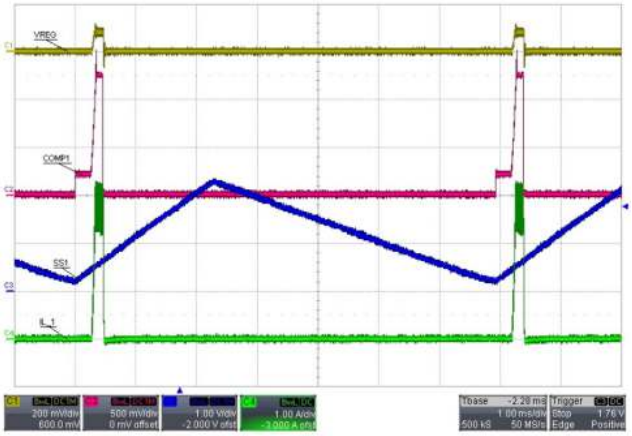

Figure 7: Pre-Regulator Hiccup Mode Operation when VREG is Shorted to GND and C_{SS1} = 22 nF

CH1=VREG, CH2=COMP1, CH3=SS1, CH4=IL1, 1 ms/DIV

For the pre-regulator, hiccup mode is enabled when PWM switching begins. If V_{VREG} is less than 1.3 V, the number of overcurrent pulses (OCP) is limited to only 30. If V_{VREG} is greater than 1.3 V, the number of OCP pulses is increased to 120 to accommodate the possibility of starting into a relatively high output capacitance.

Adjustable Synchronous Buck Regulator (1V25/ADJ)

The A4408 integrates the high-side and low-side MOSFETs necessary for implementing an adjustable output synchronous buck regulator. The synchronous buck is optimized for 1.25 V_{OUT}/700 mA_{DC}/1 A_{PEAK} but can produce higher output voltages if a feedback resistor divider is inserted between VOUT and the 1V25/FBadj pin. The synchronous buck's pulse-by-pulse current limit depends on duty cycle and switching frequency, as shown in Figure 8.

An internal current sense amplifier sources 80 to 100 µA to the LX2 pin. At no load, this current will slowly charge the output capacitors and raise the output voltage. Therefore, the system must always sink at least 100 µA, or a pull-down resistor (<2.49 kΩ) should be used as shown in the Applications Schematic.

Protection and safety functions provided by the synchronous buck are:

1. Undervoltage detection
2. Overvoltage detection
3. Switch-node-to-ground short-circuit protection
4. Pulse-by-pulse current limit
5. Hiccup short-circuit protection; lab measurement shown in Figure 9 and detailed timing diagram shown in Figure 23

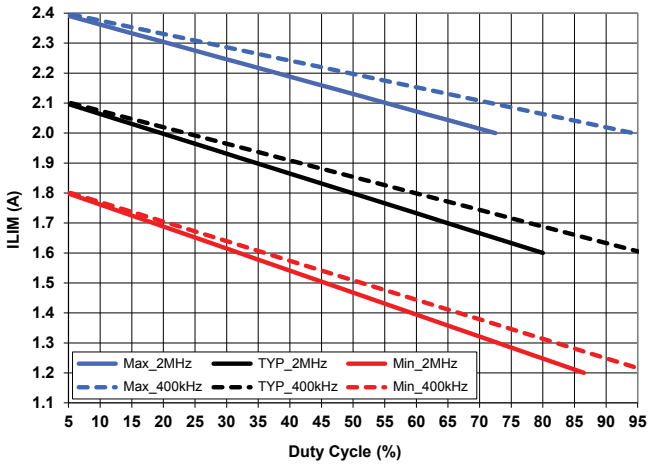

Figure 8: Synchronous Buck Pulse-by-Pulse Current Limit

The synchronous buck is powered by the 5.35 V pre-regulator output. An external LC filter is required to complete the synchronous buck regulator. The A4408 includes a compensation pin (COMP2) and a soft-start pin (SS2) for the synchronous buck.

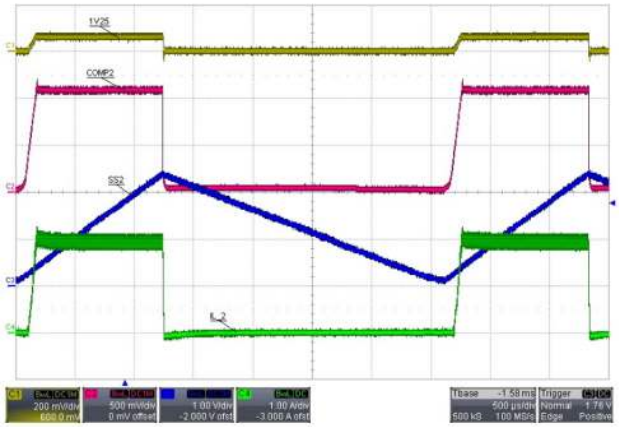

Figure 9: Synchronous Buck Hiccup Mode Operation when 1V25 is Shorted to GND and C_{SS2} = 10 nF

CH1=1V25, CH2=COMP2, CH3=SS2, CH4=IL2, 500 µs/DIV

For the synchronous buck, hiccup mode is enabled when V_{SS2} = $V_{HIC2(EN)}$ (1.2 V_{TYP}). If $V_{1V25/FBadj}$ is less than 450 mV_{TYP}, the number of overcurrent pulses (OCP) is limited to only 30. If $V_{1V25/FBadj}$ is greater than 450 mV_{TYP}, the number of OCP pulses is increased to 120 to accommodate the possibility of starting into a relatively high output capacitance.

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Low-Dropout Linear Regulators (LDOs)

The A4408 has three low-dropout linear regulators (LDOs), one 3.3 V / 165 mA_{MAX} (3V3), one 5 V / 325 mA_{MAX} (V5), and one high-voltage protected 5 V / 115 mA_{MAX} (V5P). The switching pre-regulator efficiently regulates the battery voltage to an intermediate value to power the LDOs. This pre-regulator topology reduces LDO power dissipation and junction temperature.

All linear regulators provide the following protection features:

1. Undervoltage and overvoltage detection
2. Current limit (ILIM) with foldback short-circuit protection (IFBK); see Figure 10

The protected 5 V regulator (V5P) includes protection against accidental short-circuit to the battery voltage. This makes this output most suitable for powering remote sensors or circuitry via a wiring harness where short-to-battery is possible.

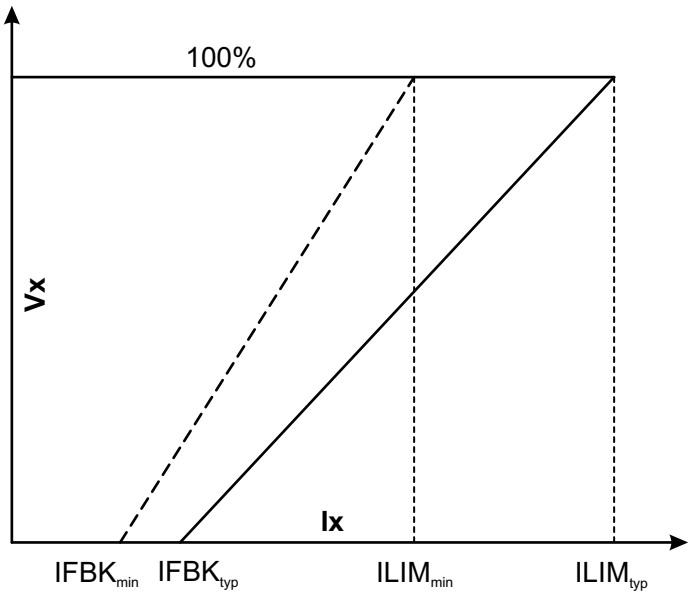

Figure 10: Typical LDO Foldback Characteristics

Tracking Input (TRACK)

The V5P LDO is a tracking regulator. It can be set to use either V5 or 3V3 as its reference by setting the TRACK input pin to a logic low or high. If the TRACK input is left unconnected, an internal current source will set the TRACK pin to a logic high.

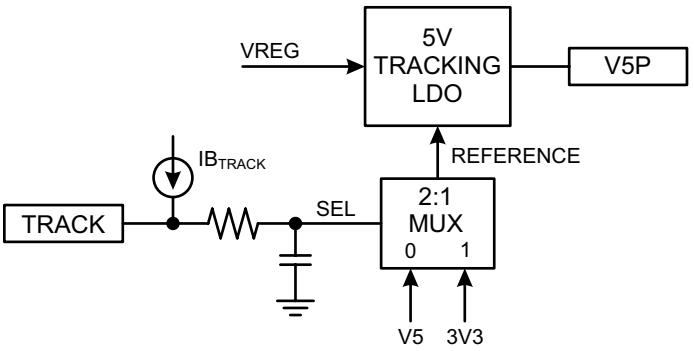

Figure 11: The V5P reference is set by the TRACK input.

Watchdog Timer (WDT)

The A4408 watchdog timer monitors the time between rising edges of a clock (i.e., the clock period) applied to the WD_{IN} pin. This clock should be generated by the primary microcontroller or DSP. A watchdog fault will occur if the time between rising edges is longer than the time set by the resistor (R_{ADJ}) at the watchdog programming pin (WD_{ADJ}). A watchdog fault will pulse NPOR low for $t_{WD(FAULT)}$ (typically 2 ms). The watchdog circuitry is shown in Figure 12.

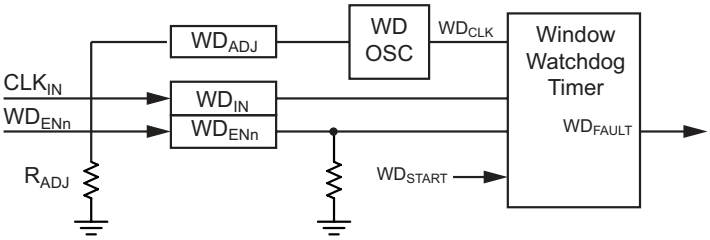

Figure 12: Watchdog Timer Block Diagram

The watchdog time is programmable via the WD_{ADJ} pin according to the following equation:

$$R_{ADJ} = 3.240 \times t_{WD(TO,SLOW)}$$

where $t_{WD(TO,SLOW)}$ is the longest expected clock period (in ms) and R_{ADJ} is the external resistor value (in kΩ) needed from the WD_{ADJ} pin to ground. A detailed watchdog timing diagram is shown in Figure 24.

The watchdog is enabled when two conditions are met:

1. The WD_{ENn} pin is a logic low, and
2. All the regulators (1V25/FBadj, 3V3, V5, and V5P) have been above their undervoltage thresholds for the watchdog start delay time, $t_{dWD(START)}$ (140 ms_{TYP}).

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The watchdog start delay allows the microcontroller or DSP to complete its initialization routines before delivering a clock to the WD_{IN} pin. A timing diagram documenting $t_{dWD(START)}$ is shown in Figure 25.

After regulator startup, if the WD_{IN} clock is missing (i.e. stuck low or stuck high) for at least $t_{dWD(START)} + t_{WD(TO,SLOW)}$ the A4408 will set NPOR, reset its counters, and repeat the watchdog startup delay. NPOR will periodically pulse low as long as no WDIN clock is applied. A timing diagram for the missing clock situation is shown in Figure 25.

Dual Bandgaps (BG_{VREF}, BG_{FAULT})

Dual bandgaps, or references, are implemented within the A4408. One bandgap (BG_{VREF}) is dedicated solely to closed-loop control of the output voltages. The second bandgap (BG_{FAULT}) is employed for fault monitoring functions. Having redundant bandgaps improves reliability of the A4408.

If the reference bandgap is out of specification (BG_{VREF}), then the output voltages will be out of specification and the monitoring bandgap will report a fault condition by setting NPOR and/or POK5V low.

If the monitoring bandgap is out of specification (BG_{FAULT}), then the outputs will remain in regulation, but the monitoring circuits will report a fault condition by setting NPOR and/or POK5V low.

The reference and monitoring bandgap circuits include two smaller secondary bandgaps that are used to detect undervoltage of the main bandgaps during power-up.

Adjustable Frequency and Synchronization (FSET/SYNC)

The PWM switching frequency of the A4408 is adjustable from 250 kHz to 2.4 MHz. Connecting a resistor from the FSET/SYNC pin to ground sets the switching frequency. An FSET resistor with ±1% tolerance is recommended. The FSET resistor can be calculated using the following equation:

$$R_{FSET} = \left(\frac{21{,}693}{f_{OSC}} \right) - 2.215$$

where R_{FSET} is in kΩ and f_{OSC} is the desired oscillator (PWM) frequency in kHz.

A graph of switching frequency versus FSET resistor values is shown in Figure 13.

The PWM frequency of the A4408 may be increased or decreased by applying a clock to the FSET/SYNC pin. The clock must satisfy the voltage thresholds and timing requirements shown in the Electrical Characteristics table.

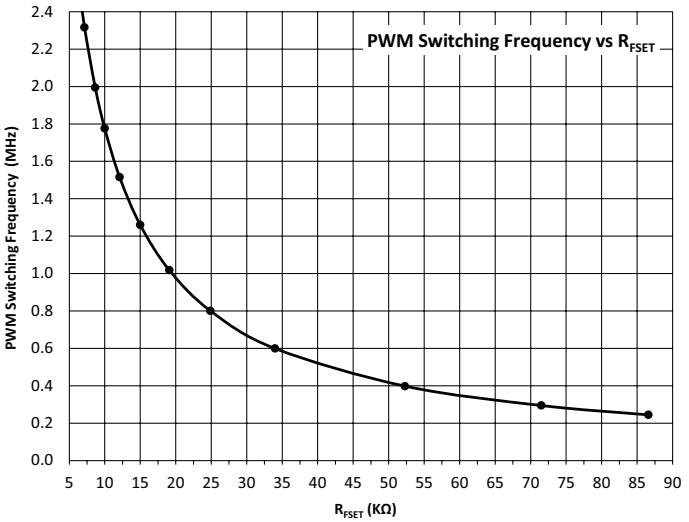

Figure 13: Switching Frequency vs. FSET Resistor Values

Frequency Dithering and LX1 Slew Rate Control

The A4408 includes two innovative techniques to help reduce EMI/EMC for demanding automotive applications.

First, the A4408 performs pseudo-random dithering of the PWM frequency. Dithering the PWM frequency spreads the energy above and below the base frequency set by R_{FSET}. A typical fixed-frequency PWM regulator will create distinct "spikes" of energy at f_{OSC}, and at higher frequency multiples of f_{OSC}. Conversely, the A4408 spreads the spectrum around f_{OSC}, thus creating a lower magnitude at any comparable frequency. Frequency dithering is disabled if SYNC is used or V_{VIN} drops below approximately 8.3 V.

Second, the A4408 includes a pin to adjust the rising slew rate of the LX1 pin by simply changing the value of the resistor from the SLEW pin to ground. Slower rise times of LX1 reduce ringing and high-frequency harmonics of the regulator. The rise time may be adjusted to be relatively long and will increase thermal dissipation of the pre-regulator if set too high. Typical LX1 slew rates are shown in Table 1.

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Table 1: Typical LX1 Rising Slew Rate vs. R_{SLEW}; LX1 Snubber 8.66 Ω / 330 pF

R_{SLEW} (kΩ)	LX1 Rising Slew Rate (V/ns)	LX1 10%-90% Transition Time at 12 V_{VIN} (ns)
8.66	1.06	9.1
22.1	0.90	10.7
46.4	0.79	12.1
71.5	0.65	14.8
100	0.50	19.2
121	0.38	25.2
150	0.29	33.1

Enable Inputs (ENB, ENBAT)

Two enable pins are available on the A4408. A logic high on either of these pins enables the A4408. One enable (ENB) is logic-level compatible for microcontroller or DSP control. The other input (ENBAT) must be connected to the high-voltage ignition (IGN) or accessory (ACC) switch through a relatively low-value series resistance, 2 to 3.6 kΩ. For transient suppression, it is strongly recommended that a 0.22 to 0.47 µF capacitor be placed after the series resistance to form a low-pass filter to the ENBAT pin as shown in the Applications Schematic.

Bias Supply (V_{CC})

The bias supply (V_{CC}) is generated by an internal linear regulator. This supply is the first rail to start up. Most of the internal control circuitry is powered by this supply. The bias supply includes some unique features to ensure reliable operation of the A4408. These features include:

1. Input voltage (V_{VIN}) undervoltage lockout
2. Undervoltage detection
3. Short-to-ground protection
4. Operation from either $V_{LDO3.6V}$ or V_{VREG}, whichever is higher

Charge Pump (VCP, CP1, CP2)

A charge pump provides the voltage necessary to drive the high-side N-channel MOSFETs in the pre-regulator and the linear regulators.

Two external capacitors are required for charge pump operation. During the first half of the charge pump cycle, the flying capacitor between pins CP1 and CP2 is charged from either V_{VIN} or V_{VREG}, whichever is highest. During the second half of the charge pump cycle, the voltage on the flying capacitor charges the VCP capacitor. For most conditions, the V_{VCP} minus V_{VIN} voltage is regulated to approximately 6.5 V.

The charge pump can provide enough current to operate the pre-regulator and the LDOs at 2.2 MHz (full load) and 125°C ambient, provided V_{VIN} is greater than 6 V. Optional components D3, D4, and CP3 (refer to Figure 14) must be included if V_{VIN} drops below 6 V. Diode D3 should be a silicon diode rated for at least 200 mA/50 V with less than 50 µA of leakage current when V_R = 13 V and T_A = 125°C. Diode D4 should be a 1 A Schottky diode with a very low forward voltage (V_F) rated to withstand at least 30 V.

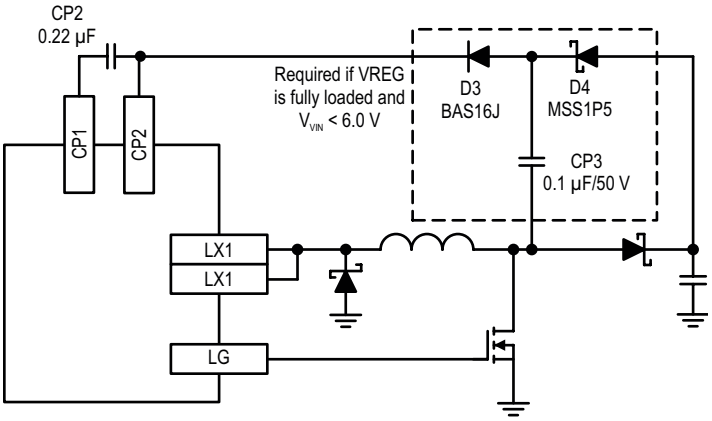

Figure 14: Charge pump enhancement components D3, D4, and CP3 are required if V_{VIN} < 6 V.

The charge pump incorporates some protection features:

1. Undervoltage lockout of PWM switching
2. Overvoltage "latched" shutdown of the A4408

Startup and Shutdown Sequences

The startup and shutdown sequences of the A4408 are fixed. If no faults exist and ENBAT or ENB transition high, the A4408 will perform its startup routine. If ENBAT and ENB are low for at least $t_{dEN(FILT)} + t_{dLDO(OFF)}$ (typically 65 µs), the A4408 will enter a shutdown sequence. The startup and shutdown sequences are summarized in Table 3 and shown in timing diagrams in Figure 18 and Figure 19.

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Fault Reporting (NPOR, MODE, POK5V)

The A4408 includes two open-drain outputs to report regulator status. The NPOR circuit monitors all regulator outputs for under- and overvoltage (1V25/FBadj, 3V3, V5, V5P), the watchdog timer output (WD_{FAULT}), and the thermal monitor (TSD). The POK5V circuit monitors the V5 and V5P output for undervoltage. The NPOR and POK5V block diagrams are shown in Figure 15.

The MODE input pin modifies the NPOR circuit to raise or lower the 5 V undervoltage thresholds. If the MODE pin is low, the undervoltage thresholds are relatively high, at $V_{V5(UV,L1)}$. If the MODE pin is high, the undervoltage thresholds are set much lower, at $V_{V5(UV,L2)}$. The MODE pin does not influence the POK5V circuit. The POK5V undervoltage threshold is always at $V_{V5(POK,L)}$. The MODE input is shown in Figure 15. Timing diagrams of the MODE pin functionality is shown in Figure 16 and Figure 17.

There is a delay from the time all regulator voltages have risen above their undervoltage thresholds to the rising edge of NPOR, $t_{dNPOR(ON)}$. This delay allows the microcontroller or DSP plenty of time to fully power-up and complete its initialization routines. The NPOR circuit also incorporates a delay, t_{dOV}, between the instant any regulator output exceeds its overvoltage threshold and when NPOR transitions low. There is minimal NPOR delay if any fault, other than overvoltage, occurs that requires NPOR to transition low. There are no significant delays in the POK5V output after V5 or V5P have risen above or fallen below their undervoltage thresholds. Timing diagram in this datasheet shows the functionality of NPOR and POK5V.

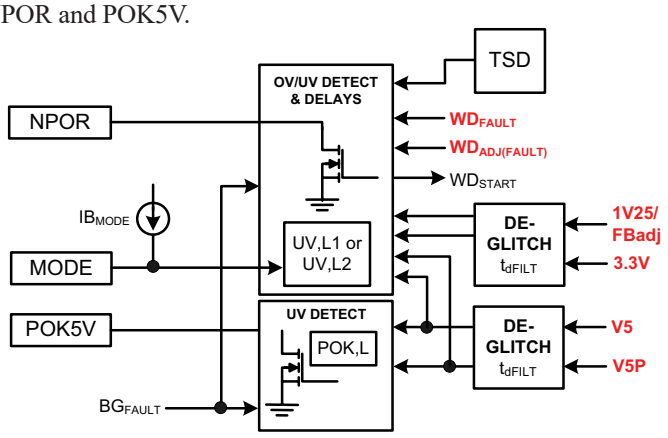

Figure 15: Fault Reporting Circuit

The V5P monitor is unique: if V5P is accidently connected to the battery voltage, then NPOR will bypass the normal overvoltage delay and set itself low immediately. Timing diagrams showing overvoltage possibilities for V5P are shown in Figure 21.

The fault modes and their effects on NPOR and POK5V are covered in detail in Table 4.

Fault Flags (FF0, FF1)

The A4408 also includes two open-drain fault flags: FF0 and FF1. If a fault condition occurs and NPOR transitions low, FF0 and FF1 will be latched into one of three states to retain the type of fault: undervoltage of any regulator or charge pump (including V5P disconnect), hiccup mode (or TSD), or watchdog fault. A fourth state indicates no-fault. Fault flag functionality is summarized in Table 2 and shown in most timing diagrams in this datasheet.

FF0 and FF1 are only valid if NPOR has first transitioned high. This means the A4408 must successfully complete the startup sequence and NPOR transitions high.

The FF0 and FF1 latches are reset when all enable inputs are low and the soft-start capacitor voltages (SS1, SS2) have decayed below their reset thresholds.

Table 2: FF0 and FF1 Fault Flag Status Conditions

FF0	FF1	Type of Fault Detected When NPOR↴
Low	Low	Undervoltage (Synchronous buck, 3V3, V5, V5P, or VCP), or $V_{V5P} > V_{V5P(DISC)}$
Low	Hi-Z	VREG or Synchronous buck in hiccup mode, or thermal shutdown (TSD)
Hi-Z	Low	Watchdog Timer (WDT) fault
Hi-Z	Hi-Z	No fault, default condition

Both VREG and the synchronous buck do not enter hiccup mode for a specific number of PWM cycles. Therefore, when setting FF0 and FF1, precedence is given to detecting a hiccup condition (i.e., an undervoltage will occur before hiccup mode is set). To accomplish this, the undervoltage detection is delayed by $t_{dFFx(UV)}$.

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Table 3: Startup and Shutdown Logic (signal names consistent with Functional Block Diagram)

A4408 Status Signals						Regulator Control Bits (0 = OFF, 1 = ON)			A4408 MODE
EN	MPOR	$VSS_{1/2}$ LOW	VREG UV	1V25 UV	3×LDO UV	VREG ON	1V25 ON	LDOs ON	
X	1	X	X	X	X	0	0	0	RESET
0	0	1	1	1	1	0	0	0	OFF
1	0	0	1	1	1	1	0	0	STARTUP
1	0	0	0	1	1	1	1	0	↓
1	0	0	0	0	1	1	1	1	↓
1	0	0	0	0	0	1	1	1	RUN
0	0	0	0	0	0	1	1	1	$t_{dEN(FILT)} + t_{dLDO(OFF)}$
0	0	0	0	0	0	1	1	0	SHUTDOWN
0	0	0	0	0	1	1	0	0	↓
0	0	0	0	1	1	0	0	0	↓
0	0	0	0	1	1	0	0	0	↓
0	0	0	1	1	1	0	0	0	Pause
0	0	1	1	1	1	0	0	0	OFF

X = DON'T CARE

EN = ENBAT1 + ENBAT2 + ENB

$VSS_{1/2}$ LOW = VSS1 < $V_{SS1(RST)}$ × V_{SS2} < $V_{SS2(RST)}$

3 × LDO UV = 3V3_UV + V5_UV + V5P_UV

MPOR = $V_{VIN(UVLO)}$ + VCC_UV + VCP_UV + BG1_UV + BG2_UV + FSET_UV/OV + TSD + SLEW_UV/OV (latched) + VCP_OV (latched) + D1MISSING (latched) + $I_{LIM(LX1)}$ (latched) + OV > t_{dOV} (latched)

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Table 4: Summary of Fault Mode Operation

FAULT TYPE and CONDITION	A4408 RESPONSE TO FAULT	NPOR	POK5V $V5_{SNR}$/ $V5_{CAN}$/V5P	LATCHED FAULT?	RESET METHOD
V5P Short to VBAT	NPOR and POK5V transition low soon after V5P disconnect occurs.	Low when $V5P_{SENSE}$ decays	Low when $V5P_{SENSE}$ decays	NO	Check for short circuits on V5P
V5, V5P, 3V3, or Synchronous Buck Overvoltage	If the OV condition persists for more than t_{dOV}, then set NPOR low and turn off all regulators.	Immediately set low after t_{dOV}	Low only if V5 or V5P are too low	YES	Check for short circuits then cycle EN or VIN
V5 or V5P Undervoltage	Closed-loop control will try to raise the voltage, but may be constrained by the foldback current limit.	Low	Low	NO	Remove the short circuit or decrease the load
3V3 or Synchronous Buck Undervoltage	Closed-loop control will try to raise the voltage, but may be constrained by the foldback or pulse-by-pulse current limit	Low	Not affected	NO	Remove the short circuit or decrease the load
V5 or V5P Overcurrent	Foldback current limit will reduce the output voltage.	Low if V5 or V5P are too low	Low if V5 or V5P are too low	NO	Remove the short circuit or decrease the load
3V3 Overcurrent	Foldback current limit will reduce the output voltage.	Low if $V_{3V3} < V_{3V3(UV,L)}$	Not affected	NO	Remove the short circuit or decrease the load
1V25/FBadj pin open circuit (Synchronous buck output set to 1.25 V, i.e. no FB divider)	The 1V25/FBadj pin will be pulled high by an internal current source; COMP2 will respond by going low; LX2 will operate at zero cycle; and the synchronous buck output ≈ 0 V.	Low	High	NO	Repair the open circuit, check the 1V25 circuitry
Synchronous Buck Output Shorted to Ground, $V_{SS2} < V_{HIC2(EN)}$, $V_{1V25} < 450$ mV	Continues to PWM, but turns off LX2 when the high-side MOSFET current exceeds I_{LIM2}.	Low	Not affected	NO	Remove the short circuit
Synchronous Buck Overcurrent $V_{SS2} > V_{HIC2(EN)}$, $V_{1V25/FBadj} < 450$ mV	Enters hiccup mode after 30 OCP faults.	Low	Not affected	NO	Decrease the load
Synchronous Buck Overcurrent $V_{SS2} > V_{HIC2(EN)}$, $V_{1V25/FBadj} > 450$ mV	Enters hiccup mode after 120 OCP faults.	Low if $V_{1V25/FBadj} < V_{1V25(UV,L)}$	Not affected	NO	Decrease the load
VREG Pin Open Circuit	V_{VREG} will decay to 0 V; LX1 will switch at maximum duty cycle so the voltage on the output capacitors will be very close to V_{VIN}.	Low if 3V3, 1V25/ FBadj, V5, or V5P are too low	Low if V5 or V5P are too low	NO	Connect the VREG pin
VREG Overcurrent $V_{VREG} < 1.3$ V, $V_{COMP1} = V_{EA1(VO,MAX)}$	Enters hiccup mode after 30 OCP faults.	Low	Low	NO	Decrease the load
VREG Overcurrent $V_{VREG} > 1.3$ V, $V_{COMP1} = V_{EA1(VO,MAX)}$	Enters hiccup mode after 120 OCP faults.	Low if 3V3, 1V25/ FBadj, V5, or V5P are too low	Low if V5 or V5P are too low	NO	Decrease the load
VREG Overvoltage $V_{VREG} > V_{REG(OV,H)}$	Temporarily stop PWM switching of LX1.	High	High	NO	None
VREG Asynchronous Diode (D1) Missing	Results in an MPOR after 1 detection, so all regulators are shut off.	Low if 3V3, 1V25/ FBadj, V5, or V5P are too low	Low if V5 or V5P are too low	YES	Populate D1 then cycle EN or VIN

Continued on next page...

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Table 4: Summary of Fault Mode Operation (continued)

FAULT TYPE and CONDITION	A4408 RESPONSE TO FAULT	NPOR	POK5V $V5_{SNR}$/ $V5_{CAN}$/V5P	LATCHED FAULT?	RESET METHOD
Asynchronous Diode (D1) Short-Circuited or LX1 Shorted to Ground	Results in an MPOR after 2 detections of the high-side MOSFET current exceeding $I_{LIM(LX1)}$, so all regulators are off.	Low if 3V3, 1V25/ FBadj, V5, or V5P are too low	Low if V5 or V5P are too low	YES	Remove the short, then cycle EN or VIN
Slew Pin Open Circuit (SLEW_OV)	Results in an MPOR, so all regulators are off.	Low	Low	YES	Connect SLEW pin then cycle EN or VIN
Slew Pin Shorted to Ground (SLEW_UV)	Results in an MPOR, so all regulators are off.	Low	Low	YES	Remove the short, then cycle EN or VIN
FSET/SYNC Pin Shorted to Ground or Open Circuit	LX1 operates at a default oscillator frequency of 1 MHz; VREG achieves 5.35 V; boost function is disabled; synchronous buck and LDOs remain disabled.	Low	Low	NO	Remove short circuit, connect the pin, or populate RFSET
Charge Pump (VCP) Overvoltage	Results in an MPOR, so all regulators are off.	Low	Low	YES	Check VCP/CP1/ CP2, then cycle EN or VIN
Charge Pump (VCP) Undervoltage	Results in an MPOR, so all regulators are off.	Low	Low	NO	Check VCP/CP1/ CP2
VCP Pin Open Circuit	Results in VCP_UV and an MPOR, so all regulators are off.	Low	Low	NO	Connect the VCP pin or populate C_{CP}
VCP Pin Shorted to Ground	Results in high current from the charge pump and (intentional) fusing of an internal trace. Also results in MPOR, so all regulators are off.	Low	Low	NO	Remove the short circuit and replace the A4408
CP1 or CP2 Pin Open Circuit	Results in VCP_UV and an MPOR, so all regulators are off.	Low	Low	NO	Connect the CP1 or CP2 pins
CP1 Pin Shorted to Ground	Results in VCP_UV and an MPOR, so all regulators are off.	Low	Low	NO	Remove the short circuit
CP2 Pin Shorted to Ground	Results in high current from the charge pump and (intentional) fusing of an internal trace. Also results in MPOR so all regulators are off.	Low	Low	NO	Remove the short circuit and replace the A4408
BG_{VREF} or BG_{FAULT} Undervoltage	Results in an MPOR, so all regulators are off.	Low	Low	NO	Raise VIN or wait for BGs to power up
BG_{VREF} or BG_{FAULT} Overvoltage	If BG_{VREF} is too high, all regulators will appear to be OV (because BG_{FAULT} is good). If BG_{FAULT} is too high, all regulators will appear to be UV (because BG_{VREF} is good).	Low	Low	NO	Replace the A4408
VCC Undervoltage or Shorted to Ground	Results in an MPOR, so all regulators are off.	Low	Low	NO	Raise VIN or remove short from VCC pin
WD_{ADJ} pin Shorted to Ground or Open Circuit	A WD_{ADJ} fault sets the NPOR output low. The remainder of the A4408 operates normally.	Low	High	NO	Remove the short circuit or connect the pin
Thermal Shutdown	Results in an MPOR, so all regulators are off.	Low	Low	NO	Let the A4408 cool

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TIMING DIAGRAMS

(Not to Scale)

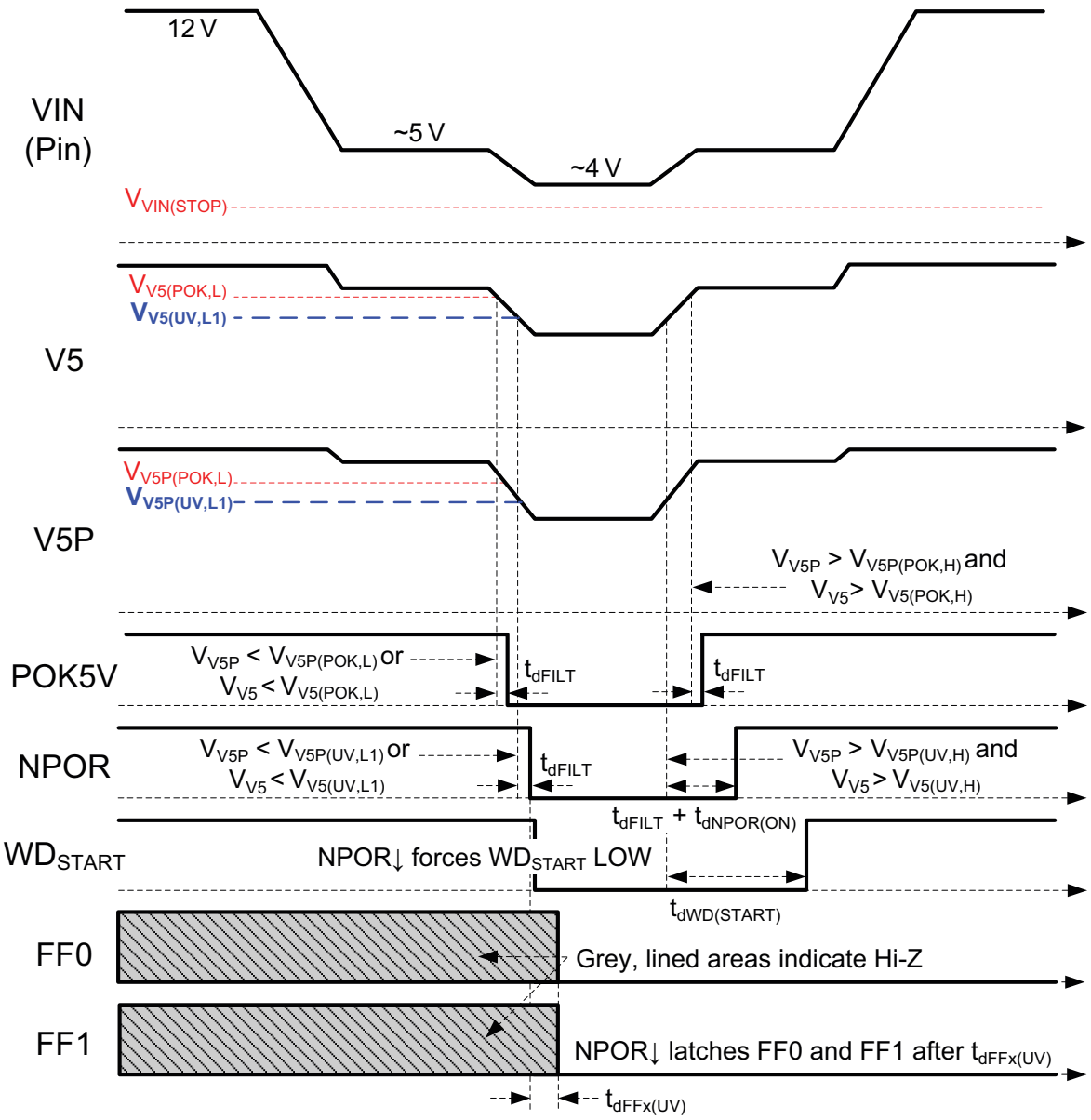

Figure 16: Low VIN Operation with MODE = Low, and ENB or ENBAT High

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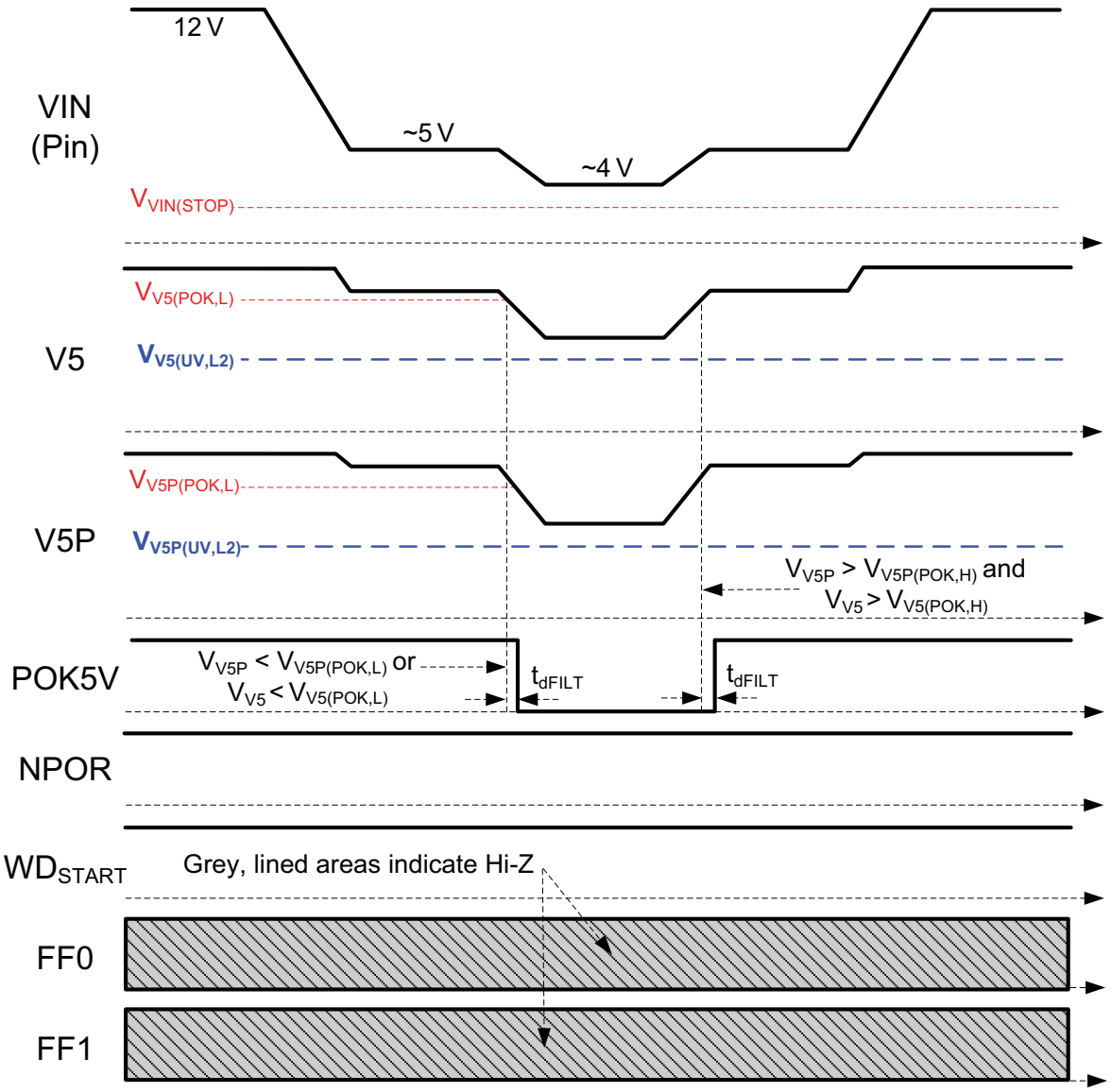

Figure 17: Low VIN Operation with MODE = High, and ENB or ENBAT High

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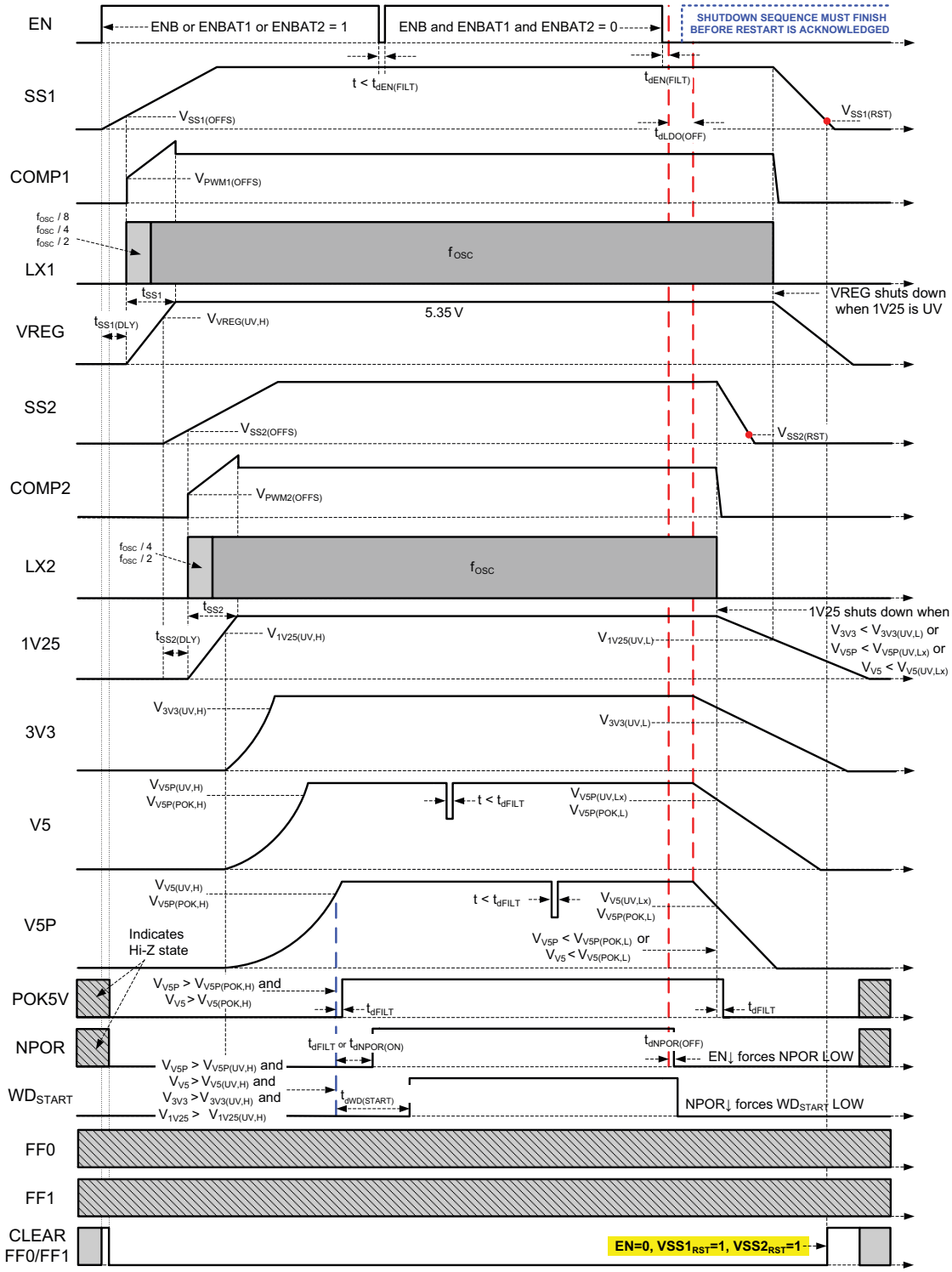

Figure 18: Startup and Shutdown due to EN while V_{VIN} = 12 V_{DC}

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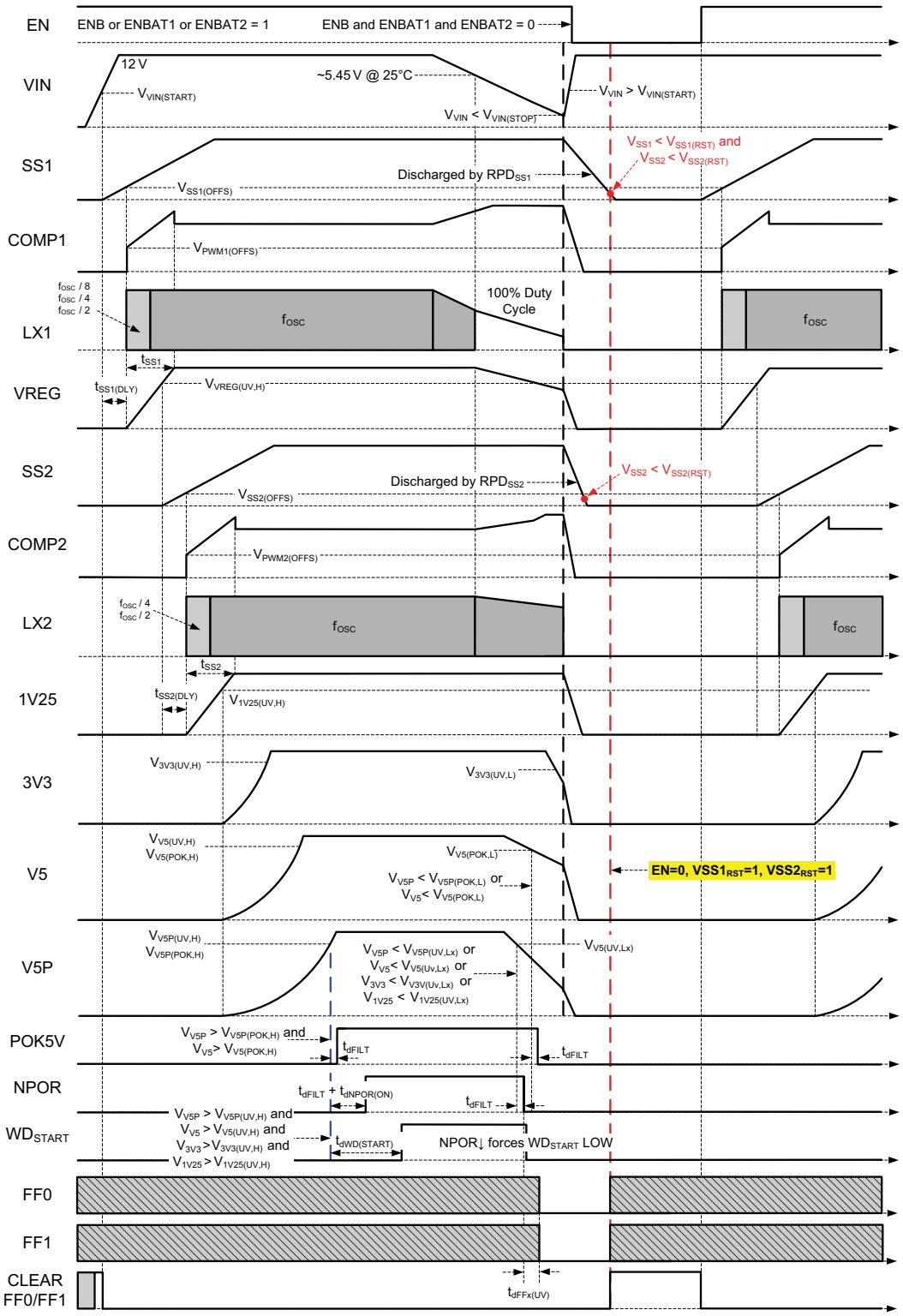

Figure 19: Startup and Dropout/Shutdown due to V_{VIN} while EN = 1

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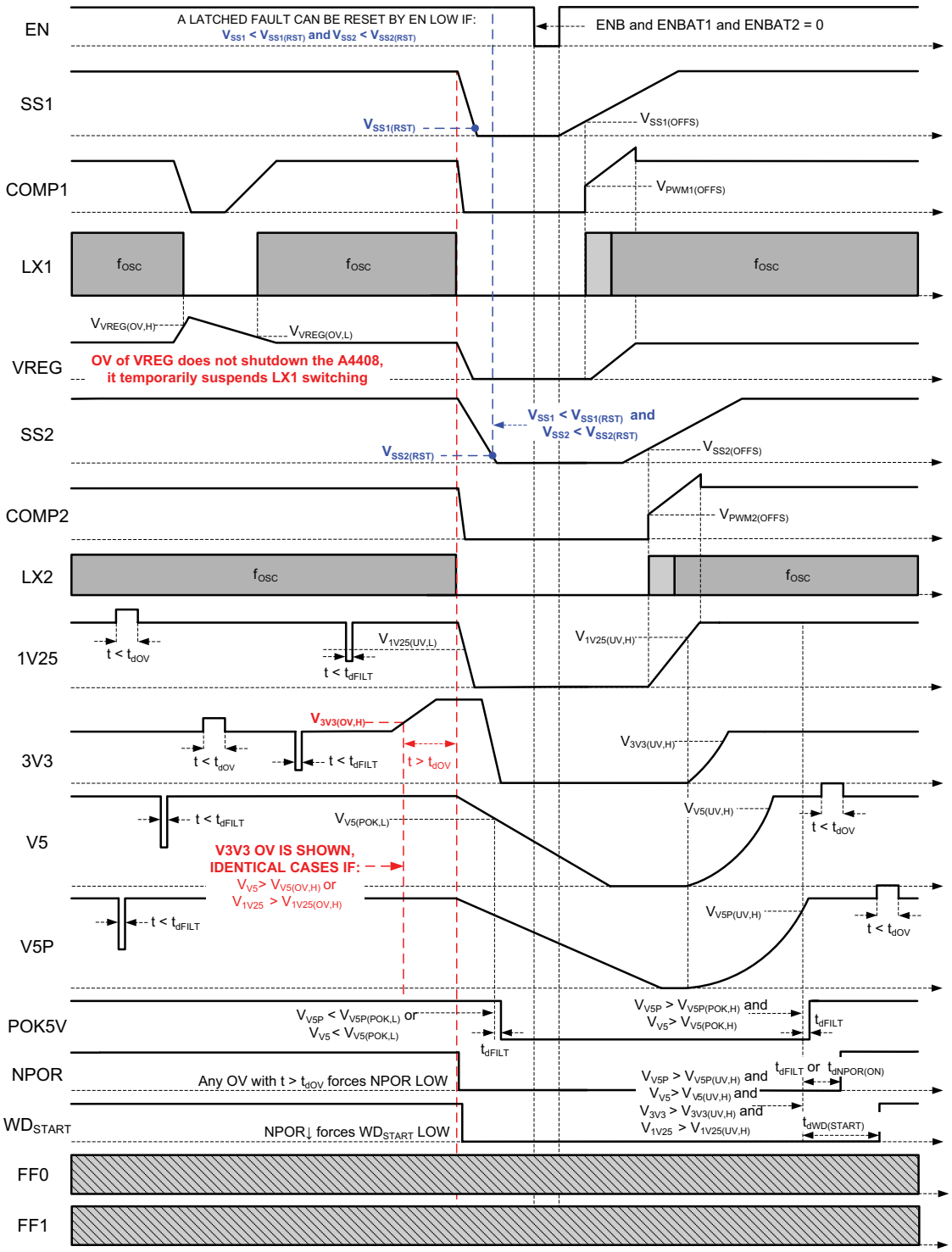

Figure 20: Overvoltage of VREG, Synchronous Buck, 3V3, or V5 with Reset by EN

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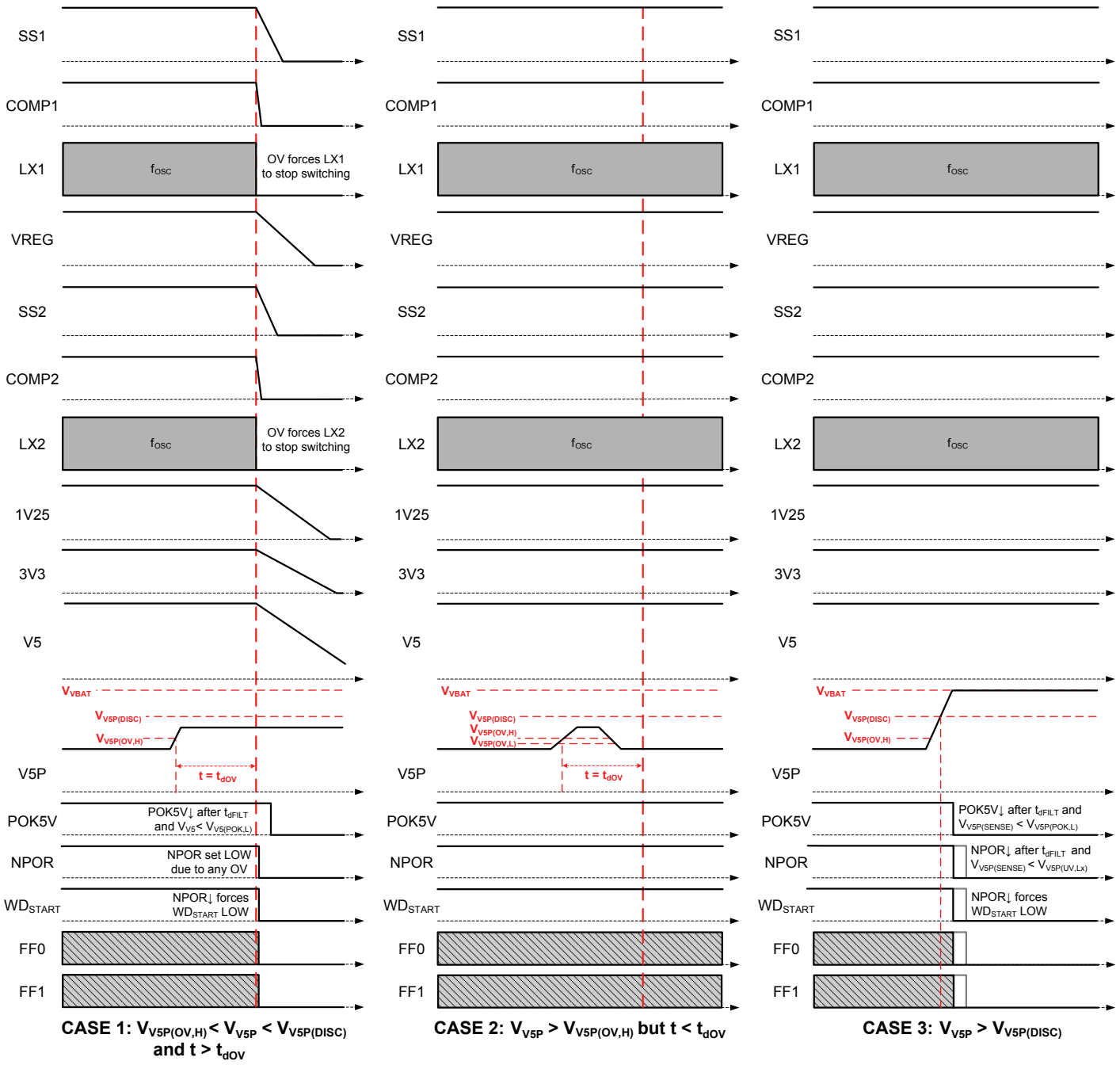

Figure 21: Possible Overvoltage Cases for V5P

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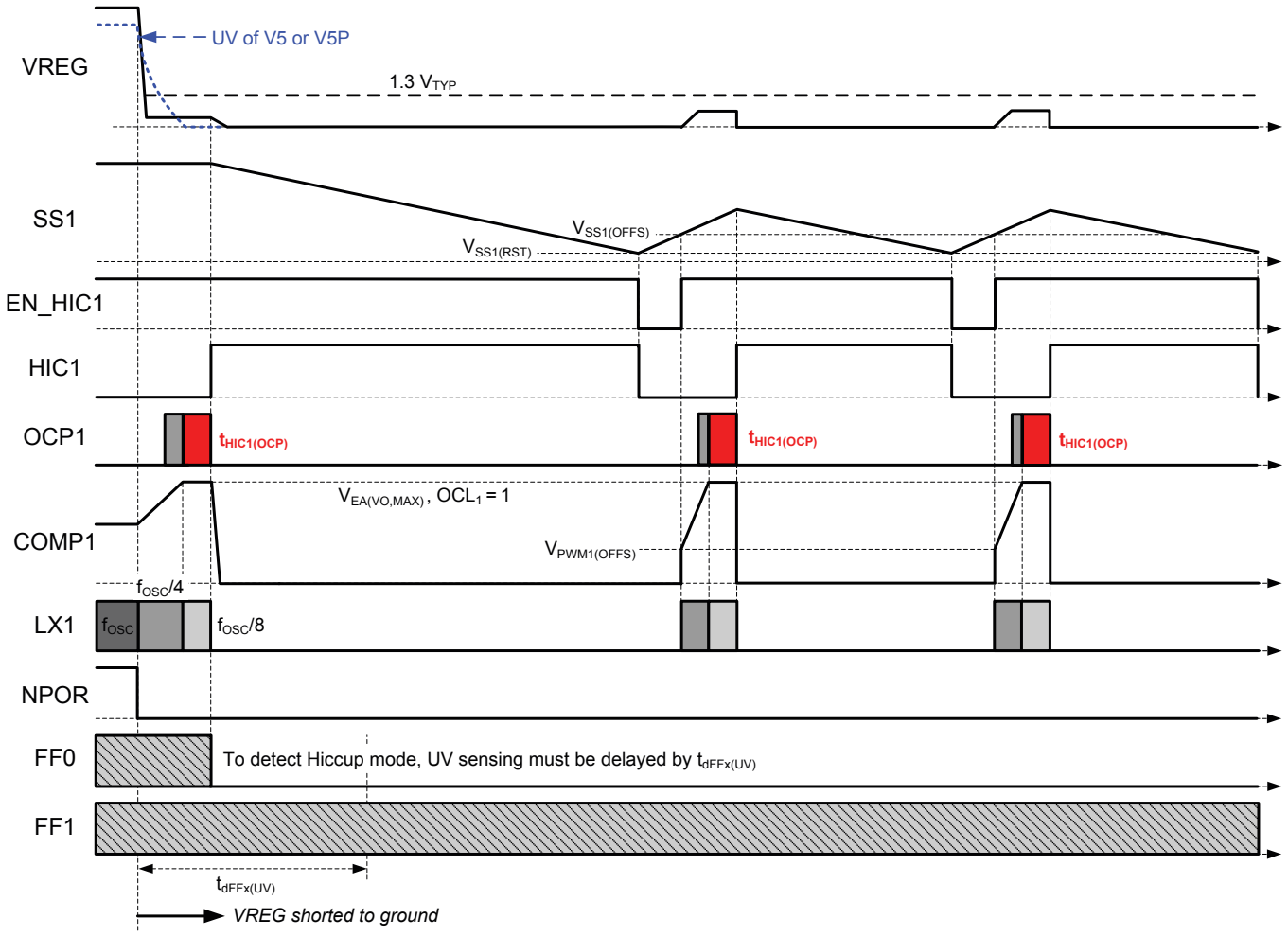

Figure 22: Hiccup Mode Operation when VREG is shorted to GND

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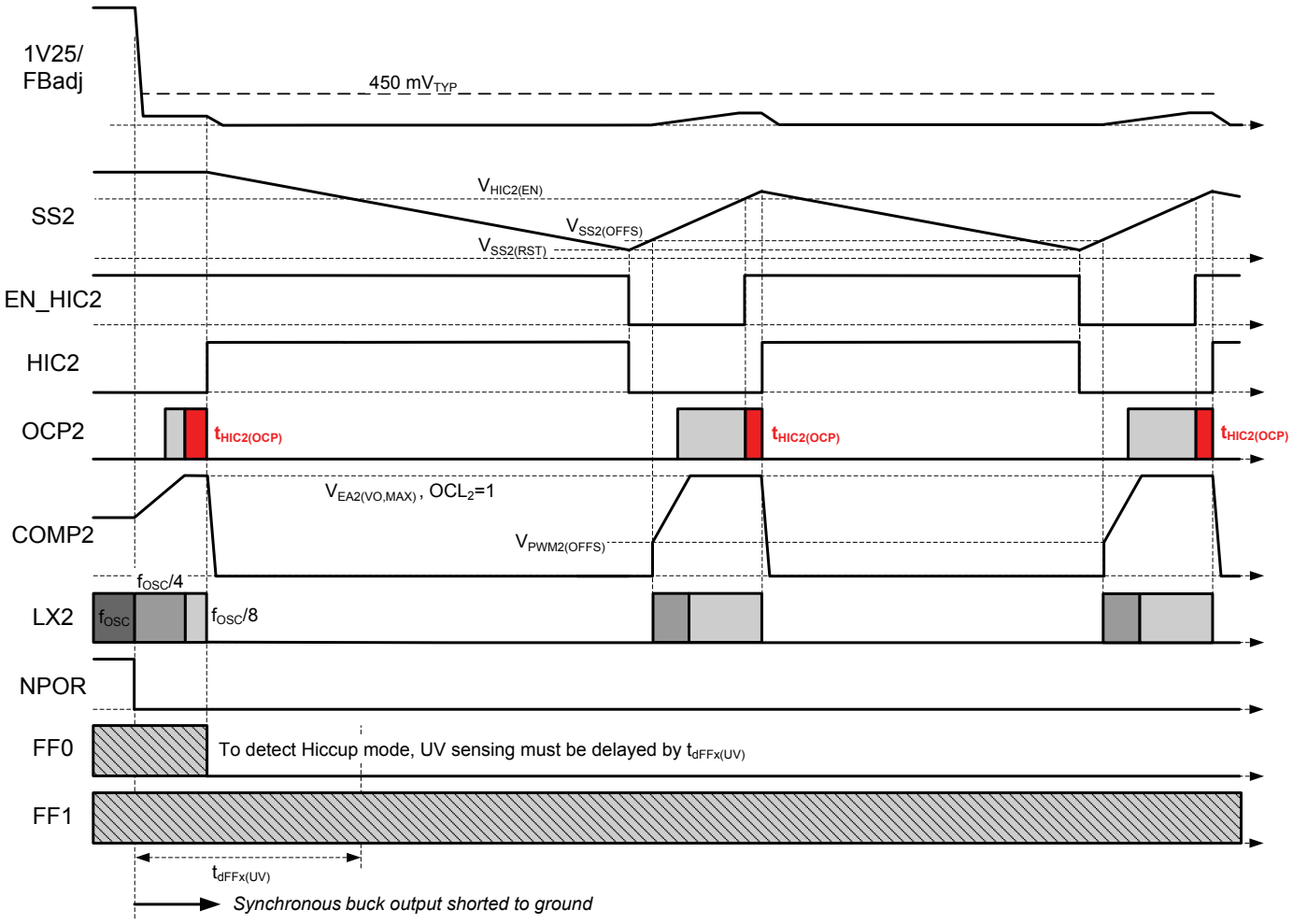

Figure 23: Hiccup Mode Operation when the Synchronous Buck output is shorted to GND

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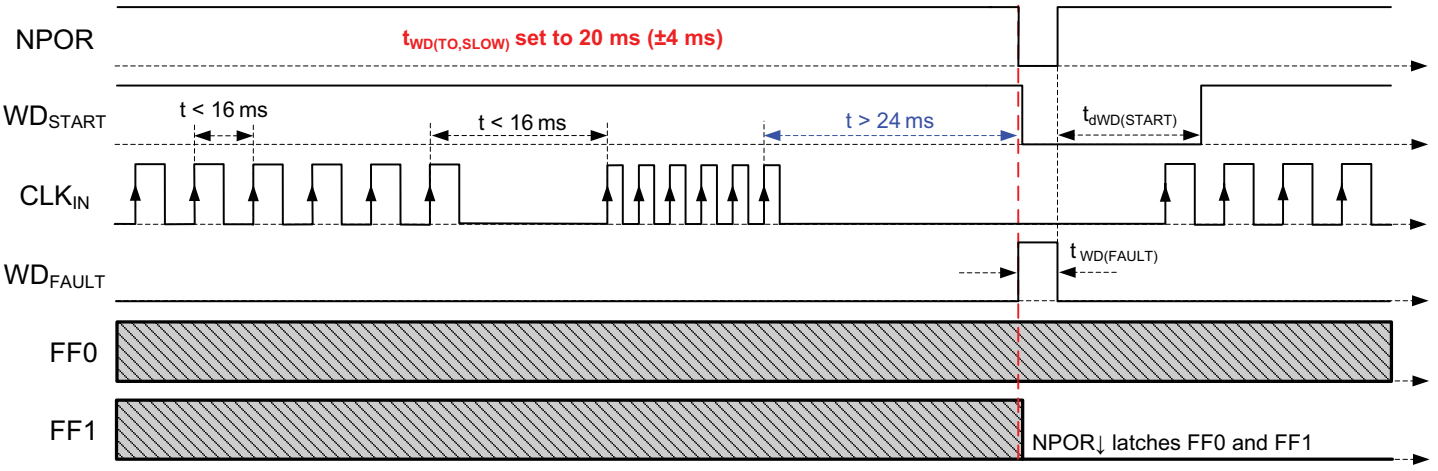

Figure 24: Typical Watchdog Timer Operation

WD will not indicate a fault if the rising edges of CLK_{IN} occur within 16 ms of each other.
WD will indicate a fault if the rising edges of CLK_{IN} occur more than 24 ms apart.

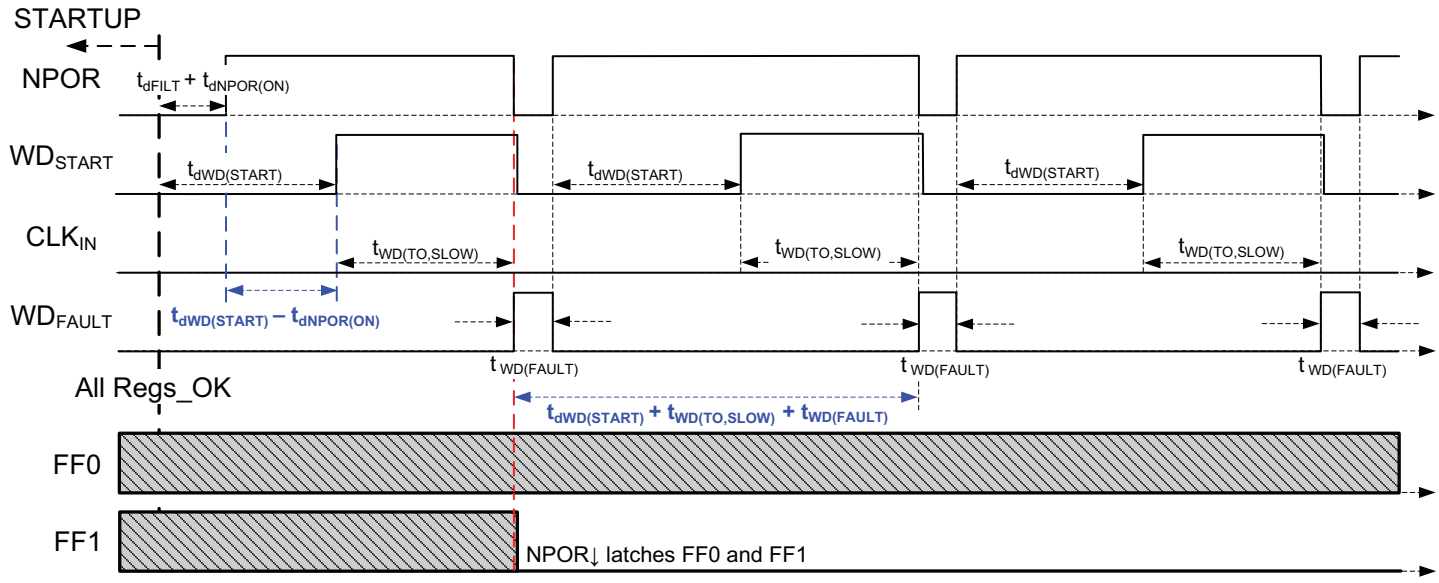

Figure 25: Watchdog Timer Operation Showing Start Delay and Missing CLK_{IN}

After startup, if CLK_{IN} is stuck low (or high), NPOR will periodically pulse LOW for 2 ms.
The time between NPOR fault indications will be $t_{dWD(START)} + t_{WD(TO,SLOW)} + t_{WD(FAULT)}$.

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DESIGN AND COMPONENT SELECTION

PWM Switching Frequency (R_{FSET})

When the PWM switching frequency is chosen, the designer should be aware of the minimum controllable on-time, $t_{ON(MIN)}$, of the A4408. If the system's required on-time is less than the A4408 minimum controllable on-time, then switch node jitter will occur and the output voltage will have increased ripple or oscillations.

The PWM switching frequency should be calculated using equation 1, where $t_{ON(MIN)}$ is the minimum controllable on-time of the A4408 (85 ns_{TYP}) and $V_{VIN(MAX)}$ is the maximum required operational input voltage (not the peak surge voltage).

$$f_{OSC} < \frac{5.35\ V}{t_{ON(MIN)} \times V_{VIN(MAX)}} \quad (1)$$

If the A4408 synchronization function is used, then the base oscillator frequency should be chosen such that jitter will not result at the maximum synchronized switching frequency according to equation 1.

Charge Pump Capacitors

The charge pump requires two capacitors: a 1 µF connected from pin VCP to VIN, and a 0.22 µF connected between pins CP1 and CP2. These capacitors should be high-quality ceramic capacitors, such as X5R or X7R, with voltage ratings of at least 16 V.

Pre-Regulator Output Inductor (L1)

For peak current-mode control, it is well known that the system will become unstable when the duty cycle is above 50% without adequate Slope Compensation (S_E). However, the slope compensation in the A4408 is a fixed value based on the oscillator frequency (f_{OSC}). Therefore, it's important to calculate an inductor value so the falling slope of the inductor current (S_F) will work well with the A4408 fixed slope compensation.

Equation 2 can be used to calculate a range of values for the output inductor for the pre-regulator. In equation 2, slope compensation (S_{E1}) is a function of the switching frequency (f_{OSC}) according to equation 3, and V_F is the asynchronous diodes forward voltage.

$$\frac{(5.25\ V + V_F)}{S_{E1}} \le L1 \le \frac{(5.45\ V + V_F)}{\frac{S_{E1}}{2}} \quad (2)$$

$$S_{E1} = 7.188 \times 10^{-4} \times f_{OSC} + 0.0425 \quad (3)$$

When using equations 2 and 3, f_{OSC} is in kHz, S_{E1} is in A/µs, and L1 will be in µH.

If equation 2 yields an inductor value that is not a standard value, then the next highest standard value should be used. The final inductor value should allow for 10%-20% of initial tolerance and 20%-30% of inductor saturation.

The inductor should not saturate given the peak operating current according to equation 4. In equation 4, $V_{VIN(MAX)}$ is the maximum continuous input voltage, such as 18 V, and V_F is the asynchronous diodes forward voltage.

$$I_{PEAK1} = 5.1\ A - \frac{S_{E1} \times (5.25\ V + V_F)}{1.1 \times f_{OSC} \times (V_{VIN(MAX)} + V_F)} \quad (4)$$

After an inductor is chosen, it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to ground at maximum continuous input voltage and the highest expected ambient temperature.

The inductor ripple current can be calculated using equation 5.

$$\Delta I_{L1} = \frac{(V_{VIN} - 5.35\ V) \times 5.35\ V}{f_{OSC} \times L_1 \times V_{VIN}} \quad (5)$$

Pre-Regulator Output Capacitance

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage, and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

Within the first few PWM cycles, the deviation of V_{VREG} will depend mainly on the magnitude of the load step (ΔI_{LOAD1}), the value of the output inductor (L1), the output capacitance (C_{OUT}), and the maximum duty cycle of the pre-regulator (D_{MAX1}). Equations 6 and 7 can be used to calculate a minimum output capacitance to maintain V_{VREG} within 1% of its target for a 750 mA load step at only 6 V_{VIN}.

$$C_{OUT(VREG)} \ge \frac{L1 \times (750\ mA)^2}{2 \times (6.0\ V - 5.25\ V) \times (0.01 \times 5.25\ V) \times D_{MAX1}} \quad (6)$$

$$D_{MAX} = \left(\frac{1}{f_{OSC}} - 80\ ns\right) \times f_{OSC} \quad (7)$$

After the load transient occurs, the output voltage will deviate

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from its nominal value until the error amplifier can bring the output voltage back to its nominal value. The speed at which the error amplifier will bring the output voltage back to its setpoint will depend mainly on the closed-loop bandwidth of the system. Selection of the compensation components (R_{Z1}, C_{Z1}, C_{P1}) are discussed in more detail in the Pre-Regulator Compensation section of this datasheet.

The output voltage ripple (ΔV_{VREG}) is a function of the output capacitors parameters: C_{OUT}, ESR_{Co}, and ESL_{Co} according to equation 8.

$$\Delta V_{VREG} = \Delta I_L \times ESR_{Co} + \frac{V_{VIN} - V_{VREG}}{L_O} \times ESL_{Co} + \frac{\Delta I_L}{8 \times f_{OSC} \times C_{OUT}} \quad (8)$$

The type of output capacitors will determine which terms of equation 8 are dominant. For the A4408 and automotive environments, only ceramic capacitors are recommended. The ESR_{CO} and ESL_{CO} of ceramic capacitors are virtually zero, so the peak-to-peak output voltage ripple of V_{VREG} will be dominated by the third term of equation 8.

$$\Delta V_{VREG(PP)} = \frac{\Delta I_L}{8 \times f_{OSC} \times C_{OUT}} \quad (9)$$

Pre-Regulator Ceramic Input Capacitance

The ceramic input capacitors must limit the voltage ripple at the VIN pin to a relatively low voltage during maximum load. Equation 10 can be used to calculate the minimum input capacitance,

$$C_{IN} \geq \frac{I_{VREG(MAX)} \times 0.25}{0.90 \times f_{OSC} \times 50\,mV_{PP}} \quad (10)$$

where $I_{VREG(MAX)}$ is the maximum current from the pre-regulator,

$$I_{VREG(MAX)} = I_{V5} + I_{V5P} + I_{3V3} + \frac{V_{OUT(ADJ)} \times I_{OUT(ADJ)}}{5.25\ V \times 80\%} + 20\,mA \quad (11)$$

A good design should consider the DC bias effect on a ceramic capacitor—as the applied voltage approaches the rated value, the capacitance value decreases. The X7R-type capacitors should be the primary choices due to their stability versus both DC bias and temperature. For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size (i.e. 1206/16 V or 1210/50 V).

Also, for improved EMI/EMC performance, it is recommended that two small capacitors be placed as close as physically possible to the VIN pins to address frequencies above 10 MHz. For example, a 0.1 µF/X7R/0603 and a 220 pF/COG/0402 capacitor will address frequencies up to 20 MHz and 200 MHz, respectively.

Pre-Regulator Asynchronous Diode (D1)

The highest peak current in the asynchronous diode (D1) occurs during overload and is limited by the A4408. Equation 4 can be used to calculate this current.

The highest average current in the asynchronous diode occurs when V_{VIN} is at its maximum, D_{BOOST} = 0%, and D_{BUCK} = minimum (10%),

$$I_{AVG} = (1 - D_{BUCK}) \times I_{VREG(MAX)} = 0.9 \times I_{VREG(MAX)} \quad (12)$$

where $I_{VREG(MAX)}$ is calculated using equation 11.

Pre-Regulator Boost MOSFET (Q1)

The maximum RMS current in the boost MOSFET (Q1) occurs when V_{VIN} is very low and the boost operates at its maximum duty cycle,

$$I_{Q1(RMS)} = \sqrt{D_{MAX(BST)} \times \left[\left(I_{PEAK1} - \frac{\Delta I_{L1}}{2}\right)^2 + \frac{\Delta I_{L1}}{12}\right]} \quad (13)$$

where I_{PEAK1} and ΔI_{L1} are derived using equations 4 and 5, respectively, and $D_{MAX(BST)}$ is identified in the Electrical Characteristics table.

The boost MOSFET should have a total gate charge of less than 14 nC at a V_{GS} of 5 V. The V_{DS} rating of the boost MOSFET should be at least 20 V. Several recommended part numbers are shown in the Functional Block Diagram / Typical Schematic.

Pre-Regulator Boost Diode (D2)

In buck mode, the maximum average current in this diode is simply the output current, calculated with equation 11. However, in buck-boost mode, the peak currents in this diode may increase significantly. The A4408 will limit the current to the value calculated by equation 4.

Pre-Regulator Soft-Start and Hiccup Timing (C_{SS1})

The soft-start time of the pre-regulator is determined by the value of the capacitance at the soft-start pin (C_{SS1}).

If the A4408 is starting into a very heavy load, a very fast soft-start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. This occurs because the total of the full load current, the inductor ripple current, and the additional current required to charge the output capacitors ($I_{C(OUT)} = C_{OUT} \times V_{OUT} / t_{SS}$) is higher than the pulse-by-pulse current threshold, as shown in Figure 26.

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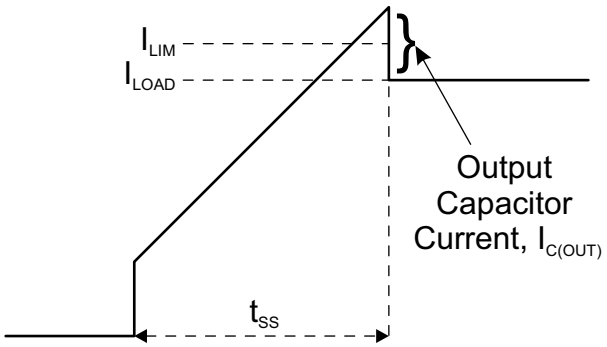

Figure 26: Output Current (I_{CO}) During Startup

To avoid prematurely triggering hiccup mode, the soft-start time (t_{SS1}) should be calculated using equation 14,

$$t_{SS1} = 5.35\ V \times \frac{C_{OUT}}{I_{C(OUT)}} \qquad (14)$$

where C_{OUT} is the output capacitance, and $I_{C(OUT)}$ is the amount of current allowed to charge the output capacitance during soft-start (recommend 0.1 A < $I_{C(OUT)}$ < 0.3 A). Higher values of $I_{C(OUT)}$ result in faster soft-start time, and lower values of $I_{C,OUT}$ ensure that hiccup mode is not falsely triggered. Allegro recommends starting the design with an $I_{C(OUT)}$ of 0.1 A and increasing it only if the soft-start time is too slow.

Then, C_{SS1} can be calculated based on equation 15:

$$C_{SS1} \geq \frac{I_{SS1(SU)} \times t_{SS1}}{0.8\ V} \qquad (15)$$

If a non-standard capacitor value for C_{SS1} is calculated, the next higher value should be used.

The voltage at the soft-start pin will start from 0 V and will be charged by the soft-start current ($I_{SS1(SU)}$). However, PWM switching will not begin immediately because the voltage at the soft-start pin must rise above the soft-start offset voltage ($V_{SS1(OFFS)}$). The soft-start delay ($t_{SS1(DLY)}$) can be calculated using equation 16.

$$t_{SS1(DLY)} = C_{SS1} \times \frac{V_{SS1(OFFS)}}{I_{SS1(SU)}} \qquad (16)$$

When the A4408 is in hiccup mode, the soft-start capacitor sets the hiccup period. During a startup attempt, the soft-start pin charges the soft-start capacitor with $I_{SS1(SU)}$ and discharges the same capacitor with $I_{SS1(HIC)}$ between startup attempts.

Pre-Regulator Compensation (R_{Z1}, C_{Z1}, C_{P1})

Although the A4408 can operate in buck-boost mode at low input voltages, it still can be considered a buck converter when examining the control loop. The following equations can be used to calculate the compensation components.

First, select the target crossover frequency for the final system. While switching at over 2 MHz, the crossover is governed by the required phase margin. Since a type II compensation scheme is used, the system is limited to the amount of phase that can be added. Hence, a crossover frequency (f_{C1}) in the region of 35 kHz is selected. The total system phase will drop off at crossover frequencies about 100 kHz. The R_{Z1} calculation is based on the gain required to set the crossover frequency and can be calculated by equation 17.

$$R_{Z1} = \frac{13.38 \times \pi \times f_{C1} \times C_{OUT}}{gm_{POWER1} \times gm_{EA1}} \qquad (17)$$

The series capacitor (C_{Z1}) along with the resistor (R_{Z1}) set the location of the compensation zero. This zero should be placed no lower than ¼ of the crossover frequency and should be kept to minimum value. Equation 18 can be used to estimate this capacitor value.

$$C_{Z1} > \frac{4}{2\pi \times R_{Z1} \times f_{C1}} \qquad (18)$$

Allegro recommends adding a small capacitor (C_{P1}) in parallel with the series combination of R_{Z1}/C_{Z1} to roll off the error amps gain at high frequency. This capacitor usually helps reduce LX1 pulse-width jitter, but if too large, it will also decrease the loop's phase margin.

Allegro recommends using this capacitor to set a pole at approximately 5× the loop's crossover frequency (f_{C1}), as shown in equation 19. If a non-standard capacitor value results, the next higher available value should be used.

$$C_{P1} \approx \frac{1}{2\pi \times R_{Z1} \times 5 \times f_{C1}} \qquad (19)$$

An Excel-based design tool is available from Allegro that accepts customer specifications and recommends values for both the power and compensation components. The pre-regulator bode plot in Figure 27 was generated with this tool. The bandwidth of this system (f_{C1}) is 30 kHz, the phase margin (PM1) is 61 degrees, and the gain margin (GM1) is 25 dB.

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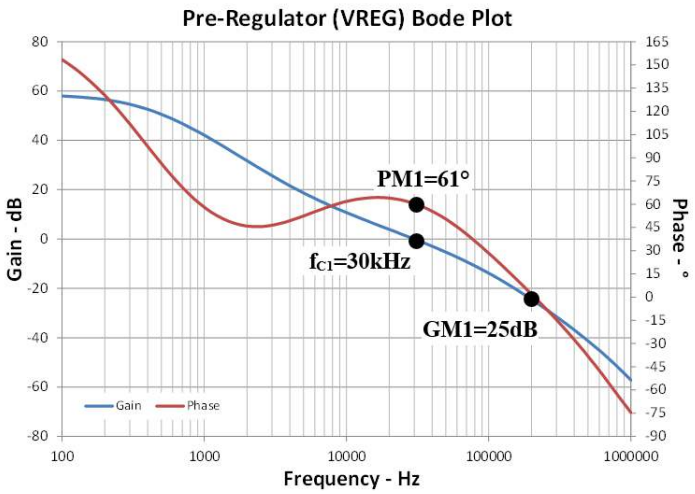

Figure 27: Bode Plot for the Pre-Regulator

R_{Z1} = 22.1 kΩ, C_{Z1} = 1.5 nF, C_{P1} = 47 pF
Lo = 4.7 µH, Co = 5 × 10 µF/16 V/1206

Synchronous Buck Component Selection

Similar design methods can be used for the synchronous buck; however, the complexity of variable input voltage and boost operation are removed.

Setting the Output Voltage (R_{FB1} and R_{FB2})

The A4408 was optimized to deliver 1.25 V from the synchronous buck—where the output of the synchronous buck is connected directly to the $FB_{1V25/ADJ}$ pin. The absence of a resistor divider from VOUT to the $FB_{1V25/ADJ}$ pin results in robust fault conditions (i.e. if the feedback trace is open, the output of the synchronous buck will be 0 V).

If required, the output of the synchronous buck may be programmed from 1.25 to 3.3V. This is achieved by adding a resistor divider from its output to ground and connecting the center point to the $FB_{1V25/ADJ}$ pin, as shown in Figure 28.

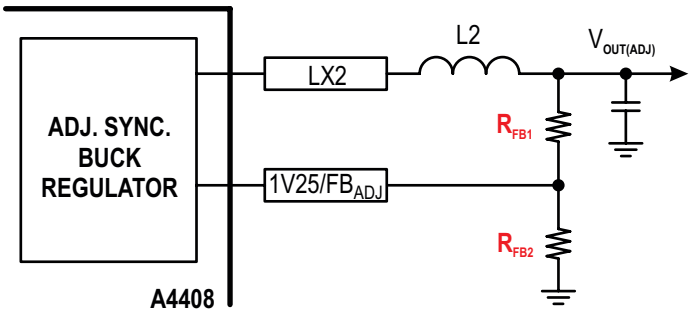

Figure 28: Setting the Synchronous Buck Output

The ratio of the feedback resistors can be calculated based on equation 20.

$$\frac{R_{FB1}}{R_{FB2}} = \left(\frac{V_{OUT(ADJ)}}{1.25\ V} - 1\right) \quad (20)$$

Synchronous Buck Output Inductor (L2)

Equation 21 can be used to calculate a range of values for the output inductor for the synchronous buck regulator. Slope compensation (S_{E2}) can be calculated using equation 22.

$$\frac{V_{OUT(ADJ)}}{2 \times S_{E2}} \leq L2 \leq \frac{V_{OUT(ADJ)}}{S_{E2}} \quad (21)$$

$$S_{E2} = 3.063 \times 10^{-4} \times f_{OSC} + 0.0175 \quad (22)$$

When working with equations 21 and 22, f_{OSC} is in kHz, S_{E2} is in A/µs, and L2 will be in µH.

If equation 21 yields an inductor value that is not a standard value, then the next closest available value should be used. The final inductor value should allow for 10%-20% of initial tolerance and 20%-30% for inductor saturation.

The inductor should not saturate given the peak current at overload according to equation 23.

$$I_{PEAK2} = 2.4\ A - \frac{S_{E2} \times V_{OUT(ADJ)}}{1.1 \times f_{OSC} \times 5.45\ V} \quad (23)$$

Once the inductor value is known, the ripple current can be calculated using equation 24.

$$\Delta I_{L2} = \frac{(5.35\ V \times V_{OUT(ADJ)}) \times V_{OUT(ADJ)}}{f_{OSC} \times L2 \times 5.35\ V} \quad (24)$$

Synchronous Buck Output Capacitance

Within the first few PWM cycles, the deviation of $V_{OUT(ADJ)}$ will depend mainly on the magnitude of the load step (ΔI_{LOAD2}), the value of the output inductor (L2), the output capacitance ($C_{OUT(ADJ)}$), and the maximum duty cycle of the synchronous converter (D_{MAX2}). Equations 25 and 26 can be used to calculate a minimum output capacitance to maintain 1.25 V within 1.2% of its target for a 400 mA load step.

$$C_{OUT(1V25)} \geq \frac{L2 \times (400\ mA)^2}{2 \times V_{OUT(ADJ)} \times (0.012 \times 1.25V) \times D_{MAX2}} \quad (25)$$

$$D_{MAX2} = \left(\frac{1}{f_{OSC}} - 110\ ns\right) \times f_{OSC} \quad (26)$$

After the load transient occurs, the output voltage will deviate from its nominal value until the error amplifier can bring the output voltage back to its nominal value. The speed at which the error amplifier will bring the output voltage back to its setpoint will depend mainly on the closed-loop bandwidth of the system. Selection of the compensation components (R_{Z2}, C_{Z2}, C_{P2}) are discussed in more detail in the Synchronous Buck Compensation section of this datasheet.

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Allegro recommends the use of ceramic capacitors for the synchronoous buck. The peak-to-peak voltage ripple of the synchronous buck ($\Delta V_{OUT(ADJ,PP)}$) can be calculated with equation 27.

$$\Delta V_{VOUT(ADJ,PP)} = \frac{\Delta I_{L2}}{8 \times f_{OSC} \times C_{OUT(ADJ)}} \quad (27)$$

Synchronous Buck Compensation (R_{Z2}, C_{Z2}, C_{P2})

Again, similar techniques as used with the pre-regulator can be used to compensate the synchronous buck.

For the synchronous buck, select 100 kHz for the crossover frequency (f_{C2}) of the synchronous buck. Then, equation 28 can be used to calculate R_{Z2}.

$$R_{Z2} = \frac{V_{OUT(ADJ)} \times 2\pi \times f_{C2} \times C_{OUT(ADJ)}}{1.25\ V \times gm_{POWER2} \times gm_{EA2}} \quad (28)$$

The series capacitor (C_{Z2}) along with the resistor (R_{Z2}) set the location of the compensation zero. This zero should be placed no lower than ¼ of the crossover frequency and should be kept to minimum value. Equation 29 can be used to estimate this capacitor value.

$$C_{Z2} > \frac{4}{2\pi \times R_{Z2} \times f_{C2}} \quad (29)$$

Allegro recommends adding a small capacitor (C_{P2}) in parallel with the series combination of R_{Z2}/C_{Z2} to roll off the error amp gain at high frequency. This capacitor usually helps reduce LX2 pulse-width jitter, but if too large, it will also decrease the loop's phase margin.

Allegro recommends using this capacitor to set a pole at approximately 8× the loop's crossover frequency (f_{C2}), as shown in equation 30. If a non-standard capacitor value results, use the next higher available value.

$$C_{P2} \approx \frac{1}{2\pi \times R_{Z2} \times 8 \times f_{C2}} \quad (30)$$

Allegro's Excel-based design tool accepts specifications for the synchronous buck and recommends values for both the power and compensation components. The synchronous buck bode plot in Figure 29 was generated with this tool. The bandwidth of this system (f_{C2}) is 90 kHz, the phase margin (PM2) is 56 degrees, and the gain margin (GM2) is 17 dB.

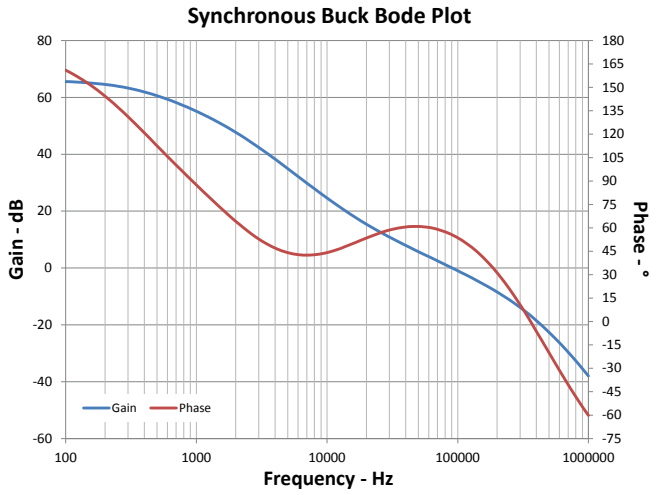

Figure 29: Bode Plot for the Sync. Buck at 1.25 V_{OUT}

R_{Z2} = 6.81 kΩ, C_{Z2} = 1.5 nF, C_{P2} = 47 pF
L2 = 4.7 µH, $C_{OUT(ADJ)}$ = 3 × 10 µF/16 V/1206

Synchronous Buck Soft-Start and Hiccup Timing

The soft-start time of the synchronous buck is determined by the value of the capacitance at the soft-start pin (C_{SS2}).

If the A4408 is starting into a very heavy load, a very fast soft-start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. To avoid prematurely triggering hiccup mode, the soft-start time (t_{SS2}) should be calculated according to equation 31,

$$t_{SS2} = V_{OUT(ADJ)} \times \frac{C_{OUT(ADJ)}}{I_{C(OUT)}} \quad (31)$$

where $V_{OUT(ADJ)}$ is the output voltage, $C_{OUT(ADJ)}$ is the output capacitance, $I_{C(OUT)}$ is the amount of current allowed to charge the output capacitance during soft-start (recommend 75 mA < $I_{C(OUT)}$ < 150 mA). Higher values of $I_{C(OUT)}$ result in faster soft-start times and lower values of $I_{C(OUT)}$ ensure that hiccup mode is not falsely triggered. For the synchronous buck, Allegro recommends starting the design with an $I_{C(OUT)}$ of 100 mA and increasing it only if the soft-start time is too slow.

Then, C_{SS2} can be selected based on equation 32,

$$C_{SS2} > \frac{I_{SS2(SU)} \times t_{SS2}}{1.25\ V} \quad (32)$$

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If a non-standard capacitor value for C_{SS2} is calculated, the next larger value should be used.

The voltage at the soft-start pin will start from 0 V and will be charged by the soft-start current ($I_{SS2(SU)}$). However, PWM switching will not begin instantly because the voltage at the soft-start pin must rise above the soft-start offset voltage ($V_{SS2(OFFS)}$). The soft-start delay ($t_{SS2(DLY)}$) can be calculated using equation 33,

$$t_{SS2(DLY)} = C_{SS2} \times \left(\frac{V_{SS2(OFFS)}}{I_{SS2(SU)}} \right) \quad (33)$$

When the A4408 is in hiccup mode, the soft-start capacitor sets the hiccup period. During a startup attempt, the soft-start pin charges the soft-start capacitor with $I_{SS2(SU)}$ and discharges the same capacitor with $I_{SS1(HIC)}$ between startup attempts.

Linear Regulators

The three linear regulators only require a single ceramic capacitor located near the A4408 to ensure stable operation. The range of acceptable values is shown in the Electrical Characteristics table. A 2.2 µF capacitor per regulator is a good starting point.

As the LDO outputs are routed throughout the PCB, it is recommended that a 0.1 µF/0603 ceramic capacitor be placed as close as possible to each load point for local filtering and high-frequency noise reduction.

Also, since the V5P output may be used to power remote circuitry, its load may include external wiring. The inductance of this wiring will cause LC-type ringing and negative spikes at the V5P pin if a “fast” short-to-ground occurs. It is recommended that a small Schottky diode be placed close to the V5P pin to limit the negative voltages, as shown in the Applications Schematic. The MSS1P5 (or equivalent) is a good choice.

Internal Bias (V_{CC})

The internal bias voltage should be decoupled at the VCC pin using a 1 µF ceramic capacitor. It is not recommended to use this pin as a source.

Signal Pins (NPOR, POK5V, FF0, FF1)

The A4408 has many signal-level pins. The NPOR, POK5V, FF0, and FF1 are open-drain outputs and require external pull-up resistors. Allegro recommends sizing the external pull-up resistors so each pin will sink less than 2 mA when it is a logic

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low.

RC Snubber Calculations (R_{SNUBx}, C_{SNUBx})

Allegro strongly recommends including provisions for RC snubbers from LX1, LX2, and LXb to ground, as shown in the Applications Schematic. The LX1 and LX2 snubbers are required to meet automotive EMC requirements. The LXb snubber may be needed to reduce system noise when V_{VIN} is less than 7 V and the boost MOSFET (LG pin) starts switching. If the A4408 is used in buck-only mode, the LXb snubber is not necessary. A simple method to calculate the RC snubber component values is presented here.

Use the tip-and-barrel technique on a oscilloscope probe to measure the frequency of the turn-on ringing of the LX node without an RC snubber. The oscilloscope bandwidth must be set to its maximum, at least 200 MHz. The tip-and-barrel oscilloscope probe technique is show in Figure 30. Typical LX ringing and frequency without a snubber are shown in Figure 31.

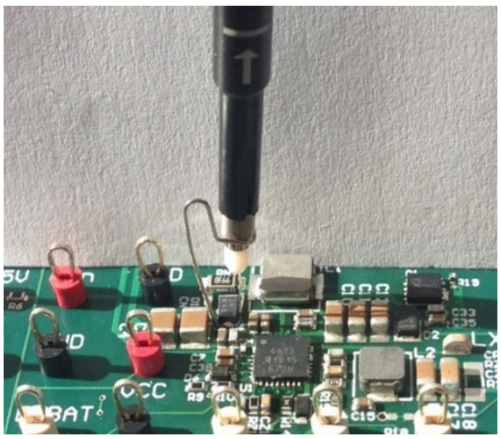

Figure 30: Measuring LX ringing with tip-and-barrel

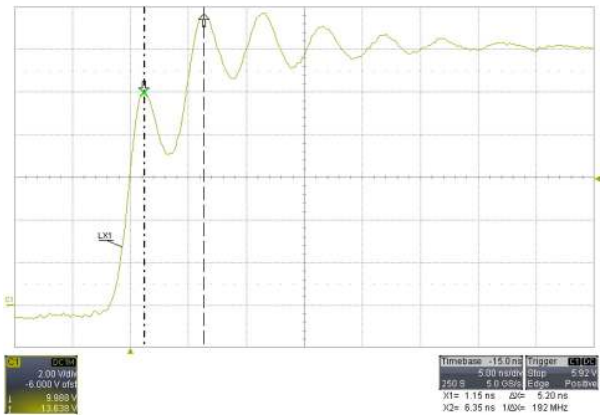

Figure 31: Typical LX1 ring frequency at turn-on without a snubber and V_{VIN} = 12 V: f_{RING} = 192 MHz

After the ring frequency has been measured, the total capacitance at the LX node must be estimated. For the buck-boost pre-regulator, the LX1 pin (5 to 10 pF), the PCB (10 to 30 pF), and the asynchronous diode will all contribute to the capacitance. The asynchronous diode junction capacitance (~70 pF at 12 V_R) is usually shown in the datasheet, as shown in Figure 32.

For the synchronous buck, there is no external diode, so the total capacitance will consist of the LX2 pin, the internal synchronous MOSFET (10 to 20 pF), and the PCB.

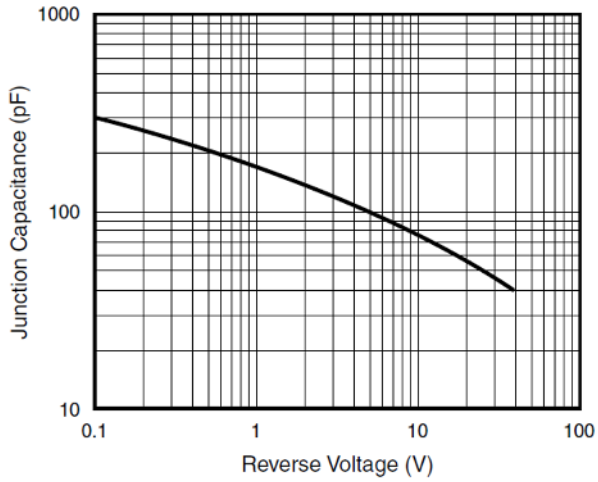

Figure 32: Typical diode junction capacitance

The total capacitance is calculated using equation 34,

$$C_{TOT} = C_{DIODE} + C_{LX1\_PIN} + C_{PCB} \quad (34)$$

$$= 70\ pF + 7.5\ pF + 20\ pF = 97.5\ pF$$

Knowing the ring frequency and the total capacitance, the inductive component of the ringing can be calculated using equation 35.

$$L_{RING} = \frac{1}{4 \times \pi^2 \times f_{RING}^2 \times C_{TOT}} \quad (35)$$

$$L_{RING} = \frac{1}{4 \times \pi^2 \times 192\ MHz^2 \times 97.5\ pF} = 7.05\ nH$$

The snubber resistor is calculated using equation 36.

$$R_{SNUB} = \sqrt{\frac{L_{RING}}{C_{TOT}}} \quad (36)$$

$$R_{SNUB} = \sqrt{\frac{7.05\ nH}{97.5\ pF}} = 8.66\ \Omega\ (standard\ value)$$

Finally, the snubber capacitor can be calculated using equa-

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tion 37. If equation 37 results in a non-standard value, use the next higher standard value.

$$C_{SNUB} = \frac{1}{2.5 \times f_{RING} \times R_{SNUB}} \quad (37)$$

$$C_{SNUB} = \frac{1}{2.5 \times 192\ MHz \times 8.66\ \Omega} = 270\ pF\ (standard)$$

It is very important to calculate the power dissipated by the resistor at the maximum steady-state (DC) input operating voltage, using equation 38. Once the maximum power dissipation is known, an adequate component considering power derating at the maximum ambient temperature can be chosen. In this example, $V_{VIN(MAX,DC)}$ = 18 V and f_{OSC} = 2.2 MHz is used.

$$P_{SNUB} = \tfrac{1}{2} \times C_{SNUB} \times V_{VIN}^2 \times f_{SW} \quad (38)$$

$$P_{SNUB} = \tfrac{1}{2} \times 270\ pF \times 18\ V^2 \times 2.2\ MHz = 96\ mW$$

To support 100 mW at high ambient temperature, a 1206 size resistor is needed. A 1206 size resistor can dissipate 250 mW up to 100°C and 100 mW (40%) up to almost 135°C, as shown in Figure 33.

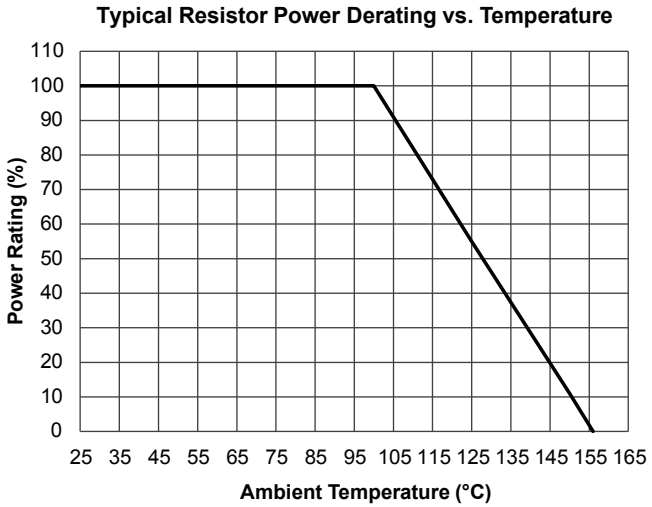

Figure 33: Resistor power derating

versus ambient temperature

Figure 34 shows the LX waveform with the RC snubber components, 8.66 Ω + 270 pF—the 192 MHz high-frequency ringing has been eliminated.

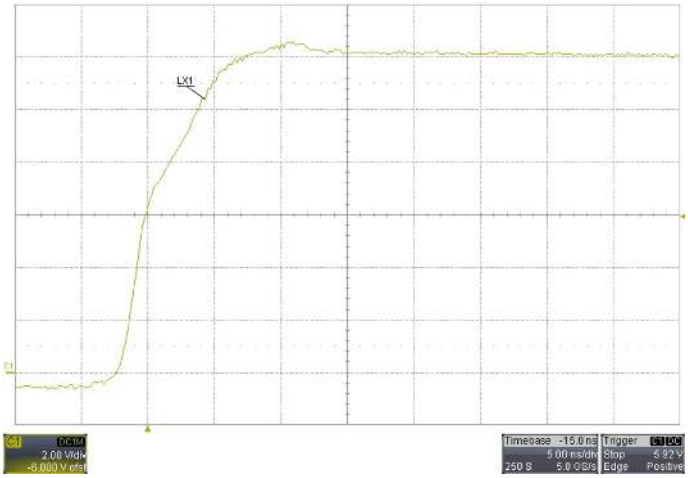

Figure 34: LX1 waveform including an RC snubber consisting of 8.66 Ω + 270 pF

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PCB LAYOUT RECOMMENDATIONS

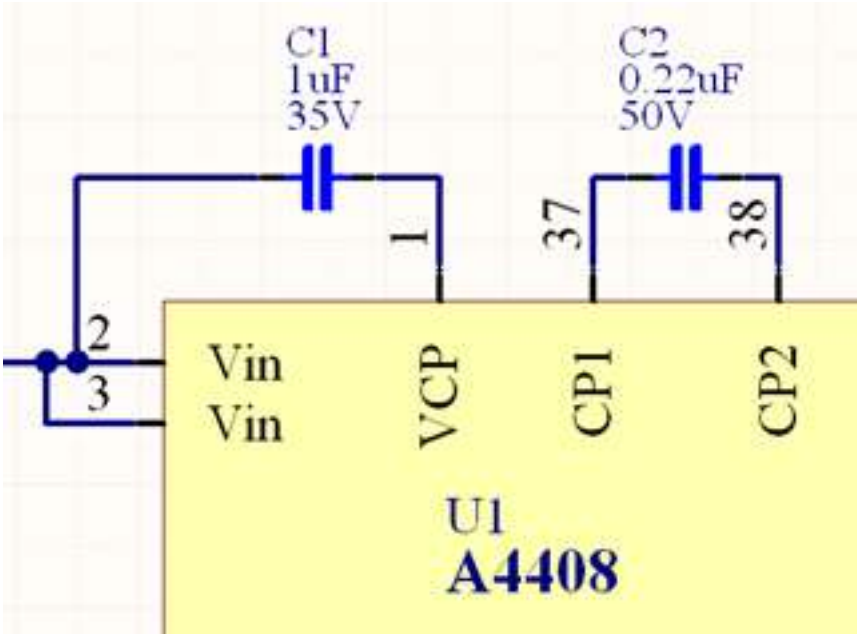

Figure 35: Charge Pump capacitor C1 and C2.
Place these components near pins 1, 2, 37, and 38.

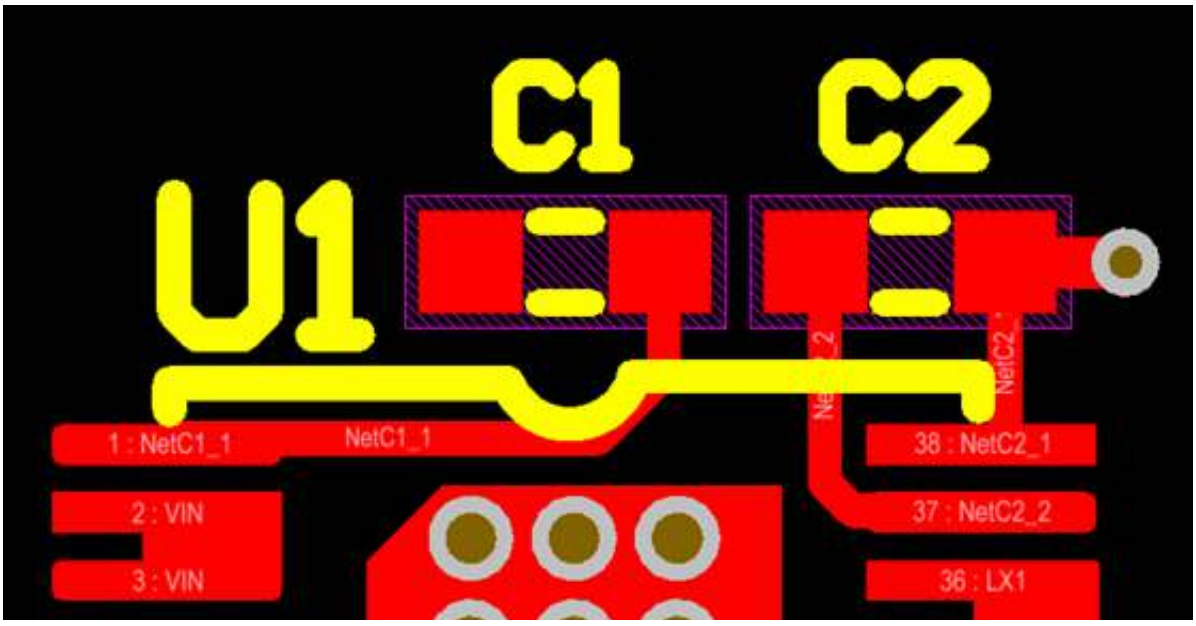

Figure 36: Recommended placement and connection of the two charge pump capacitors.
1) Start the layout by placing these components near pins 1, 2, 37, and 38.

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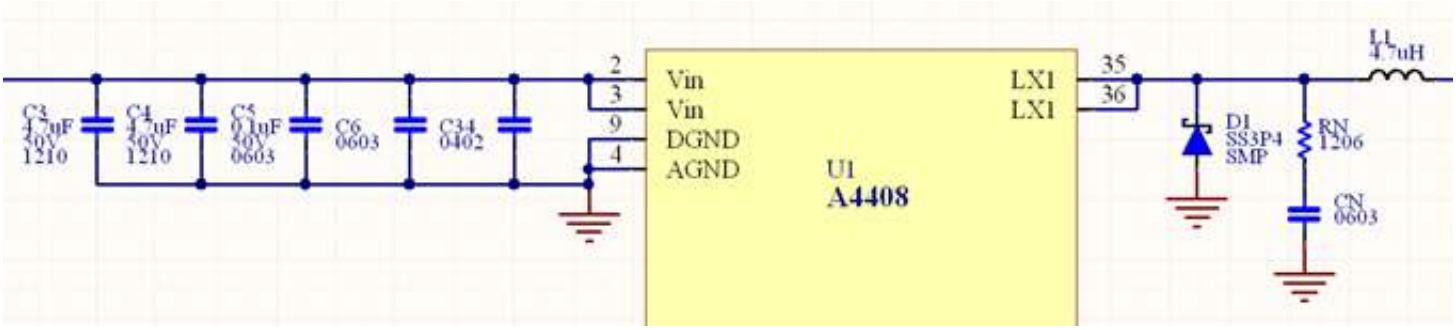

Figure 37: The most critical power component connections for the pre-regulator.
Place these components onto the PCB layout after the charge pump capacitors.

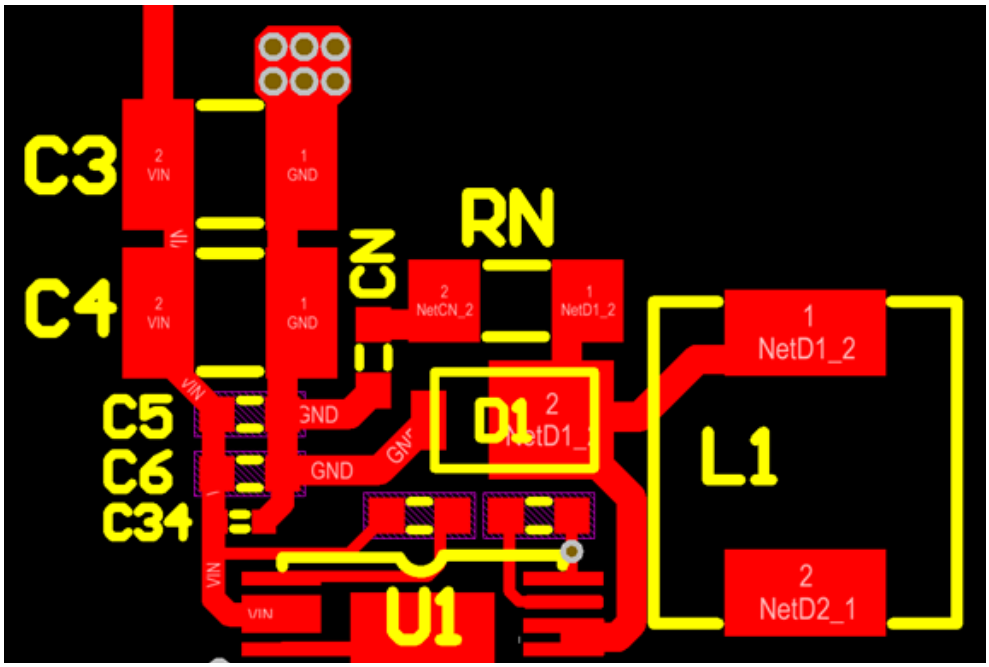

Figure 38: Recommended placement and routing of the most critical power components.

1) All of these components must be on the same layer as the A4408 (U1).
2) Routing between these components must not be interrupted by other traces.
3) Input capacitors (C34, C3, C4, C5, and C6) are located very close to the VIN pins.
4) Minimize the total loop area from C34/C6/C5 through U1 + D1.
5) The six ground vias “North” of C3 are placed so they only conduct DC current.
6) The switch node trace (LX1) is very short and just wide enough to carry about 3 A.
7) High frequency currents passing through D1 are directly routed to C34, C6, C5, and C4.
8) The snubber components connect directly from the LX1 node to ground.

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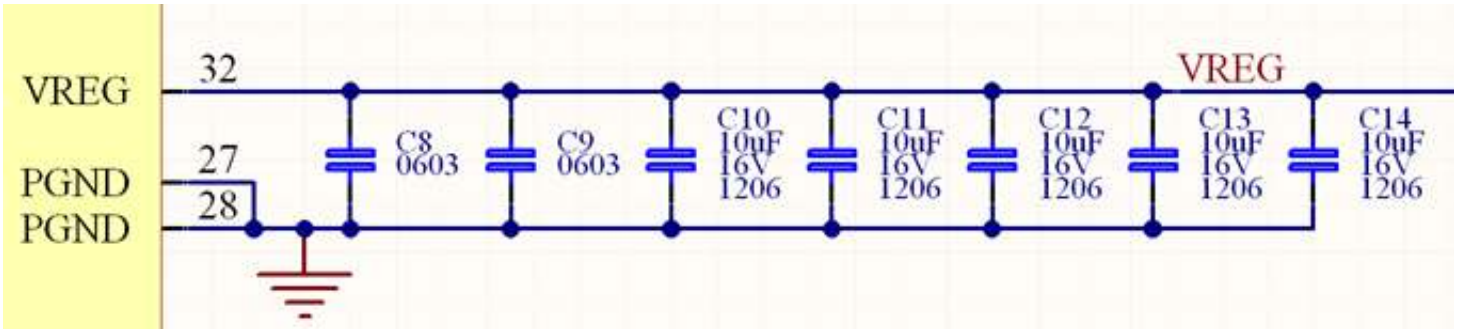

Figure 39: VREG capacitors (C8-C14) and PGND connections.
The VREG capacitors are the input bypass capacitors for the synchronous buck.
Place these capacitors so the loop from the VREG to PGND is short and uninterrupted.

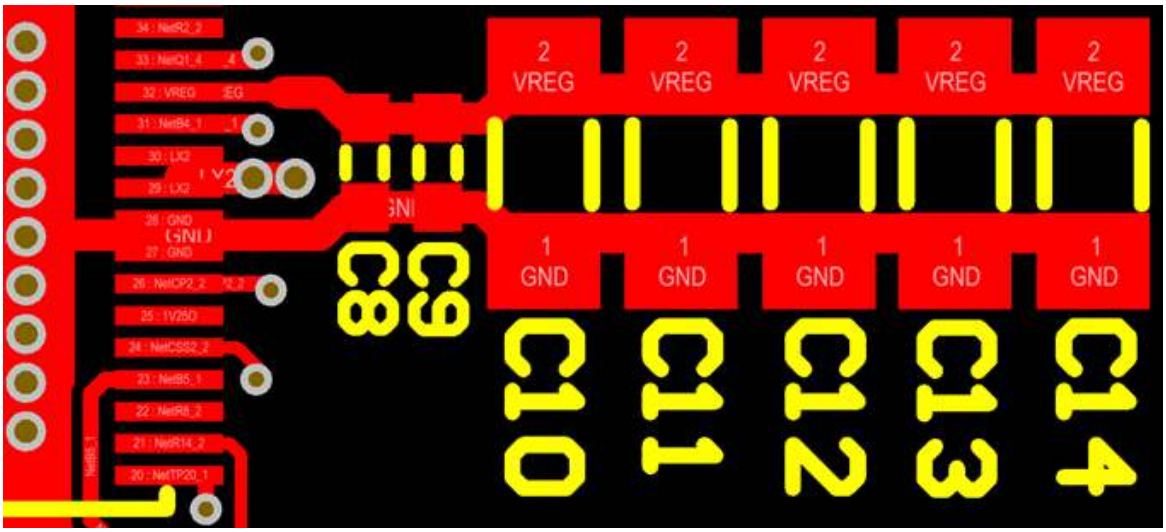

Figure 40: Recommended placement of the VREG capacitors and their PGND connection.

1) Place these components on the same layer as the A4408 (U1).
2) Minimize the loop from capacitors C8-C12 to the VREG pin and PGND pin.
3) The ground connection from the capacitors to the PGND pins is uninterrupted.
4) Connect the two PGND pins to the thermal pad (i.e. ground) under the A4408.
5) Note, the LX2 trace (pins 23 and 24) uses a via to avoid interrupting the PGND trace.

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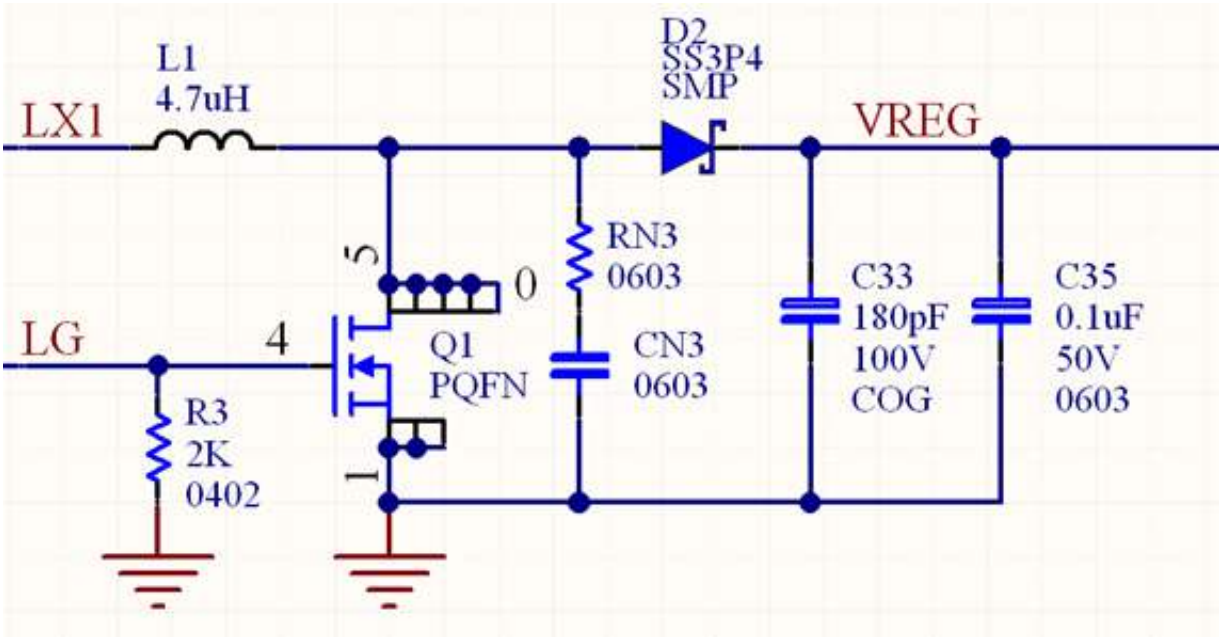

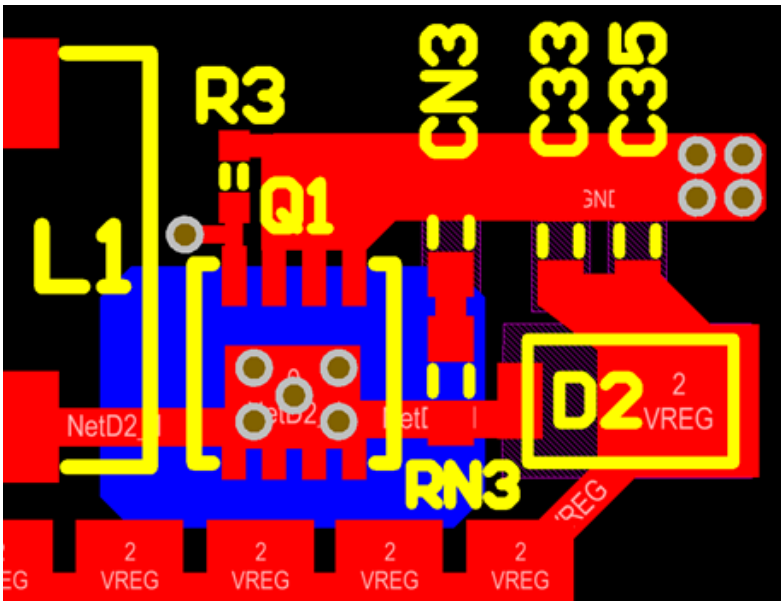

Figure 41: Recommended placement and routing of the Boost MOSFET and diode (Q1, D2), local bypass capacitors (C33, C35), and snubber components (RN3, CN3).

1) Minimize the hot loop between C33/C35 to D2 and to Q2.

2) Place a connection to the ground plane outside the hot loop (see 4 vias next to C35).

3) Include a thermal area on the bottom of the PCB (blue polygon) as thermal relief for Q1.

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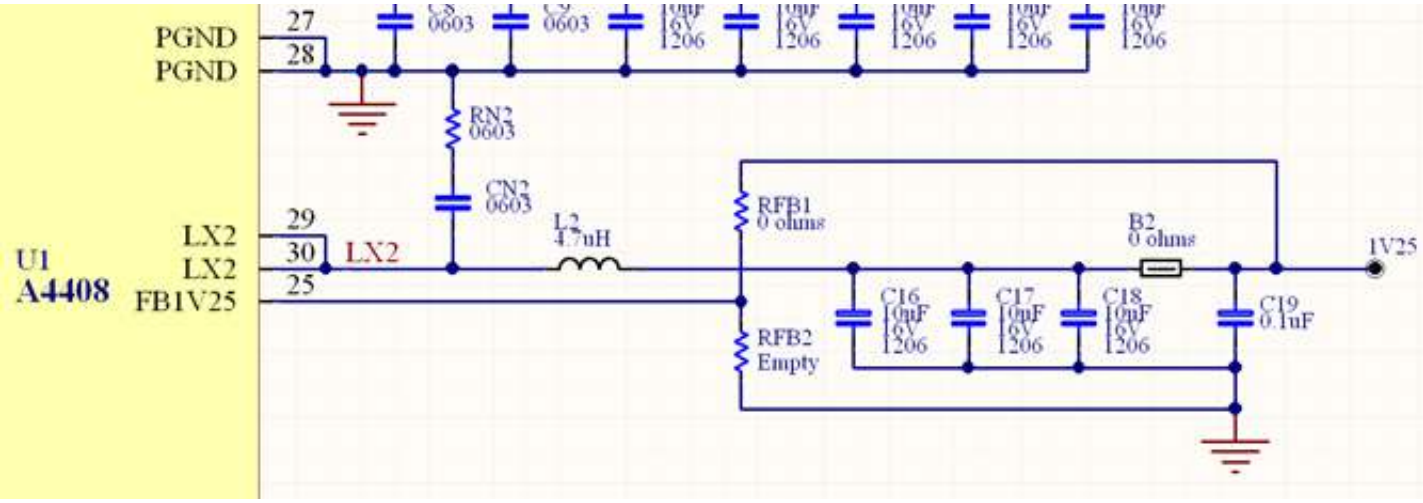

Figure 42: Synchronous buck output capacitors (C16-C18), snubber (RN2, CN2), and feedback resistor divider (RFB1, RFB2).

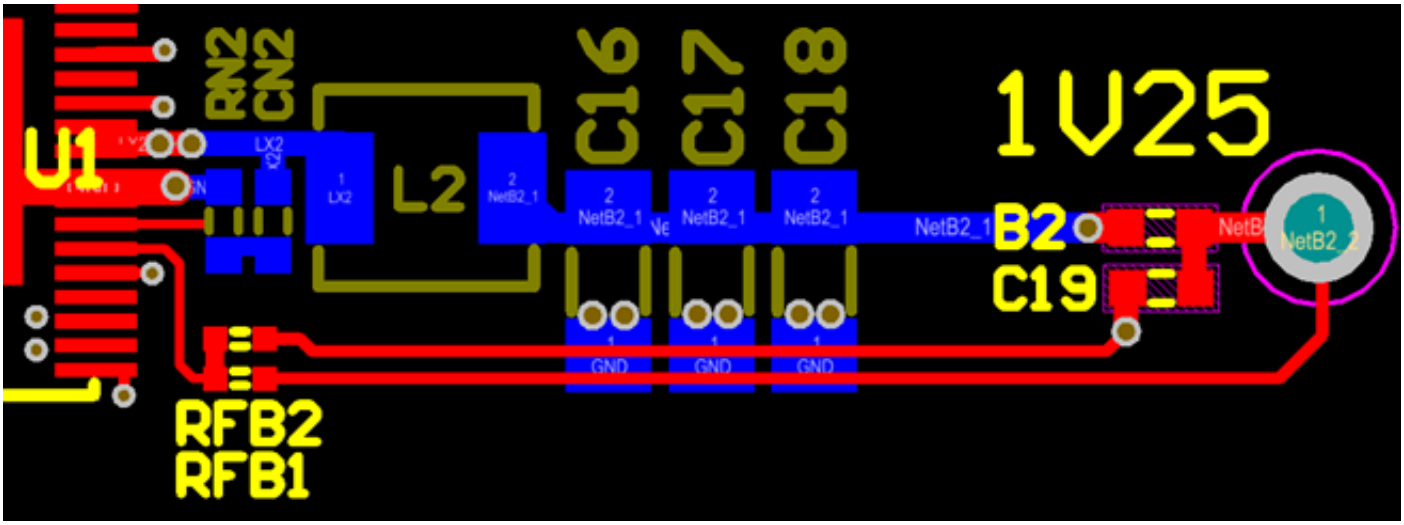

Figure 43: Recommended placement and routing of the synchronous buck inductor (L2), snubber (RN2, CN2), output capacitors (C16-C18), and feedback resistor divider (RFB1, RFB2).

1) Minimize the length and width of the LX2 trace. The width should accommodate 2.4 A_{MAX}.

2) The LX2 trace is on the bottom layer so the VREG capacitors can connect directly to PGND.

3) The snubber is on the same layer as the inductor and is grounded at PGND.

4) The feedback trace (1V25/FB_{ADJ}) is routed to the point of loading and after any filtering (B2).

5) If used, the feedback resistor divider (RFB1, RFB2) must be located near the FB_{ADJ} pin.

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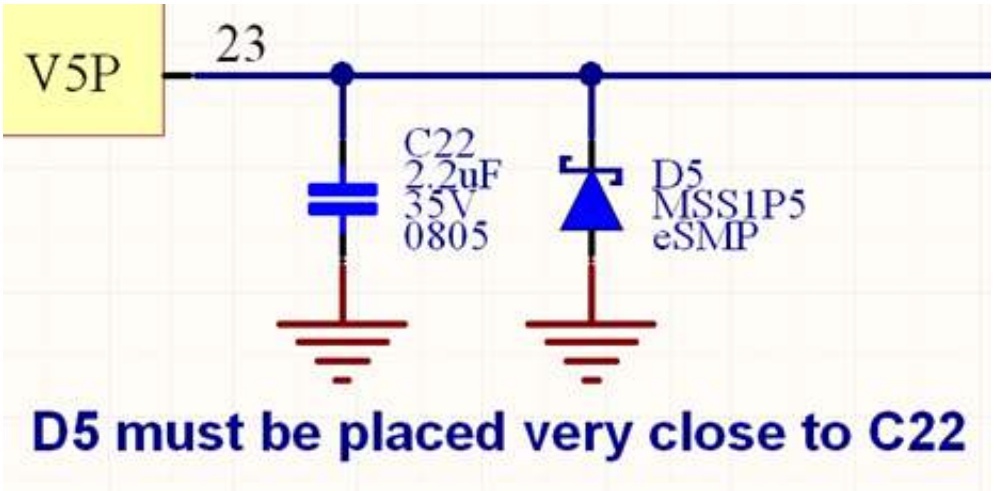

Figure 44: LDO (V5P) output capacitor and negative clamp diode (C22, D5).

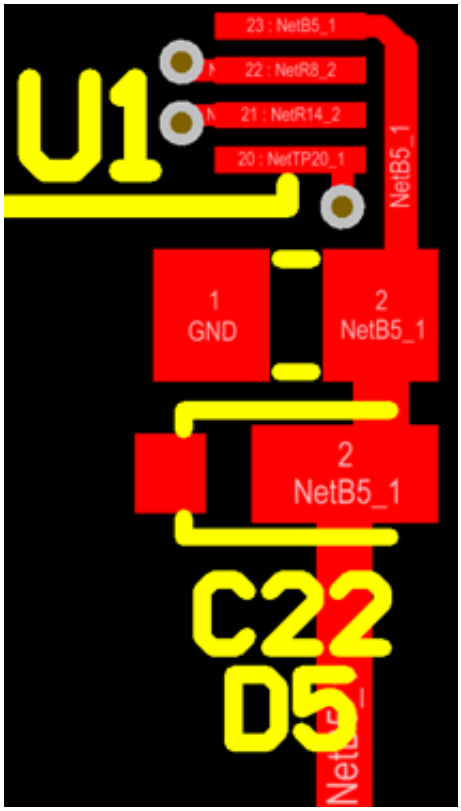

Figure 45: Recommended placement and routing of the LDO (V5P), output capacitor (C22), and negative clamp diode (D5).

1) Place the output capacitor and negative clamp diode close to the V5P output pin.

2) Connect these two components to the ground plane near the A4408.

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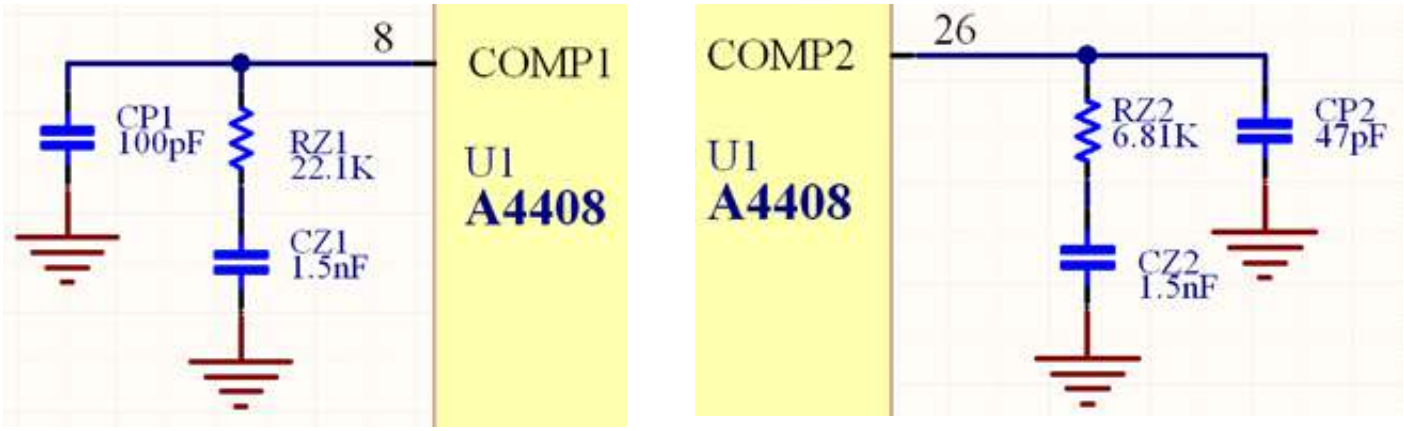

Figure 46: The COMP1 (RZ1, CZ1, CP1) and COMP2 (RZ2, CZ2, CP2) components.

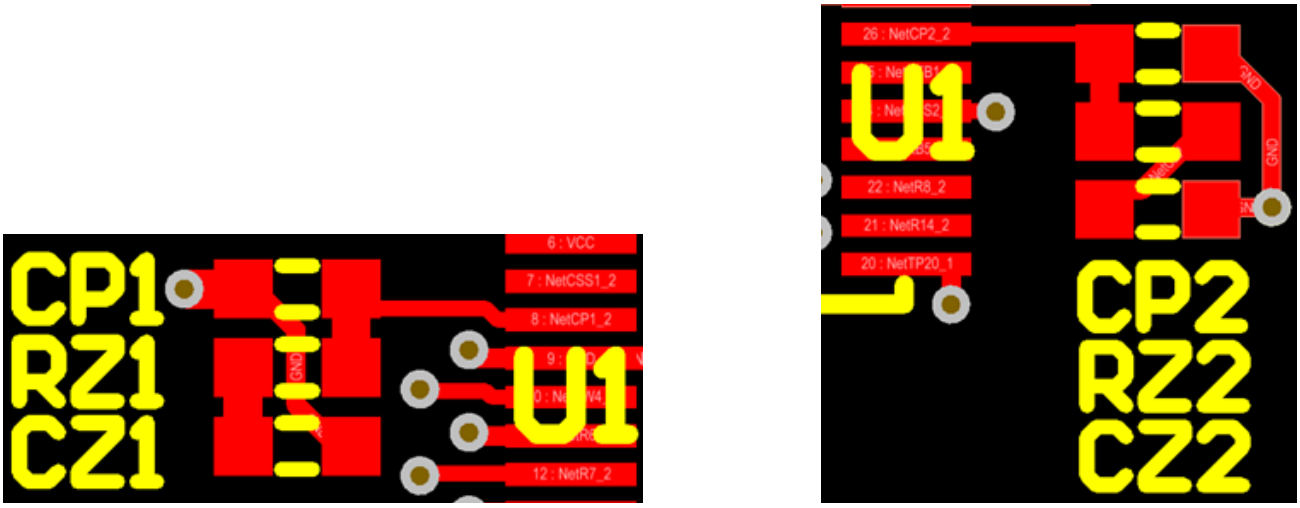

Figure 47: Recommended placement and routing of COMP1 and COMP2 components.

1) These components can by placed on the bottom of the PCB, near pins 9 and 20.

2) Place a via very close to pins 9 and 20.

3) Keep noisy traces, like LX1 and LX2, as far away as possible from these components.

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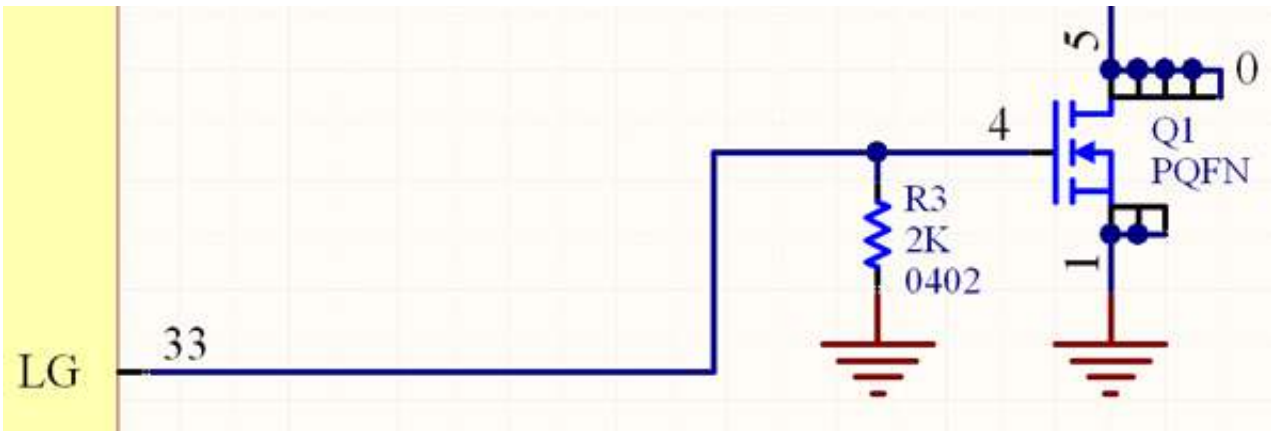

Figure 48: The gate drive from LG (pin 33) to the boost MOSFET.

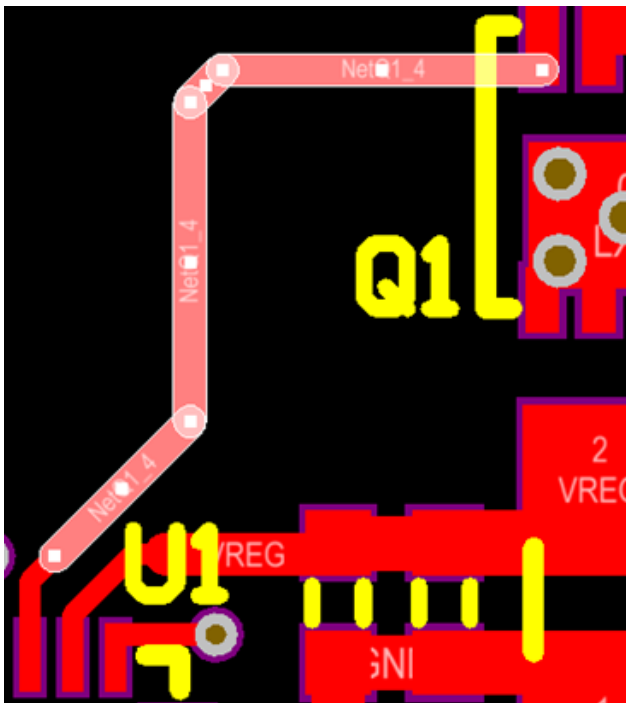

Figure 49: Recommended routing of the gate driver to the boost MOSFET.

1) It is best to keep the gate drive trace (LG) short and on the same layer as U1 and Q1 (i.e. no vias).

2) Here, the trace routes on the top layer and makes a short vertical run under L1.

3) The return path for the gate driver is layer #2, which is a ground plane.

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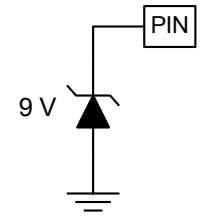
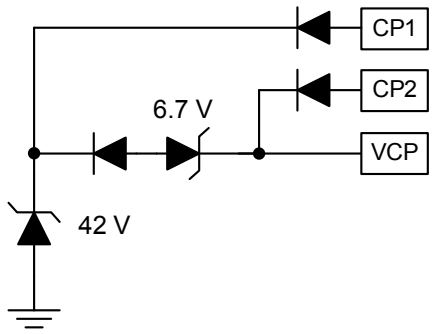
INPUT/OUTPUT STRUCTURES

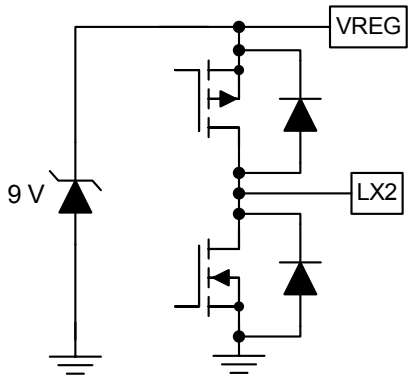
NPOR, POK5V, V5, 3V3, VREG, ENB, ENBAT1, ENBAT2, FF0, FF1, FB_{ADJ}, COMP1, COMP2, SS1, SS2, FSET/SYNC, TRACK, MODE, WD_{IN}, WD_{ENn}, WD_{ADJ}, VCC, LG



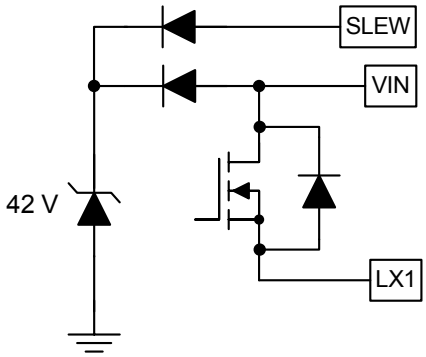
VCP, CP1, CP2



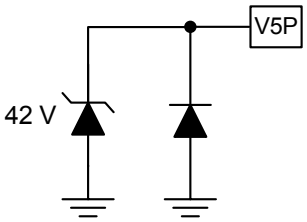
VREG, LX2



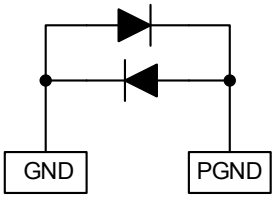
VIN, LX1, SLEW



V5P



GND, PGND



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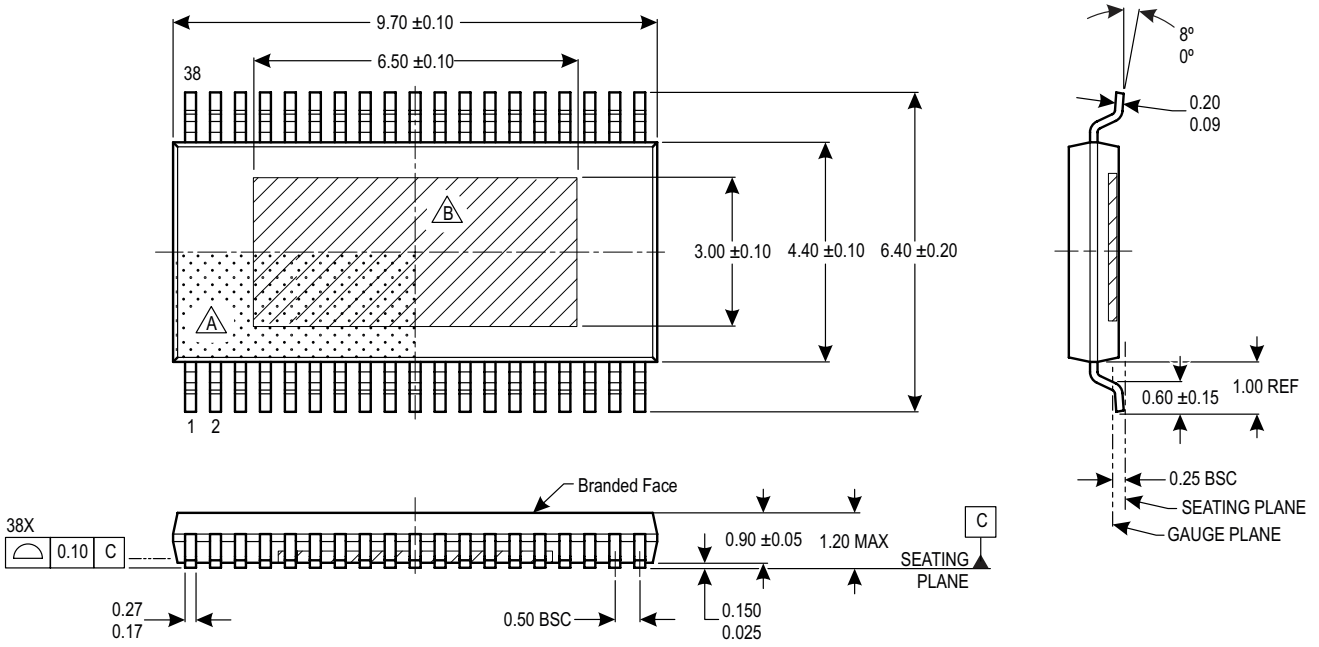
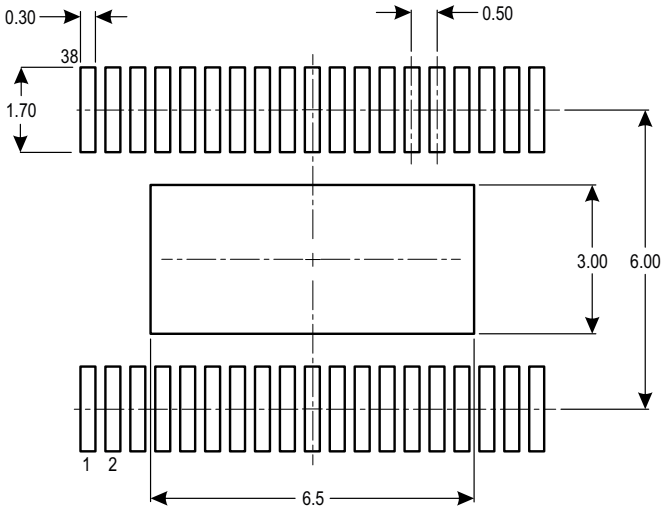
PACKAGE OUTLINE DRAWING

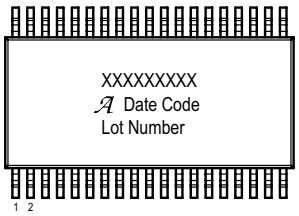
For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153 BDT-1)
Dimensions in millimeters
NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





C PCB Layout Reference View



D Standard Branding Reference View

Line 1, 2, 3 = 13 Characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP50P640X120-39M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

Figure 50: Package LV, 38-Pin eTSSOP

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Revision History

Number	Date	Description
–	September 23, 2016	Initial release
1	January 27, 2017	Updated Transconductance max value (page 8, 2nd condition), Pulse-by-Pulse Current Limit max value (page 9, 2nd condition), Low-Side MOSFET Leakage max value (page 10, 2nd condition), Transconductance min and max values (page 10, 1st condition), High-Side MOSFET Pulse-by-Pulse Current Limit max value (page 11). Deleted High-Side MOSFET Pulse-by-Pulse Current Limit 2nd condition (page 11). Added footnote to Boost Duty Cycle (LG Pin) 1st condition (page 8).
2	June 22, 2017	Added Input/Output Structures (page 53).
3	September 12, 2017	Corrected Minimum and Maximum Output Voltage symbols (page 8). Added footnote to SS1 Delay and Ramp Time (page 9). Added footnote to SS2 to V_{1V25} Delay Time and V_{1V25} Ramp Time (page 11). Updated V_{1V25} Ramp Time typical value (page 11). Corrected $t_{SS1(DLY)}$ and $t_{SS2(DLY)}$ symbols (pages 30, 31, 39, 42). Corrected equation 32 (page 41). Corrected equation 33 (page 42).
4	September 29, 2017	Updated Thermal Characteristics table (page 2).
5	October 4, 2017	Corrected Hiccup Mode test conditions (page 9). Updated Adjustable Synchronous Buck Regulator section (page 20). Updated Bias Supply section (page 23).
6	January 23, 2018	Updated V5 Current Limit minimum value (page 12).
7	January 31, 2019	Minor editorial updates.
8	July 30, 2019	Updated Figure 18 (page 30)
9	September 5, 2019	Updated Figure 18 (page 30)
10	September 18, 2019	Updated Figure 18 (page 30)
11	September 9, 2022	Updated package drawing (page 54) and minor editorial updates

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