

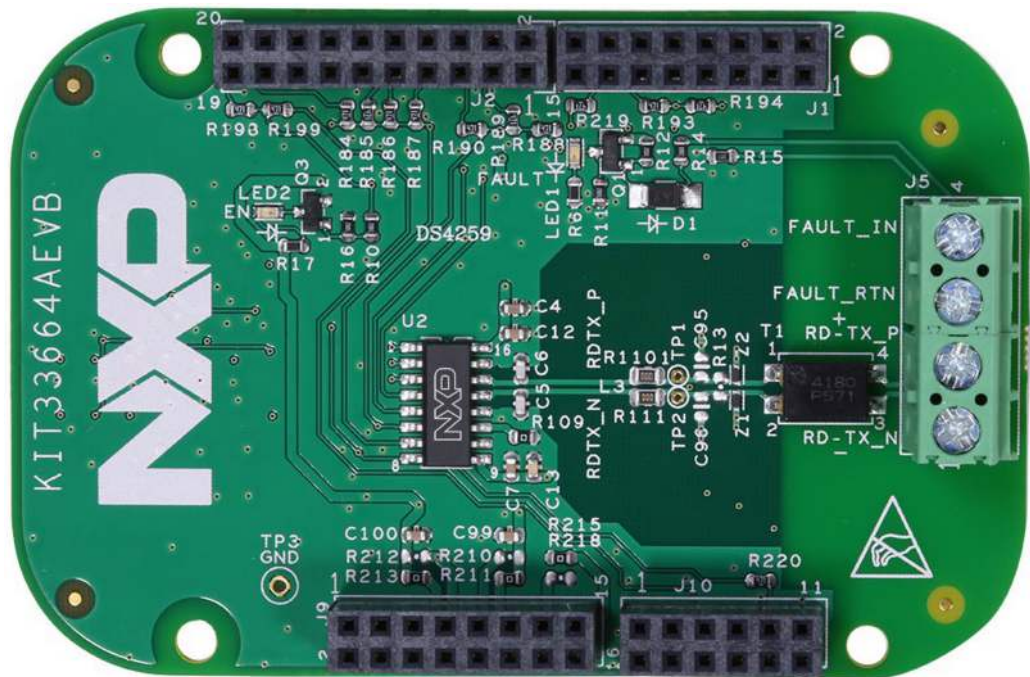
KT33664AEVBUG

KIT33664AEVB evaluation board

Rev. 2.0 — 25 October 2016

User guide

1 KIT33664AEVB



2 Important notice

NXP provides the enclosed product(s) under the following conditions: This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

Should this evaluation kit not meet the specifications indicated in the kit, it may be returned within 30 days from the date of delivery and will be replaced by a new kit.

NXP reserves the right to make changes without further notice to any products herein. NXP makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typical", must be validated for each customer application by customer's technical experts.

NXP does not convey any license under its patent rights nor the rights of others. NXP products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the NXP product could create a situation where personal injury or death may occur.

Should the Buyer purchase or use NXP products for any such unintended or unauthorized application, the Buyer shall indemnify and hold NXP and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges NXP was negligent regarding the design or manufacture of the part. NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. © 2016 NXP B.V.

3 Getting started

3.1 Kit contents/packing list

The KIT33664AEVB contents include:

- Assembled and tested evaluation board/module in anti-static bag
- Quick start guide

The FRDM-33664AEVM contents include:

- Assembled and tested KIT33664AEVB evaluation board
- FRDM-KL25Z board
- Quick start guide

3.2 Jump start

NXP's analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic ICs and system-in-package devices that use proven high-volume SMARTMOS technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost and improved performance in powering state of the art systems.

1. Go to <http://www.nxp.com/KIT33664AEVB>.
2. Review your Tools Summary Page.
3. Locate and click:



4. Download the documents, software, and other information.

Once the files are downloaded, review the user guide in the bundle. The user guide includes setup instructions, BOM and schematics. Jump start bundles are available on each tool summary page with the most relevant and current information. The information includes everything needed for design.

3.3 Required equipment

The kit requires the following items:

- 5.0 V power supply, 50 mA capability
- 3.3 V power supply, 50 mA capability (If the application requires a 3.3 V logic threshold)
- Freedom board (optional)

4 Understanding the KIT33664AEVB

4.1 Board overview

The KIT33664AEVB and FRDM-33664AEVM are hardware evaluation tools that support system designs based on NXP’s MC33664ATL1EG device.

MC33664 is a transceiver physical layer transformer driver that links a microcontroller to a high speed isolated communication network. The transceiver converts SPI data bits into pulse bit information that is transferred to the bus network. Slave response messages use the same structure to send pulse bit information to the MC33664, which is then converted to a SPI bit stream and sent back to the MCU.

The MC33664 transceiver physical layer transformer driver can also convert MCU SPI data bits to pulse bit information for MC33771 and MC33772 devices being used in a BMS system.

4.2 Board features

The main features of the evaluation board are:

- MC33664 Isolated Communication Transceiver in a 16-pin SOICN package
- SPI interface
- LED indicators
- Fault detection report
- Isolated communication by transformers with connectors

4.3 Block diagram

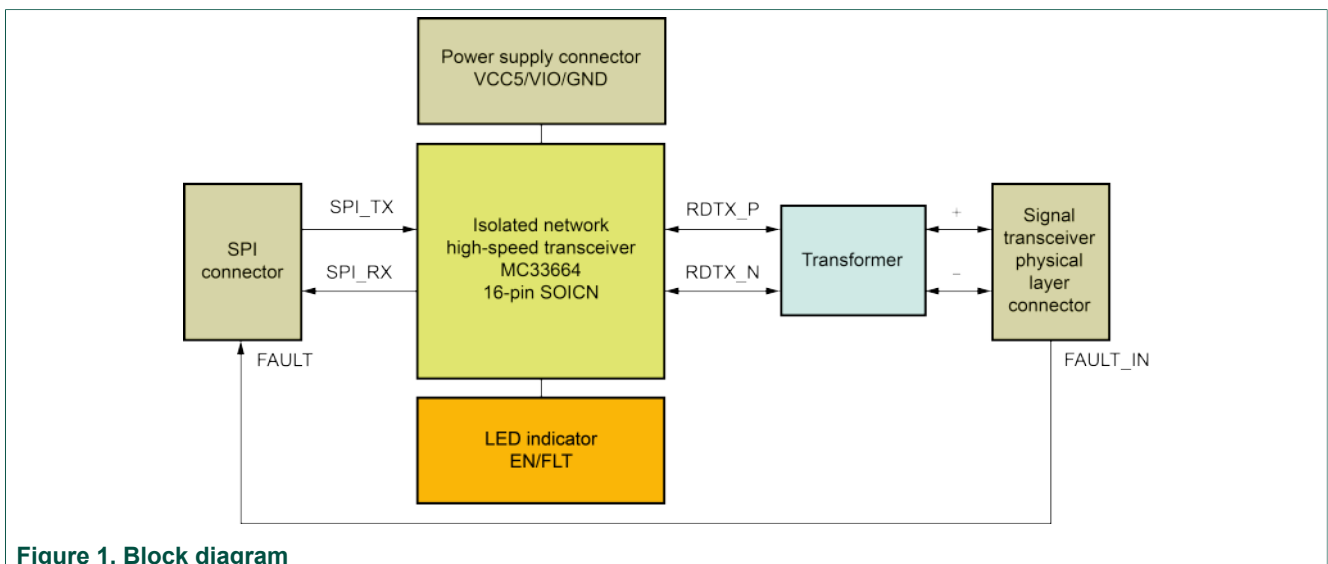


Figure 1. Block diagram

4.4 Device features

The MC33664 is an Isolated Communication Network High Speed Transceiver IC for managing isolated high speed differential communication. The device supports the following functions:

- 2.0 Mbps isolated network communication rate
- Dual SPI architecture for message confirmation
- Robust conducted and radiated immunity with wake-up
- 3.3 V and 5.0 V compatible logic thresholds
- Low sleep mode current with automatic bus wake-up
- Ultra-low radiated emissions

5 Getting to know the hardware

5.1 Board description

The KIT33664AEVB and FRDM-33664AEVM boards allow the user to exercise all the functions of the MC33664.

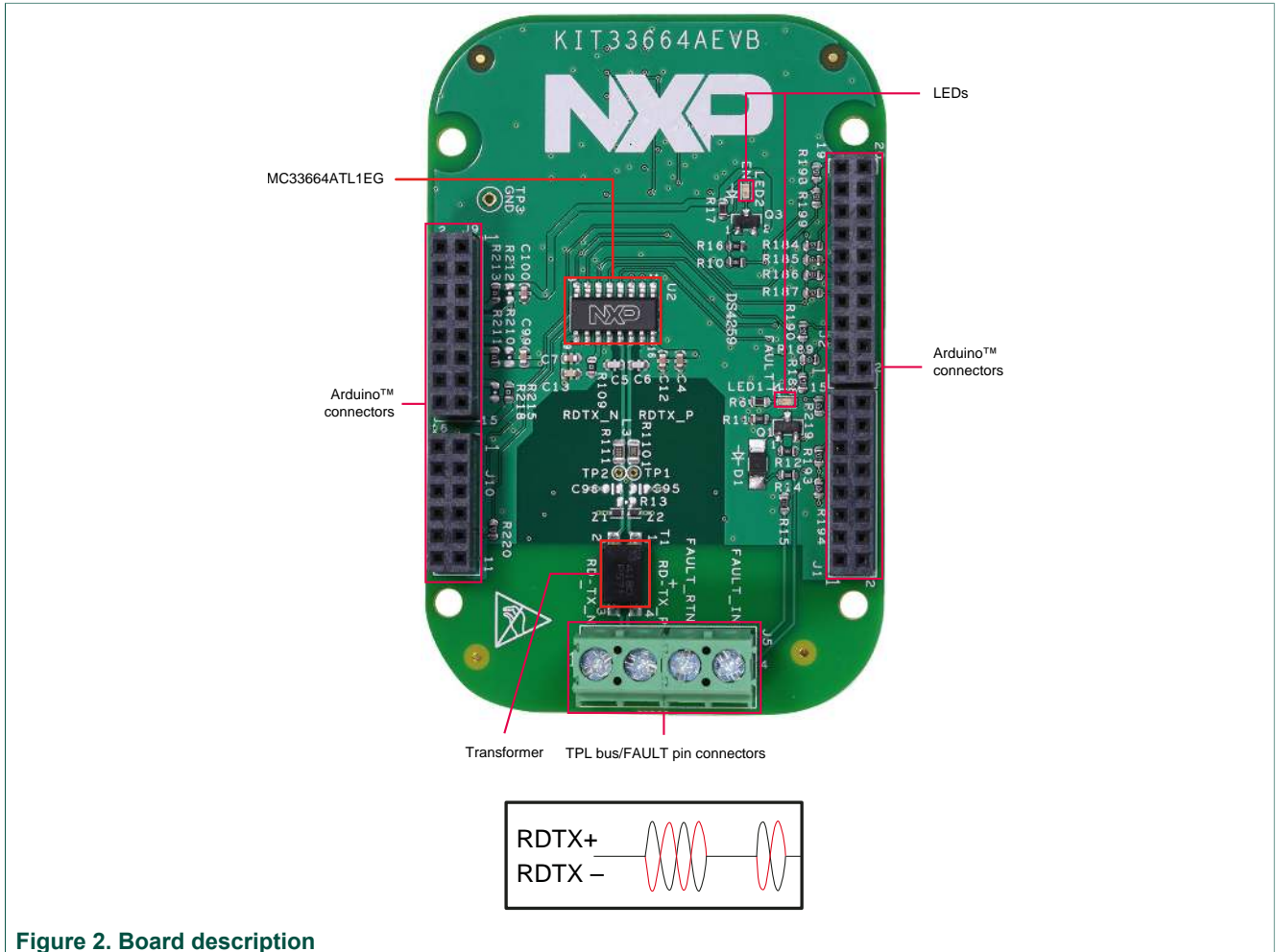


Figure 2. Board description

Table 1. Board description

| Name | Description |
|------------------------------|--|
| LEDs | Indicators for on-board operations |
| Arduino™ connectors | Connectors for attaching a Freedom board and routing SPI signals and power lines |
| Transformer | Bus Isolator Transformer |
| TPL bus/ FAULT pin connector | Connector for TPL bus cables and FAULT pin connections |
| MC33664ATL1EG | Isolated Network High Speed Transceiver |

5.2 LEDs

Figure 3 and Table 2 show the locations and description of the LEDs on the board.

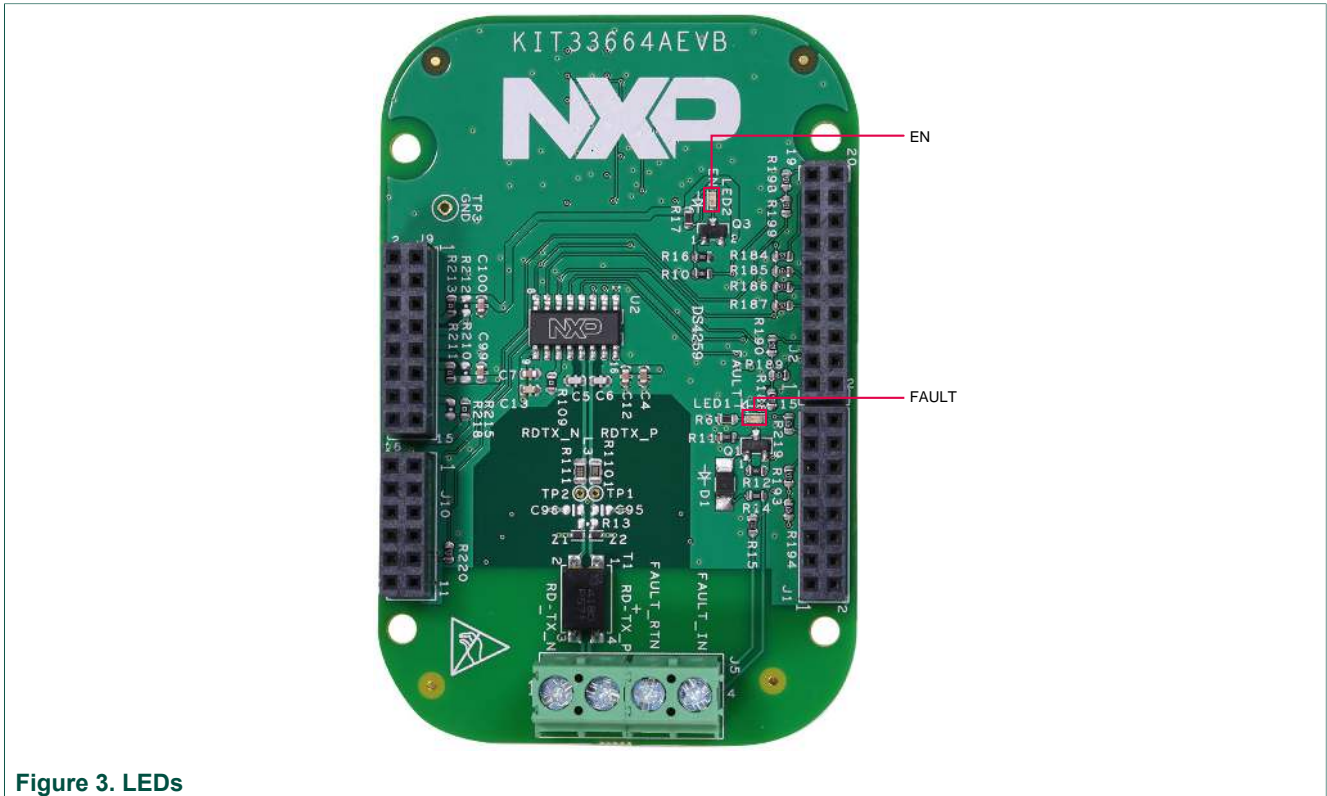


Figure 3. LEDs

Table 2. LEDs

| LED Name | Description |
|----------|--|
| EN | LED that indicates the operating mode. If the EN LED lights, the device is in normal operating mode. The device transmits and receives messages through SPI_TX for the transmission and SPI_RX for the reception. If the EN LED is off, the device is in sleep mode and no transmission is allowed. (See Table 3). |
| FAULT | Lights when the FAULT pin is set high (VIO) by the MCU |

The MC33664 has the following modes of operation by the VIO and EN pins:

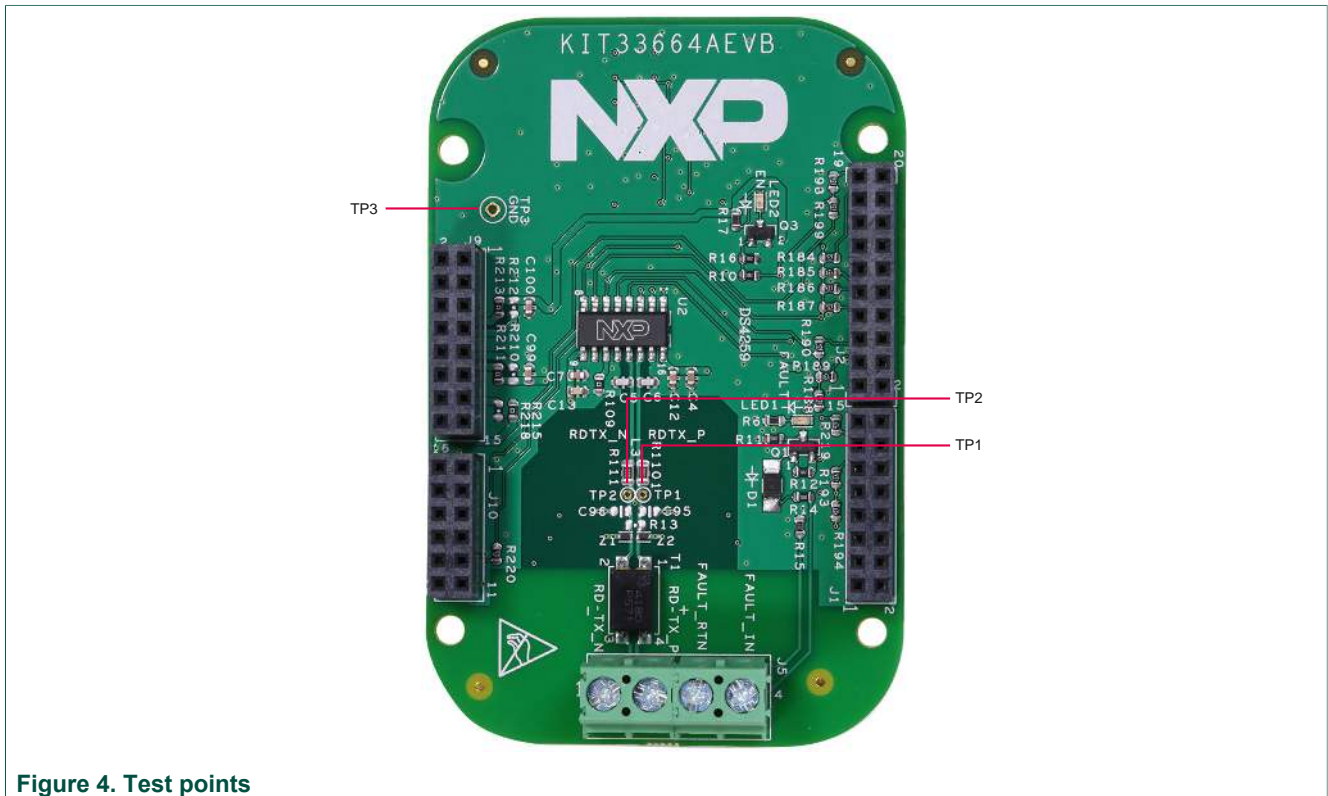
Table 3. Modes of operation

| Device mode | EN pin | VIO pin | EN LED | Comment |
|-------------|--------|---------|--------|---|
| Normal | 1 | 1 | On | The MC33664 operates as a full transceiver. MCU messages transmitted on the SPI_TX emerge on the SPI_RX for the MCU to read. |
| Sleep | 0 | 1 | Off | In sleep mode, the transceiver activates the INTB pin when a valid wake-up sequence is detected. The INTB pin remains low until the rising edge of the EN pin places the device in normal mode. |

| Device mode | EN pin | VIO pin | EN LED | Comment |
|-------------|--------|---------|--------|---|
| Reset | — | 0 | Off | The RDTX± outputs are in high-impedance and the device is not able to transmit, receive, or report bus wake-up events |

5.3 Test points

Figure 4 and Table 4 show the locations and description of test points on the board.



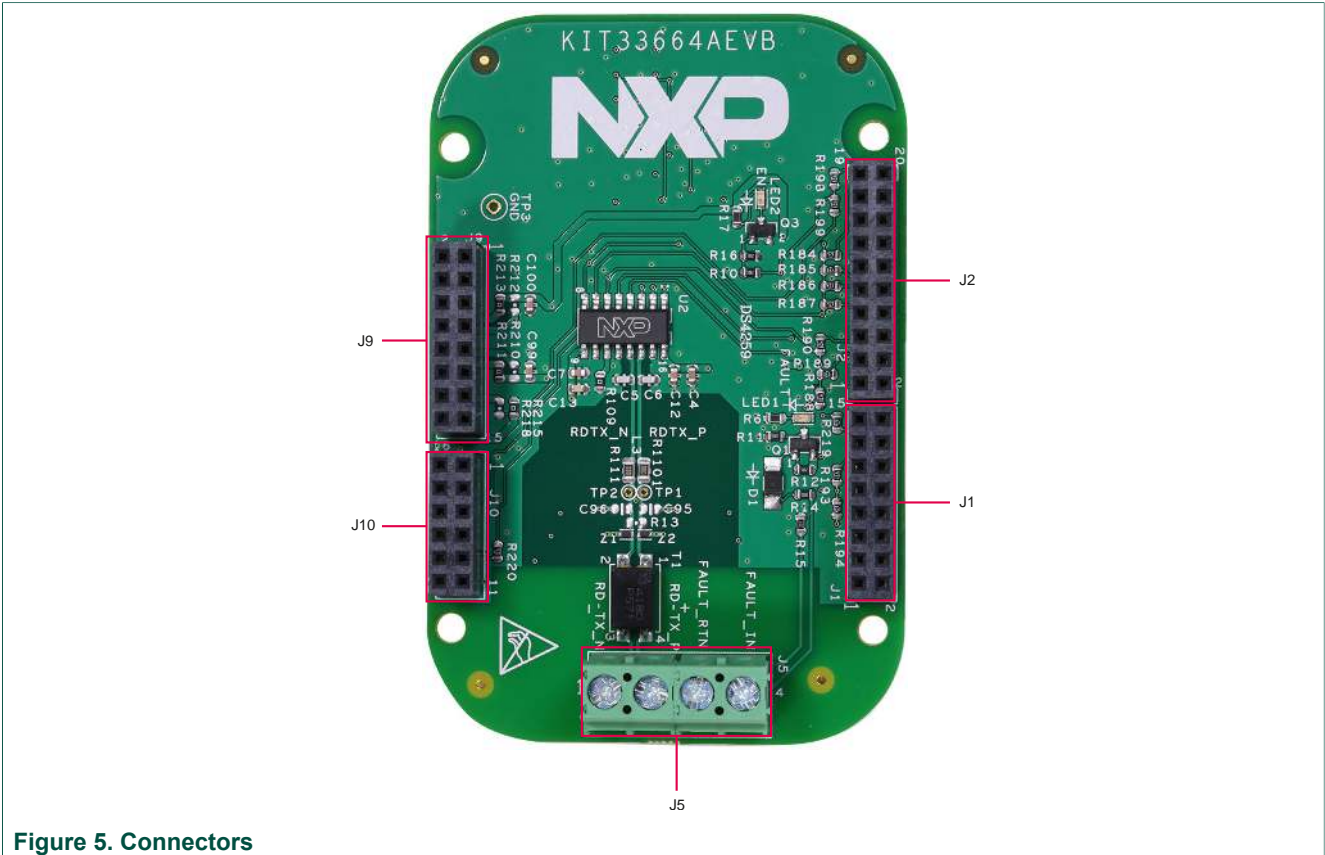


Figure 5. Connectors

Table 5. Connector J1

| Pin # | Signal name | Description |
|---------|-------------|--|
| 1 to 16 | — | Connections depend on configuration. See Table 10 and Table 11 |

Table 6. Connector J2

| Pin # | Signal name | Description |
|---------|-------------|--|
| 1 to 20 | — | Connections depend on configuration. See Table 10 and Table 11 |

Table 7. Connector J5

| Pin # | Signal name | Description |
|-------|-------------|--|
| 1 | RD_TX_N | TPL bus connection to the RDTX- pin (pin 13) on the isolated network high-speed transceiver device (MC33664) |
| 2 | RD_TX_P | TPL bus connection to the RDTX+ (pin 14) pin on the isolated network high-speed transceiver device (MC33664) |
| 3 | FAULT_RTN | TPL bus connection to FAULT_RTN |
| 4 | FAULT_IN | TPL bus connection to FAULT_IN |

Table 8. Connector J9

| Pin # | Signal name | Description |
|---------|-------------|--|
| 1 to 16 | — | Connections depend on configuration. See Table 10 and Table 11 |

Table 9. Connector J10

| Pin # | Signal name | Description |
|---------|-------------|--|
| 1 to 12 | — | Connections depend on configuration. See Table 10 and Table 11 |

5.5 Signal bus terminal description

The transceiver (NET_N / NET_P) differential signal output is isolated by a transformer T1. Z1 and Z2 serve as ESD protection. All capacitors marked DNP are not populated on the board.

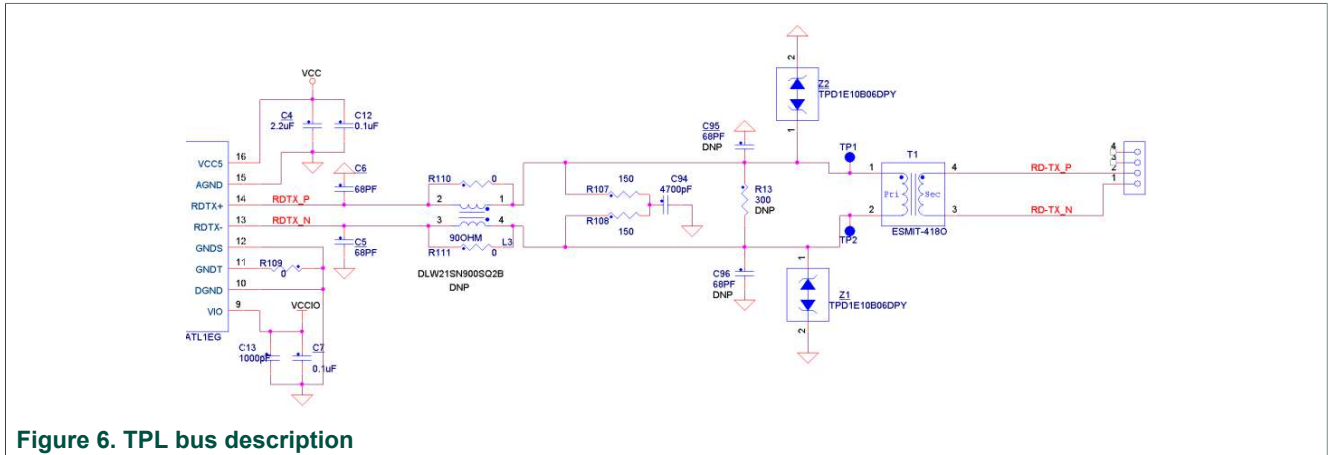


Figure 6. TPL bus description

6 Setting up the hardware

6.1 Fault input detection

An external low impedance connection (through a relay, optocoupler or similar components) between J5 – 3 (FAULT_RTN) and J5 – 4 (FAULT_IN) sets (VCCIO) the FAULT signal.

The FAULT signal alerts the MCU that an external FAULT condition has occurred. The FAULT signal is sent to the appropriate Freedom board pin or to pin J1-6 by default (see [Table 10](#)).

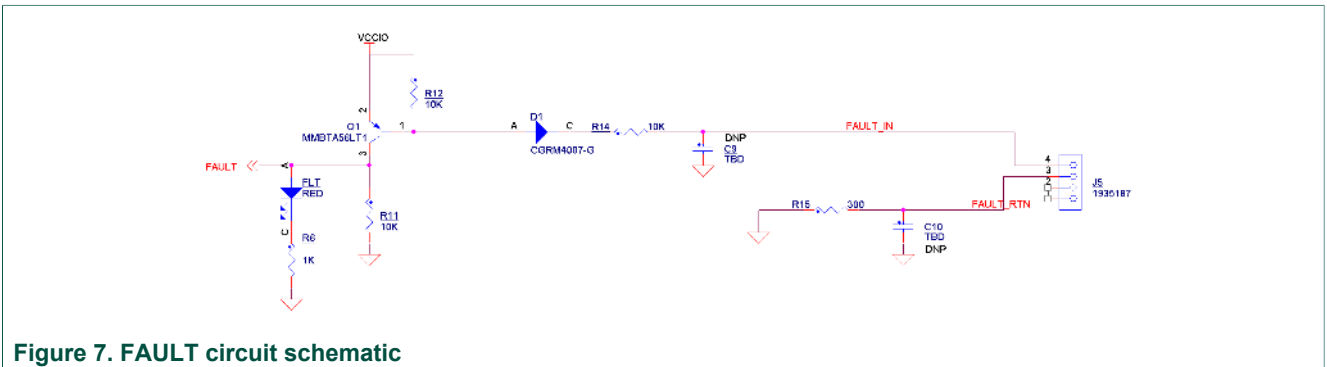


Figure 7. FAULT circuit schematic

7 Configuring the hardware

The KIT33664AEVB can be configured as a shield board connected to selected Freedom boards or it can be used in a stand-alone configuration (without a Freedom board).

7.1 Freedom board configuration

The KIT33664AEVB is compatible with the following Freedom evaluation boards:

- FRDM-KL25Z (Default factory setup configuration)
- FRDM-KV31F
- FRDM-KE06Z
- FRDM-KL43Z
- FRDM-KW40Z

The layout and the drill of the connectors allow all of these boards to be mounted directly to the KIT33664AEVB (see [Figure 8](#)). When both boards are connected together, the SPI connector is directly connected with the MCU SPI pins. The routing of SPI signals through the Arduino™ connectors depends on the specific Freedom board being used. In this configuration, power is supplied to the KIT33664AEVB through a USB cable connected between the Freedom board and a PC. No external power supply is required.



Figure 8. KIT33664AEVB mounted to a FRDM-KL25Z

The board must be modified to be compatible with each specific Freedom board. This modification consists of adding or removing shunts (0 Ω resistors) on the board. Most of the resistors are located on the bottom side of the board.

The tables below show the SPI signal routing and the KIT33664AEVB resistor modifications applicable to each board.

Table 10. KIT33664AEVB configuration table

| Signal name | Connector pin | KL25Z (default configuration) | |
|-------------|---------------|-------------------------------|------------|
| | | Add | Remove |
| FAULT | J1 – 6 | R165 | R208, R209 |
| INTB | J1 – 8 | R176 | R202, R203 |
| SCLK_TX | J1 – 9 | | |
| CSB_TX | J1 – 14 | | |

| | KL25Z (default configuration) | | |
|---------|-------------------------------|------|------|
| DATA_TX | J2 - 8 | R162 | R161 |
| SCLK_RX | J9 - 7 | | |
| CSB_RX | J9 - 5 | | |
| DATA_RX | J2 - 19 | | |
| EN | J2 - 18 | | |

| | KE06 | | |
|-------------|---------------|------|------------|
| Signal name | Connector pin | Add | Remove |
| FAULT | J1 - 10 | R170 | R171 |
| INTB | J3 - 10 | | |
| SCLK_TX | J1 - 8 | R203 | R202, R176 |
| CSB_TX | J1 - 6 | R209 | R165, R208 |
| DATA_TX | J1 - 12 | R206 | R207 |
| SCLK_RX | J2 - 12 | | |
| CSB_RX | J2 - 6 | | |
| DATA_RX | J2 - 8 | R161 | R162 |
| EN | J3 - 6 | | |

| | KL43 | | |
|-------------|---------------|------|------------|
| Signal name | Connector pin | Add | Remove |
| FAULT | J1 - 8 | R202 | R203, R176 |
| INTB | J4 - 10 | | |
| SCLK_TX | J1 - 15 | R201 | R200 |
| CSB_TX | J1 - 6 | R209 | R165, R208 |
| DATA_TX | J1 - 11 | R204 | R205 |
| SCLK_RX | J2 - 12 | | |
| CSB_RX | J2 - 6 | | |
| DATA_RX | J2 - 8 | R161 | R162 |
| EN | J4 - 6 | | |

| | KW40 | | |
|-------------|---------------|------|------------|
| Signal name | Connector pin | Add | Remove |
| FAULT | J1 - 8 | R202 | R203, R176 |
| INTB | J4 - 10 | | |
| SCLK_TX | J1 - 12 | R207 | R206 |
| CSB_TX | J1 - 10 | R171 | R170 |
| DATA_TX | J1 - 6 | R208 | R209, R165 |
| SCLK_RX | J2 - 12 | | |

| | KW40 | | |
|---------|--------|------|------|
| CSB_RX | J2 - 6 | | |
| DATA_RX | J2 - 8 | R161 | R162 |
| EN | J4 - 6 | | |

| | KV31 | | |
|-------------|---------------|------|------------|
| Signal name | Connector pin | Add | Remove |
| FAULT | J1 -8 | R202 | R203, R176 |
| INTB | J4 - 10 | | |
| SCLK_TX | J1 - 11 | R205 | R204 |
| CSB_TX | J1 - 6 | R209 | R165, R208 |
| DATA_TX | J1 - 13 | | |
| SCLK_RX | J2 - 12 | | |
| CSB_RX | J1 - 15 | R200 | R201 |
| DATA_RX | J2 - 10 | | |
| EN | J4 - 6 | | |

7.1.1 Step-by-step instructions for setting up the hardware in a Freedom board configuration

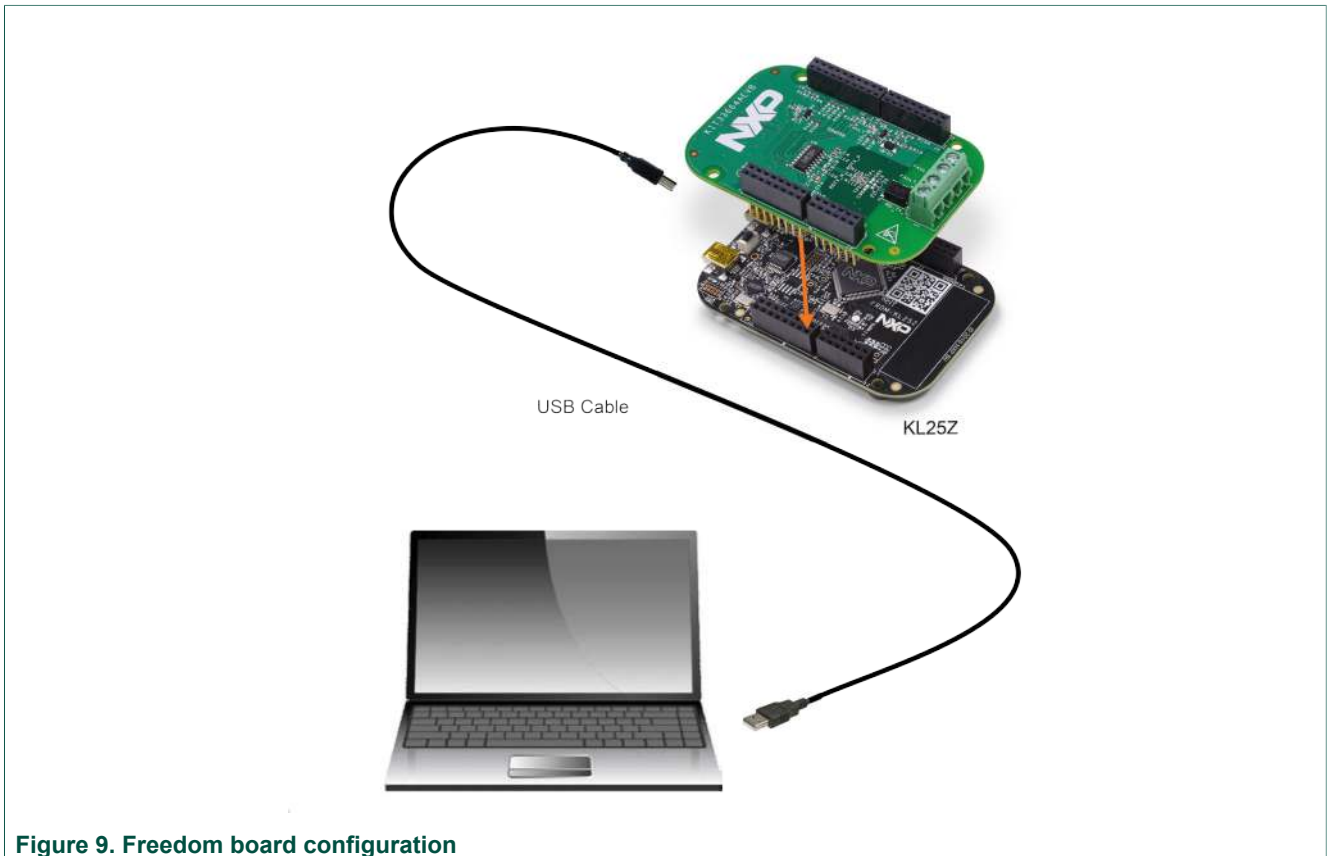


Figure 9. Freedom board configuration

[Figure 9](#) shows the board configured for use with a Freedom board. The process for configuring the hardware is as follows:

1. Mount the KIT33664AEVB to the surface of the Freedom board by means of the on-board Arduino™ connectors (connectors J1, J2, J9 and J10).
2. Connect a USB cable between a PC and the USB port on the Freedom board. The KIT33664AEVB board draws power through the USB connection.

Microcode must be loaded onto the Freedom board to enable the exercising of board functions. For the Freedom-KL25Z, the microcode is included as a .srec file that is included with the KIT33664AEVB zip file. For other Freedom boards, the user must develop and download their own microcode to the Freedom board.

7.2 Standalone configuration

When the board is used in standalone mode, the SPI signals must be manually connected to connectors J1, J2 and J9 on the board.

Table 11. Standalone configuration table

| Signal | Pin |
|---------|---------|
| FAULT | J1 – 6 |
| INTB | J1 – 8 |
| SCLK_TX | J1 – 9 |
| CSB_TX | J1 – 14 |
| DATA_TX | J2 – 8 |
| SCLK_RX | J9 – 7 |
| CSB_RX | J9 – 5 |
| DATA_RX | J2 – 19 |
| EN | J2 – 18 |

Power supply connections to the KIT33664AEVB are:

- VCC (5.0 V): J9 – 10
- VCCIO (3.3 V or 5.0 V depending on the required communication signal levels): J9 – 8
- GND: J9 – 12, J9 – 14, J2 – 14

7.2.1 Step-by-step instructions for setting up the hardware

When used in a standalone configuration, the power, ground, SPI signals and TPL signals must be manually attached to the board.

[Figure 10](#) shows the KIT33664AEVB in standalone configuration.

Note: Users who are not fully knowledgeable in NXP MCU's and the Freedom board architecture should avoid using standalone mode.

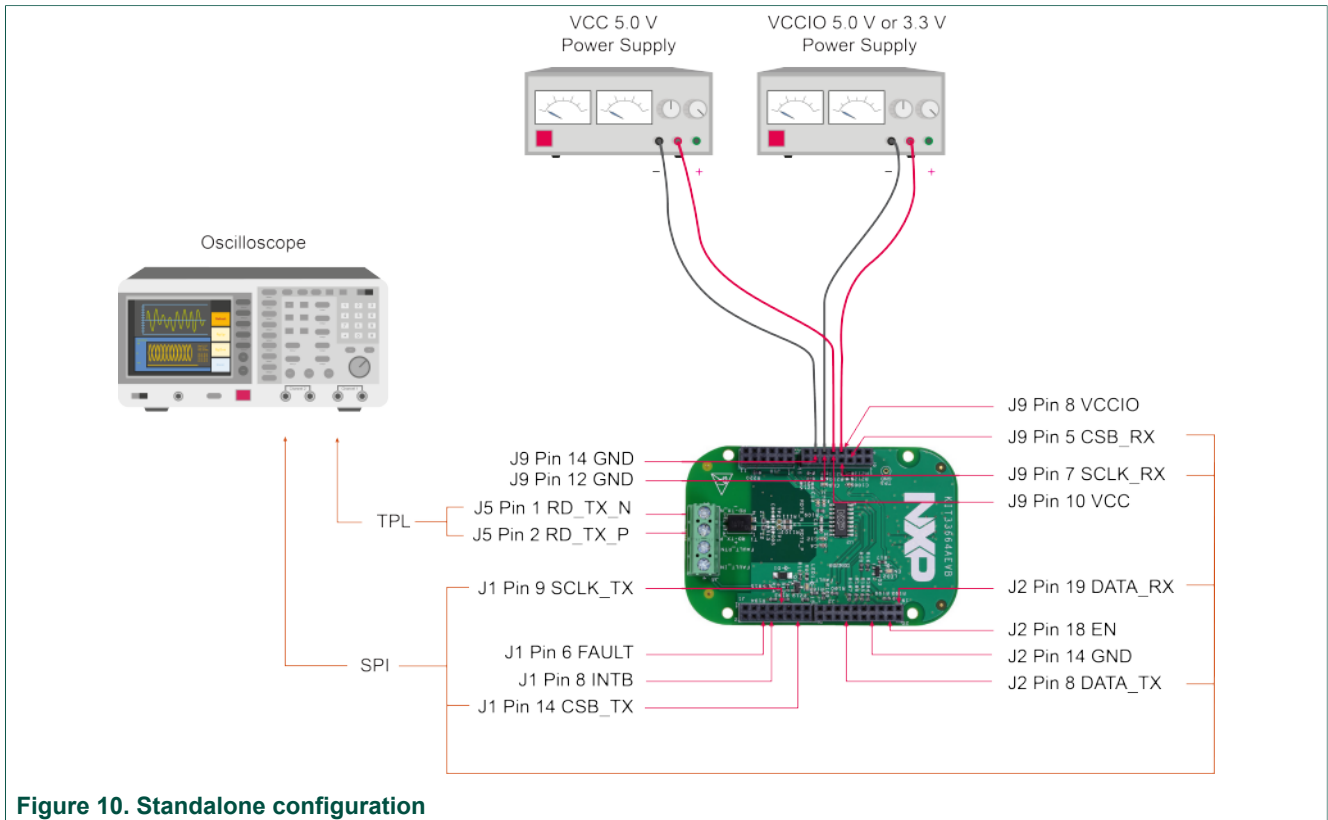


Figure 10. Standalone configuration

The process for configuring the hardware is as follows:

1. On the KIT33664AEVB, physically connect the SPI bus communication signals to the appropriate positions on connectors J1, J2 and J9 (see [Table 10](#)).
2. Connect the TPL signals to connector J5 (see [Table 7](#)).
3. Connect VCC to the 5.0 V power supply as follows:
 - Make sure that the power supply is switched off.
 - Connect the power supply's positive terminal to Pin 10 on Connector J9.
 - Connect the power supply's negative terminal to Pin 14 on Connector J9.
4. Connect VCCIO to either a 5.0 V power supply or a 3.3 V power supply (depending on the communication signal requirements).
 - Make sure the power supply is switched off.
 - Connect the power supply's positive terminal to Pin 8 on Connector J9.
 - Connect the power supply's negative terminal to Pin 12 on Connector J9.
5. Connect the SPI signals (TX, RX, SCKLK, CSB) and the TPL signals (RDTX+, RDTX-) to an oscilloscope.
6. Observe the isolated differential signal and the SPI signal on the oscilloscope. [Figure 11](#) shows the protocol of the output signal on the IC pins.

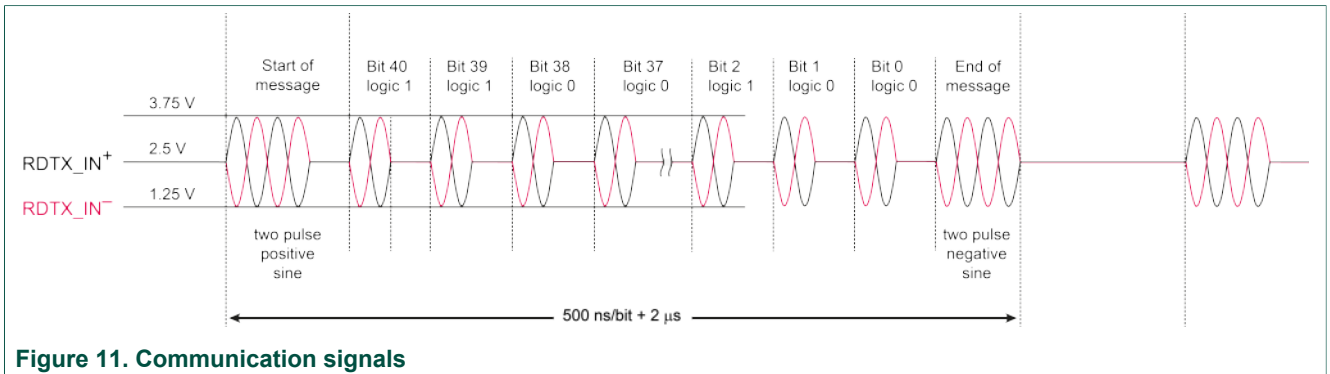


Figure 11. Communication signals

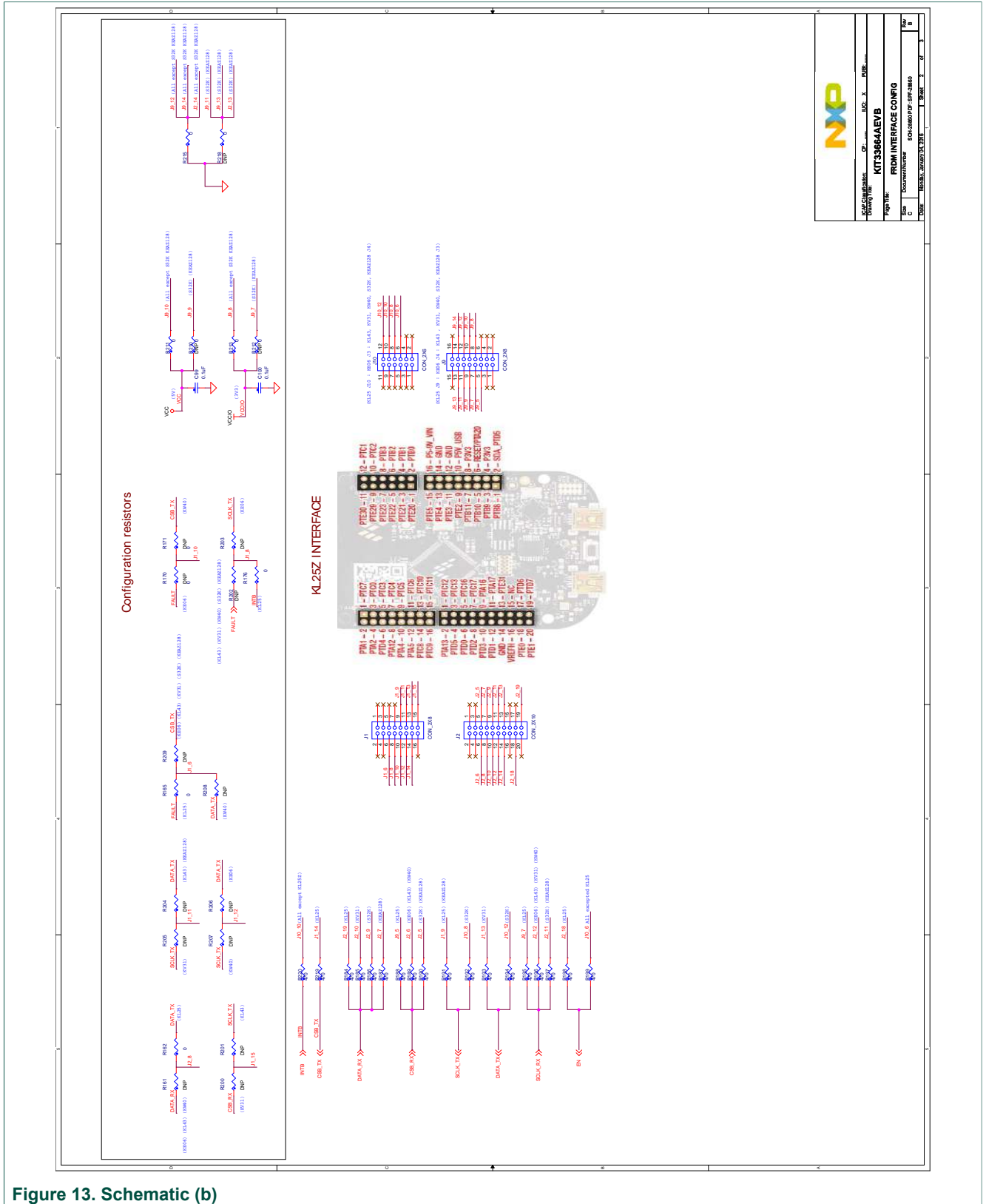


Figure 13. Schematic (b)

9 Board layout

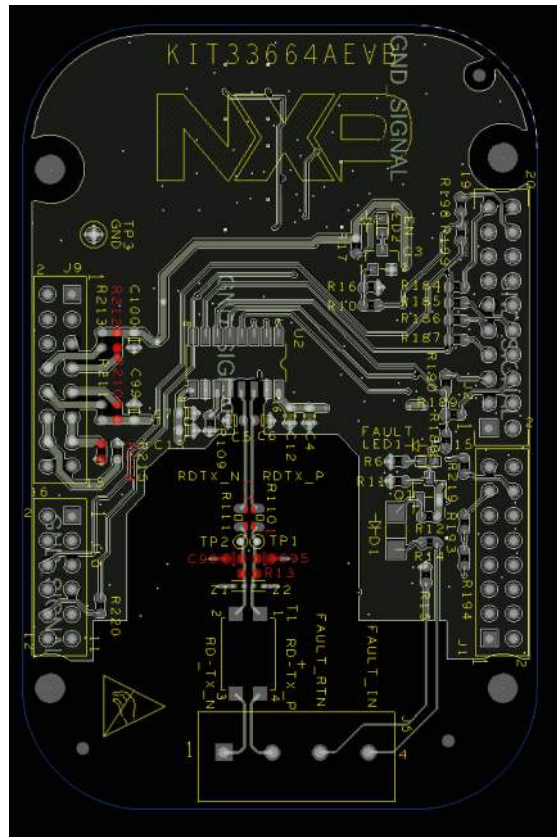


Figure 14. Top layer

10 Bill of materials

Table 12. Bill of Materials

| Item | Qty | Schematic label | Value | Description | Part number | Assy opt |
|--------------------------------|-----|--|-----------------|--|---------------|----------|
| Integrated Circuits [1] | | | | | | |
| 1 | 1 | U2 | - | Isolated Network High Speed Transceiver 16-Pin SOICN - NXP | MC33664ATL1EG | - |
| 2 | 2 | Z1, Z2 | - | ESD Protection diode 0402 | TPD1E10B06DPY | - |
| 3 | 1 | T1 | 120 μ H | Transformer | ESMIT-4180/C | - |
| Transistors [1] | | | | | | |
| 4 | 1 | Q1 | - | Driver Transistor PNP 80V SOT23 | MMBTA56LT1G | - |
| 5 | 1 | Q3 | - | Driver Transistor NPN 80V SOT23 | SMMBTA06LT1G | - |
| Diodes [1] | | | | | | |
| 6 | 1 | D1 | - | Diode General purpose 1kV 1A SOD123 | CGRM4007-G | - |
| LEDs [1] | | | | | | |
| 7 | 2 | FLT, EN | - | LED 630 nm RED 0603 SMD | SML-311UTT86 | - |
| Capacitors [1] | | | | | | |
| 8 | 2 | C5, C6 | 68 pF | 50 V Capacitor C0603 | - | - |
| 9 | 1 | C4 | 2.2 μ F | 6.3 V Capacitor C0603 | - | - |
| 10 | 4 | C7, C12, C99, C100 | 100 nF | 50 V Capacitor C0603 | - | - |
| 11 | 1 | C13 | 1 nF | 50 V Capacitor C0603 | - | - |
| 12 | 1 | C94 | 4.7 nF | 50 V Capacitor C0603 | - | - |
| 13 | 7 | C9, C10, C95, C96 | - | Capacitor C0603 | - | [2] |
| Resistors [1] | | | | | | |
| 14 | 4 | R1, R2, R4, R5 | 4.70 k Ω | Resistor R0603 | - | - |
| 15 | 2 | R6, R17 | 1.0 k Ω | Resistor R0603 | - | - |
| 16 | 4 | R10, R11, R12, R14 | 10 k Ω | Resistor R0603 | - | - |
| 17 | 1 | R15 | 300 Ω | Resistor R0603 | - | - |
| 18 | 2 | R107, R108 | 150 Ω | Resistor R0402 | - | - |
| 19 | 7 | R109, R162, R165, R176, R211, R213, R215 | 0 Ω | Resistor R0603 | - | - |
| 20 | 2 | R110, R111 | 0 Ω | Resistor R0805 | - | - |
| 21 | 18 | R184, R185, R186, R187, R188, R189, R190, R191, R192, R193, R194, R195, R196, R197, R198, R199, R219, R220 | 470 Ω | Resistor R0603 | - | - |

| Item | Qty | Schematic label | Value | Description | Part number | Assy opt |
|---|-----|---|-------|--|----------------|----------|
| 22 | 17 | R13, R161, R170, R171, R200, R201, R202, R203, R204, R205, R206, R207, R208, R209, R210, R212, R218 | - | Resistor R0603 | - | [2] |
| Switches, connectors, jumpers and testpoints | | | | | | [1] |
| 23 | 1 | J5 | - | Connector Terminal block 4POS 5.08MM PCB | 1935187 | - |
| 24 | 2 | J1, J9 | - | CON2X8 | SSQ-108-23-G-D | - |
| 25 | 1 | J2 | - | CON2X10 | SSQ-110-23-G-D | - |
| 26 | 1 | J10 | - | CON2X6 | SSQ-106-23-G-G | - |

[1] NXP does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

[2] Do Not Populate

11 References

Table 13. References

| NXP support pages | Description | URL |
|-------------------|----------------------|---|
| KIT33664AEVB | Tool Summary Page | http://www.nxp.com/KIT33664AEVB |
| MC33664 | Product Summary Page | http://www.nxp.com/MC33664 |
| FRDM-KL25Z | Tool Summary Page | http://www.nxp.com/FRDM-KL25Z |
| FRDM-KV31F | Tool Summary Page | http://www.nxp.com/FRDM-KV31F |
| FRDM-KE06Z | Tool Summary Page | http://www.nxp.com/FRDM-KE06Z |
| FRDM-KL43Z | Tool Summary Page | http://www.nxp.com/FRDM-KL43Z |
| FRDM-KW40Z | Tool Summary Page | http://www.nxp.com/FRDM-KW40Z |

12 Revision history

| Revision | Date | Description of changes |
|----------|---------|---------------------------------------|
| 1.0 | 5/2016 | Initial release |
| 2.0 | 10/2016 | Added kit contents for FRDM-33664AEVM |

13 Contact information

Visit <http://www.nxp.com/support> for a list of phone numbers within your region.

Visit <http://www.nxp.com/warranty> to submit a request for tool warranty.

14 Legal information

14.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

14.2 Disclaimers

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit,

and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/salestermsandconditions.

14.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — is a trademark of NXP B.V.

the NXP logo — is a trademark of NXP B.V.

Freescale — is a trademark of NXP B.V.

the Freescale logo — is a trademark of NXP B.V.

SMARTMOS — is a trademark of NXP B.V.

Tables

| | | | | | |
|---------|--------------------------|---|----------|--|----|
| Tab. 1. | Board description | 6 | Tab. 8. | Connector J9 | 10 |
| Tab. 2. | LEDs | 7 | Tab. 9. | Connector J10 | 10 |
| Tab. 3. | Modes of operation | 7 | Tab. 10. | KIT33664AEVB configuration table | 12 |
| Tab. 4. | Test points | 8 | Tab. 11. | Standalone configuration table | 15 |
| Tab. 5. | Connector J1 | 9 | Tab. 12. | Bill of Materials | 22 |
| Tab. 6. | Connector J2 | 9 | Tab. 13. | References | 24 |
| Tab. 7. | Connector J5 | 9 | | | |

Figures

| | | | | | |
|---------|--|----|----------|-----------------------------------|----|
| Fig. 1. | Block diagram | 4 | Fig. 9. | Freedom board configuration | 14 |
| Fig. 2. | Board description | 6 | Fig. 10. | Standalone configuration | 16 |
| Fig. 3. | LEDs | 7 | Fig. 11. | Communication signals | 17 |
| Fig. 4. | Test points | 8 | Fig. 12. | Schematic (a) | 18 |
| Fig. 5. | Connectors | 9 | Fig. 13. | Schematic (b) | 19 |
| Fig. 6. | TPL bus description | 10 | Fig. 14. | Top layer | 20 |
| Fig. 7. | FAULT circuit schematic | 11 | Fig. 15. | Bottom layer | 21 |
| Fig. 8. | KIT33664AEVB mounted to a FRDM-KL25Z ... | 12 | | | |

Contents

| | | |
|-----------|---|-----------|
| 1 | KIT33664AEVB | 1 |
| 2 | Important notice | 2 |
| 3 | Getting started | 3 |
| 3.1 | Kit contents/packing list | 3 |
| 3.2 | Jump start | 3 |
| 3.3 | Required equipment | 3 |
| 4 | Understanding the KIT33664AEVB | 4 |
| 4.1 | Board overview | 4 |
| 4.2 | Board features | 4 |
| 4.3 | Block diagram | 4 |
| 4.4 | Device features | 5 |
| 5 | Getting to know the hardware | 6 |
| 5.1 | Board description | 6 |
| 5.2 | LEDs | 7 |
| 5.3 | Test points | 8 |
| 5.4 | Connectors | 8 |
| 5.5 | Signal bus terminal description | 10 |
| 6 | Setting up the hardware | 11 |
| 6.1 | Fault input detection | 11 |
| 7 | Configuring the hardware | 12 |
| 7.1 | Freedom board configuration | 12 |
| 7.1.1 | Step-by-step instructions for setting up the hardware in a Freedom board configuration | 14 |
| 7.2 | Standalone configuration | 15 |
| 7.2.1 | Step-by-step instructions for setting up the hardware | 15 |
| 8 | Schematic | 18 |
| 9 | Board layout | 20 |
| 10 | Bill of materials | 22 |
| 11 | References | 24 |
| 12 | Revision history | 24 |
| 13 | Contact information | 24 |
| 14 | Legal information | 25 |

© NXP B.V. 2016. All rights reserved

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Released on 25 October 2016
