High Temperature, 16-Bit, 600 kSPS PulSAR ADC

Data Sheet **AD7981**

FEATURES

- Extreme high temperature operation
  - Specified temperature range
    - −55°C to +210°C (10-lead FLATPACK)
    - −55°C to +175°C (10-lead MSOP)
- High performance
  - Pseudo differential analog input range
    - 0 V to V_{REF} with V_{REF} between 2.4 V and 5.1 V
  - Throughput: 600 kSPS
    - Zero latency architecture
  - 16-bit resolution with no missing codes
  - INL: ±2.5 LSB maximum, DNL: ±0.9 LSB maximum
  - Dynamic range: 92 dB, V_{REF} = 5 V
  - SNR: 91 dB at f_{IN} = 1 kHz, V_{REF} = 5 V
  - THD: −102 dB at f_{IN} = 1 kHz, V_{REF} = 5 V
  - SINAD: 90.5 dB at f_{IN} = 1 kHz, V_{REF} = 5 V
- Low power dissipation
  - Single-supply 2.5 V operation with 1.8 V to 5 V logic interface
  - 2.25 mW typical at 600 kSPS (VDD only)
  - 4.65 mW typical at 600 kSPS (total)
  - 75 µW typical at 10 kSPS
- Proprietary serial interface
  - SPI-/QSPI-/MICROWIRE-/DSP-compatible
- Daisy-chain multiple ADCs and busy indicator
- Small footprint
  - 10-lead, 3 mm × 3 mm, monometallic wire bonding MSOP
  - 10-lead, 0.255 inches × 0.255 inches, monometallic wire bonding FLATPACK

APPLICATIONS

- Oil and gas exploration
- Avionics
- Heavy industrial
- High temperature environments
- Scientific instrumentation

TYPICAL APPLICATION CIRCUIT

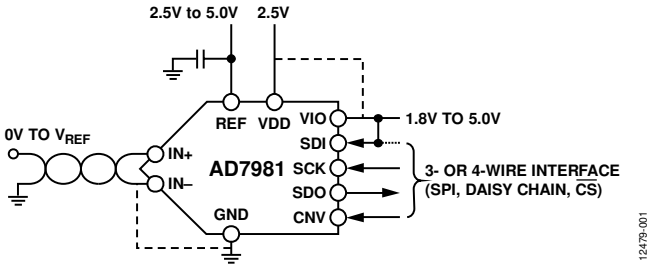

Figure 1.

GENERAL DESCRIPTION

The AD7981[1] is a 16-bit, successive approximation, PulSAR® analog-to-digital converter (ADC) designed for high temperature operation. The AD7981 is capable of sample rates of up to 600 kSPS while maintaining low power consumption from a single power supply, VDD. It is a fast throughput, high accuracy, high temperature, successive approximation register (SAR) ADC, packaged in a small form factor with a versatile serial port interface (SPI).

On the CNV rising edge, the AD7981 samples an analog input, IN+, between 0 V and REF with respect to a ground sense, IN−. The reference voltage, REF, is applied externally and can be set independent of the supply voltage, VDD. The device power scales linearly with throughput.

The SPI-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single, 3-wire bus and provides an optional busy indicator. It is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic, using the separate supply, VIO.

For space constrained applications, the AD7981 is available in a 10-lead mini small outline package (MSOP) with operation specified from −55°C to +175°C and 10-lead ceramic flat package (FLATPACK) with operation specified from −55°C to +210°C. These packages are designed for robustness at extreme temperatures, including monometallic wire bonding, and are qualified for up to 1000 hours of operation at the maximum temperature rating.

The AD7981 is a member of a growing series of high temperature qualified products offered by Analog Devices, Inc. For a complete selection of available high temperature products, see the high temperature product list and qualification data available at www.analog.com/hightemp.

[1] Protected by U.S. Patent 6,703,961.

Rev. C Document Feedback

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10/2014—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.5 V, VIO = 1.71 V to 5.5 V, V_{REF} = 5 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	IN+ − IN−	0		V_{REF}	V
Absolute Input Voltage	IN+	−0.1		V_{REF} + 0.1	V
	IN−	−0.1		+0.1	V
Analog Input Common-Mode Rejection Ratio (CMRR)	f_{IN} = 100 kHz		60		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance		See the Analog Input section			
ACCURACY					
No Missing Codes		16			Bits
Differential Nonlinearity (DNL)	V_{REF} = 5 V	−0.9	±0.4	+0.9	LSB[1]
	V_{REF} = 2.5 V		±0.5		LSB[1]
Integral Nonlinearity (INL)					
10-Lead MSOP[2]	V_{REF} = 5 V	−2.0	±0.7	+2.0	LSB[1]
	V_{REF} = 2.5 V		±0.6		LSB[1]
10-Lead FLATPACK[2]	V_{REF} = 5 V	−2.5	±0.7	+2.5	LSB[1]
	V_{REF} = 2.5 V		±0.6		LSB[1]
Transition Noise	V_{REF} = 5 V		0.75		LSB[1]
	V_{REF} = 2.5 V		1.2		LSB[1]
Gain Error[3]	T_{MIN} to T_{MAX}		±2		LSB[1]
Gain Error Temperature Drift			±0.35		ppm/°C
Zero Error[3]	T_{MIN} to T_{MAX}	−1	±0.08	+1	mV
Zero Temperature Drift			0.45		ppm/°C
Power Supply Sensitivity	VDD = 2.5 V ± 5%		±0.1		LSB[1]
THROUGHPUT					
Conversion Rate		0		600	kSPS
Transient Response	Full-scale step			290	ns
AC ACCURACY[4]					
Dynamic Range	V_{REF} = 5 V		92		dB
	V_{REF} = 2.5 V		87		dB
Oversampled Dynamic Range[5]	OSR = 256		110		dB
Signal-to-Noise Ratio (SNR)	f_{IN} = 1 kHz, V_{REF} = 5 V	89	91		dB
	f_{IN} = 1 kHz, V_{REF} = 2.5 V		86		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 1 kHz		104		dB
Total Harmonic Distortion (THD)	f_{IN} = 1 kHz		−102		dB
Signal-to-Noise-and-Distortion (SINAD) Ratio	f_{IN} = 1 kHz, V_{REF} = 5 V		90.5		dB
	f_{IN} = 1 kHz, V_{REF} = 2.5 V		85.5		dB

[1] LSB means least significant bit. With the 5 V input range, 1 LSB is 76.3 µV.
[2] MSOP operation is specified from −55°C to +175°C and FLATPACK operation specified is specified from −55°C to +210°C.
[3] See the Terminology section. These specifications include full temperature range variation, but not the error contribution from the external reference.
[4] All ac accuracy specifications (in dB) are referred to an input full-scale range (FSR). Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[5] The oversampled dynamic range is the ratio of the peak signal power to the noise power (for a small input) measured in the ADC output fast Fourier transform (FFT) from dc up to $f_S/(2 \times OSR)$, where f_S is the ADC sample rate and OSR is the oversampling ratio.

VDD = 2.5 V, VIO = 1.71 V to 5.5 V, V_{REF} = 5 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE					
Voltage Range (V_{REF})		2.4		5.1	V
Load Current	600 kSPS, V_{REF} = 5 V		330		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			10		MHz
Aperture Delay	VDD = 2.5 V		2		ns
DIGITAL INPUTS					
Logic Levels					
Input Voltage					
Low (V_{IL})	VIO > 3 V	−0.3		0.3 × VIO	V
	VIO ≤ 3 V	−0.3		0.1 × VIO	V
High (V_{IH})	VIO > 3 V	0.7 × VIO		VIO + 0.3	V
	VIO ≤ 3 V	0.9 × VIO		VIO + 0.3	µA
Input Current					
Low (I_{IL})		−1		+1	µA
High (I_{IH})		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial, 16 bits, straight binary			
Pipeline Delay		Conversion results available immediately after completed conversion			
Output Voltage					
Low (V_{OL})	I_{SINK} = 500 µA			0.4	V
High (V_{OH})	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD		2.375	2.5	2.625	V
VIO		1.71		5.5	V
Standby Current[1, 2]	VDD and VIO = 2.5 V		0.35		µA
Power Dissipation	VDD = 2.625 V, V_{REF} = 5 V, VIO = 3 V				
Total	10 kSPS		75		µW
	600 kSPS (MSOP)		4.65	7	mW
	600 kSPS (FLATPACK)		4.65	12	mW
VDD Only	600 kSPS		2.25		mW
REF Only	600 kSPS		1.5		mW
VIO Only	600 kSPS		0.9		mW
Energy per Conversion			7.75		nJ/sample
TEMPERATURE RANGE					
Specified Performance[3]	T_{MIN} to T_{MAX}				
10-Lead FLATPACK		−55		+210	°C
10-Lead MSOP		−55		+175°C	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During the acquisition phase.
[3] Qualified for up to 1000 hours of operation at the maximum temperature rating.

TIMING SPECIFICATIONS

VDD = 2.375 V to 2.625 V, VIO = 1.71 V to 5.5 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated. See Figure 2 for load conditions.

Table 3.

Parameter[1]	Symbol	Min	Typ	Max	Unit
CONVERSION AND ACQUISITION TIMES					
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	800		1200	ns
Acquisition Time	t_{ACQ}	290			ns
Time Between Conversions	t_{CYC}	1667			ns
CNV PULSE WIDTH ($\overline{CS}$ MODE)	t_{CNVH}	10			ns
SCK					
SCK Period ($\overline{CS}$ Mode)	t_{SCK}				
VIO Above 4.5 V		10.5			ns
VIO Above 3 V		12			ns
VIO Above 2.7 V		13			ns
VIO Above 2.3 V		15			ns
VIO Above 1.71 V		22			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO Above 4.5 V		11.5			ns
VIO Above 3 V		13			ns
VIO Above 2.7 V		14			ns
VIO Above 2.3 V		16			ns
VIO Above 1.71 V		23			ns
SCK Low Time	t_{SCKL}				
VIO Above 2.3 V		4.5			ns
VIO Above 1.71 V		6			ns
SCK High Time	t_{SCKH}				
VIO Above 2.3 V		4.5			ns
VIO Above 1.71 V		6			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	3			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				9.5	ns
VIO Above 3 V				11	ns
VIO Above 2.7 V				12	ns
VIO Above 2.3 V				14	ns
VIO Above 1.71 V			14	21	ns
$\overline{CS}$ MODE					
CNV or SDI Low to SDO D15 MSB Valid	t_{EN}				
VIO Above 3 V				10	ns
VIO Above 2.3 V				15	ns
VIO Above 1.71 V			18	40	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$	5			ns
SDI Valid Hold Time from CNV Rising Edge	$t_{HSDICNV}$				ns
VIO Above 2.3 V		2			ns
VIO Above 1.71 V		10			ns

Parameter[1]	Symbol	Min	Typ	Max	Unit
CHAIN MODE					
SDI Valid Hold Time from CNV Rising Edge	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Falling Edge	$t_{HSDISCK}$	3			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$			15	ns

[1] Timing parameters measured with respect to a falling edge are defined as triggered at x% VIO. Timing parameters measured with respect to a rising edge are defined as triggered at y% VIO. For VIO ≤ 3 V, x = 90 and y = 10. For VIO > 3 V, x = 70 and y = 30. The minimum V_{IH} and maximum V_{IL} are used. See the Digital Inputs parameter in Table 2.

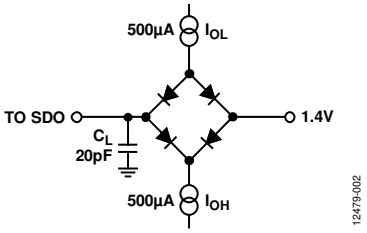


Figure 2. Load Circuit for Digital Interface Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Analog Inputs	
IN+, IN− to GND[1]	−0.3 V to V_{REF} + 0.3 V or ±130 mA
Supply Voltage	
REF, VIO to GND	−0.3 V to +6 V
VDD to GND	−0.3 V to +3 V
VDD to VIO	+3 V to −6 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature[2]	
10-Lead MSOP	175.12°C
10-Lead FLATPACK	210.13°C
Lead Temperature Soldering	260°C reflow as per JEDEC J-STD-020
ESD Ratings	
Human Body Model	2 kV
Machine Model	200 V
Field Induced Charged Device Model	1.25 kV

[1] See the Analog Input section. A transient with a very short duration of 10 ms applied on the analog inputs, IN+ and IN−, during latch-up testing shows that these diodes can then handle a forward-biased current of 130 mA maximum.

[2] The maximum junction temperature consists of the maximum specified ambient temperature plus self heating rise under normal operating conditions.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
RM-10	146.76	38.12	°C/W
F-10-2	107.5	25.5	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on the use of a 2S2P JEDEC PCB. See the Ordering Guide.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

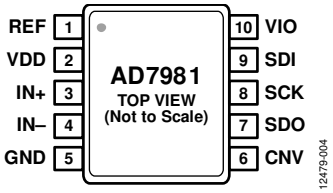


Figure 3. 10-Lead MSOP Pin Configuration

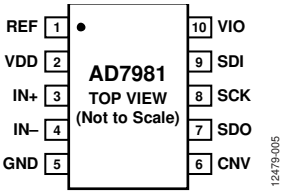


Figure 4. 10-Lead FLATPACK Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type [1]	Description
1	REF	AI	Reference Input Voltage. The REF range, V_{REF}, is from 2.4 V to 5.1 V. V_{REF} is referred to the GND pin. Decouple REF with a 10 µF capacitor as close as possible to the pin.
2	VDD	P	Power Supply.
3	IN+	AI	Analog Input. This pin is referred to IN−. The voltage range, for example, the difference between IN+ and IN−, is 0 V to V_{REF}.
4	IN−	AI	Analog Input Ground Sense. Connect this pin to the analog ground plane or to a remote sense ground.
5	GND	P	Power Supply Ground.
6	CNV	DI	Conversion Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the device: chain or $\overline{CS}$ mode. In $\overline{CS}$ mode, it enables the SDO pin when low. In chain mode, read the data when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the device is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
10	VIO	P	Input/Output Interface Digital Power. VIO is nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).

[1] AI is the analog input, P is the power, DI is the digital input, and DO is the digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 2.5 V, V_{REF} = 5.0 V, VIO = 3.3 V, T_A = 25°C, unless otherwise noted.

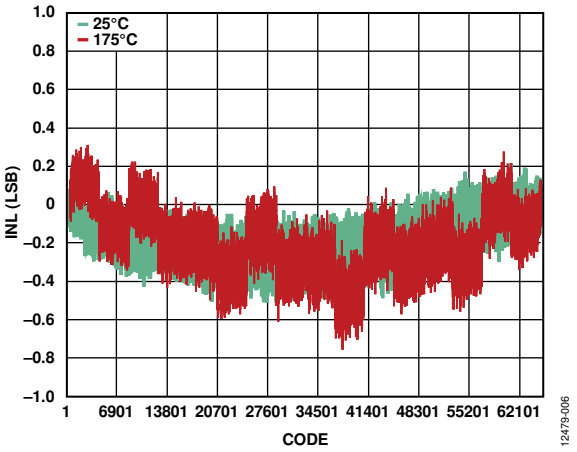


Figure 5. Integral Nonlinearity (INL) vs. Code and Temperature, V_{REF} = 5.0 V, MSOP

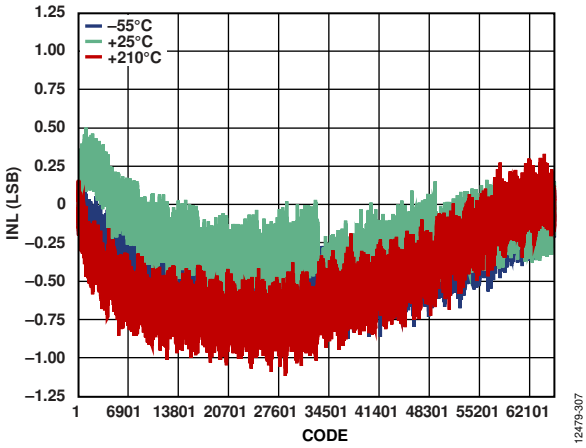


Figure 8. Integral Nonlinearity (INL) vs. Code and Temperature, V_{REF} = 5.0 V, FLATPACK

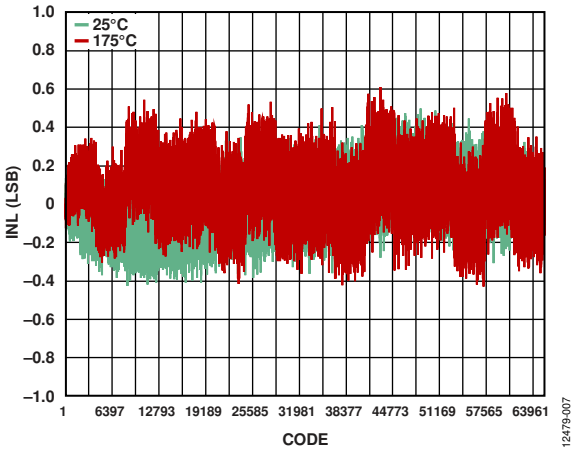


Figure 6. Integral Nonlinearity (INL) vs. Code and Temperature, V_{REF} = 2.5 V, MSOP

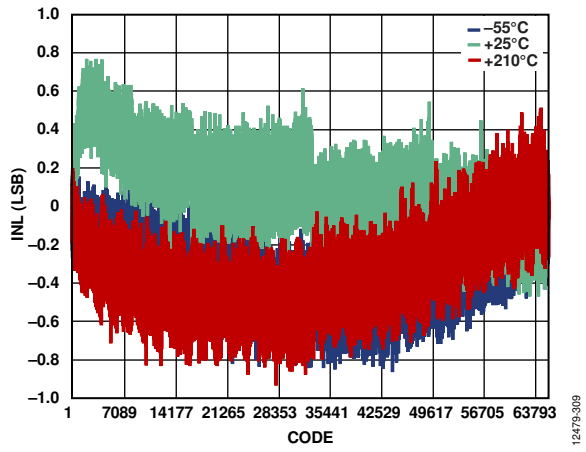


Figure 9. Integral Nonlinearity (INL) vs. Code and Temperature, V_{REF} = 2.5 V, FLATPACK

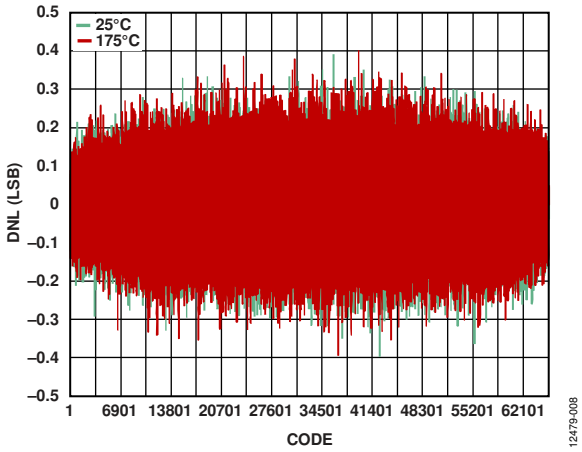


Figure 7. Differential Nonlinearity (DNL) vs. Code and Temperature, V_{REF} = 5.0 V, MSOP

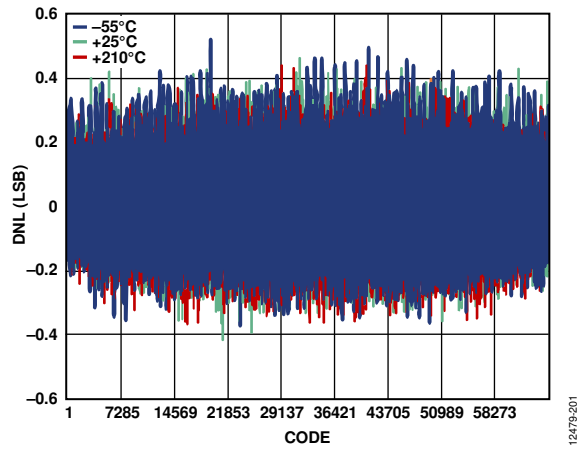


Figure 10. Differential Nonlinearity (DNL) vs. Code and Temperature, V_{REF} = 5.0 V, FLATPACK

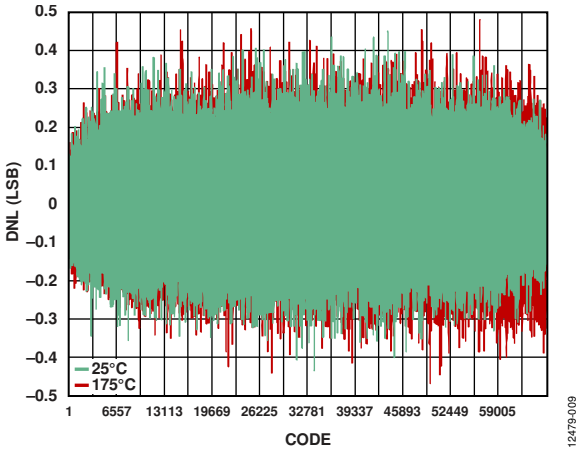


Figure 11. Differential Nonlinearity (DNL) vs. Code and Temperature, V_{REF} = 2.5 V, MSOP

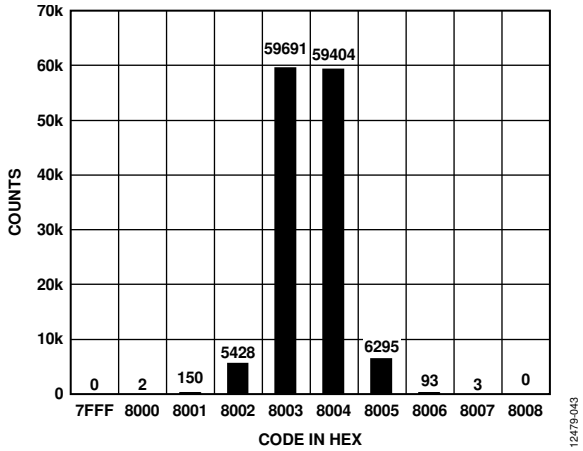


Figure 12. Histogram of a DC Input at the Code Transition, V_{REF} = 5.0 V

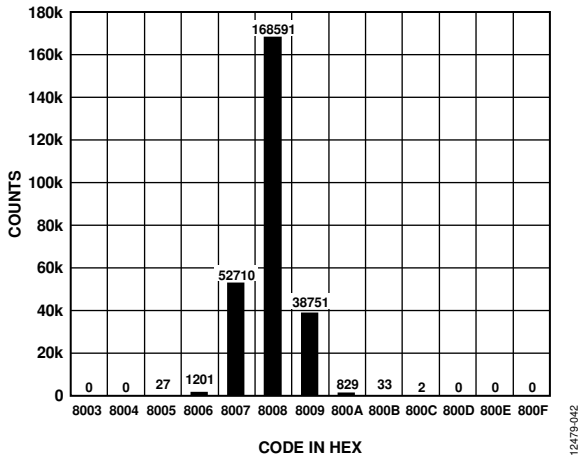


Figure 13. Histogram of a DC Input at the Code Center, V_{REF} = 5.0 V

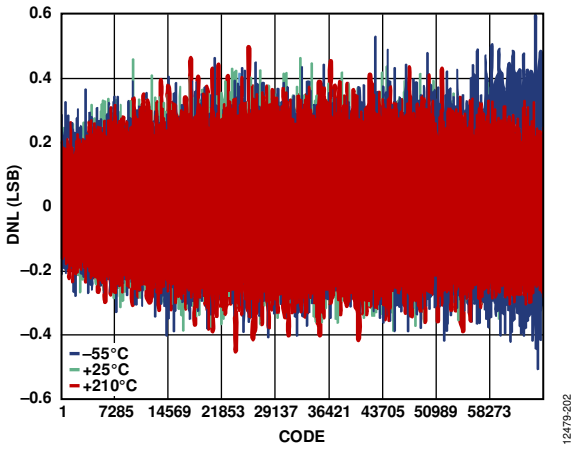


Figure 14. Differential Nonlinearity (DNL) vs. Code and Temperature, V_{REF} = 2.5 V, FLATPACK

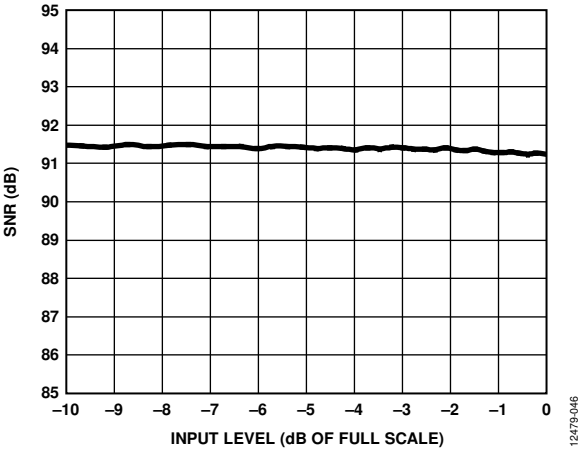


Figure 15. SNR vs. Input Level

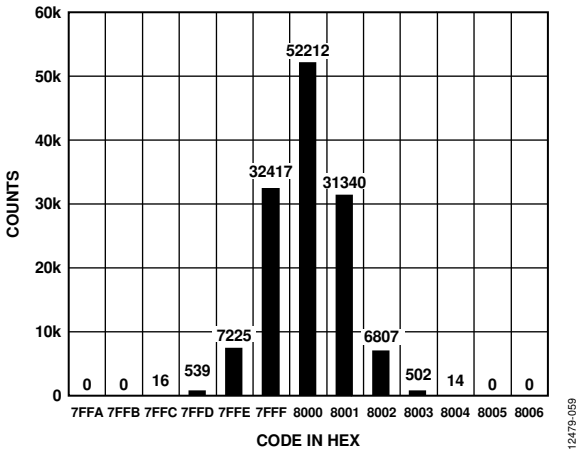


Figure 16. Histogram of a DC Input at the Code Center, V_{REF} = 2.5 V

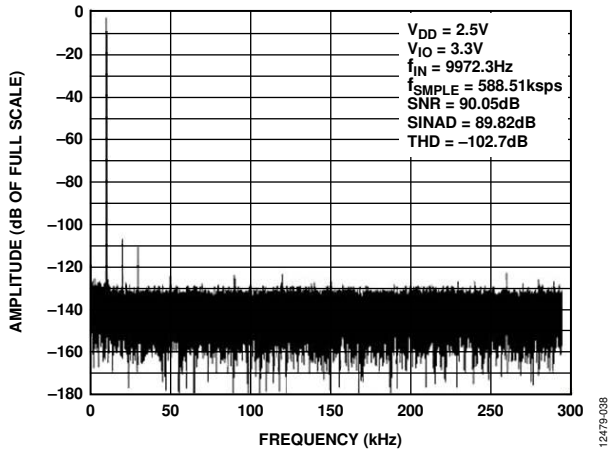


Figure 17. 10 kHz FFT, V_{REF} = 5.0 V

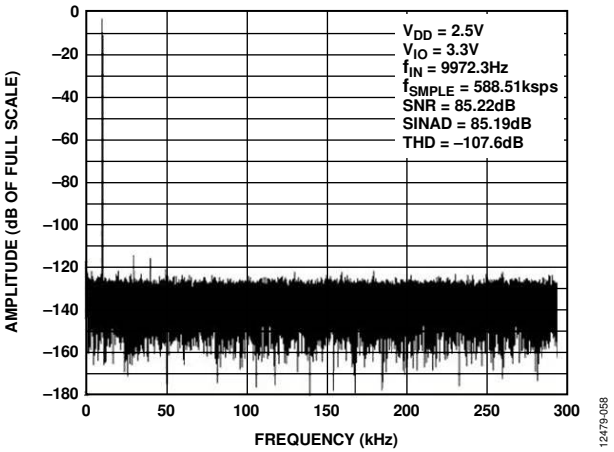


Figure 20. 10 kHz FFT, V_{REF} = 2.5 V

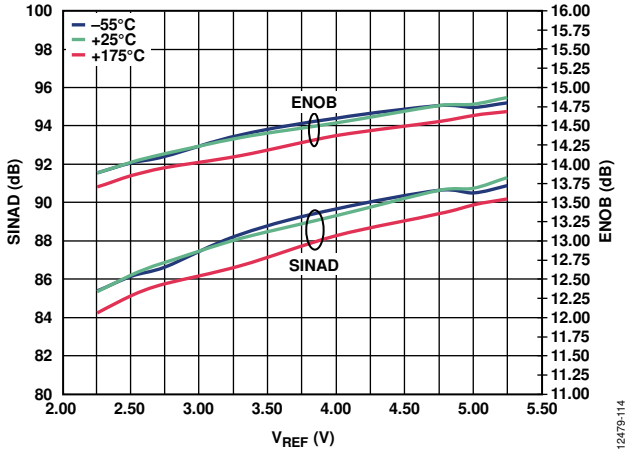


Figure 18. SINAD and ENOB vs. Reference Voltage (V_{REF}), MSOP

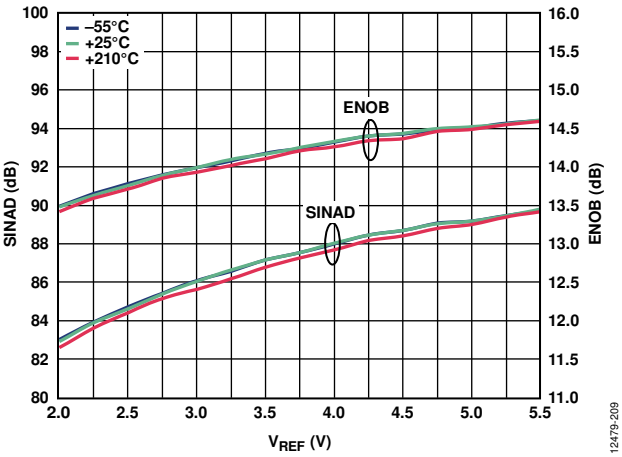


Figure 21. SINAD and ENOB vs. Reference Voltage (V_{REF}), FLATPACK

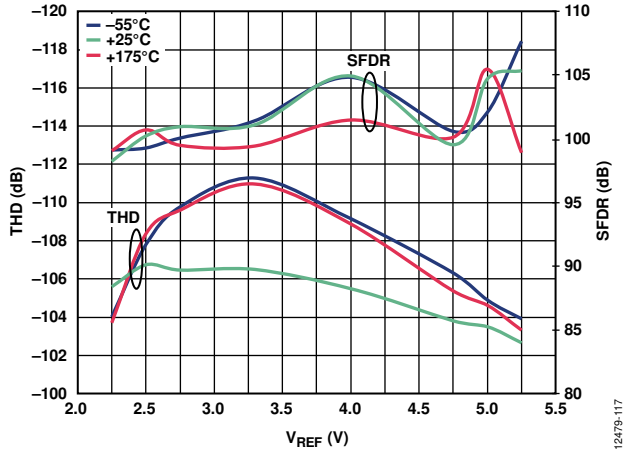


Figure 19. THD and SFDR vs. Reference Voltage (V_{REF}), MSOP

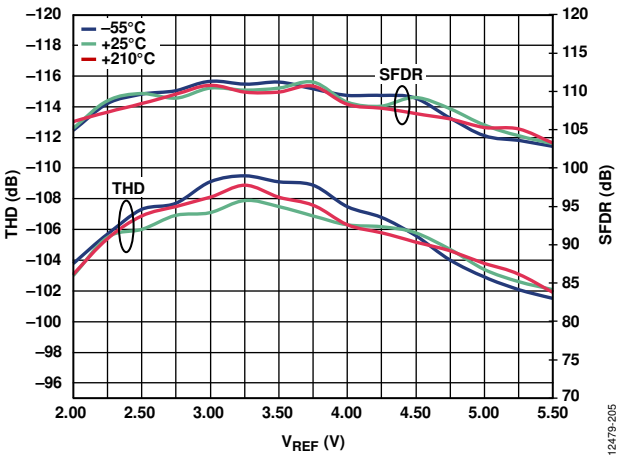


Figure 22. THD and SFDR vs. Reference Voltage (V_{REF}), FLATPACK

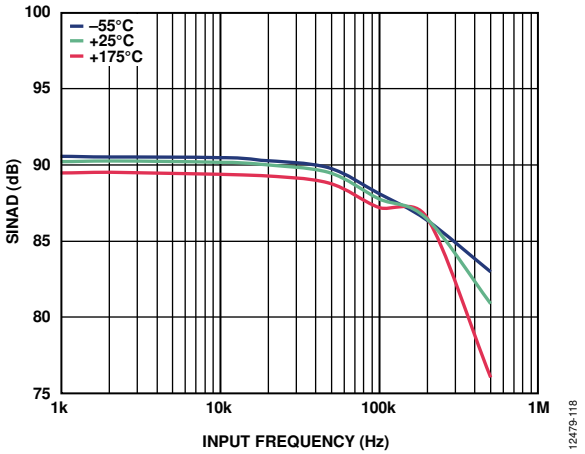


Figure 23. SINAD vs. Input Frequency, MSOP

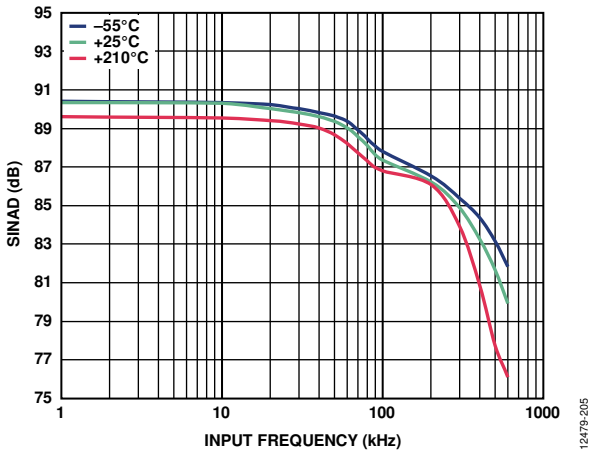


Figure 26. SINAD vs. Input Frequency, FLATPACK

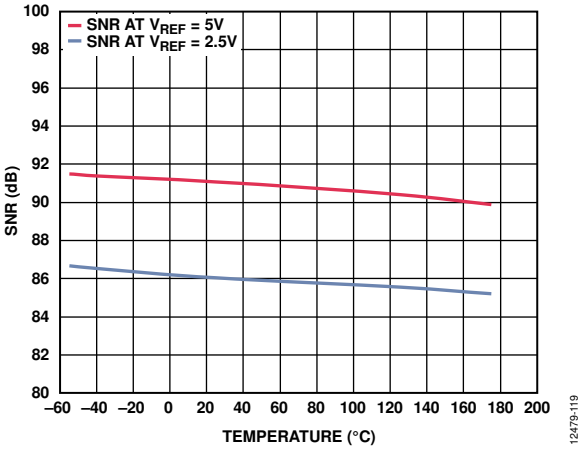


Figure 24. SNR vs. Temperature, MSOP

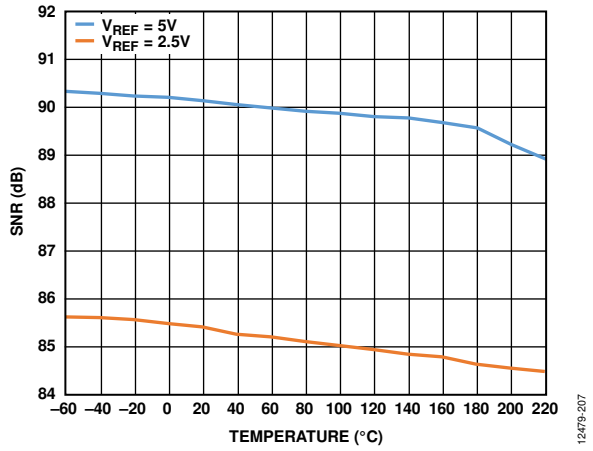


Figure 27. SNR vs. Temperature, FLATPACK

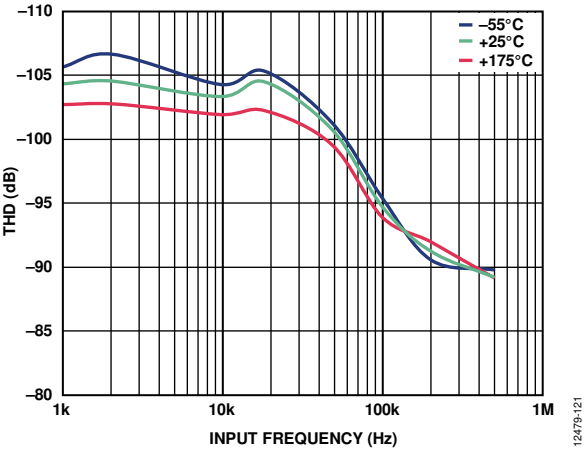


Figure 25. THD vs. Frequency, MSOP

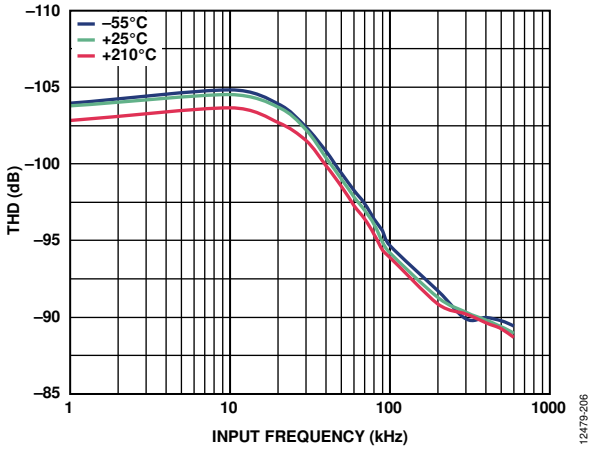


Figure 28. THD vs. Input Frequency, FLATPACK

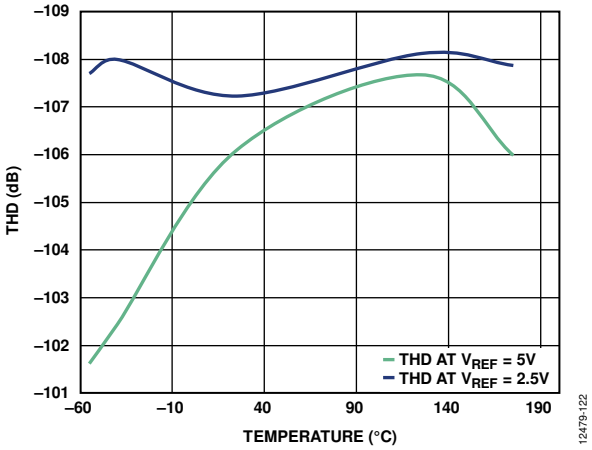


Figure 29. THD vs. Temperature, MSOP

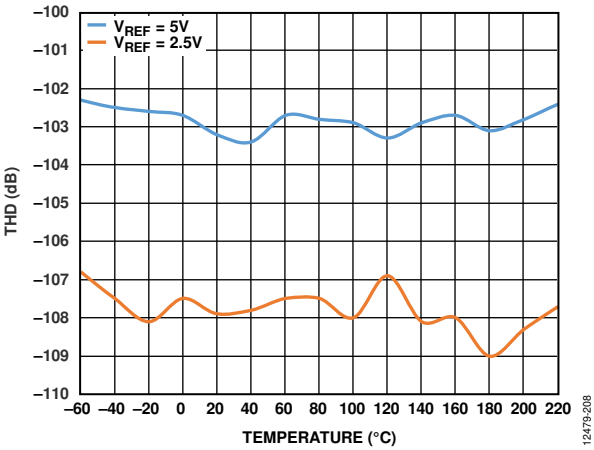


Figure 32. THD vs. Temperature, FLATPACK

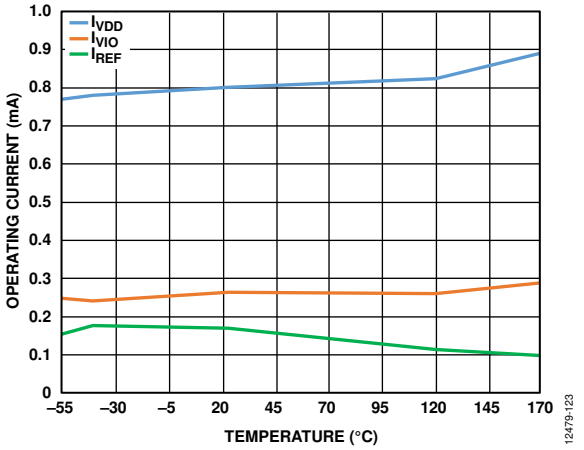


Figure 30. Operating Current vs. Temperature, MSOP

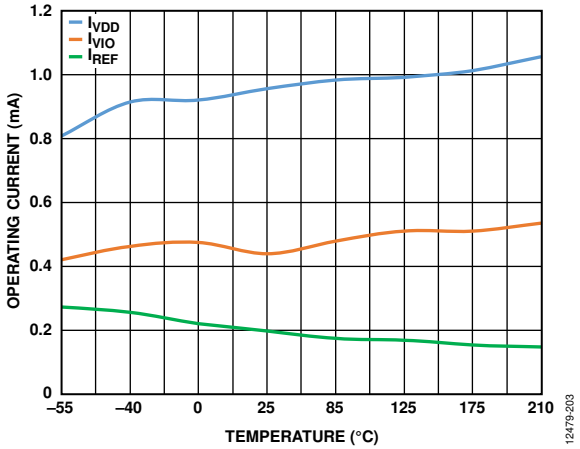


Figure 33. Operating Current vs. Temperature, FLATPACK

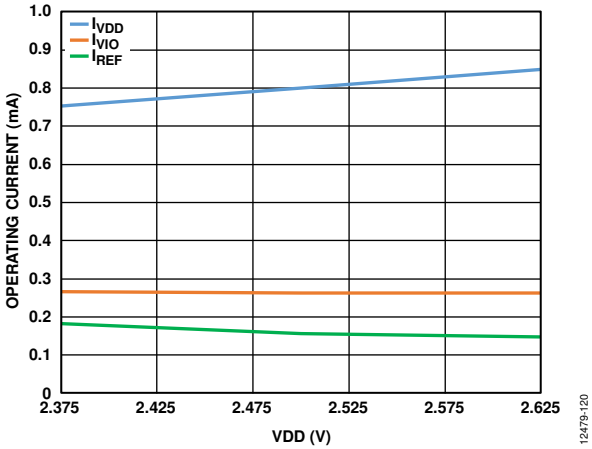


Figure 31. Operating Current vs. Supply Voltage (VDD)

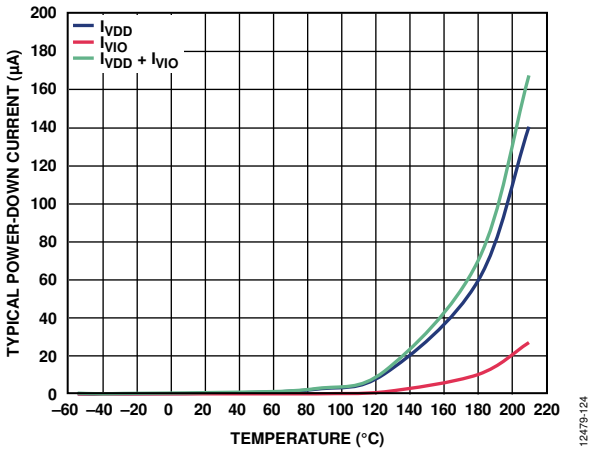


Figure 34. Typical Power-Down Current vs. Temperature

TERMINOLOGY

Integral Nonlinearity (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 37).

Differential Nonlinearity (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error
The first transition occurs at a level ½ LSB above analog ground (38.1 µV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111 … 10 to 111 … 11) occurs for an analog voltage 1½ LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset is adjusted out.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula and is expressed in bits:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

Noise Free Code Resolution
Noise free code resolution is the number of bits beyond which it is impossible to distinctly resolve individual codes. It is calculated as follows and is expressed in bits:

$$\textit{Noise Free Code Resolution} = \log_2(2^N/\textit{Peak-to-Peak Noise})$$

Effective Resolution
Effective resolution is calculated as follows and is expressed in bits:

$$\textit{Effective Resolution} = \log_2(2^N/\textit{RMS Input Noise})$$

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. It is measured with a signal at −60 dBFS to include all noise sources and DNL artifacts. The value for dynamic range is expressed in dB.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

Signal-to-Noise-and-Distortion (SINAD) Ratio
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

Aperture Delay
Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

THEORY OF OPERATION

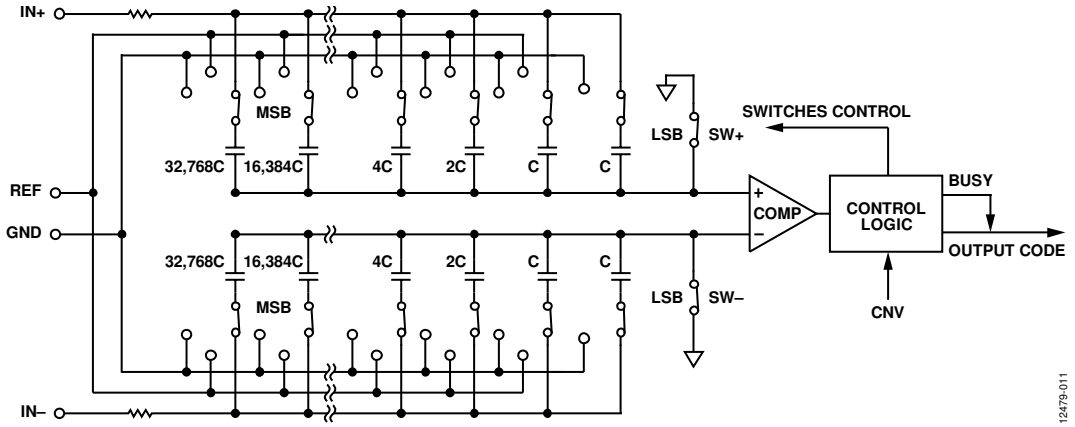


Figure 35. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7981 is a fast, low power, single-supply, precise 16-bit ADC that uses a successive approximation architecture.

The AD7981 is capable of converting 600,000 samples per second (600 kSPS) and powers down between conversions. When operating at 10 kSPS, for example, it consumes 75 µW typically, ideal for battery-powered applications.

The AD7981 provides the user with on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

The AD7981 can be interfaced to any 1.8 V to 5 V digital logic family. It is housed in a 10-lead MSOP and 10-lead FLATPACK. These packages, which combine space savings and allow flexible configurations, are designed for robustness at extreme temperatures.

CONVERTER OPERATION

The AD7981 is a successive approximation ADC based on a charge redistribution digital-to-analog converter (DAC). Figure 36 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the input of the comparator are connected to GND via the SW+ and SW− switches. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs, IN+ and IN−, captured at the end of the acquisition phase, is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/65,536$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the device returns to the acquisition phase, and the control logic generates the ADC output code and a busy signal indicator.

Because the AD7981 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

Transfer Functions

The ideal transfer characteristic for the AD7981 is shown in Figure 37 and Table 6.

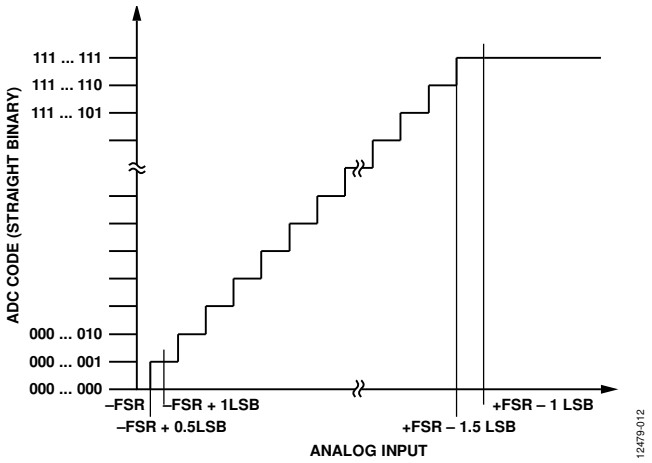


Figure 36. ADC Ideal Transfer Function

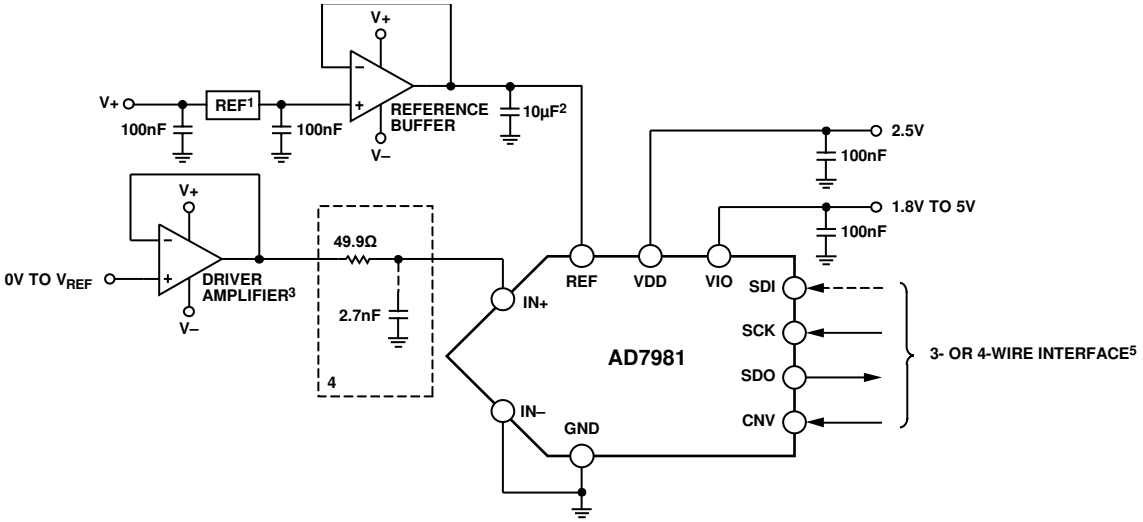
Table 7. Output Codes and Ideal Input Voltages

	Analog Input	
Description	**V_{REF} = 5 V**	**Digital Output Code**
FSR – 1 LSB	4.999924 V	0xFFFF[1]
Midscale + 1 LSB	2.500076 V	0x8001
Midscale	2.5 V	0x8000
Midscale – 1 LSB	2.499924 V	0x7FFF
–FSR + 1 LSB	76.3 µV	0x0001
–FSR	0 V	0x0000[2]

[1] This is also the code for an overranged analog input (V_{IN+} – V_{IN-} above V_{REF} – V_{GND}).
[2] This is also the code for an underranged analog input (V_{IN+} – V_{IN-} below V_{GND}).

TYPICAL CONNECTION DIAGRAM

Figure 38 shows an example of the recommended connection diagram for the AD7981 when multiple supplies are available.



[1]SEE THE VOLTAGE REFERENCE INPUT SECTION FOR REFERENCE SELECTION.
[2]C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR.
[3]SEE THE DRIVER AMPLIFIER CHOICE SECTION.
[4]SUGGESTED FILTER CONFIGURATION. SEE THE ANALOG INPUT SECTION.
[5]SEE THE DIGITAL INTERFACE SECTION FOR THE MOST CONVENIENT INTERFACE MODE.

Figure 37. Typical Application Diagram with Multiple Supplies

ANALOG INPUT

Figure 39 shows an equivalent circuit of the input structure of the AD7981.

The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN+ and IN−. Ensure that the analog input signal never exceeds the supply rails by more than 0.3 V, because this causes these diodes to become forward-biased and to start conducting current. A transient with a very short duration of 10 ms applied on the analog inputs, IN+ and IN−, during latch-up testing shows that these diodes can then handle a forward-biased current of 130 mA maximum. For instance, these conditions may eventually occur when the supplies of the input buffer (U1) are different from VDD. In such a case (for example, an input buffer with a short circuit), use the current limitation to protect the device.

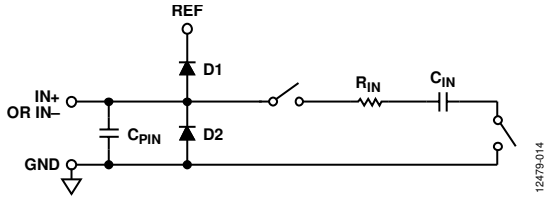


Figure 38. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected.

During the acquisition phase, model the impedance of the analog inputs (IN+ and IN−) as a parallel combination of the capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 400 Ω and is a lumped component composed of some serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, where the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} combine to make a one-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, drive the AD7981 directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

DRIVER AMPLIFIER CHOICE

Although the AD7981 is easy to drive, the driver amplifier must meet the following requirements:

- Keep the noise generated by the driver amplifier as low as possible to preserve the SNR and transition noise performance of the AD7981. The noise coming from the driver is filtered by the one-pole, low-pass filter of the AD7981 analog input circuit made by R_{IN} and C_{IN}, or by the external filter, if one is used. Because the typical noise of the AD7981 is 47.3 µV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log\left(\frac{47.3}{\sqrt{47.3^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}}\right)$$

  where:
  f_{-3dB} is the input bandwidth in MHz of the AD7981 (10 MHz) or the cutoff frequency of the input filter, if one is used.
  N is the noise gain of the amplifier (for example, 1 in buffer configuration).
  e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.
- For ac applications, the driver must have THD performance commensurate with the AD7981.
- For multichannel multiplexed applications, the driver amplifier and the AD7981 analog input circuit must settle for a full-scale step onto the capacitor array at a 16-bit level (0.0015%, 15 ppm). In an amplifier data sheet, settling times at 0.1% to 0.01% are more commonly specified, and may differ significantly from the settling time at a 16-bit level and, therefore, must be verified prior to driver selection.

The AD8634 is a rail-to-rail output, precision, low power, high temperature qualified, dual amplifier recommended for driving the input of the AD7981.

VOLTAGE REFERENCE INPUT

The AD7981 voltage reference input, REF, has a dynamic input impedance and must therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in the Printed Circuit Board (PCB) Layout section.

When REF is driven by a very low impedance source, a ceramic chip capacitor is appropriate for optimum performance. The high temperature qualified low temperature drift ADR225 2.5 V reference and the low power AD8634 reference buffer are recommended for the AD7981.

The REF pin must be decoupled with a ceramic chip capacitor of at least 10 µF (X5R, 1206 size) for optimum performance.

There is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

POWER SUPPLY

The AD7981 uses two power supply pins: a core supply, VDD, and a digital input/output interface supply, VIO. VIO allows direct interfacing with any logic between 1.8 V and 5 V. To reduce the number of supplies needed, tie VIO and VDD together. When VIO is greater than or equal to VDD, the AD7981 is insensitive to power supply sequencing. In normal operation, if the magnitude of VIO is less than the magnitude of VDD, VIO must be applied before VDD. Additionally, it is insensitive to power supply variations over a wide frequency range, as shown in Figure 40.

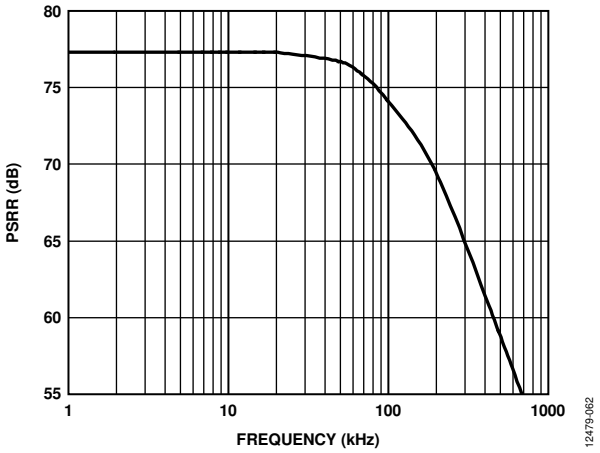


Figure 39. PSRR vs. Frequency

The AD7981 powers down automatically at the end of each conversion phase and, therefore, the power scales linearly with the sampling rate, which makes the device ideal for low sampling rate (even of a few Hz) and low battery-powered applications.

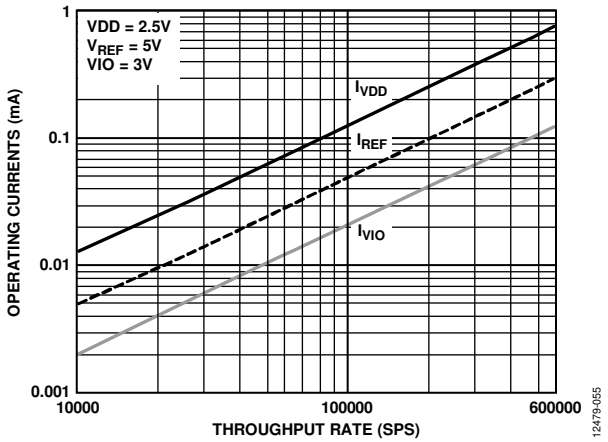


Figure 40. Operating Currents vs. Throughput Rate

DIGITAL INTERFACE

Although the AD7981 has a reduced number of pins, it offers flexibility in its serial interface modes.

The AD7981, when in $\overline{CS}$ mode, is compatible with SPI, QSPI™, MICROWIRE™, and digital hosts. The AD7981 interface can use either a 3-wire or 4-wire interface. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections and is useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). The 4-wire interface is useful in low jitter sampling or simultaneous sampling applications.

The AD7981, when in chain mode, provides a daisy-chain feature using the SDI input for cascading multiple ADCs on a single data line, similar to a shift register.

The mode in which the device operates depends on the SDI level when the CNV rising edge occurs. $\overline{CS}$ mode is selected if SDI is high, and chain mode is selected if SDI is low. The SDI hold time is such that, when SDI and CNV are connected together, chain mode is selected.

In either mode, the AD7981 offers the flexibility to optionally force a start bit in front of the data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and to trigger the data reading. Otherwise, without a busy indicator, the user must time out the maximum conversion time prior to readback.

The busy indicator feature is enabled in the following modes:

- In $\overline{CS}$ mode if CNV or SDI is low when the ADC conversion ends (see Figure 45 and Figure 49, respectively).
- In chain mode if SCK is high during the CNV rising edge (see Figure 53).

$\overline{CS}$ MODE, 3-WIRE WITHOUT A BUSY INDICATOR

The 3-wire $\overline{CS}$ mode without a busy indicator is typically used when a single AD7981 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 42, and the corresponding timing is given in Figure 43.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. When a conversion is initiated, it continues until completion, irrespective of the state of CNV, which can be useful, for instance, for bringing CNV low to select other SPI devices, such as analog multiplexers. However, CNV must return high before the minimum conversion time elapses and then held high for the maximum conversion time to avoid the generation of the busy signal indicator. When the conversion is complete, the AD7981 enters the acquisition phase and powers down.

When CNV goes low, the MSB is output onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that it has an acceptable hold time. After the 16th SCK falling edge or when CNV goes high, whichever is earlier, SDO returns to high impedance.

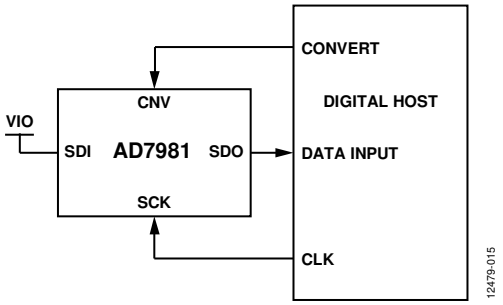


Figure 41. 3-Wire $\overline{CS}$ Mode Without Busy Indicator Connection Diagram (SDI High)

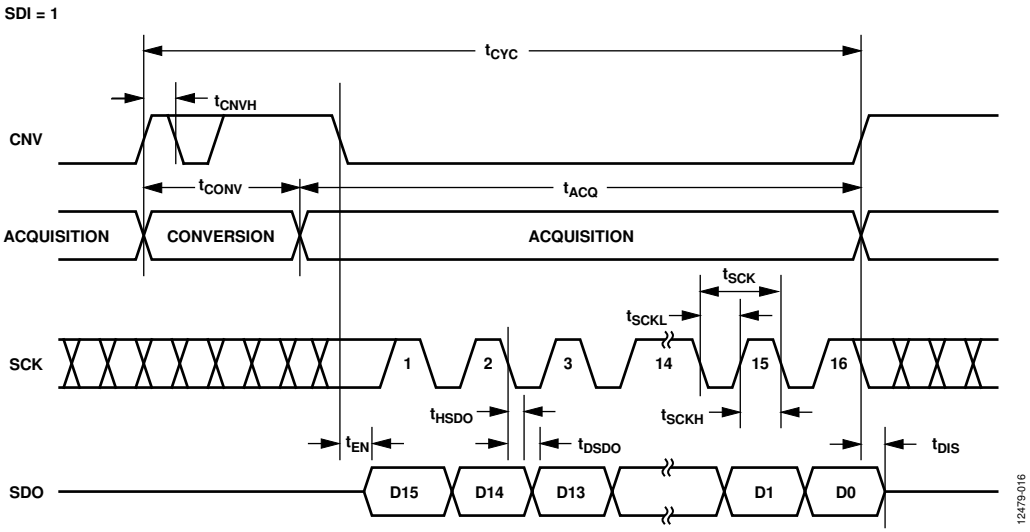


Figure 42. 3-Wire $\overline{CS}$ Mode Without Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 3-WIRE WITH A BUSY INDICATOR

The 3-wire $\overline{CS}$ mode with a busy indicator is typically used when a single AD7981 is connected to an SPI-compatible digital host having an interrupt input. The connection diagram is shown in Figure 44, and the corresponding timing is given in Figure 45.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion, irrespective of the state of CNV. Prior to the minimum conversion time, CNV can be used to select other SPI devices, such as analog multiplexers, but CNV must be returned low before the minimum conversion time elapses and then held low for the maximum conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDO goes from high impedance to low. With a pull-up resistor on the SDO line, use this transition as an interrupt signal to initiate the data reading controlled by the digital host. The AD7981 then enters the acquisition phase and powers down. The data bits are clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge captures the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 17th SCK falling edge or when CNV goes high, whichever is earlier, SDO returns to high impedance.

If multiple AD7981 devices are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Keep this contention as short as possible to limit extra power dissipation.

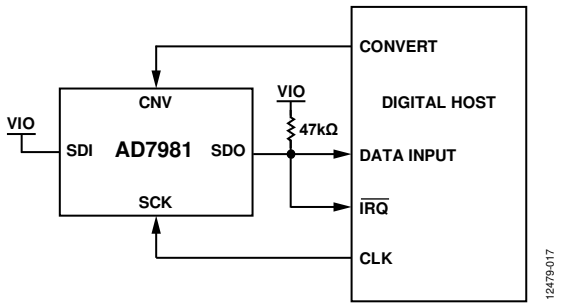


Figure 43. 3-Wire $\overline{CS}$ Mode with Busy Indicator Connection Diagram (SDI High)

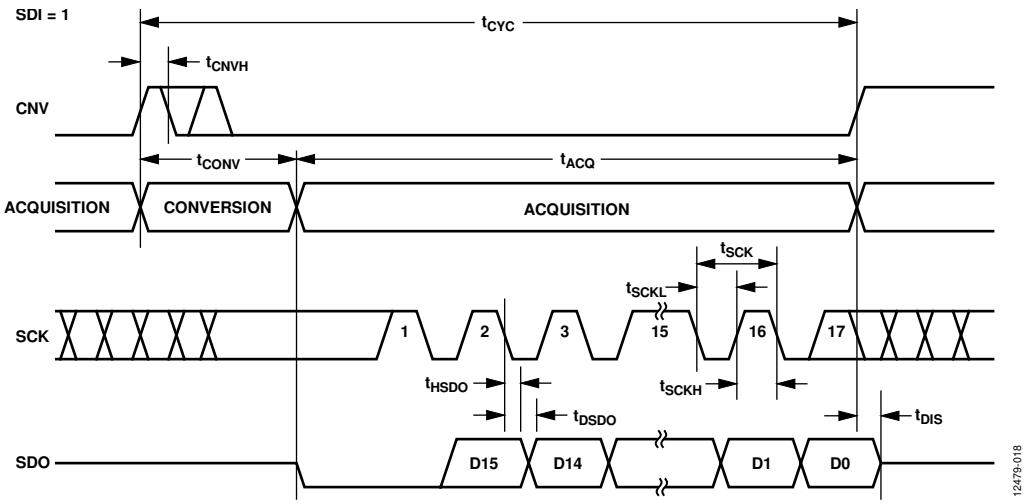


Figure 44. 3-Wire $\overline{CS}$ Mode with Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 4-WIRE WITHOUT A BUSY INDICATOR

The 4-wire $\overline{CS}$ mode without a busy indicator is typically used when multiple AD7981 devices are connected to an SPI-compatible digital host. A connection diagram example using two AD7981 devices is shown in Figure 46, and the corresponding timing is given in Figure 47.

With SDI high, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned high before the minimum conversion time elapses and then held high for the maximum conversion time to avoid the generation of the busy signal indicator.

When the conversion is complete, the AD7981 enters the acquisition phase and powers down. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge captures the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge or when SDI goes high, whichever is earlier, SDO returns to high impedance, and another AD7981 can be read.

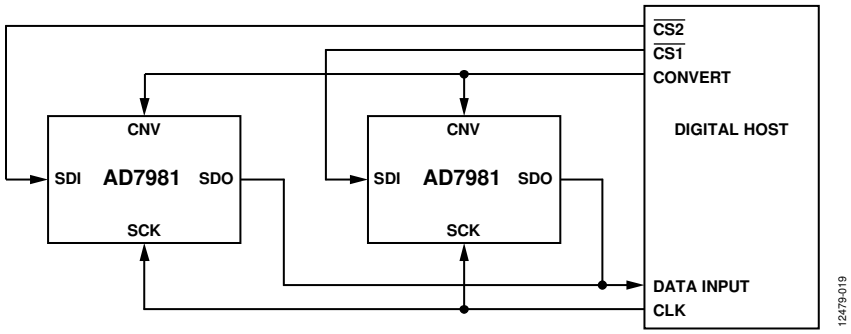


Figure 45. 4-Wire $\overline{CS}$ Mode Without Busy Indicator Connection Diagram

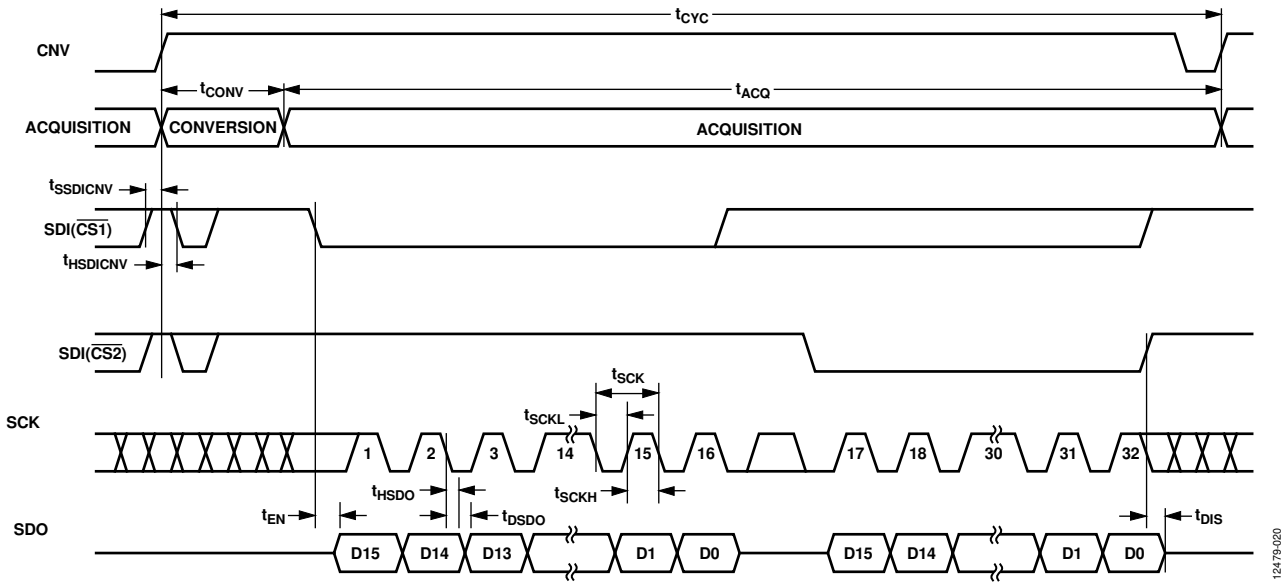


Figure 46. 4-Wire $\overline{CS}$ Mode Without Busy Indicator Serial Interface Timing

$\overline{CS}$ MODE, 4-WIRE WITH A BUSY INDICATOR

The 4-wire $\overline{CS}$ mode with a busy indicator is typically used when a single AD7981 is connected to an SPI-compatible digital host that has an interrupt input, and it is desired to keep CNV, which is used to sample the analog input, independent of the signal used to select the data reading. This requirement is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in Figure 48, and the corresponding timing is given in Figure 49.

With SDI high, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time elapses and then held low for the maximum conversion time to guarantee the generation of the busy signal indicator. When the conversion is complete, SDO goes from high impedance to low.

With a pull-up resistor on the SDO line, use this transition as an interrupt signal to initiate the data readback controlled by the digital host. The AD7981 then enters the acquisition phase and powers down. The data bits are clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge captures the data, a digital host using the SCK falling edge allows a faster reading rate provided it has an acceptable hold time. After the optional 17th SCK falling edge or SDI going high, whichever is earlier, the SDO returns to high impedance.

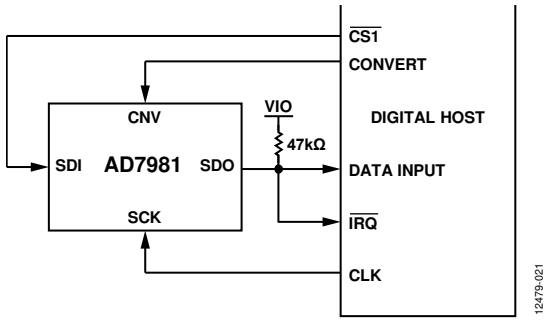


Figure 47. 4-Wire $\overline{CS}$ Mode with Busy Indicator Connection Diagram

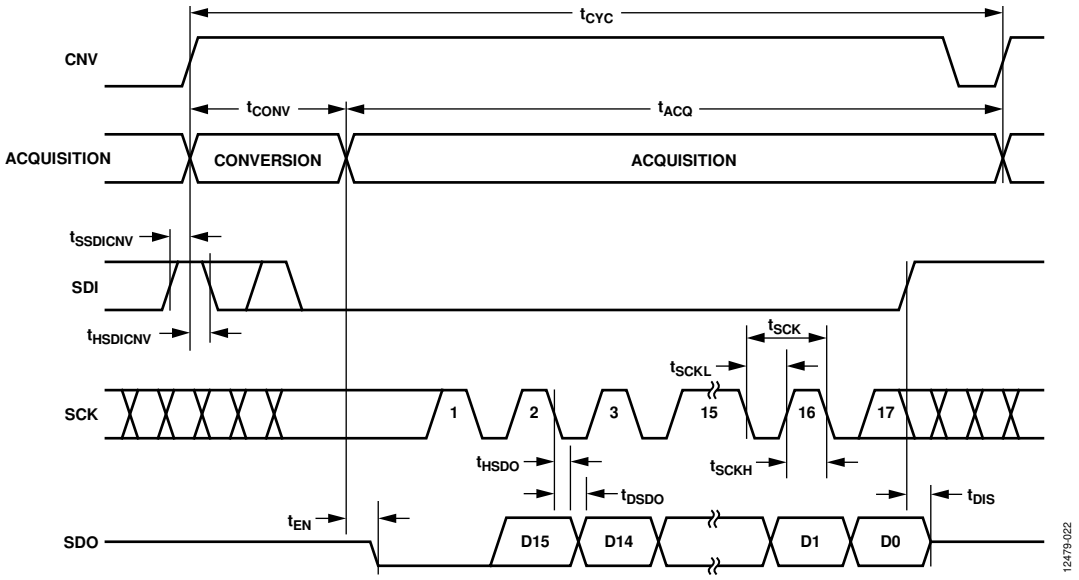


Figure 48. 4-Wire $\overline{CS}$ Mode with Busy Indicator Serial Interface Timing

CHAIN MODE WITHOUT A BUSY INDICATOR

Use chain mode without a busy indicator to daisy-chain multiple AD7981 devices on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD7981 devices is shown in Figure 50, and the corresponding timing is given in Figure 51.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects chain mode, and disables the busy indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO, and the AD7981 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N clocks are required to read back the N ADCs. The data is valid on both SCK edges. Although the rising edge captures the data, a digital host using the SCK falling edge allows a faster reading rate and, consequently, more AD7981 devices in the chain, provided the digital host has an acceptable hold time. The total readback time allows a reduction in the maximum conversation rate.

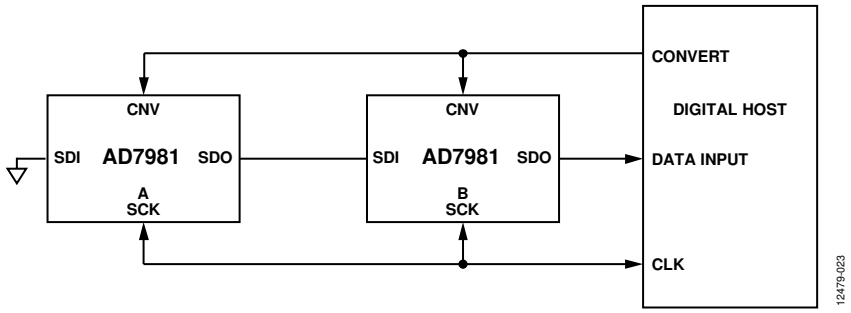


Figure 49. Chain Mode Without Busy Indicator Connection Diagram

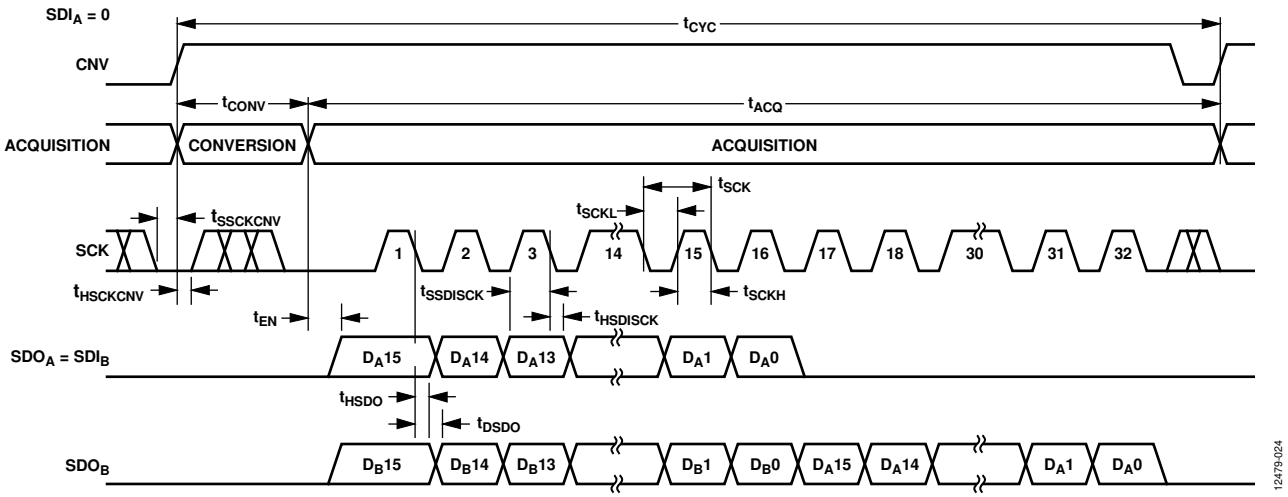


Figure 50. Chain Mode Without Busy Indicator Serial Interface Timing

CHAIN MODE WITH A BUSY INDICATOR

Chain mode with a busy indicator can also be used to daisy-chain multiple AD7981 devices on a 3-wire serial interface while providing a busy indicator. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using three AD7981 devices is shown in Figure 52, and the corresponding timing is given in Figure 53.

When SDI and CNV are low, SDO is driven low. With SCK high, a rising edge on CNV initiates a conversion, selects chain mode, and enables the busy indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, the SDO pin of the ADC closest to the digital host (see the AD7981 ADC labeled C in Figure 52) is driven high. This transition on SDO can be used as a busy indicator to trigger the data readback controlled by the digital host. The AD7981 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N + 1 clocks are required to read back the N ADCs. Although the rising edge captures the data, a digital host using the SCK falling edge allows a faster reading rate and, consequently, more AD7981 devices in the chain, provided the digital host has an acceptable hold time.

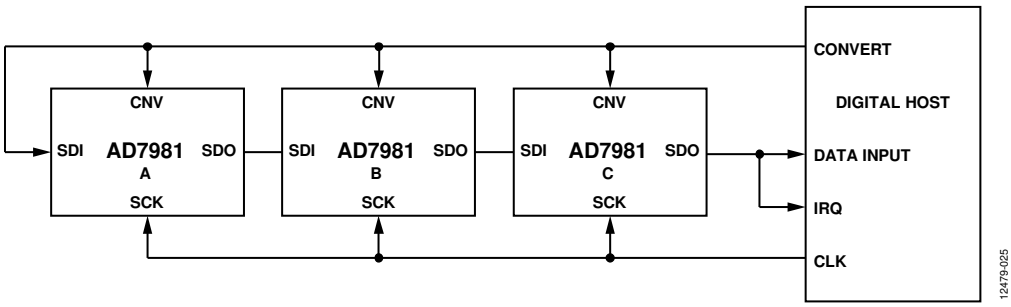


Figure 51. Chain Mode with Busy Indicator Connection Diagram

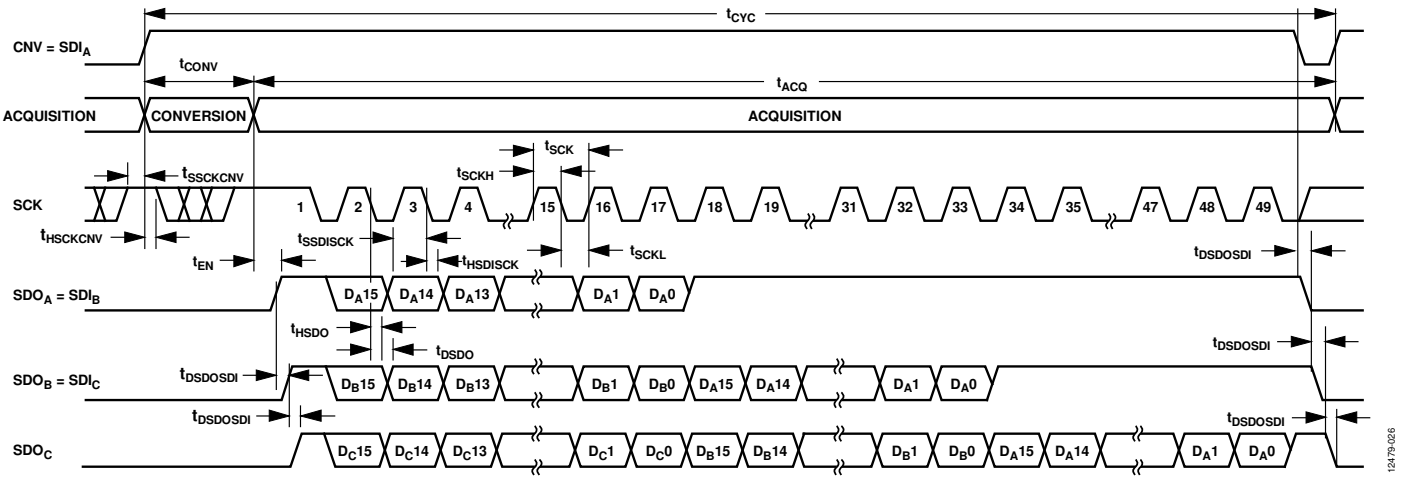


Figure 52. Chain Mode with Busy Indicator Serial Interface Timing

APPLICATIONS INFORMATION

A growing number of industries demand low power electronics that can operate reliably at temperatures of 175°C and higher. The AD7981 enables precision analog signal processing from the sensor to the processor at high temperatures for these types of applications.

Figure 54 shows the simplified signal chain of the data acquisition instrument.

In downhole drilling, avionics, and other extreme temperature environment applications, signals from various sensors are sampled to collect information about the surrounding geologic formations. These sensors take the form of electrodes, coils, piezoelectric, or other transducers. Accelerometers and gyroscopes provide information about the inclination, vibration, and rotation rate. Some of these sensors are very low bandwidth, whereas others have information in the audio frequency range and higher. The AD7981 is ideal for sampling data from sensors with varying bandwidth requirements while maintaining power efficiency and accuracy. The small footprint of the AD7981 makes it easy to include multiple channels even in space constrained layouts, such as the very narrow board widths prevalent in downhole tools. In addition, the flexible digital interface allows simultaneous sampling in more demanding applications, while also allowing simple daisy-chained readback for low pin count systems.

For a complete selection of available high temperature products, see the high temperature product list and qualification data available at www.analog.com/hightemp.

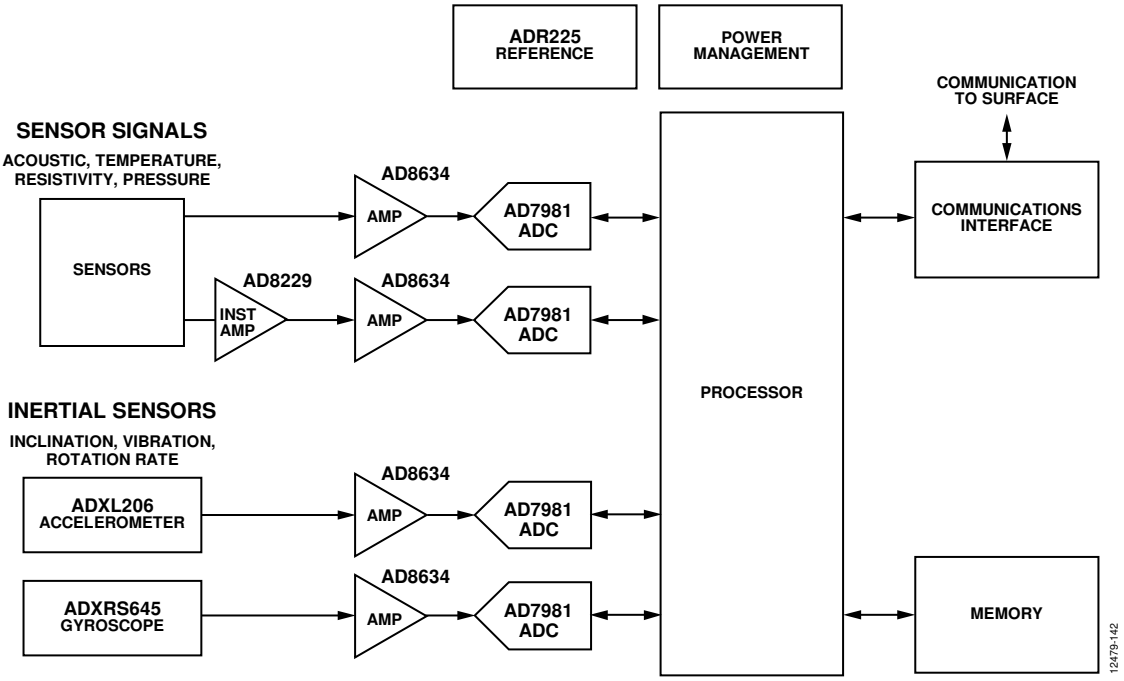


Figure 53. Simplified Data Acquisition System Signal Chain

PCB LAYOUT

Design the PCB that houses the AD7981 so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7981, with all of its analog signals on the left side and all of its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7981 is used as a shield. Fast switching signals, such as CNV or clocks, must never run near analog signal paths. Avoid crossover of digital and analog signals.

Use at least one ground plane. The ground plane can be common or split between the digital and analog section. If the ground plane is split, join the planes underneath the AD7981.

The AD7981 voltage reference input, REF, has a dynamic input impedance and must be decoupled with minimal parasitic inductances. The reference decoupling ceramic capacitor must be placed close to, ideally right up against, the REF and GND pins and connecting them with wide, low impedance traces.

Decouple the AD7981 power supplies, VDD and VIO, with ceramic capacitors, typically 100 nF, placed close to the AD7981 and connected using short and wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

An example of a layout following these rules is shown in Figure 55 and Figure 56.

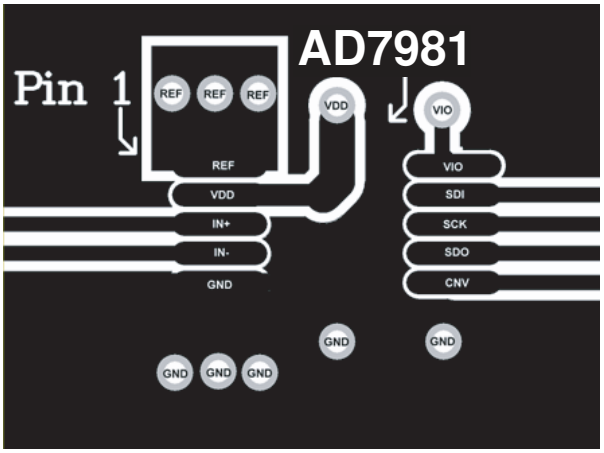


Figure 54. Example PCB Layout of the AD7981 (Top Layer)

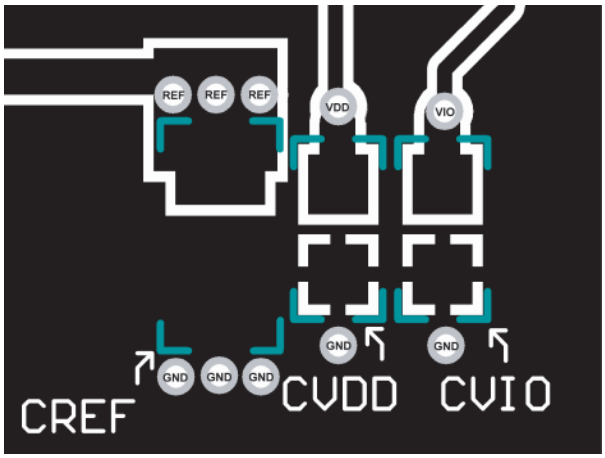


Figure 55. Example PCB Layout of the AD7981 (Bottom Layer)

OUTLINE DIMENSIONS

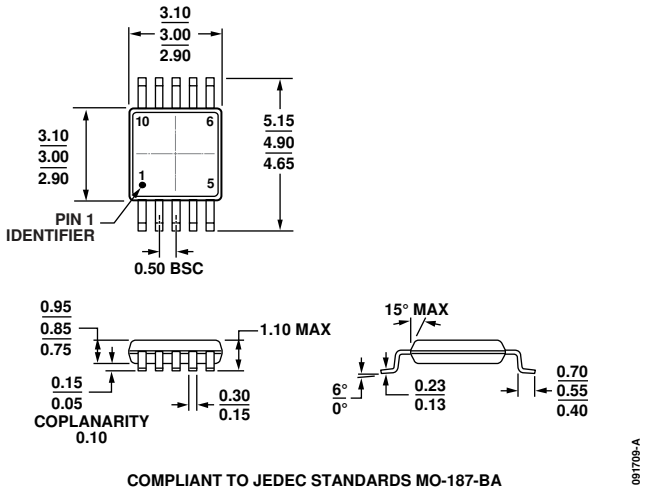


Figure 56. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

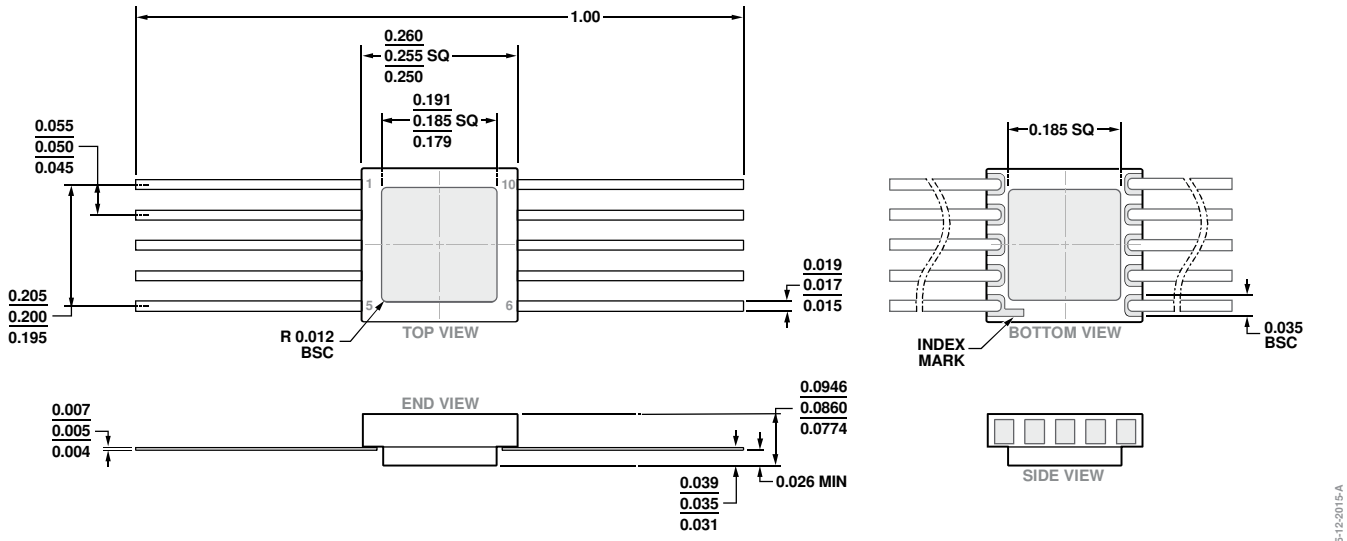


Figure 57. 10-Lead Ceramic Flat Package [FLATPACK]
(F-10-2)
Dimensions shown in inches

ORDERING GUIDE

Model[1]	Integral Nonlinearity (INL)	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
AD7981HRMZ	±2.0 LSB	−55°C to +175°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	C7C	50
AD7981HFZ	±2.5 LSB	−55°C to +210°C	10-Lead Ceramic Flat Package [FLATPACK]	F-10-2		

[1] Z = RoHS Compliant Part.