

This IC incorporates a general purpose analog circuit in a small package. This is a CMOS type operational amplifier with phase compensation circuit, which operates at a low voltage and low current consumption.

The S-19610AB is a dual operational amplifier (2 circuits).

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.

■ Features

- Low input offset voltage: $V_{IO} = +6.0 \text{ mV max. (Ta = -40°C to +125°C)}$
- Operation power supply voltage range: $V_{DD} = 2.70 \text{ V to } 5.50 \text{ V}$
- Low current consumption (Per circuit): $I_{DD} = 1.00 \text{ mA typ.}$
- Internal phase compensation: No external parts required
- Operation temperature range: $Ta = -40°C \text{ to } +125°C$
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified**1

*1. Contact our sales office for details.

■ Applications

- Current sensing
- Signal amplification
- Buffer
- Active filter

■ Package

- TMSOP-8

■ **Block Diagram**

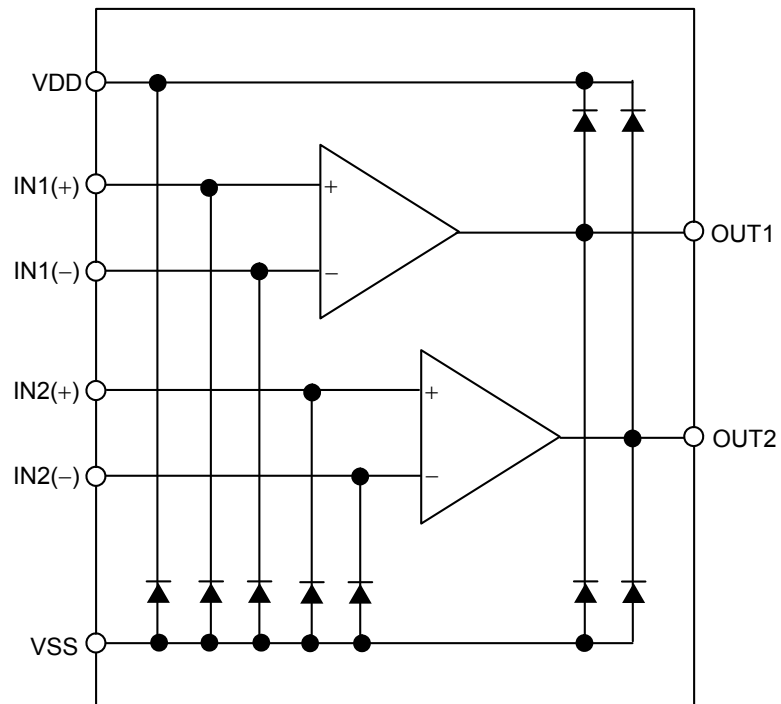


Figure 1

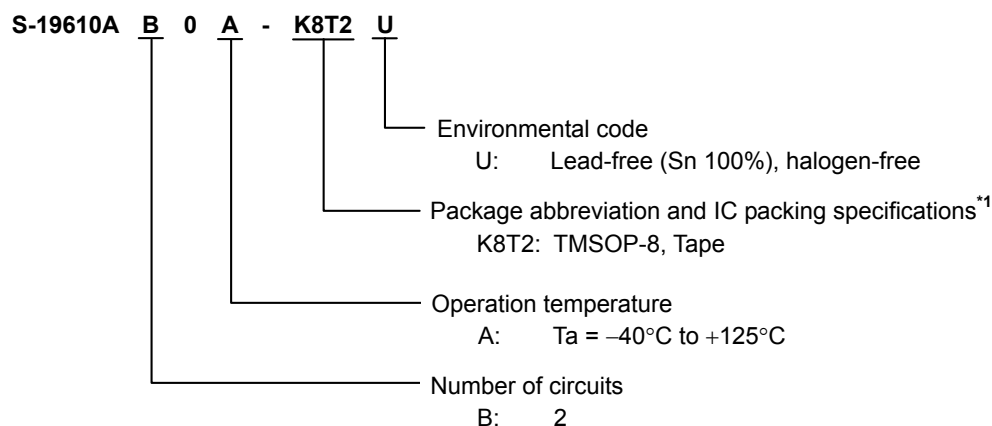
■ **AEC-Q100 Qualified**

This IC supports AEC-Q100 for the operation temperature grade 1.
 Contact our sales office for details of AEC-Q100 reliability specification.

■ **Product Name Structure**

Refer to "1. Product name" regarding the contents of product name, "2. Package" regarding the package drawings and "3. Product name list" regarding the product type.

1. Product name



*1. Refer to the tape drawing.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

3. Product name list

Table 2

Product Name	Package
S-19610AB0A-K8T2U	TMSOP-8

■ **Pin Configuration**

1. **TMSOP-8**

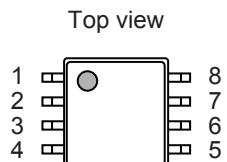


Figure 2

Table 3

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(-)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(-)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

■ Absolute Maximum Ratings

Table 4

(Ta = -40°C to +125°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V _{DD}	V _{SS} - 0.3 to V _{SS} + 7.0	V
Input voltage	V _{IN(+)} , V _{IN(-)}	V _{SS} - 0.3 to V _{SS} + 7.0	V
Output voltage	V _{OUT}	V _{SS} - 0.3 to V _{DD} + 0.3	V
Differential input voltage	V _{IND}	±7.0	V
Output pin current	I _{SOURCE}	20.0	mA
	I _{SINK}	20.0	mA
Operation ambient temperature	T _{opr}	-40 to +125	°C
Storage temperature	T _{stg}	-55 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Junction-to-ambient thermal resistance*1	θ _{JA}	TMSOP-8	Board A	-	160	-	°C/W
			Board B	-	133	-	°C/W
			Board C	-	-	-	°C/W
			Board D	-	-	-	°C/W
			Board E	-	-	-	°C/W

*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ Power Dissipation" and "Test Board" for details.

■ **Electrical Characteristics**

1. **Recommended operation condition**

Table 6

(Ta = -40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation power supply voltage range	V _{DD}	-	2.70	5.00	5.50	V	-

2. **V_{DD} = 5.0 V**

Table 7

(Ta = -40°C to +125°C unless otherwise specified)

DC Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (2 circuits)	I _{DD}	V _{CMR} = V _{OUT} = $\frac{V_{DD}}{2}$, Ta = +25°C	-	2.00	2.50	mA	5
Input offset voltage	V _{IO}	V _{CMR} = $\frac{V_{DD}}{2}$	-6.0	±3.0	+6.0	mV	1
Input offset voltage drift	$\frac{\Delta V_{IO}}{\Delta Ta}$	V _{CMR} = $\frac{V_{DD}}{2}$	-	±3	-	μV/°C	1
Input bias current	I _{BIAS}	Ta = +25°C	-	1	-	pA	-
Input offset current	I _{IO}	Ta = +25°C	-	1	-	pA	-
Common-mode input voltage range	V _{CMR}	Ta = +25°C	-0.1	-	3.8	V	2
Voltage gain (open loop)	A _{VOL}	V _{OUT} = V _{SS} + 0.5 V to V _{DD} - 0.5 V, V _{CMR} = $\frac{V_{DD}}{2}$, R _L = 1.0 MΩ, Ta = +25°C	88	110	-	dB	8
Maximum output swing voltage	V _{OH}	R _L = 1.0 MΩ	4.9	-	-	V	3
	V _{OL}	R _L = 1.0 MΩ	-	-	0.1	V	4
Common-mode input signal rejection ratio	CMRR	V _{CMR} = V _{SS} - 0.1 V to V _{DD} - 1.2 V, Ta = +25°C	70	85	-	dB	2
Power supply voltage rejection ratio	PSRR	2.70 V ≤ V _{DD} ≤ 5.50 V, Ta = +25°C	70	90	-	dB	1
Source current	I _{SOURCE}	V _{OUT} = V _{DD} - 0.12 V, Ta = +25°C	5.0	-	-	mA	6
Sink current	I _{SINK}	V _{OUT} = 0.12 V, Ta = +25°C	5.0	-	-	mA	7

Table 8

(Ta = -40°C to +125°C unless otherwise specified)

AC Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Slew rate	SR	R _L = 1.0 MΩ, C _L = 15 pF (Refer to Figure 11)	-	2.00	-	V/μs
Gain-bandwidth product	GBP	C _L = 0 pF	-	3.00	-	MHz

■ Test Circuits (Per Circuit)

1. Power supply voltage rejection ratio, input offset voltage

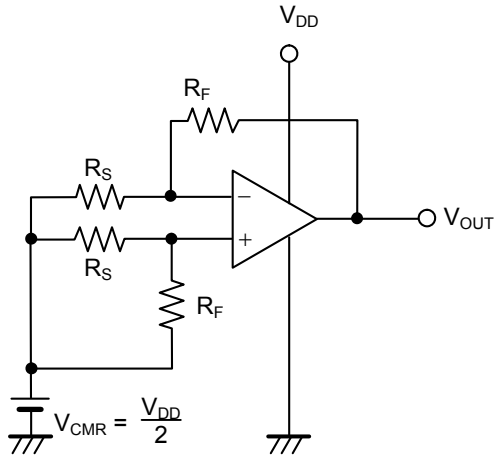


Figure 3 Test Circuit 1

• Power supply voltage rejection ratio (PSRR)

The power supply voltage rejection ratio (PSRR) can be calculated by the following expression, with V_{OUT} measured at each V_{DD} .

Test conditions:

$$V_{DD} = 2.70 \text{ V: } V_{DD} = V_{DD1}, V_{OUT} = V_{OUT1}$$

$$V_{DD} = 5.50 \text{ V: } V_{DD} = V_{DD2}, V_{OUT} = V_{OUT2}$$

$$PSRR = 20 \log \left(\left| \frac{V_{DD1} - V_{DD2}}{\left(V_{OUT1} - \frac{V_{DD1}}{2} \right) - \left(V_{OUT2} - \frac{V_{DD2}}{2} \right)} \right| \times \frac{R_F + R_S}{R_S} \right)$$

• Input offset voltage (V_{IO})

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_F + R_S}$$

2. Common-mode input signal rejection ratio, common-mode input voltage range

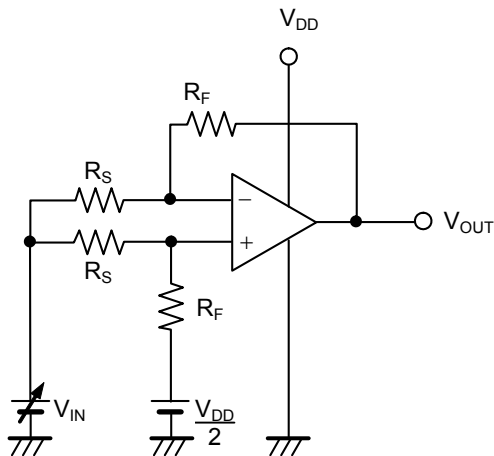


Figure 4 Test Circuit 2

• Common-mode input signal rejection ratio (CMRR)

The common-mode input signal rejection ratio (CMRR) can be calculated by the following expression, with V_{OUT} measured at each V_{IN} .

Test conditions:

$$V_{IN} = V_{CMR \text{ Max.}}: V_{IN} = V_{IN1}, V_{OUT} = V_{OUT1}$$

$$V_{IN} = V_{CMR \text{ Min.}}: V_{IN} = V_{IN2}, V_{OUT} = V_{OUT2}$$

$$CMRR = 20 \log \left(\left| \frac{V_{IN1} - V_{IN2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

• Common-mode input voltage range (V_{CMR})

The common-mode input voltage range is the range of V_{IN} in which V_{OUT} satisfies the common-mode input signal rejection ratio specifications when V_{IN} is changed.

3. Maximum output swing voltage (V_{OH})

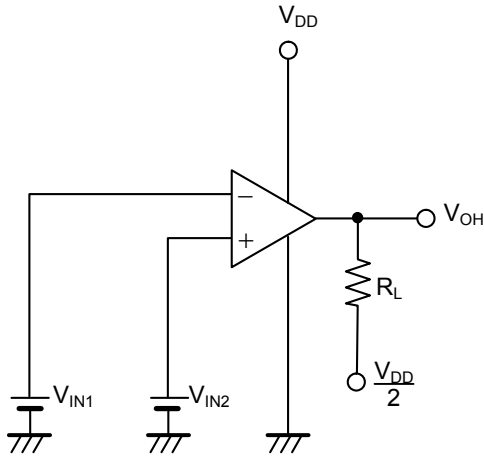


Figure 5 Test Circuit 3

• **Maximum output swing voltage (V_{OH})**

Test conditions

$$V_{IN1} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$

$$R_L = 1 \text{ M}\Omega$$

4. Maximum output swing voltage (V_{OL})

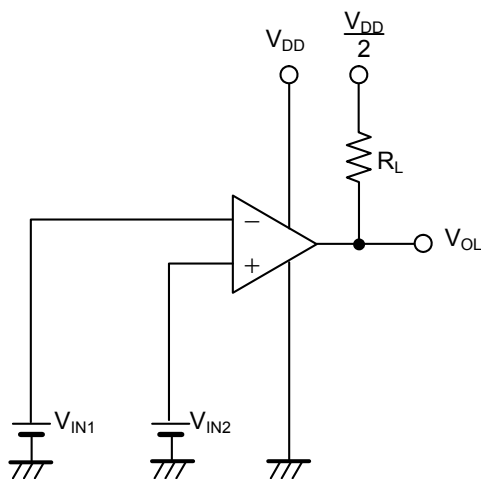


Figure 6 Test Circuit 4

• **Maximum output swing voltage (V_{OL})**

Test conditions:

$$V_{IN1} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$

$$R_L = 1 \text{ M}\Omega$$

5. Current consumption

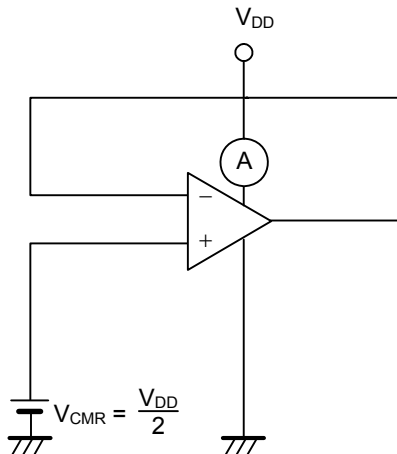


Figure 7 Test Circuit 5

• **Current consumption (I_{DD})**

6. Source current

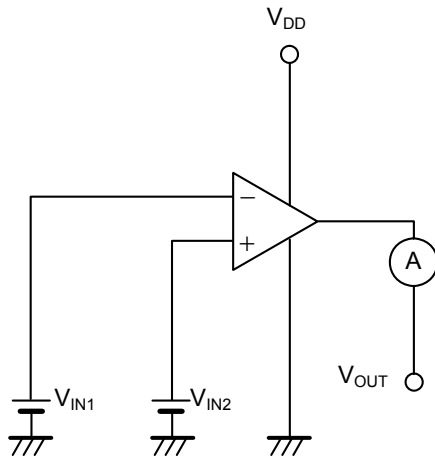


Figure 8 Test Circuit 6

• Source current (I_{SOURCE})

Test conditions:

$$V_{OUT} = V_{DD} - 0.12 \text{ V}$$

$$V_{IN1} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$

7. Sink current

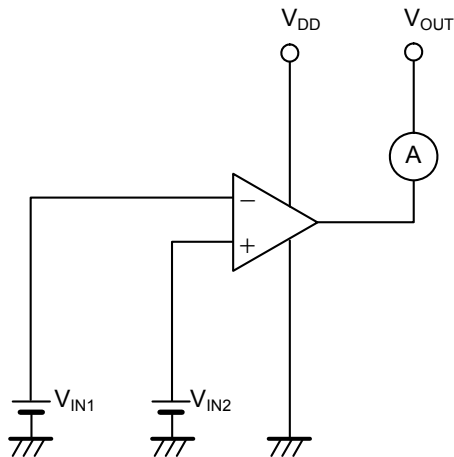


Figure 9 Test Circuit 7

• Sink current (I_{SINK})

Test conditions:

$$V_{OUT} = V_{SS} + 0.12 \text{ V}$$

$$V_{IN1} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$

8. Voltage gain

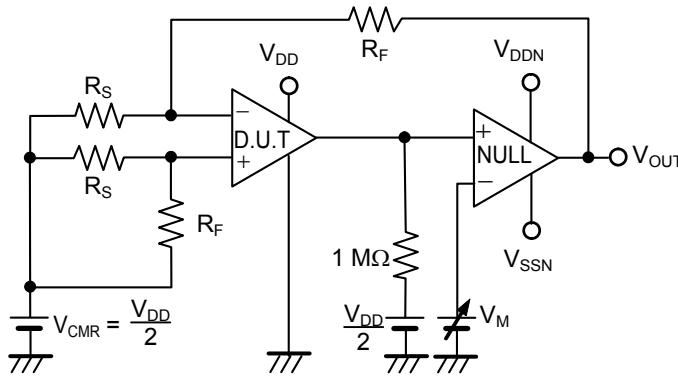


Figure 10 Test Circuit 8

• Voltage gain (open loop) (A_{VOL})

The voltage gain (A_{VOL}) can be calculated by the following expression, with V_{OUT} measured at each V_M .

Test conditions:

$$V_M = V_{DD} - 0.5 \text{ V}: V_M = V_{M1}, V_{OUT} = V_{OUT1}$$

$$V_M = 0.5 \text{ V}: V_M = V_{M2}, V_{OUT} = V_{OUT2}$$

$$A_{VOL} = 20 \log \left(\left| \frac{V_{M1} - V_{M2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

9. Slew rate (SR)

Measured by the voltage follower circuit.

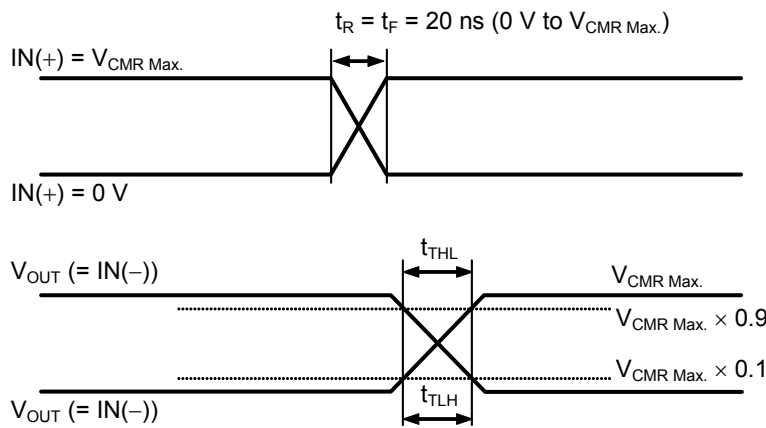


Figure 11

• Slew rate (SR)

$$SR = \frac{V_{CM \text{ Max.}} \times 0.8}{t_{TLH}}$$

$$SR = \frac{V_{CM \text{ Max.}} \times 0.8}{t_{THL}}$$

■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.
- Use this IC with the output current of 20 mA or less.
- This IC operates stably even directly connecting a load capacitance of 100 pF or less to the output pin, as shown in **Figure 12**. When connecting a load capacitance of 100 pF or more, connect a resistor of 47 Ω or more as shown in **Figure 13**. In case of connecting a filter for noise prevention, and connecting a load capacitance of 100 pF or more, also connect a resistor of 47 Ω or more as shown in **Figure 14**.

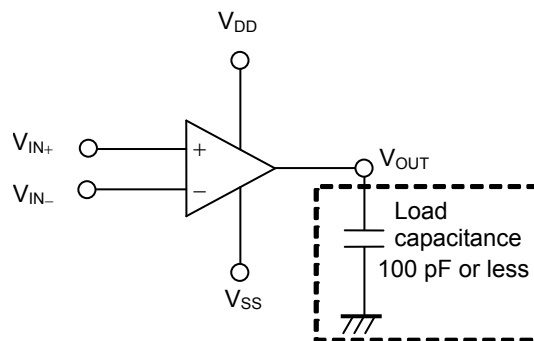


Figure 12

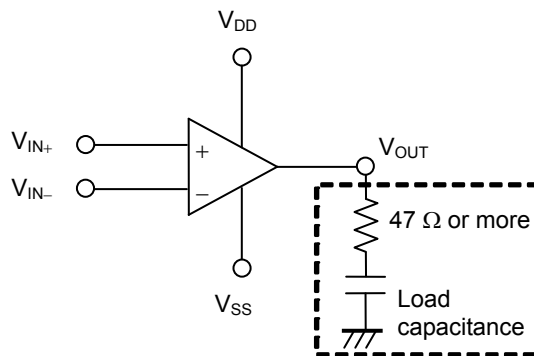


Figure 13

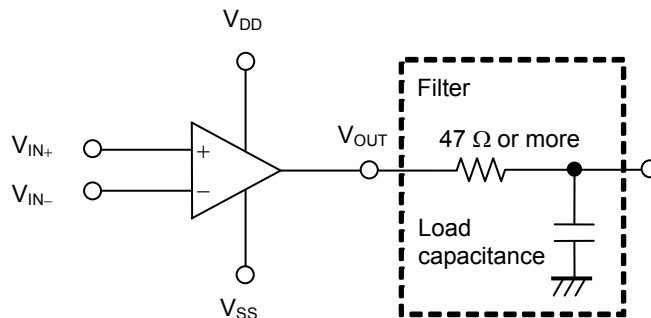
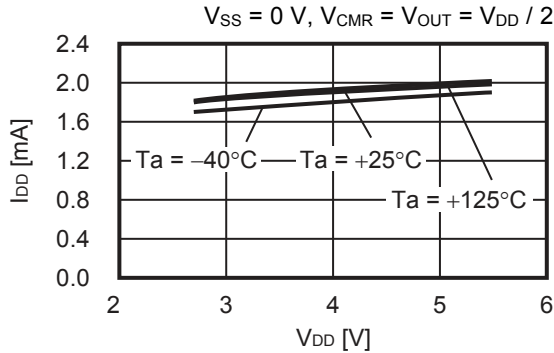


Figure 14

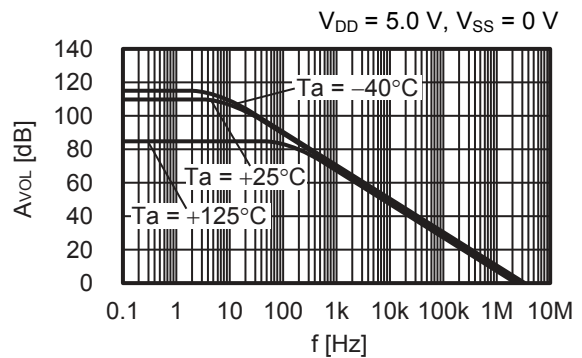
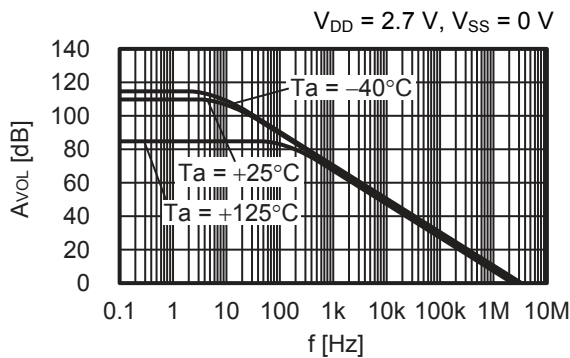
Caution The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ **Characteristics (Typical Data)**

1. Current consumption (I_{DD}) (2 circuits) vs. Power supply voltage (V_{DD})

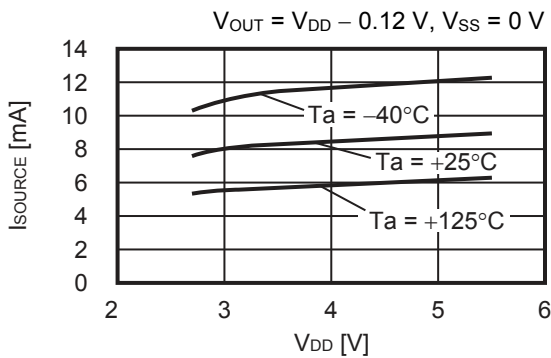


2. Voltage gain (A_{VOL}) vs. Frequency (f)

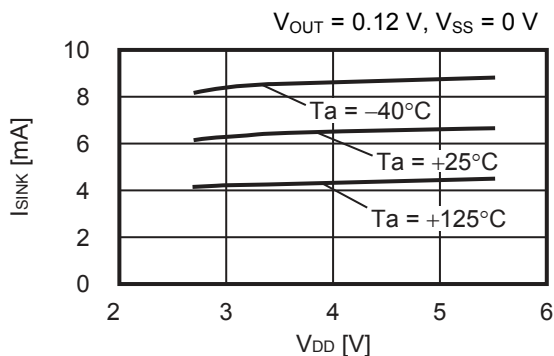


3. Output current

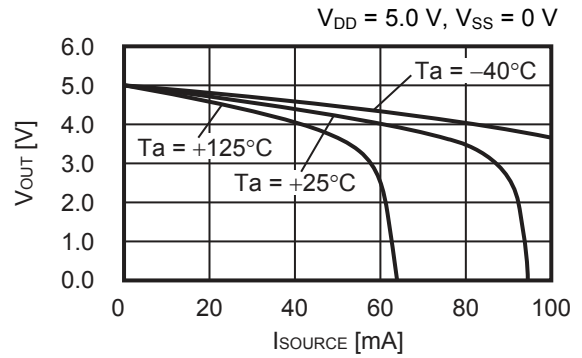
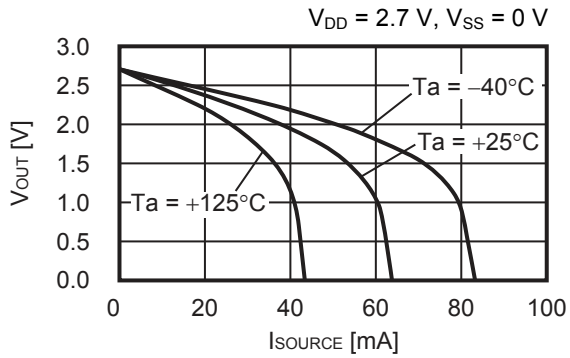
3.1 Source current (I_{SOURCE}) vs. Power supply voltage (V_{DD})



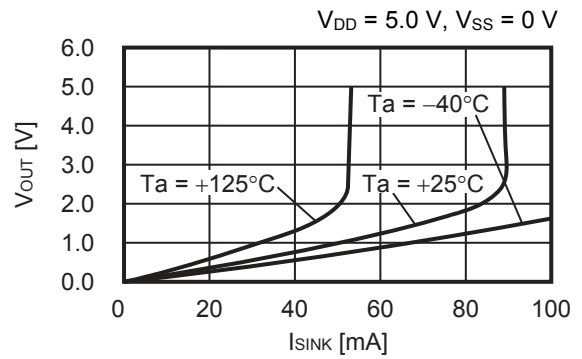
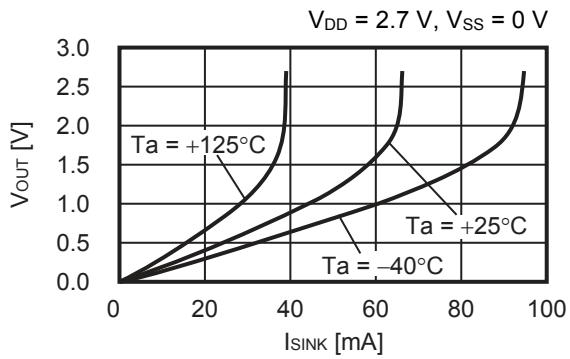
3.2 Sink current (I_{SINK}) vs. Power supply voltage (V_{DD})



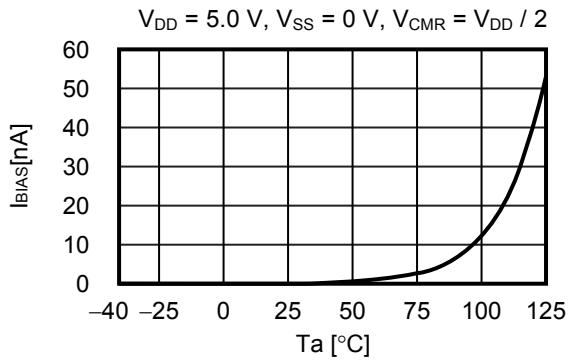
3.3 Output voltage (V_{OUT}) vs. Source current (I_{SOURCE})



3.4 Output voltage (V_{OUT}) vs. Sink current (I_{SINK})

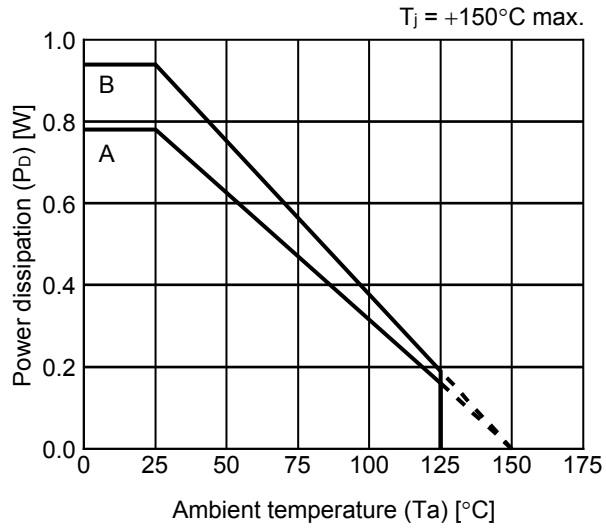


4. Input bias current (I_{BIAS}) vs. Temperature (T_a)



■ **Power Dissipation**

TMSOP-8

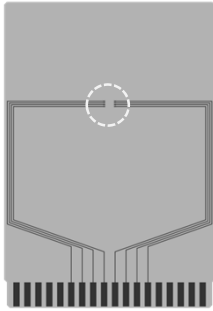


Board	Power Dissipation (P_D)
A	0.78 W
B	0.94 W
C	–
D	–
E	–

TMSOP-8 Test Board

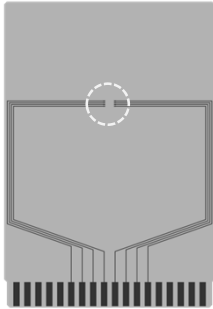
(1) Board A

 IC Mount Area



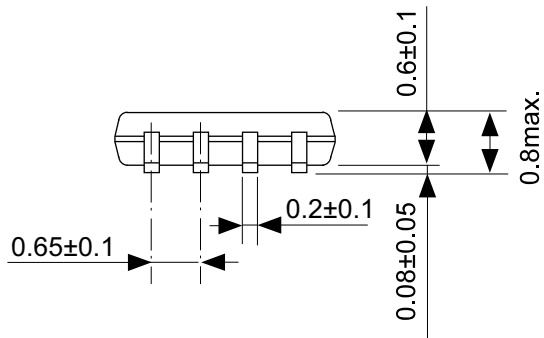
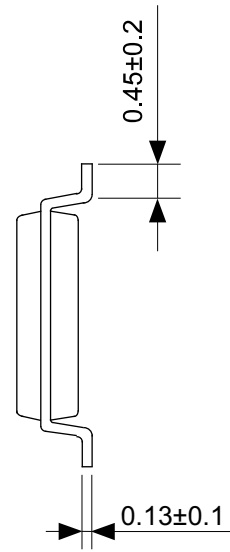
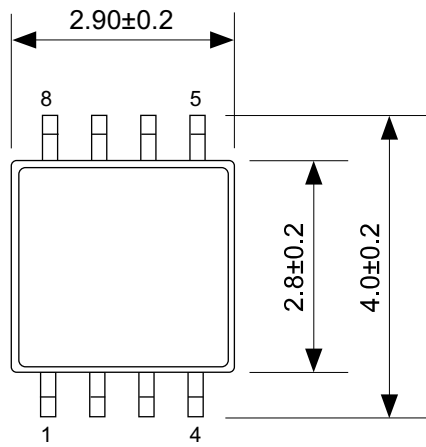
Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	2	
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via	-	

(2) Board B



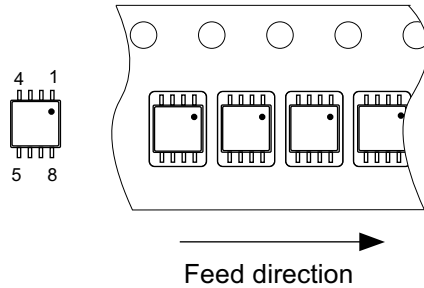
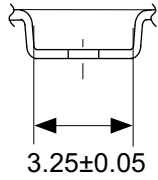
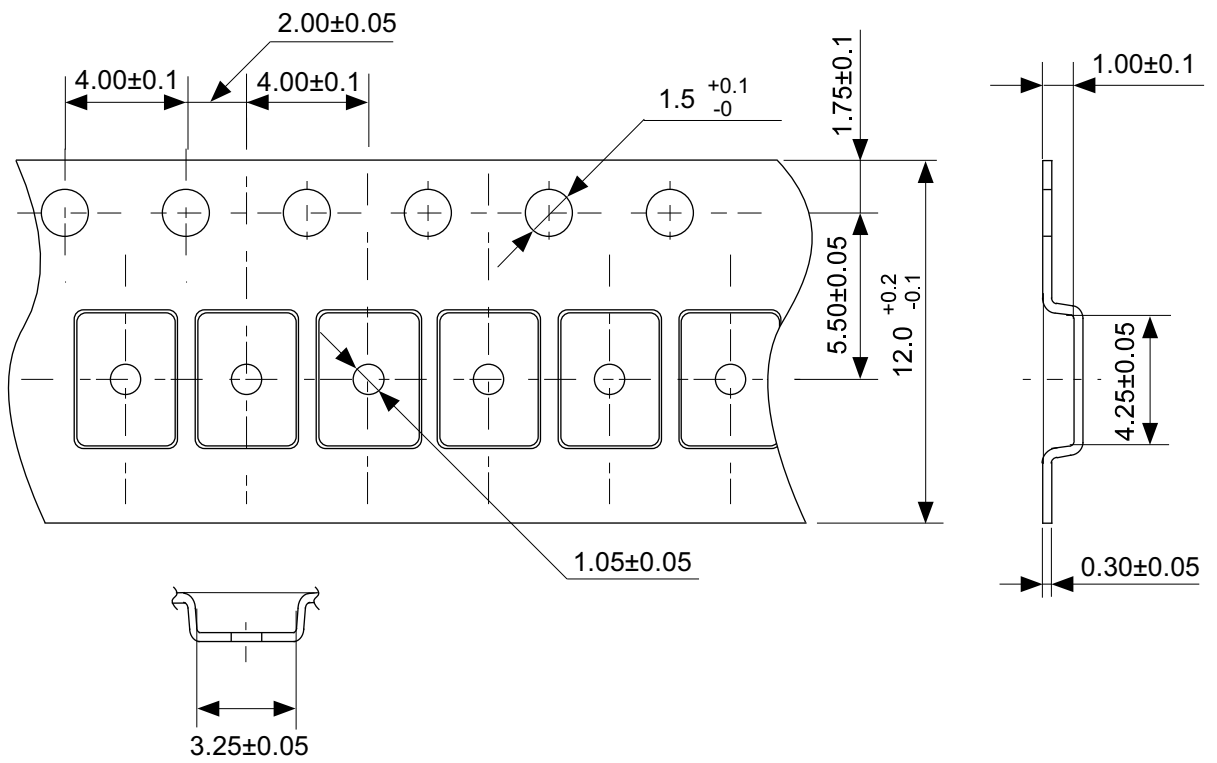
Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	4	
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via	-	

No. TMSOP8-A-Board-SD-1.0



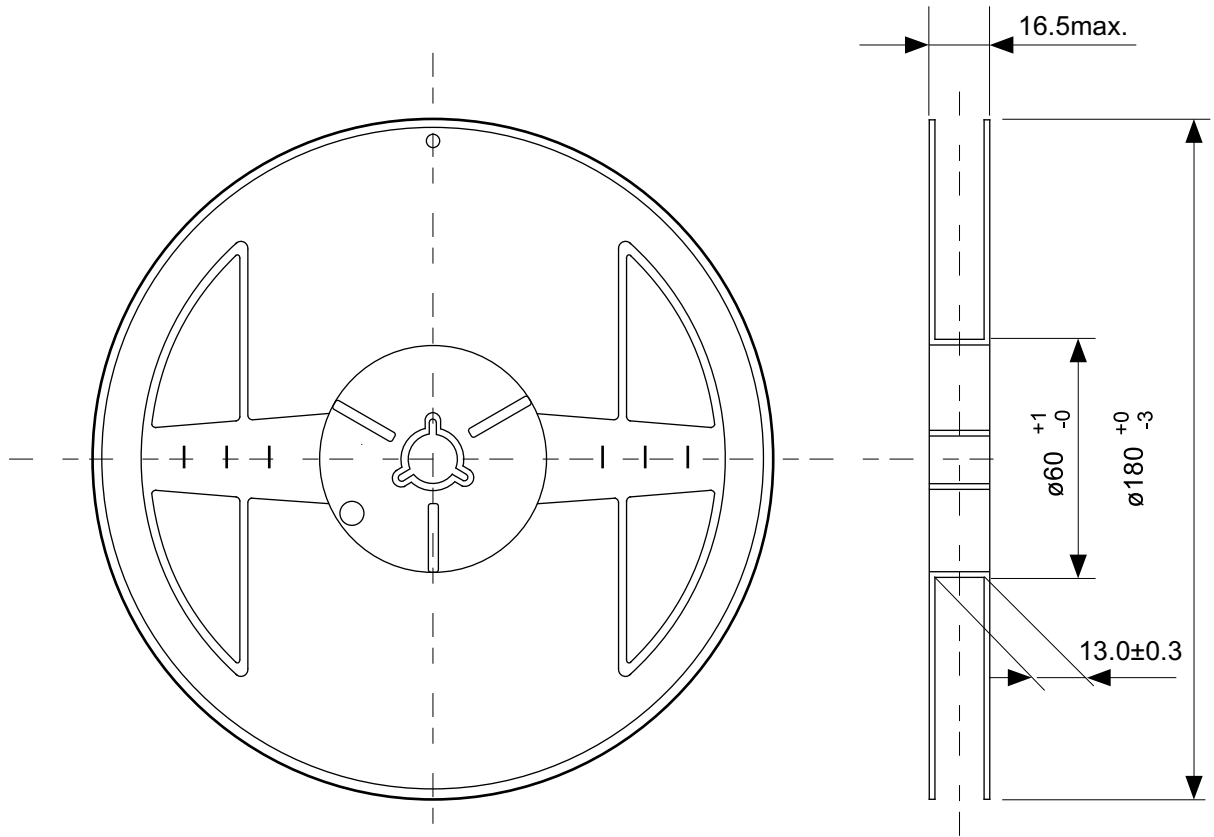
No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	

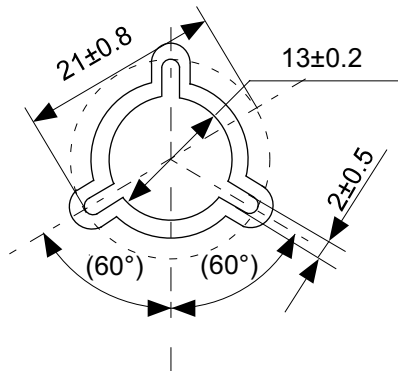


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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