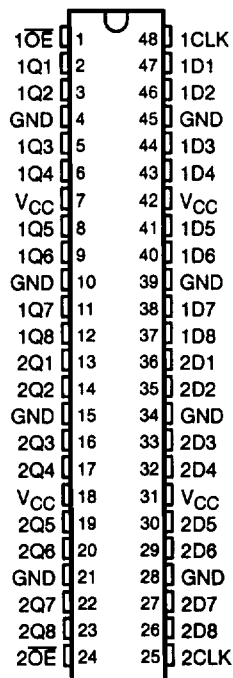


# SN54LVT16374, SN74LVT16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus™* Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16374 . . . WD PACKAGE  
SN74LVT16374 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

The 'LVT16374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN54LVT16374, SN74LVT16374

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS145E - MAY 1992 - REVISED JANUARY 1996

### description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

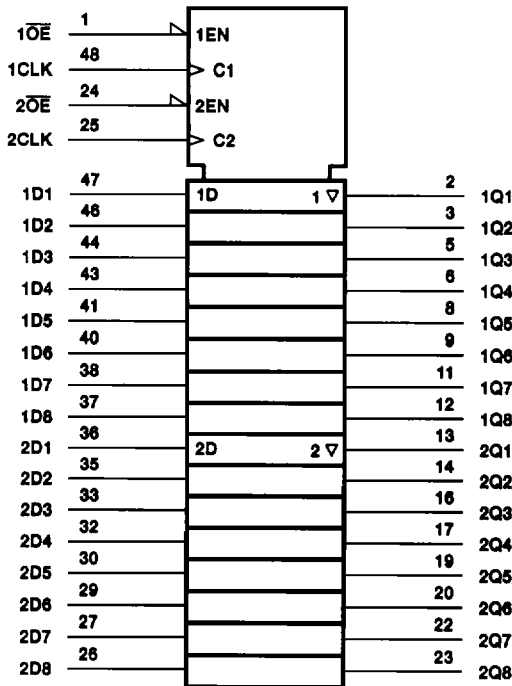
The SN74LVT16374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16374 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LVT16374 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

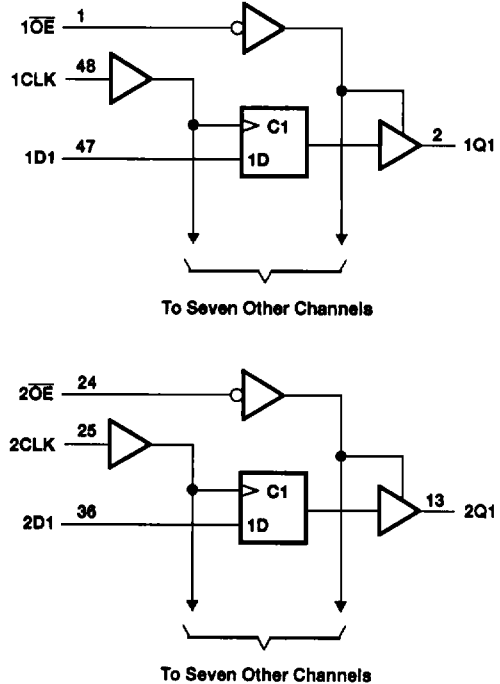
FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	$Q_0$
H	X	X	Z

### logic symbol†



### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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**SN54LVT16374, SN74LVT16374**  
**3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

SCBS145E – MAY 1992 – REVISED JANUARY 1996

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) .....	–0.5 V to 7 V
Current into any output in the low state, $I_O$ : SN54LVT16374 .....	96 mA
SN74LVT16374 .....	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVT16374 .....	48 mA
SN74LVT16374 .....	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package .....	0.85 W
DL package .....	1.2 W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

**recommended operating conditions (see Note 4)**

		SN54LVT16374		SN74LVT16374		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage	0.8		0.8		V
$V_I$	Input voltage	5.5		5.5		V
$I_{OH}$	High-level output current	–24		–32		mA
$I_{OL}$	Low-level output current	48		64		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	10		10		ns/V
	Outputs enabled	10		10		
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



**SN54LVT16374, SN74LVT16374**  
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SCBS145E - MAY 1992 - REVISED JANUARY 1998

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54LVT16374		SN74LVT16374		UNIT	
		MIN	TYP†	MAX	MIN		TYP†
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2	V
$V_{OH}$	$V_{CC} = \text{MIN to MAX}^\ddagger$ , $I_{OH} = -100\ \mu\text{A}$	$V_{CC} - 0.2$		$V_{CC} - 0.2$		V	
	$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$	2.4		2.4			
	$V_{CC} = 3\text{ V}$	2		2			
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\ \mu\text{A}$		0.2		0.2	V
		$I_{OL} = 24\text{ mA}$		0.5		0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$		0.4		0.4	
		$I_{OL} = 32\text{ mA}$		0.5		0.5	
		$I_{OL} = 48\text{ mA}$		0.55		0.55	
		$I_{OL} = 64\text{ mA}$				0.55	
$I_I$	$V_{CC} = 0\text{ or MAX}^\ddagger$ , $V_I = 5.5\text{ V}$			10		10	$\mu\text{A}$
	Control inputs $V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 1$		$\pm 1$	
	Data inputs $V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$		1		1	
		$V_I = 0$		-5		-5	
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$			$\pm 100$		$\pm 100$	$\mu\text{A}$
$I_I(\text{hold})$	Data inputs $V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$		75		75	$\mu\text{A}$
		$V_I = 2\text{ V}$		-75		-75	
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 2.7\text{ V}$			5		5	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$			-5		-5	$\mu\text{A}$
$I_{CC}$	Outputs high	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$	$I_O = 0$			0.1	mA
	Outputs low					5	
	Outputs disabled					0.1	
$\Delta I_{CC}^\S$	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$			0.2		0.2	mA
$C_i$	$V_I = 3\text{ V or }0$			5		5	pF
$C_o$	$V_O = 3\text{ V or }0$			9.5		9.5	pF

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		SN54LVT16374				SN74LVT16374				UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3 \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	0	150	0	150	0	150	0	150	MHz
$t_w$	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
$t_{su}$	Setup time, data before CLK↑		High or low	2.8	3.3	2.2	2.6			ns
$t_h$	Hold time, data after CLK↑		High or low	0.6	0.5	0.6	0			ns



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**SN54LVT16374, SN74LVT16374**  
**3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

SCBS145E - MAY 1992 - REVISED JANUARY 1996

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16374				SN74LVT16374				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYPT†	MAX	MIN		MAX
$f_{max}$			150		150		150			150		MHz
$t_{PLH}$	CLK	Q	1.9	6.6	7.4		1.9	3.6	6.3	7		ns
$t_{PHL}$			2.3	6.9	7.5		2.3	4.1	6.6	7.2		
$t_{PZH}$	$\overline{OE}$	Q	1	5.6	6.4		1	2.7	5.3	6.3		ns
$t_{PZL}$			1.3	5.3	6		1.3	2.8	5.1	5.9		
$t_{PHZ}$	$\overline{OE}$	Q	1	7.2	8.2		2.7	4.3	6.8	7.6		ns
$t_{PLZ}$			2.6	6.1	8.2		2.6	3.9	5.8	5.9		

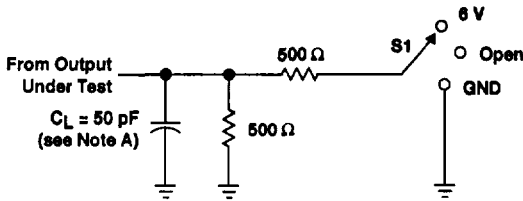
† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .



**SN54LVT16374, SN74LVT16374**  
**3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

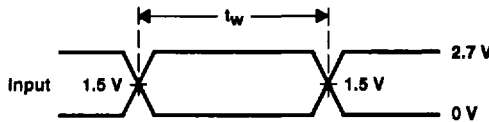
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**PARAMETER MEASUREMENT INFORMATION**

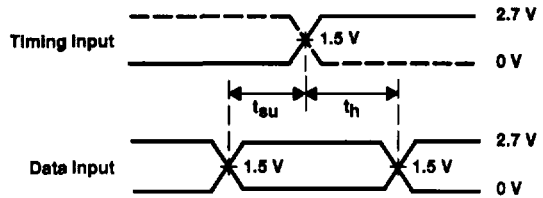


**LOAD CIRCUIT FOR OUTPUTS**

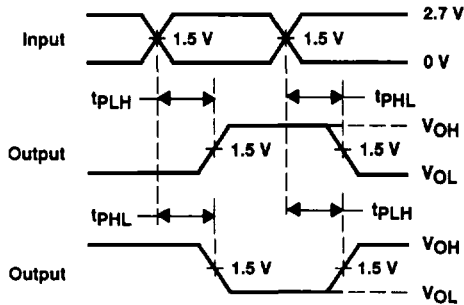
TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	6 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND



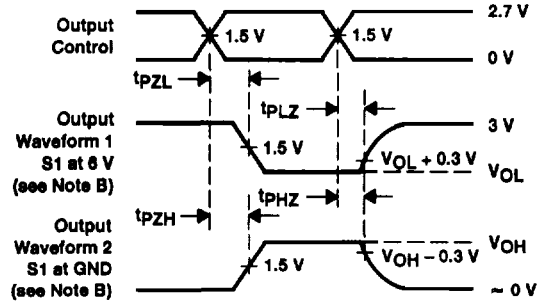
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

