

User Manual

ITA-2230 Series

**Fanless Embedded
Core i Dual Core Rackmount IPC**

ADVANTECH

Enabling an Intelligent Planet

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While unpacking ITA-2230, please ensure that the following items are included in your shipment:

- 1 x ITA-2230 series IPC
- 1 x ITA-2230 accessory box
- 1 x Warranty card

If any of these items are missing or damaged, contact your distributor or sales representative immediately. All ITA-2230 devices are mechanically and electrically inspected before shipment. Thus, your product should be free of marks and scratches and in perfect working order upon receipt. While unpacking ITA-2230, check the product for signs of shipping damage (for example, a damaged box, scratches, dents, etc.). If the device is damaged or fails to meet the specifications, notify our service department or your local sales representative immediately. Please also notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After this inspection, we will make arrangements to repair or replace the unit.

Warnings, Cautions, and Notes

Warning! Warnings indicate conditions, which if not observed, can cause personal injury!



Caution! Cautions are included to help you avoid damaging hardware or losing data. e.g.



There is a danger of a new battery exploding if it is incorrectly installed. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

Note! Notes provide optional additional information.



Safety Instructions

1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
5. Keep this equipment away from humidity.
6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
7. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
8. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
9. All cautions and warnings on the equipment should be noted.
10. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
11. Never pour any liquid into an opening. This may cause fire or electrical shock.
12. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
13. If one of the following situations arises, get the equipment checked by service personnel:
 - The power cord or plug is damaged.
 - Liquid has penetrated into the equipment.
 - The equipment has been exposed to moisture.
 - The equipment does not work well, or you cannot get it to work according to the user's manual.
 - The equipment has been dropped and damaged.
 - The equipment has obvious signs of breakage.
14. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -25° C (-13° F) OR ABOVE 60° C (140° F). THIS COULD DAMAGE THE EQUIPMENT.
15. This equipment has been tested and found to comply with the requirements for a Class A digital device. Operation of this equipment in a residential area is likely to cause harmful interference to radio communications; in such events, users are required to correct this interference.
16. This equipment is sold without a power cord. Users are advised to purchase a CCC-certified power cord.

CAUTION: THE COMPUTER IS PROVIDED WITH A BATTERY-POWERED REAL-TIME CLOCK CIRCUIT. THERE IS A DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

CAUTION

DOUBLE POLE / NEUTRAL FUSING

The fuses must be replaced by service person. Service person shall fully disconnect the power before servicing to avoid the risk of electric shock.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.
- Always disconnect the power cord from the chassis when making adjustments. Do not connect when the power is on. A sudden rush of power can damage sensitive electronic components. Only experienced electronics personnel should open the chassis. Always ground yourself to remove any static electric charge before touching the motherboard, backplane, or add-on cards. Modern electronic devices are very sensitive to static electric charges. Use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static- shielded bag.

Contents

Chapter 1	Overview	1
1.1	Introduction	2
1.2	Specification	2
1.3	Power Supply Information	2
	Table 1.1: Power supply:	2
1.4	Environment	3
	Table 1.2: Environment	3
1.5	Dimension	3
	Figure 1.1 ITA-2230 Dimension	3
	Figure 1.2 ITA-2230 Diagram	4
	Table 1.3: Part List	4
Chapter 2	Industrial Motherboard	5
2.1	Introduction	6
2.2	System Status LED	6
2.2.1	System View	6
	Figure 2.1 Front View	6
	Figure 2.2 Rear View	6
2.2.2	System Status LED Indicator	6
2.2.3	Network Interface LED Indicator	7
2.2.4	Serial Port Status LED Indicator	7
2.3	Jumpers and Connectors	7
2.3.1	Jumper Description	7
2.3.2	Jumper and Connector Location	8
	Figure 2.3 Jumper and Connector Location on Main Board	8
	Figure 2.4 Jumper and Connector Location on Backplane	9
	Table 2.1: Jumper	9
	Table 2.2: JCMOS1: Clear CMOS settings	9
	Table 2.3: PSON1: Start-up mode selection	10
	Table 2.4: VCCGPIO1: GPIO voltage selection	10
2.4	I/O Connector	10
	Figure 2.5 ITA-2230 Front I/O Connectors	10
	Figure 2.6 ITA-2230 Rear I/O Connectors	10
2.4.1	COM Connector	11
	Table 2.5: COM Connectors	11
2.4.2	HDMI Connector	11
	Table 2.6: VGA Connector Pin Assignment	11
2.4.3	VGA Connector	11
	Table 2.7: VGA	12
2.4.4	DIO Connector	12
	Table 2.8: DIO Connector	12
2.4.5	USB 2.0 Connector	13
	Table 2.9: USB2.0 Pin Assignment	13
2.4.6	USB 3.0 Connector	13
	Table 2.10: USB 3.0 Pin Assignment	13
2.4.7	Audio in Connector	13
2.4.8	LAN Connector	13
	Table 2.11: LAN Connector	14
2.4.9	Phoenix Terminal Connector	14
	Table 2.12: Phoenix Terminal Connector	14

Chapter 3 System Installation 15

3.1	Introduction	16
3.1.1	Installing Mainboard mini-PCIe card and mini SATA.....	16
	Figure 3.1 Installing mSATA and mini-PCIe	16
3.1.2	Installing HDD Module	16
	Figure 3.2 Installing HDD Module.....	17
3.1.3	Installing the Top Cover.....	17
	Figure 3.3 Installing the Top Cover	17
3.1.4	Installing Ears and Handles.....	18
	Figure 3.4 Installing the Foot Stand.....	18
3.1.5	Installing the ITAM Card Module	18
	Figure 3.5 Installing the ITAM Card Module	19

Chapter 4 AMI BIOS Setting 21

4.1	Introduction	22
	Figure 4.1 Setup Program Initial Screen	22
4.2	Entering Setup	22
	Figure 4.2 Press to Enter Setup Screen.....	22
4.2.1	Main Setup.....	23
	Figure 4.3 Main Setup Screen.....	23
4.2.2	Advanced BIOS Features Setup.....	23
	Figure 4.4 Advanced BIOS Features Setup Screen.....	24
	Figure 4.5 ACPI Configuration.....	24
	Figure 4.6 CPU Configuration (1).....	25
	Figure 4.7 CPU Configuration (2).....	25
4.2.3	SATA Configuration	26
	Figure 4.8 SATA Configuration.....	26
	Figure 4.9 Info Report Configuration	27
	Figure 4.10USB Configuration.....	27
	Figure 4.11LPC/ISA Configuration	28
	Figure 4.12Super I/O Configuration.....	29
	Figure 4.13H/W Monitor Configuration	30
	Figure 4.14CPU PPM Configuration.....	30
	Figure 4.15APM Configuration	31
	Figure 4.16PCIE COM Port Configuration (1)	31
	Figure 4.17PCIE COM Port Configuration (2).....	32
	Figure 4.18PCIE LAN Port Configuration (1).....	32
	Figure 4.19PCIE LAN Port Configuration (2).....	33
4.2.4	Advanced Chipset Features Setup	33
	Figure 4.20Advanced Chipset Features Setup.....	33
	Figure 4.21PCH-IO Configuration	34
	Figure 4.22Chipset USB Configuration	34
	Figure 4.23PCH Azalia Configuration.....	35
	Figure 4.24System Agent (SA) Configuration	36
	Figure 4.25Graphics Configuration Menu.....	36
	Figure 4.26LCD Control.....	37
4.2.5	Boot Setup	38
	Figure 4.27Boot Setup.....	38
	Figure 4.28Boot Option Priorities	39
	Figure 4.29CSM Parameter.....	39
4.2.6	Security Setup	40
	Figure 4.30Setup Security Menu	40
4.2.7	Save & Exit Setup.....	41
	Figure 4.31Setup Save & Exit Menu	41

Chapter 5 Driver Installation..... 43

5.1	Introduction	44
5.2	Driver Installation	44
5.2.1	Chipset Windows Driver Setup	45
5.2.2	VGA Windows Driver Setup	45
5.2.3	LAN windows Driver Setup	46
5.2.4	AUDIO windows Driver Setup.....	46

Chapter 6 **GPIO Programming Guide47**

6.1	ITA-2230 Digital DIO Definition	48
6.2	Configuration Sequence.....	48
6.3	Function call for reference.....	52

Appendix A **Programming the Watchdog Timer..57**

A.1	Programming the Watchdog Timer	58
A.1.1	Watchdog Timer Overview.....	58
A.1.2	Programming the Watchdog Timer	58
	Table A.1: Watchdog Timer Registers	58
A.1.3	Example Program	59

Chapter 1

Overview

1.1 Introduction

ITA-2230 is a 2U fanless embedded rackmount industrial computer with wide voltage input range. Based on Core™ i7 dual-core processor, it is a comprehensive monitoring and communication management system. The powerful computing platform supports 7/24 operation.

1.2 Specification

- **Chipset:** Intel Core™ i7 processor and Intel HM76 chipset
- **BIOS:** AMI SPI 64 Mb Flash
- **Memory:** On-board 4 GB DDR3 1600
- **Display:** Integrated HD4000, with shared memory up to 512 MB SDRAM
- **Display Mode:**
 - VGA display resolution: 2048 x 1536 @ 75 Hz
 - HDMI display resolution: 1920 x 1200 @ 60 Hz
- **Storage:** 1 x mSATA connector, 1 x 3.5" or 2 x 2.5" HDD socket
- **Expansion Slot:** 3 x ITAM slots, 1 x PC104 slot and 1 x Mini PCIe slot
- **Ethernet:** 2 x 10/100/1000M RJ45 Ethernet connector
- **USB:** 4 x USB 3.0, 4 x USB 2.0
- **VGA:** 1 x VGA
- **HDMI:** 1 x HDMI
- **Serial Port:** 2 x DB9 ports, supporting RS-232/422/485 conversion
- **Digital I/O:** 1 x 8-ch TTL GPIO
- **Audio:** 1 x speaker out, 2 x 4w amplifier, 1 x Mic-in
- **Reserved (optional connector on back panel):** 1 x PC1104 interface
- **ITAM I/O module (optional):**
 - ITAM-SR01-10A1E: 8 x serial RS-232/422/485
 - TAM-SR01-00A1E: 8 x serial RS-232/422/485 with 2.5KV optically-coupled isolation
 - ITAM-NC01-C0A1E: 8 x 10/100/1000M RJ45 Ethernet connector
 - ITAM-NC02-C0A1E: 4 x 10/100/1000M RJ45 Ethernet connector
 - ITAM-NC02-F0A1E: 4 x 10/100/1000M SFP connector
- **Dimension (W x H x D):** 483 x 88 x 325 mm
- **Weight:**
 - Single power supply: 7.7kg
 - Dual power supply: 8kg

1.3 Power Supply Information

ITA-2230 supports hot swap power supply module with dual or single power input.

Table 1.1: Power supply:

Direct/alternating Input voltage	110V DC/ 100-240V AC
Current input:	110 VDC --- 1.2 A 100-240 VAC --- 1.2-0.55 A
Power input interface	3P European terminal block
Dual power input	Power1 AC+ Power2 DC or Power1 AC+ Power2 AC or Power1 DC+Power2 DC

1.4 Environment

Table 1.2: Environment

Operating temperature:	With industrial HDD: 0~40°C With SSD: -25~60°C (with 0.7m/s airflow)
Storage temperature:	-40~85°C
Temperature	95% @ 40°C, non-condensing
Vibration	With 2.5-inch SSD: 2Grms @ 5~500 Hz, random, 1hr/axis
	With 2.5-inch HDD: 1Grms @ 5~500 Hz, random, 1hr/axis
	IEC60068-2-6 Sine 2G @ 5~500Hz, 1hr/axis
Shock	10G, IEC-68-2-27, half sine wave, 11ms duration
	With 2.5-inch HDD: 10G, IEC-68-2-27, half sine wave, 11ms duration
Security	CCC/CE/CB/UL compliant

1.5 Dimension

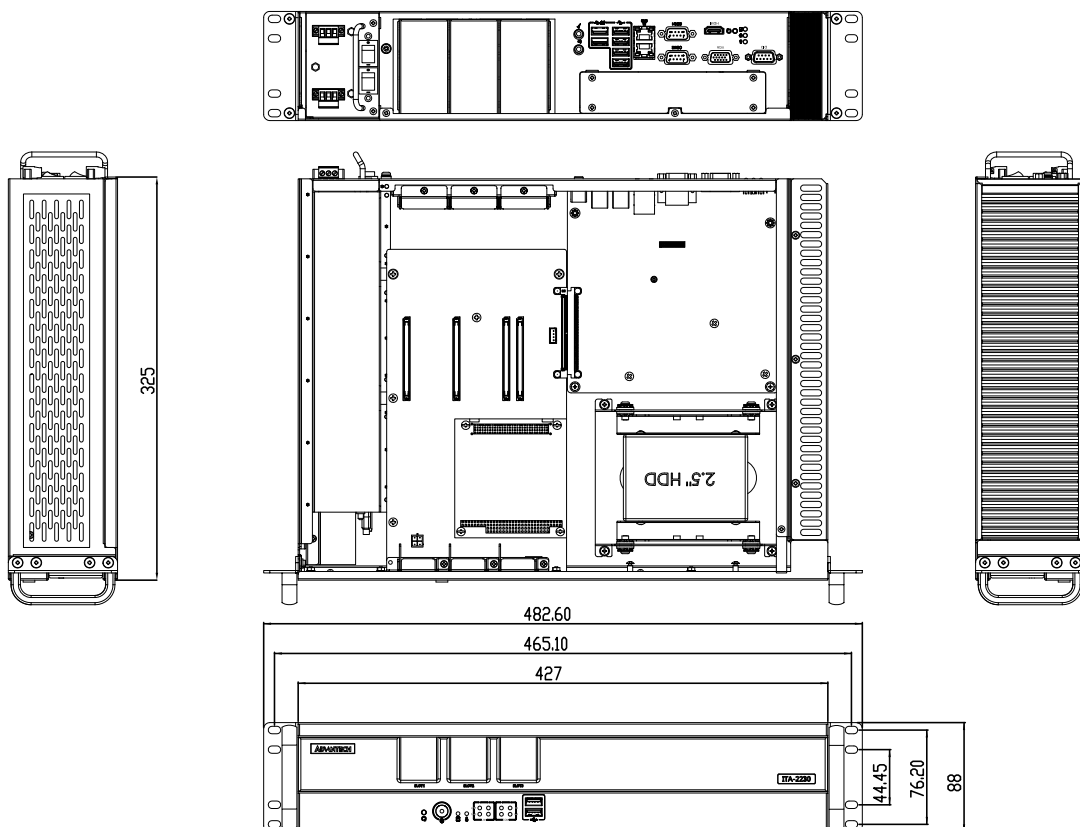


Figure 1.1 ITA-2230 Dimension

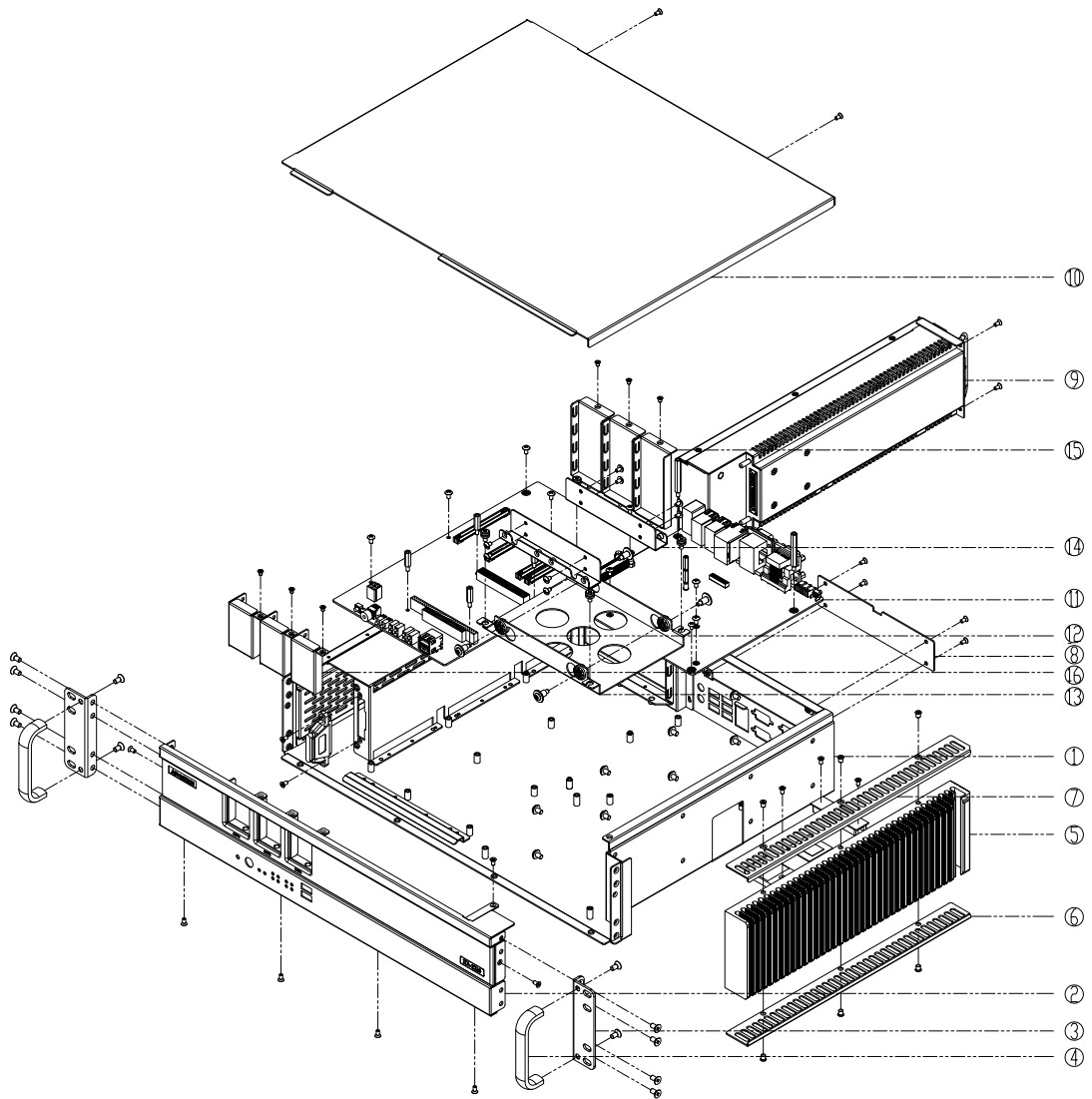


Figure 1.2 ITA-2230 Diagram

Table 1.3: Part List			
1	Base	9	Power supply module
2	Front panel	10	Top cover
3	Ear	11	Motherboard
4	Handle	12	Back plate
5	Heat sink	13	3.5 HDD bracket
6	Hand guard (top)	14	2.5 HDD adapter bracket
7	Hand guard (bottom)	15	Blank bracket (rear)
8	PC104 Blank bracket	16	Blank bracket (front)

Chapter 2

Industrial Motherboard

2.1 Introduction

This chapter introduces internal jumper settings and external pin assignment for application integration.

2.2 System Status LED

2.2.1 System View

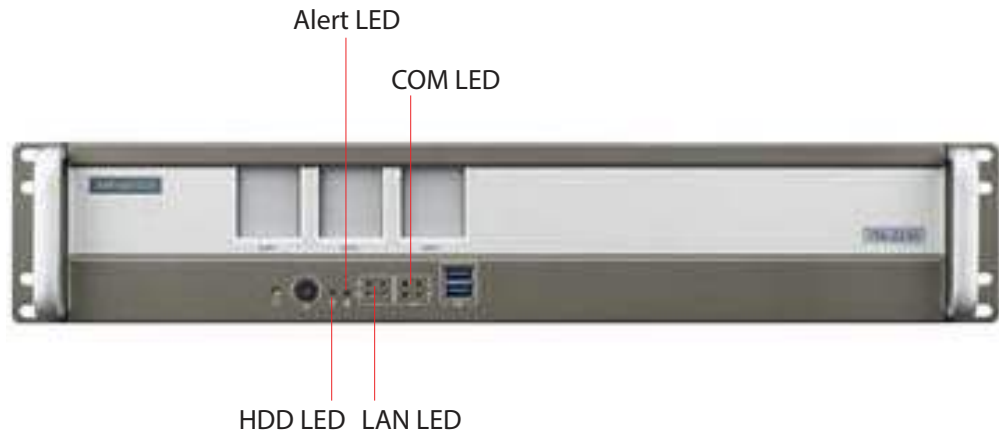


Figure 2.1 Front View



Figure 2.2 Rear View

2.2.2 System Status LED Indicator

The LED indicator at the bottom left of the front panel indicates system link/activity status.

The following table provides detailed information of LED definition.

Item	LED	Status	Color	Description
1	Power supply:	On	Green	System is powered on and safe.
		Off		System is powered off.
2	Failed	On	Red	System exception.
3	HDD LED	Flash	Orange	Receiving/transferring data.
		Off		No data is being received/transferred.

2.2.3 Network Interface LED Indicator

The following table provides detailed information of LED definition.

Item	LED	Status	Color	Description
1	1000M	On	Green	1000M Receiving/transferring network data.
	100M	On	Orange	100M Receiving/transferring network data.
	10M	Off		10M Receiving/transferring network data.
	Connected	Flash	Green	Connecting.

2.2.4 Serial Port Status LED Indicator

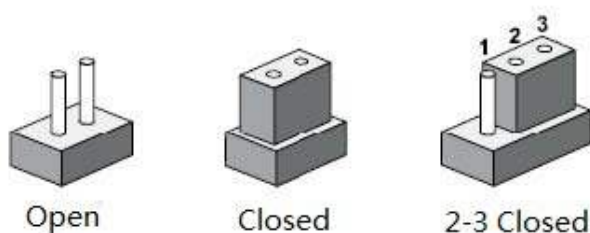
The following table provides detailed information of LED definition.

Item	LED	Status	Color	Description
1	TX Active	Flash	Green	Transferring data through the serial port.
	TX No Data	Off		No data is being transferred through the serial port.
	RX Active	Flash	Orange	Receiving data through the serial port.
	RX No Data	Off		No data is being received through the serial port.

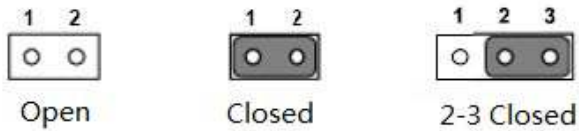
2.3 Jumpers and Connectors

2.3.1 Jumper Description

You may configure the ITA-2230 to match the needs of your application by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To close a jumper, you remove the clip. Sometime a jumper will have three pins, labelled 1, 2 and 3. In this case you would connect either pins 1 and 2, or 2 and 3.



The jumpers setting are schematically depicted in this manual as follows.



A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes. Generally, you simply need a standard cable to make most connections.

2.3.2 Jumper and Connector Location

The board has a number of connectors and jumpers that allow you to configure your system to suit your application. The table below lists the function of each of the connectors and jumpers. The locations of jumpers and connector on the board are shown in Figure 2.3 and Figure 2.4.

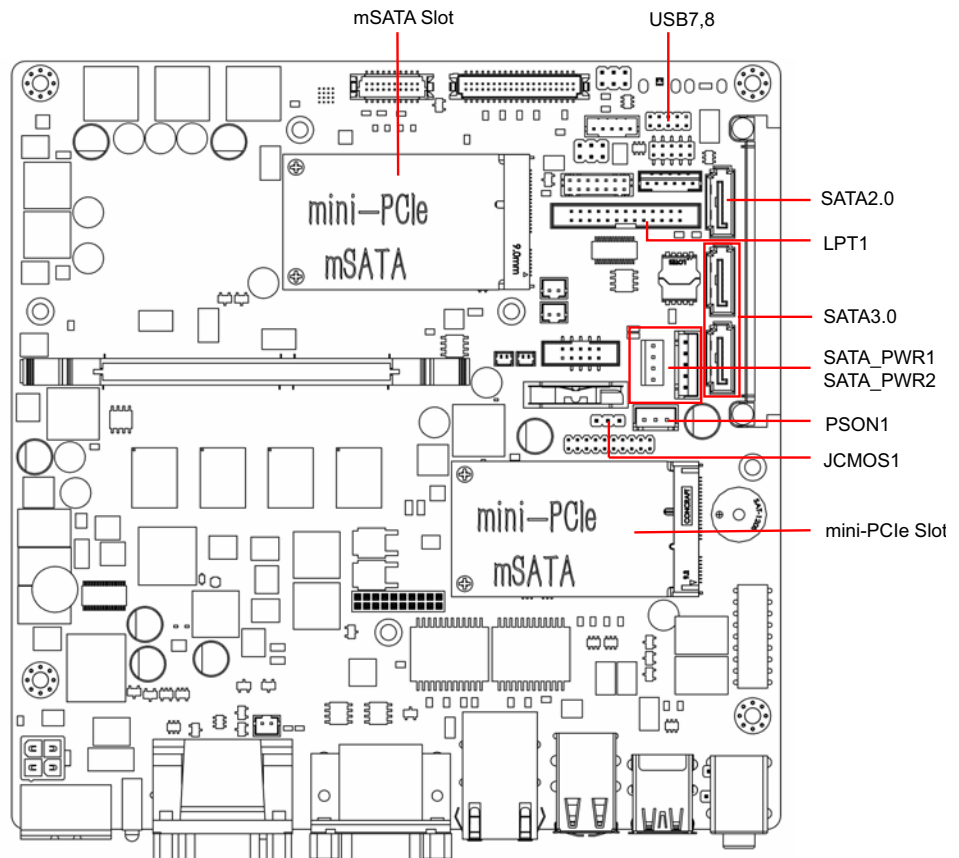


Figure 2.3 Jumper and Connector Location on Main Board

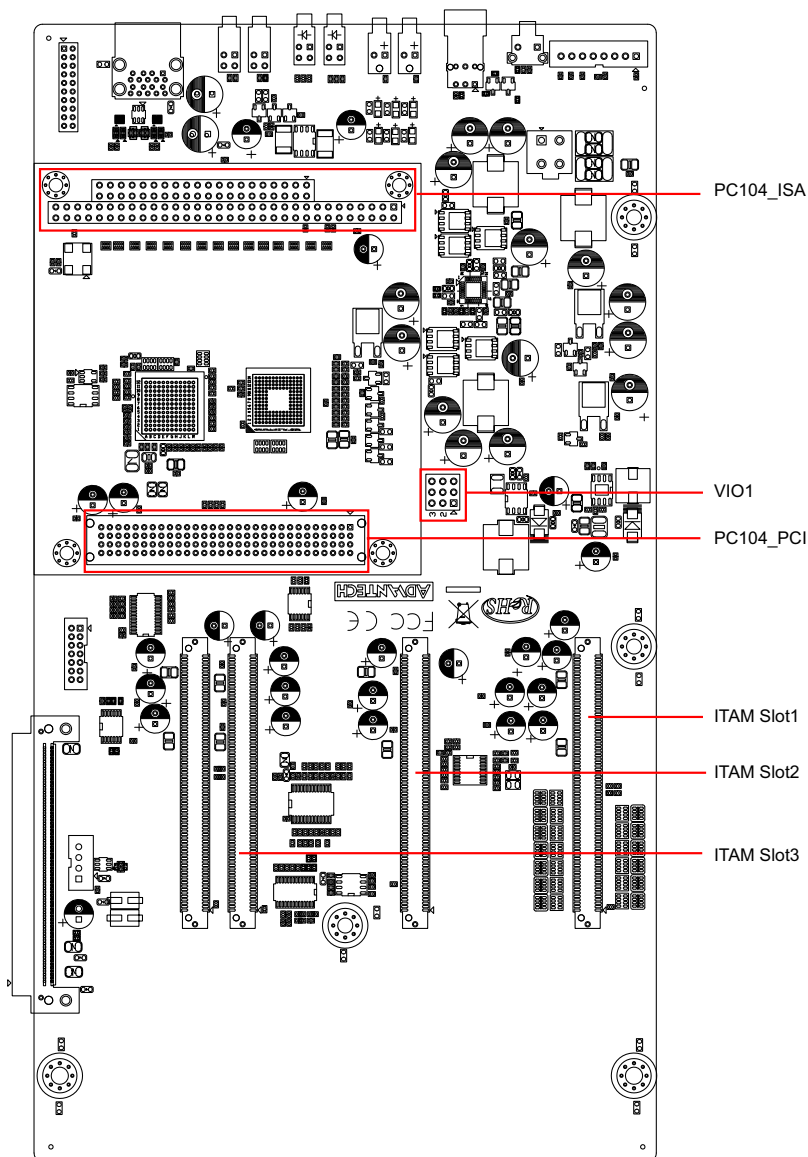


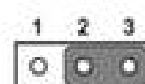
Figure 2.4 Jumper and Connector Location on Backplane

Table 2.1: Jumper

Name	Function
JCMOS1	Clear CMOS settings
PSON1	Start-up mode selection
VCCGPIO1	GPIO voltage selection



Default setting



Clear CMOS setting

Table 2.2: JCMOS1: Clear CMOS settings

Closed Pins	Setting
1-2	Normal (+V3.3_SB)*
2-3	Clear CMOS settings

*Default setting

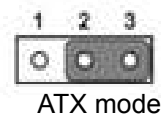
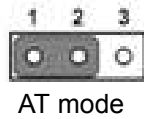


Table 2.3: PSON1: Start-up mode selection

Closed Pins	Setting
1-2	AT mode
2-3	ATX mode*
*Default setting	

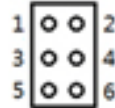


Table 2.4: VCCGPIO1: GPIO voltage selection

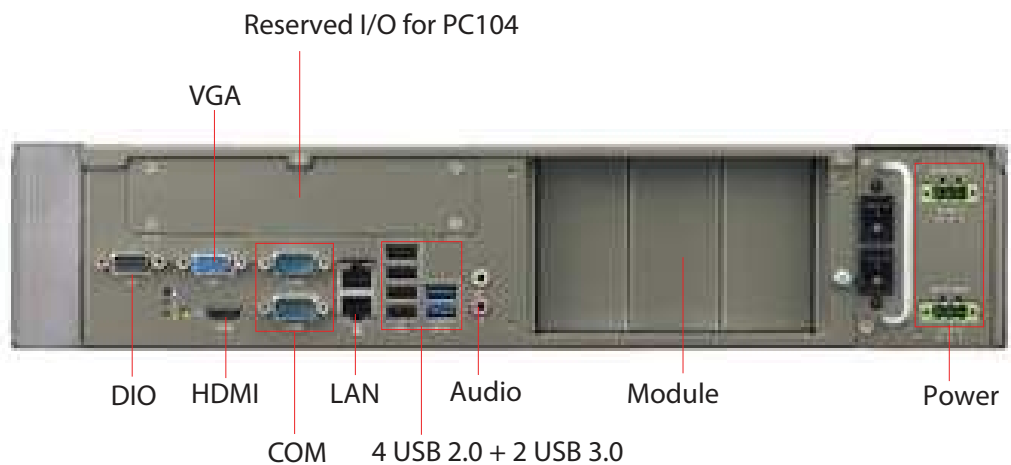
Closed Pins	Setting
1-3	+V5_SB*
2-4	+V3.3_SB
3-5	+V5
4-6	+V3.3
*Default setting	

2.4 I/O Connector



USB 3.0

Figure 2.5 ITA-2230 Front I/O Connectors



Reserved I/O for PC104
 VGA
 DIO
 HDMI
 COM
 LAN
 4 USB 2.0 + 2 USB 3.0
 Audio
 Module
 Power

Figure 2.6 ITA-2230 Rear I/O Connectors

2.4.1 COM Connector

ITA-2230 provides two DB9 connectors for RS-232/422/485.

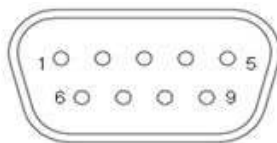


Table 2.5: COM Connectors

	RS-232	RS-422	RS-485
Pin	Signal Name	Signal Name	Signal Name
1	DCD	Tx-	DATA-
2	RxD	Tx+	DATA+
3	TxD	Rx+	NC
4	DTR	Rx-	NC
5	GND	GND	GND
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

2.4.2 HDMI Connector

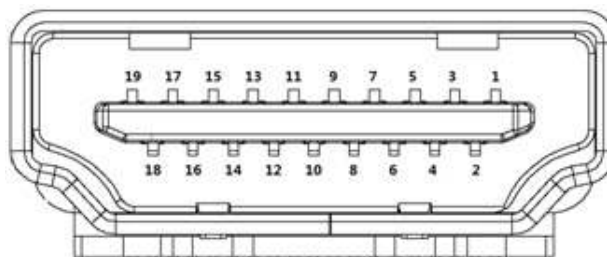


Table 2.6: VGA Connector Pin Assignment

Pin	Signal	Pin	Signal
1	TMDS Data2+	11	TMDS Clock Shield
2	TMDS Data2 Shield	12	TMDS Clock-
3	TMDS Data2-	13	CEC
4	TMDS Data1+	14	Reserved
5	TMDS Data1 Shield	15	SCL
6	TMDS Data1-	16	SDA
7	TMDS Data0+	17	DDC/CEC Ground
8	TMDS Data0 Shield	18	+5V Power
9	TMDS Data0-	19	Hot Plug Detect
10	TMDS Clock+		

2.4.3 VGA Connector

ITA-2230 offers 1 D-SUB 15-pin female connector.

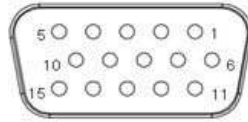


Table 2.7: VGA

Pin	Signal
1	Red(Red)
2	Green(Green)
3	Blue(Blue)
4	NC
5	GND
6	GND
7	GND
8	GND
9	+5V
10	GND
11	NC
12	DDC-DATA
13	H-SYNC
14	V-SYNC
15	DDC-CLK

2.4.4 DIO Connector

ITA-2230 provides a 8-bit DIO connector which should be connected via a cable.

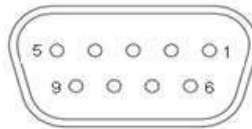


Table 2.8: DIO Connector

Pin	Signal	Pin	Signal
1	GPIO0	6	GPIO4
2	GPIO1	7	GPIO5
3	GPIO2	8	GPIO6
4	GPIO3	9	GPIO7
5	GND		

2.4.5 USB 2.0 Connector

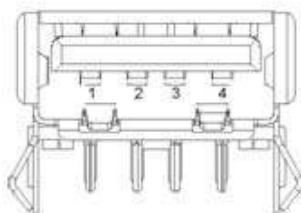


Table 2.9: USB2.0 Pin Assignment

Pin	Signal	Pin	Signal
1	+V5(VCC)	3	USB DATA+
2	USB DATA-	4	GND

2.4.6 USB 3.0 Connector

ITA-2230 provides two USB 3.0 connectors which are USB UHCI Rev. 3.0 compliant and can be disabled via BIOS setup.

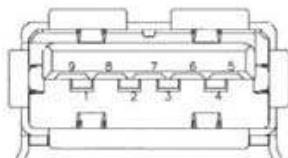
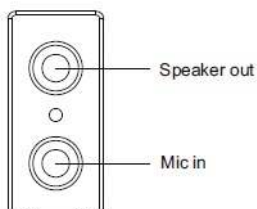


Table 2.10: USB 3.0 Pin Assignment

Pin	Signal	Pin	Signal
1	+V5(VCC)	6	StdA_SSRX+
2	D-	7	GND_DRAIN
3	D+	8	StdA_SSTX-
4	GND	9	StdA_SSTX+
5	StdA_SSRX-		

2.4.7 Audio in Connector

ITA-2230 provides one integrated Mic-in/speaker out audio connector.



2.4.8 LAN Connector

ITA-2230 provides two RJ-45 Ethernet connectors, which are IEEE 802.3U 10/100/1000 Mbps compliant, with LEDs indicating network status.

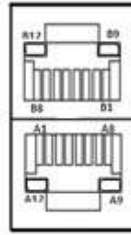


Table 2.11: LAN Connector

Pin	Signal Name
A1/B1	MDIO0+
A2/B2	MDIO0-
A3/B3	MDIO1+
A4/B4	MDIO2+
A5/B5	MDIO2-
A6/B6	MDIO1-
A7/B7	MDIO3+
A8/B8	MDIO3-
A9/B9	LED GREEN-
A10/B10	LED GREEN+
A11/B11	1000M LED
A12/B12	100m/10M LED

2.4.9 Phoenix Terminal Connector

ITA-2230 offers one 3-pin phoenix terminal connector.

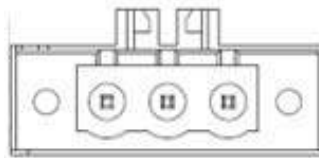


Table 2.12: Phoenix Terminal Connector

Pin	Signal Name
1	GND
2	N
3	L

- a. Instruction A: "Power installation must be performed with qualified electrician and followed with National Electrical Code, ANSI/NFPA 70 and Canadian Electrical Code, Part I, CSA C22.1."
- b. Instruction B: "Use No. 14 AWG, 75°C copper wire with RHW, THHW, THW, THWN, XHHW, USE or ZW type pressure terminal connector and 4.5 lb-in Torque force when connecting to terminal block." (2)
- c. Instruction C: "Connected mains shall be built branch circuit breaker which possessed 20 A of current rating." (3)
 - (1) According to UL 60950-1 Annex NAE 3.3
 - (2) According to UL 60950-1 Annex NAE 3.3.4 & NEC Standard Table 310.16
 - (3) According to UL 60950-1 Clause 1.7.2.2

Chapter 3

System Installation

3.1 Introduction

The following procedures will instruct you to install all modules into ITA-2230.

3.1.1 Installing Mainboard mini-PCle card and mini SATA

1. ITA-2230 mainboard has a mini-PCle slot and a mini SATA slot. Each one has a label for users to distinguish.
2. Insert mini-PCle card and mSATA card to the respective slot and fix with two screws.

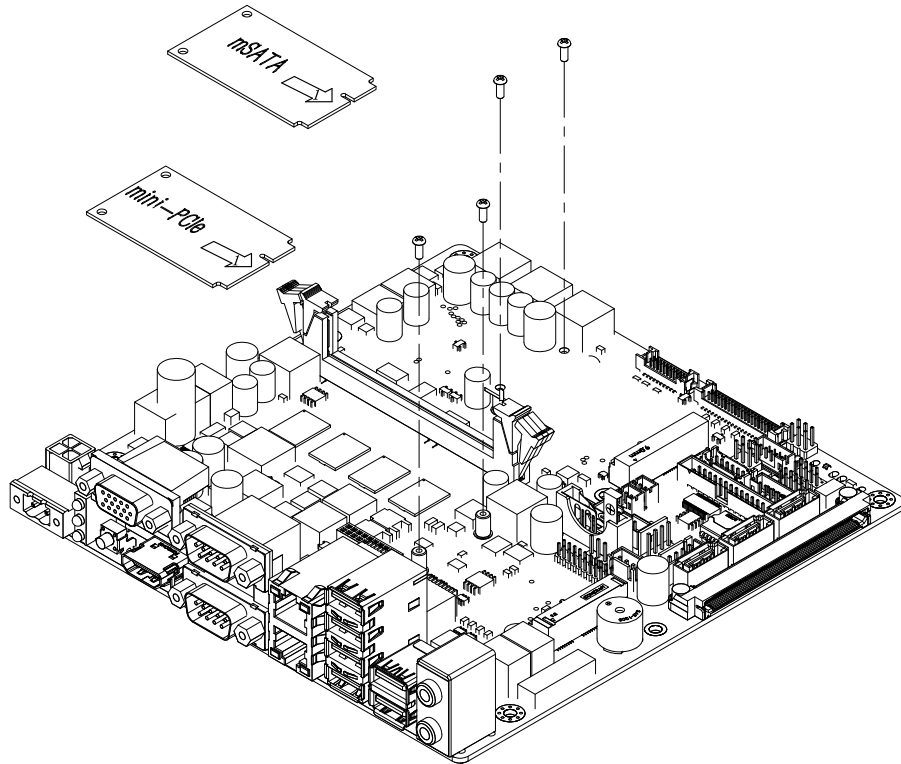


Figure 3.1 Installing mSATA and mini-PCle

3.1.2 Installing HDD Module

ITA-2230 reserves the space for two 2.5" HDD modules or one 3.5" HDD module. Please refer to the following instructions to install the HDD.

3.1.2.1 Installing 3.5" HDD

1. Open the top cover and remove the HDD holder in front of the mainboard.
2. Take four HDD rubbers from the accessory box and fill them into the four holes of HDD holder respectively.
3. Place the 3.5" HDD into HDD holder with the metal-side up. Align the screw holes on both sides of the HDD with the central holes of the rubbers, and fix with big screws.
4. Connect the HDD interface and the cable. Locate the HDD module into the chassis with HDD interface facing the backplane.

3.1.2.2 Installing 2.5" HDD

1. Place the HDD into the 2.5" HDD bracket with the metal-side up and locked it. The bracket supports up to two 2.5" HDDs.
2. Open the top cover and remove the HDD holder in front of the mainboard.

3. Take four HDD rubbers from the accessory box and fill them into the four holes of HDD holder respectively.
4. Place the assembled 2.5" HDD into HDD holder and fix with big screws.
5. Connect the HDD interface and the cable. Locate the HDD module into the chassis with HDD interface facing the backplane.

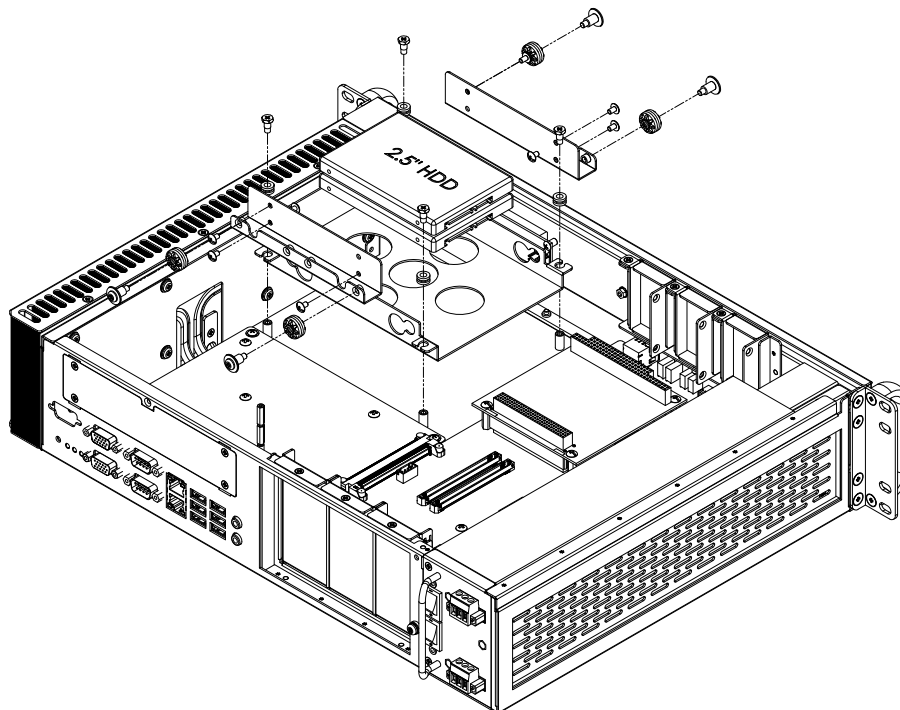


Figure 3.2 Installing HDD Module

3.1.3 Installing the Top Cover

Please refer to the following instructions to install the top cover.

1. Insert the top cover towards the front panel and make sure it's installed firmly.
2. Fix the top cover with 2 screws.

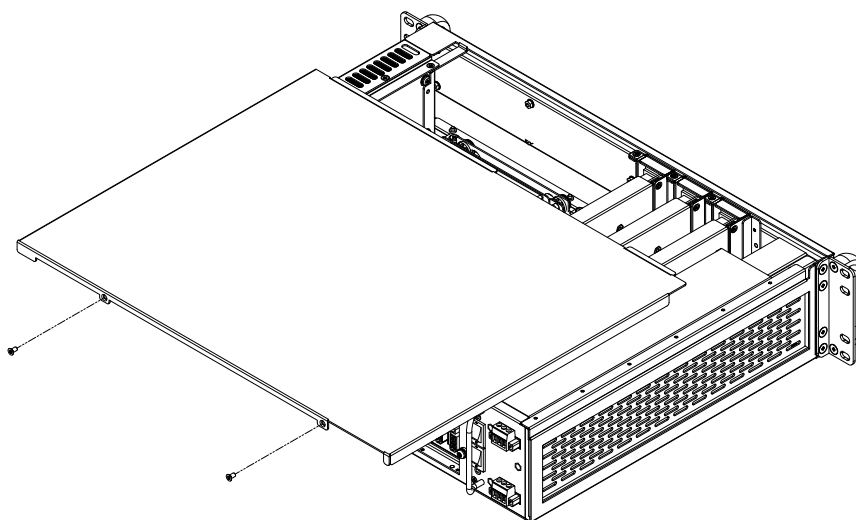


Figure 3.3 Installing the Top Cover

3.1.4 Installing Ears and Handles

Align two ears with the screw holes on both sides of the chassis, and fasten with screws. Align two handles with the screw holes on the ears, and fasten with screws.

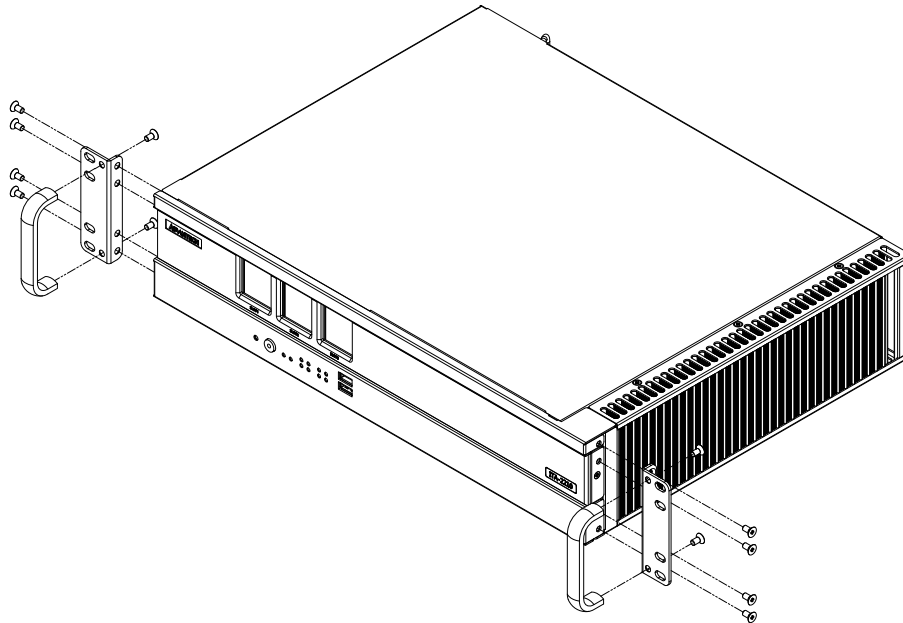


Figure 3.4 Installing the Foot Stand

3.1.5 Installing the ITAM Card Module

Please refer to the following instructions to install the ITAM card module.

1. Open the top cover of the ITA-2230 chassis.
2. Insert the ITAM module as demonstrated in the following figure.
 - a. Firstly, insert the I/O side of the module into the I/O panel of the chassis.
 - b. Then fix the front side of the module into the front panel of the chassis.
 - c. Confirm that the ITAM module interface is parallel to the ITAM slot of the back plane.
 - d. Make sure the module is fully inserted.
3. Fix the ITAM module into ITA-2230 with screws.

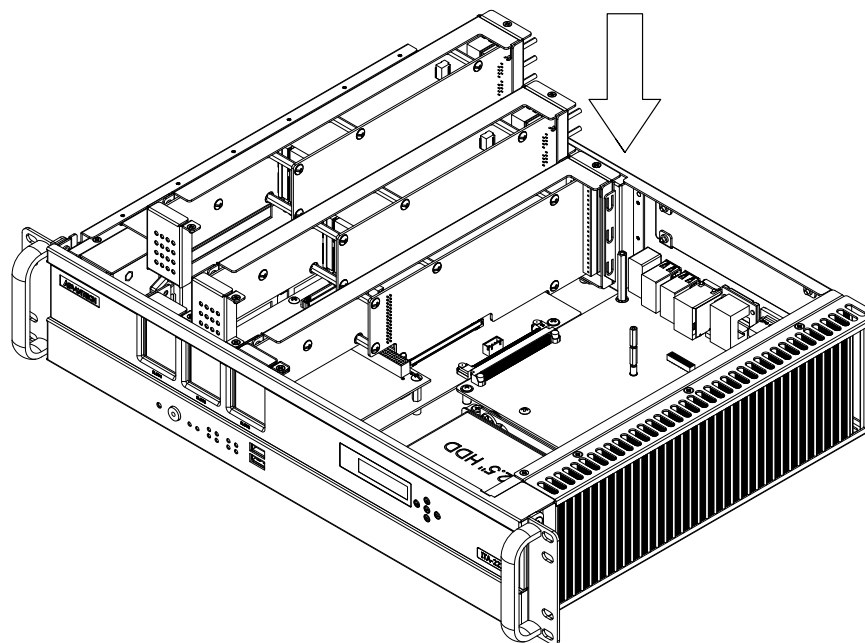


Figure 3.5 Installing the ITAM Card Module

Note! *ITA-2210 and ITA-2230 support up to 14 devices for Windows XP. (There's no restriction for Linux. ITAM cards can be combined randomly.)*



Combinations supported by XP is as follows:

ITAM Module	Number of logical devices	Maximum combination of all logical devices connected to three cards
ITAM-SR01	1	
ITAM-NC01-C	9	ITAM-SR01 x 3
ITAM-NC02-C	5	ITAM-NC01 x 1 + ITAM-SR01 x 2
ITAM-NC02-F	5	ITAM-NC02 x 1 + ITAM-SR01 x 2
On-board LAN	2	ITAM-NC x 2 + ITAM-SR01 x 1

Chapter 4

AMI BIOS Setting

4.1 Introduction

AMIBIOS has been integrated into many motherboards for over a decade. This chapter introduces how to configure BIOS for ITA-2230 series. With the AMIBIOS Setup program, you can modify BIOS settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter describes the basic navigation of the ITA-2230 setup screens.

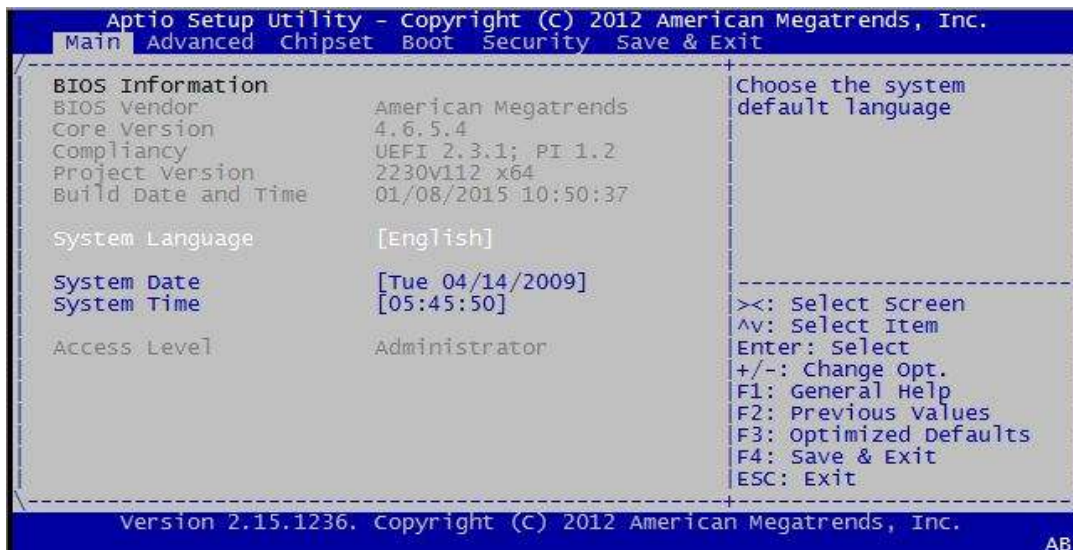


Figure 4.1 Setup Program Initial Screen

AMI's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in BIOS ROM so it retains the Setup information when the power is turned off.

4.2 Entering Setup

Turn on the computer to enter POST screen, and BIOS and CPU information will be shown. Press and you will immediately be allowed to enter Setup.

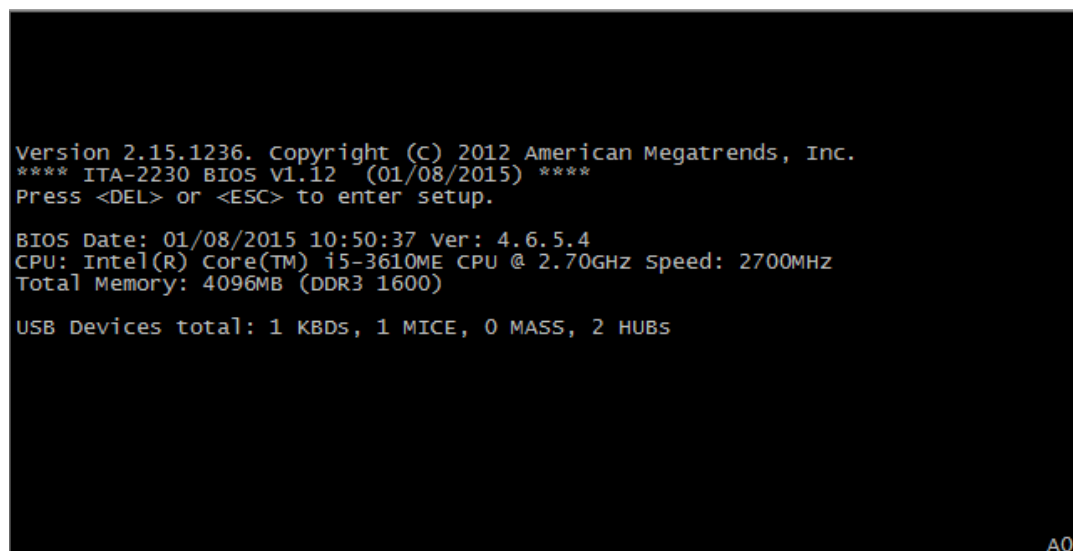


Figure 4.2 Press to Enter Setup Screen

4.2.1 Main Setup

When you first enter the BIOS Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.

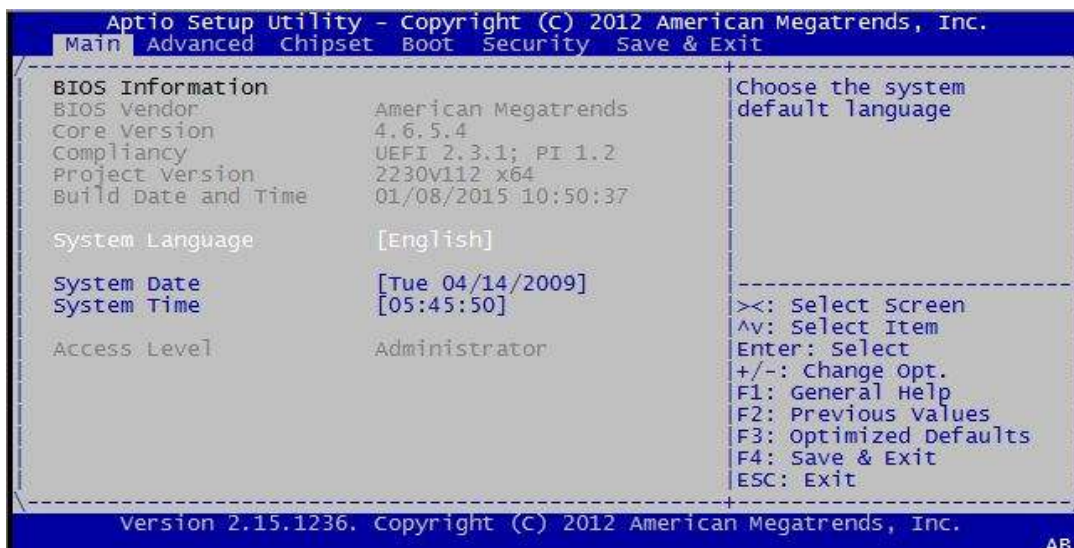


Figure 4.3 Main Setup Screen

The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

- **System Time / System Date**

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

4.2.2 Advanced BIOS Features Setup

Select the Advanced tab from the ITA-2230 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.

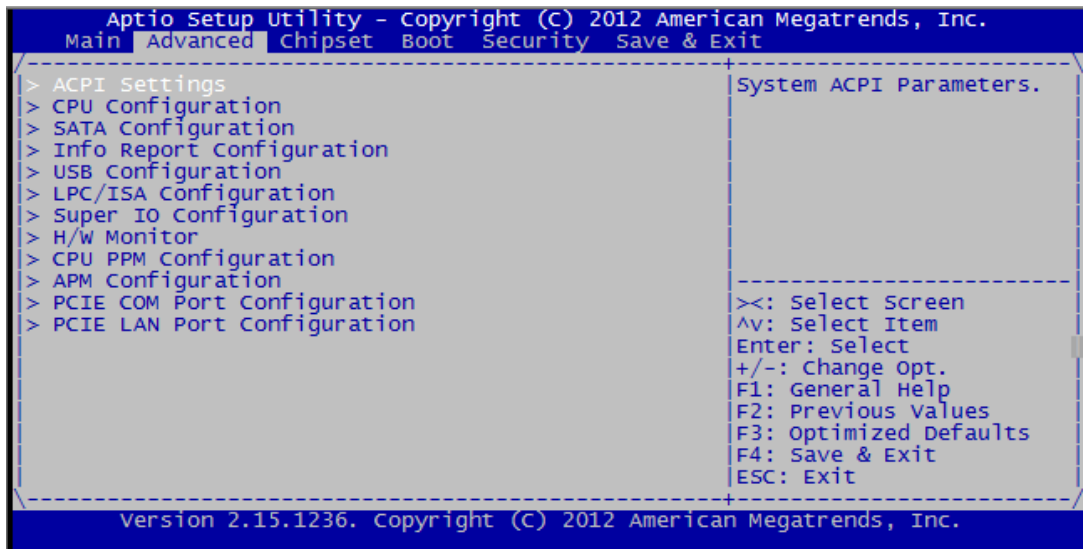


Figure 4.4 Advanced BIOS Features Setup Screen

4.2.2.1 ACPI Setting

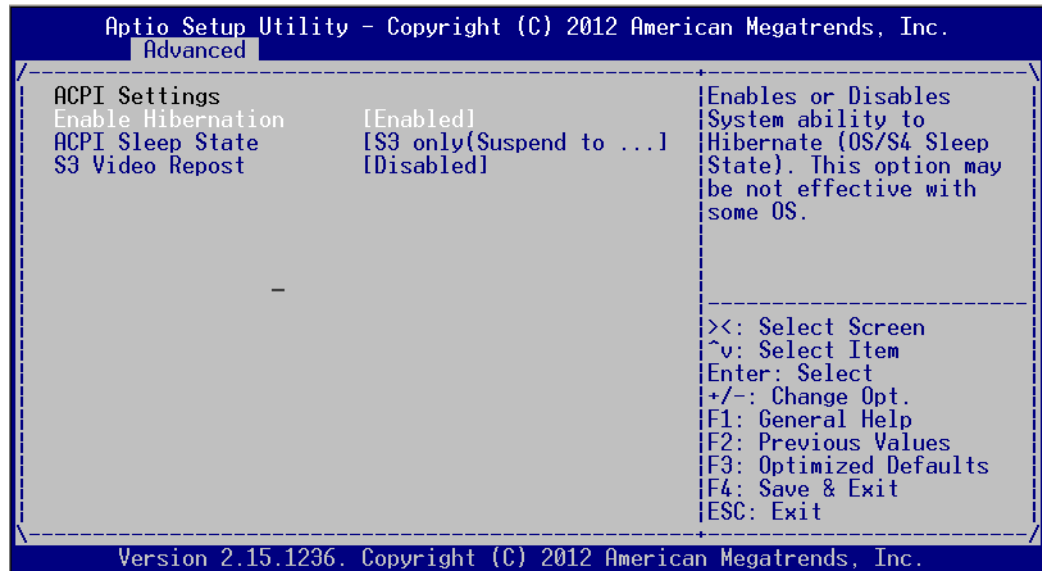


Figure 4.5 ACPI Configuration

Note! The power mode is ATX by default. If it's changed to AT, only "Advanced ACPI Configuration" is available.



- **Enable Hibernation**
This item allows users to enable or disable Hibernation.
- **ACPI Sleep State**
This item allows users to select ACPI state during system hibernation.
- **S3 Video Repost**
This item is used to decide whether to call VBIOS when the system resumes from S3/SRT. The default setting is "Disabled".

4.2.2.2 CPU Configuration

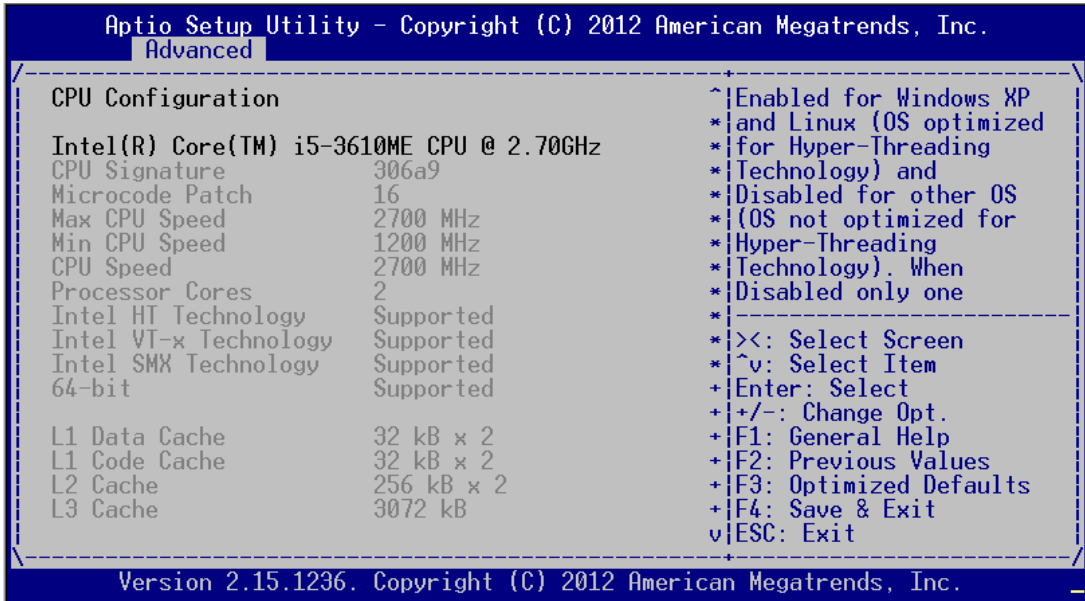


Figure 4.6 CPU Configuration (1)

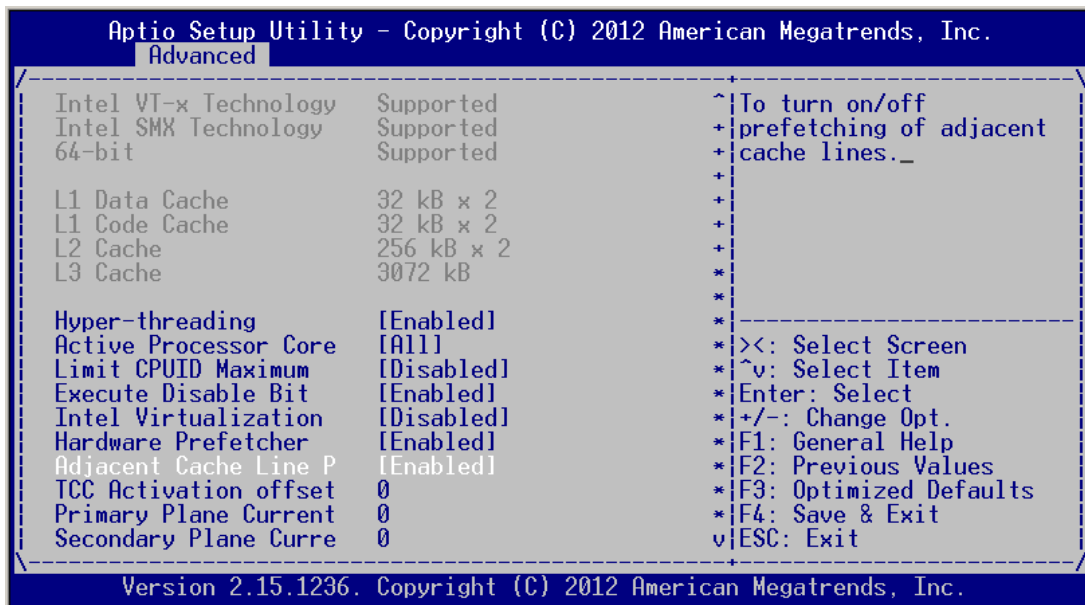


Figure 4.7 CPU Configuration (2)

- **Hyper Threading**
This item allows users to enable or disable Intel Hyper Threading Technology. The default setting is “Enabled”.
- **Active Processor Core**
This item allows users to choose how many processor cores to activate when you are using a dual or quad cores processor. The default setting is “All”.
- **Limit CPUID Maximum**
This item allows users to set the limit value for CPUID. The default setting is “Disabled”.
- **Execute Disable Bit**
This item is a hardware feature introduced by Intel in its new generation CPU. It can help CPU realize self-protection under the circumstance of hostile attack

based on buffer overflow, so as to avoid the virus attack, such as blasting wave. The default setting is “Enabled”.

- **Hardware Prefetcher**
This item allows users to enable or disable Hardware Prefetcher Technology. The default setting is “Enabled”.
- **Adjacent Cache Line Prefetch**
This item allows users to enable or disable sequential access to memory. The default setting is “Enabled”.
- **Intel Virtualization Technology**
This item is a system virtualization technology adopted in CPU produced by Intel. It allows multiple operating systems to run simultaneously on the same system. It adopts Vanderpool Technology, which allows multiple systems to run on the same system and applications can run in their own individual space. The default setting is “Enabled”.

4.2.3 SATA Configuration

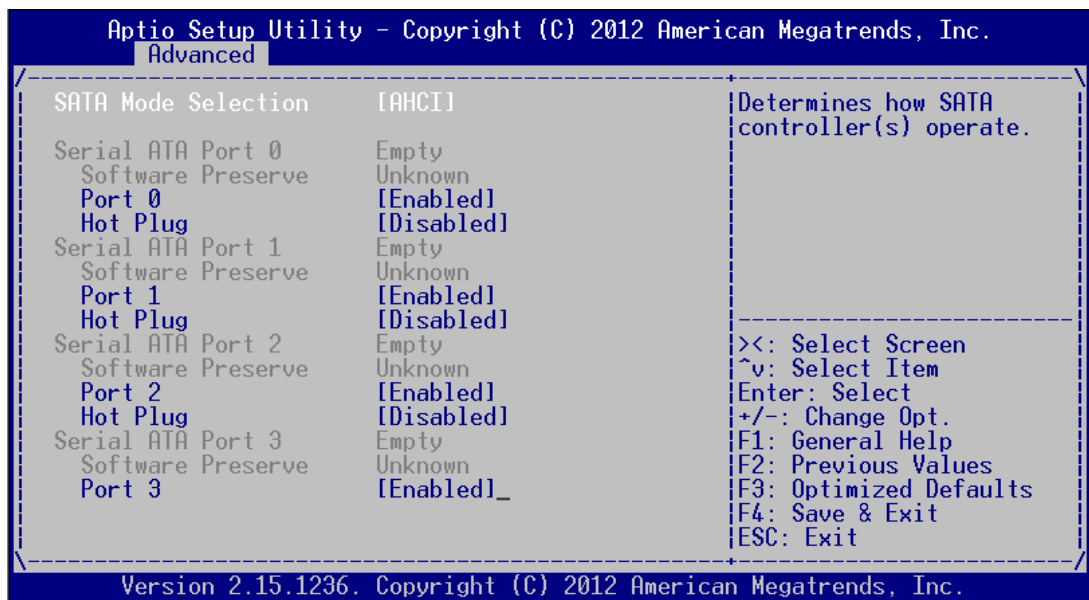


Figure 4.8 SATA Configuration

- **SATA Mode Selection**
This item allows users to select configuration mode of SATA Controller(s). The default setting is “AHCI”.

4.2.3.1 Info Report Configuration

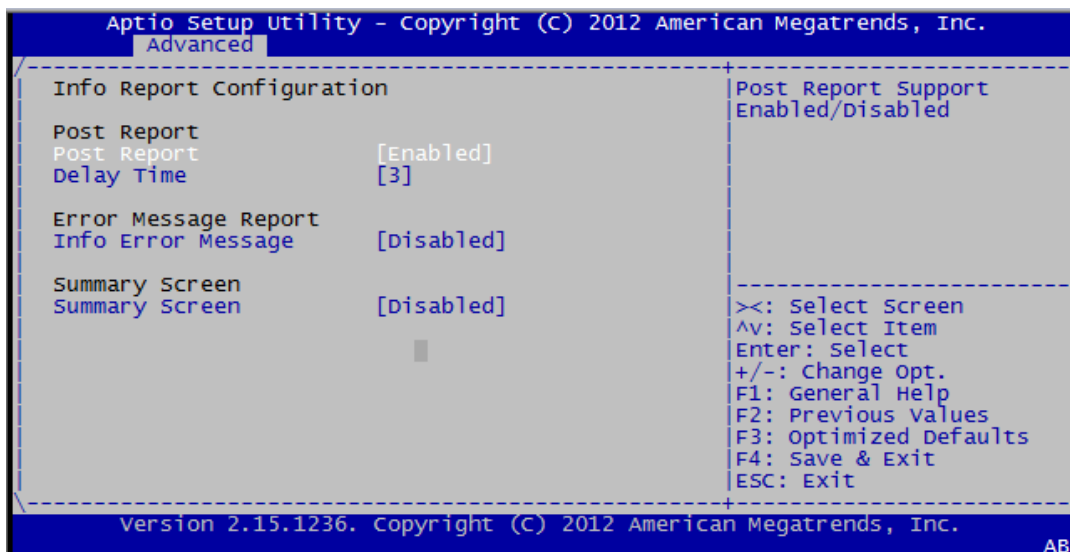


Figure 4.9 Info Report Configuration

- **Post Report**
The default setting is “Enabled”. By selecting “Enabled”, detailed information, such as CPU, Memory and BIOS, will be shown in POST screen.
- **Error Message Report**
Enable error message report. The default setting is “Disabled”.
- **Summary Screen**
Enable the summary of present configuration (e.g. BIOS version, CPU speed, memory module and installed massive storage device). The default setting is “Disabled”.

4.2.3.2 USB Configuration

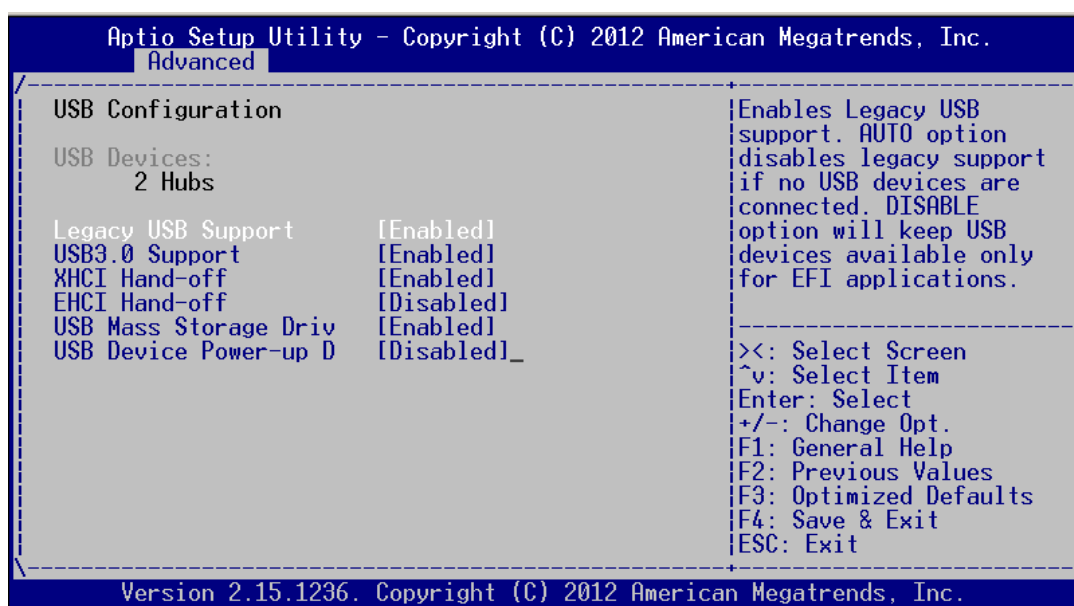


Figure 4.10 USB Configuration

- **Legacy USB Support**
This item allows users to enable support for traditional USB. It will be automatically set as “Disabled” when no USB device is connected. The default setting is “Enabled”.
- **USB 3.0 Support**
This item allows users to enable or disable USB 3.0 (XHCI). The default setting is “Enabled”.
- **XHCI Hand-off**
This item is to enable or disable function of supporting OS without XHCI Hand-off feature. The default setting is “Enabled”.
- **EHCI Hand-off**
This item is to enable or disable function of supporting OS without EHCI Hand-off feature. The default setting is “Disabled”.
- **USB Mass Storage Driver Support**
This item allows users to set the specific type of the connected USB device.
- **USB Device Power-up Delay**
- This item allows users to enable or disable the function of USB device reporting max. delay time to host controller. The default setting is “Disabled”.

4.2.3.3 LPC/ISA Configuration

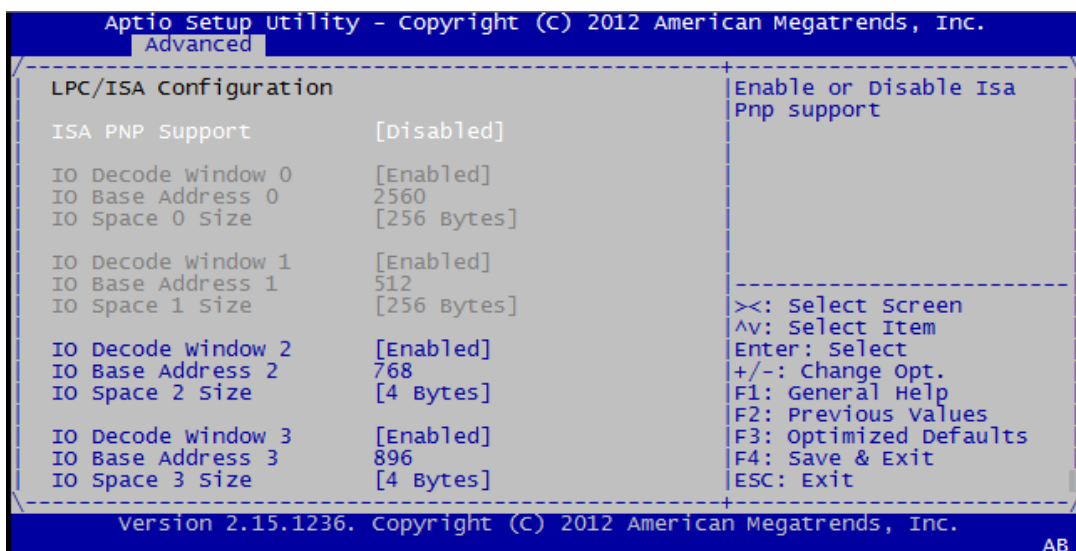


Figure 4.11 LPC/ISA Configuration

- **ISA PNP Support**
Enable ISA PNP Support. The default setting is “Disabled”.

4.2.3.4 Super I/O Configuration

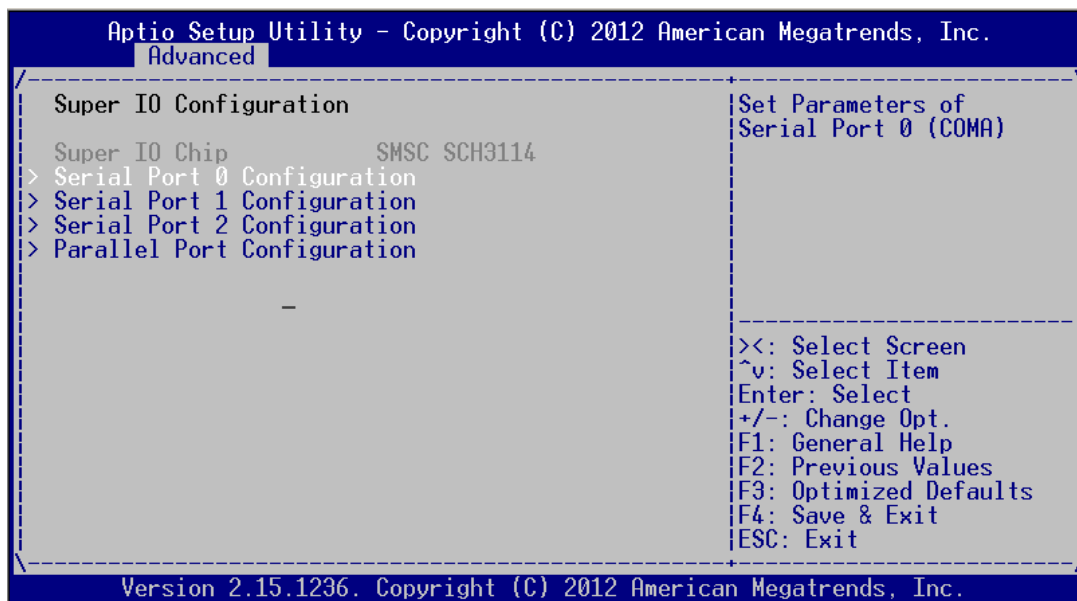


Figure 4.12 Super I/O Configuration

Serial Port 0 Configuration

■ Serial Port

This item allows users to open or close serial port. The default setting is "Enabled".

■ Serial Port Mode

This item allows users to set serial port as RS232/422/485. The default setting is "RS232".

■ Change Settings

IO=3F8h; IRQ=4;

IO=3F8h; IRQ=3,4,5,6,7,10,11,12;

This item allows users to select IO address and IRQ to change serial port settings.

■ Device Mode

– This item allow users to select device mode. The default setting is "Normal Mode".

4.2.3.5 H/W Monitor

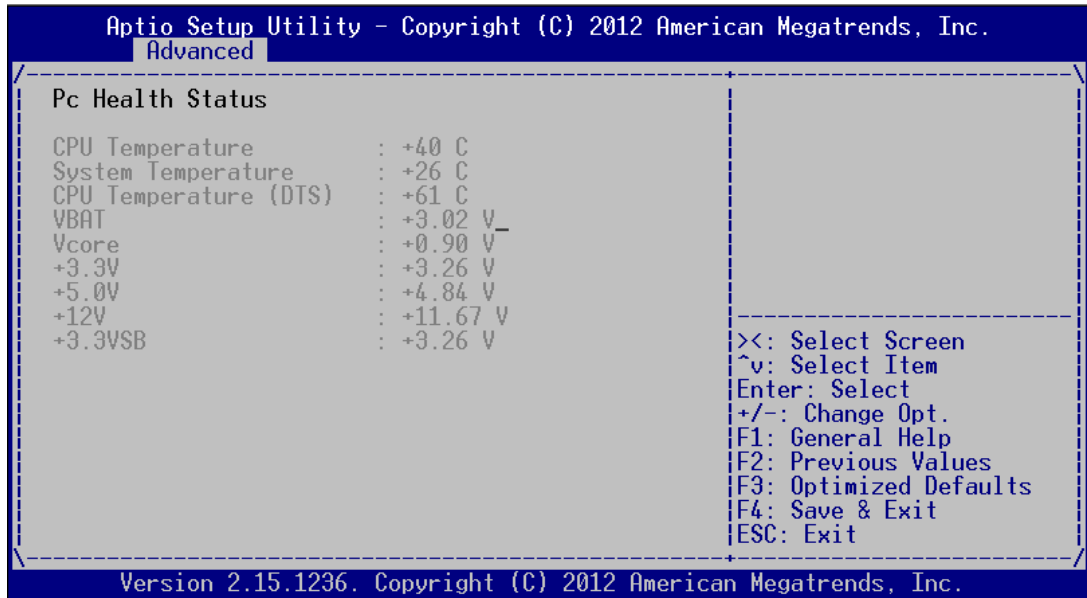


Figure 4.13 H/W Monitor Configuration

- **PC Health Status**

This item is used to hardware safety detection. BIOS will display the current system temperature, CPU temperature and other related voltage values. All these parameters have a certain range, so operations out of the range should be avoided.

4.2.3.6 CPU PPM Configuration

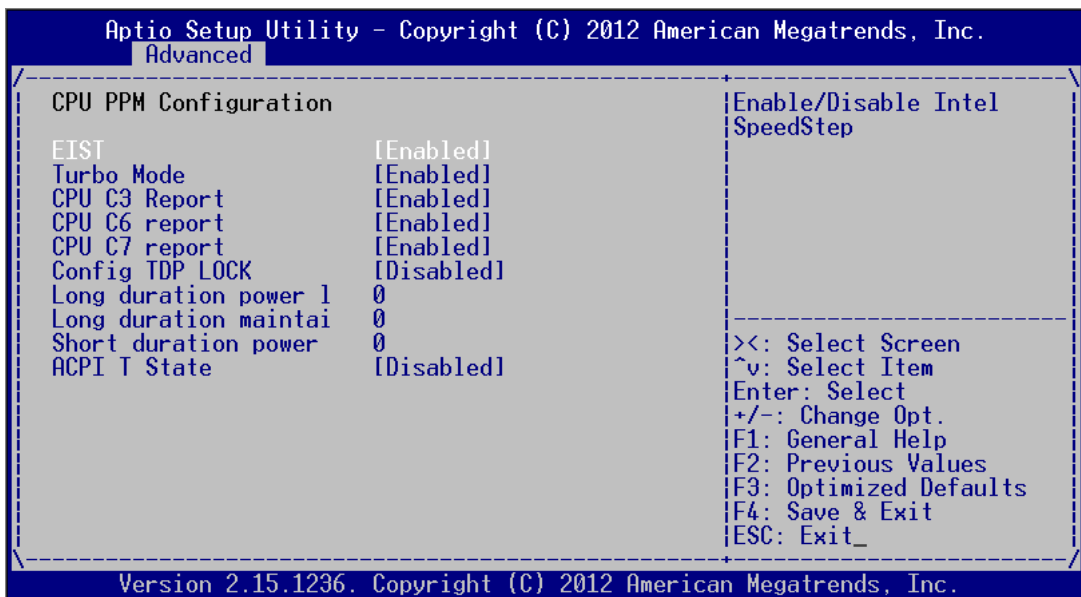


Figure 4.14 CPU PPM Configuration

- **EIST**

This item is used to set CPU Speed Step function. The default setting is “Enabled”.

- **Turbo Mode**

This item is used to set CPU Turbo mode function. The default setting is “Enabled”.

- **CPU C3/C6/7 Report**

This item is used to set CPU C-state function. The default setting is “Enabled”.

- **Config TDP LOCK**

This item is used to set Config TDP LOCK function. The default setting is “Disabled”.

- **ACPI T State**

This item is used to set ACPI T State function. The default setting is “Disabled”.

4.2.3.7 APM Configuration

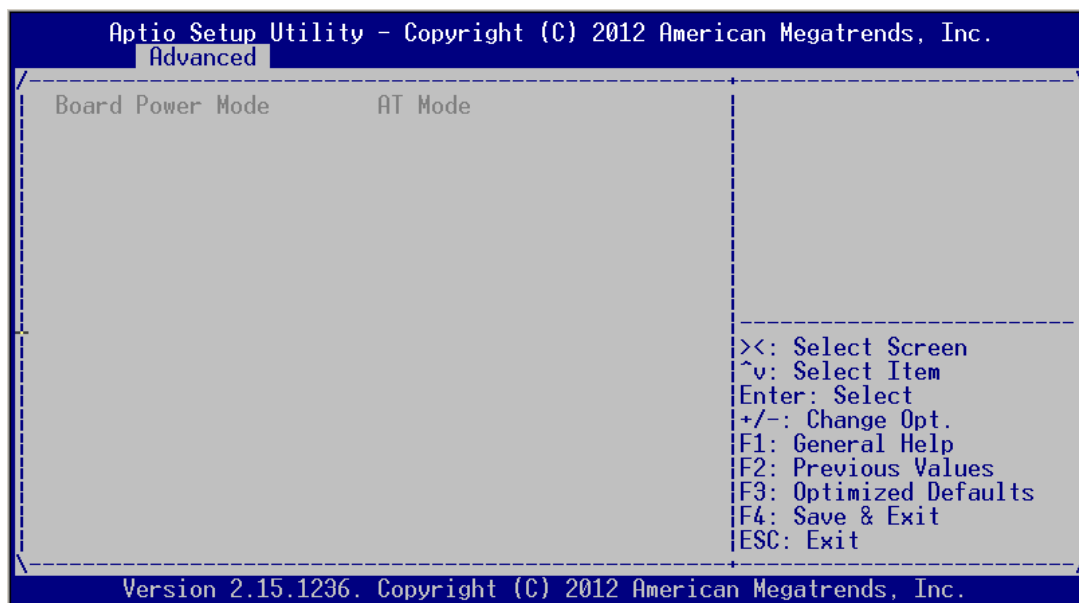


Figure 4.15 APM Configuration

- **Board Power Mode**

This item is used to set power on mode: AT or ATX mode.

4.2.3.8 PCIE COM Port Configuration

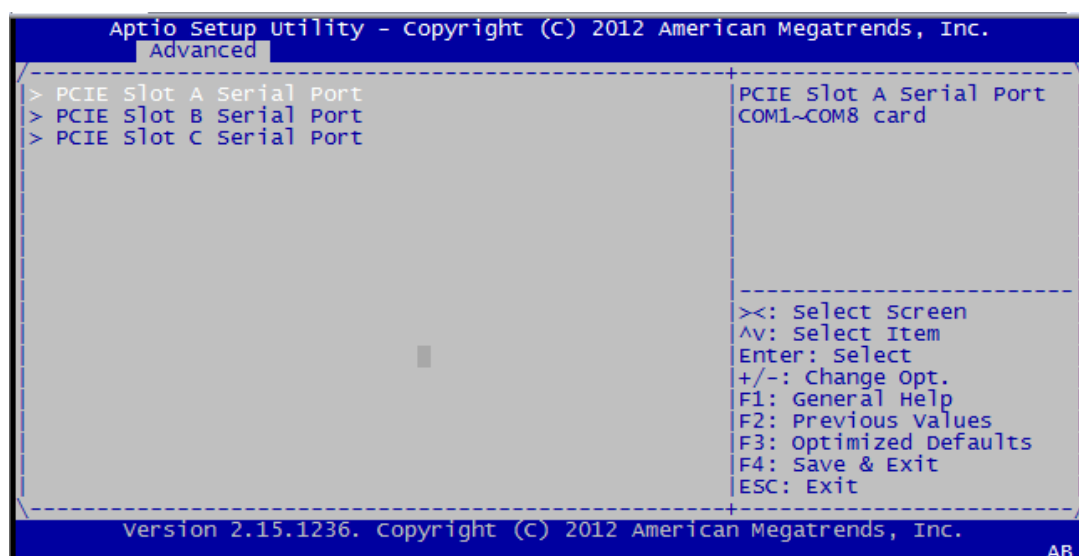


Figure 4.16 PCIE COM Port Configuration (1)

- **PCIE SLOT2 Serial Port**

This item shows the information of serial port upon PCIE slot. ITA-2230 has three PCIE slots for the expansion of ITAM I/O card.

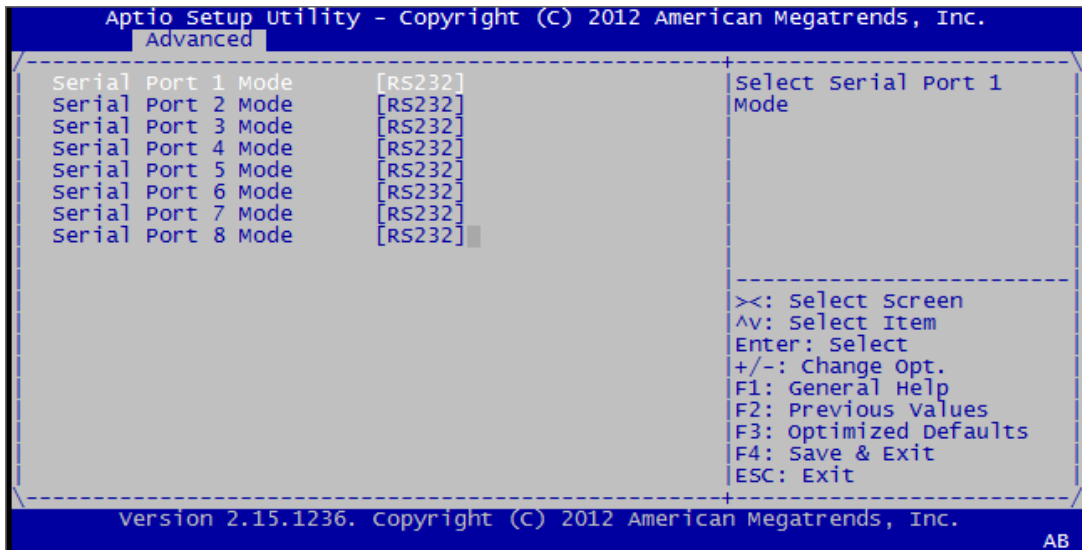


Figure 4.17 PCIE COM Port Configuration (2)

- **PCIE SLOT1 Serial Port**

This item shows the detailed information of the serial ports upon the first slot. By selecting Serial Port/Serial Port Mode 2-1 to 2-8, the RS232/RS422/RS485 mode can be configured. Set RS485 protocol to support flow control.

4.2.3.9 PCIE LAN Port Configuration

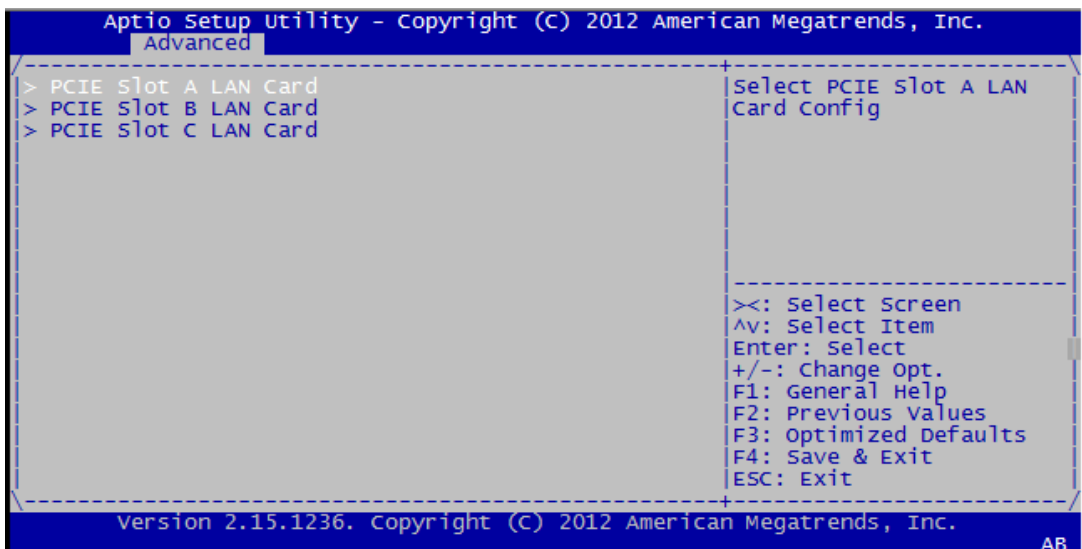


Figure 4.18 PCIE LAN Port Configuration (1)

- **PCIE SLOT1 LAN Port**

This item shows the information of serial port upon PCIE slot. ITA-2230 has three PCIE slots for the expansion of ITAM I/O card.

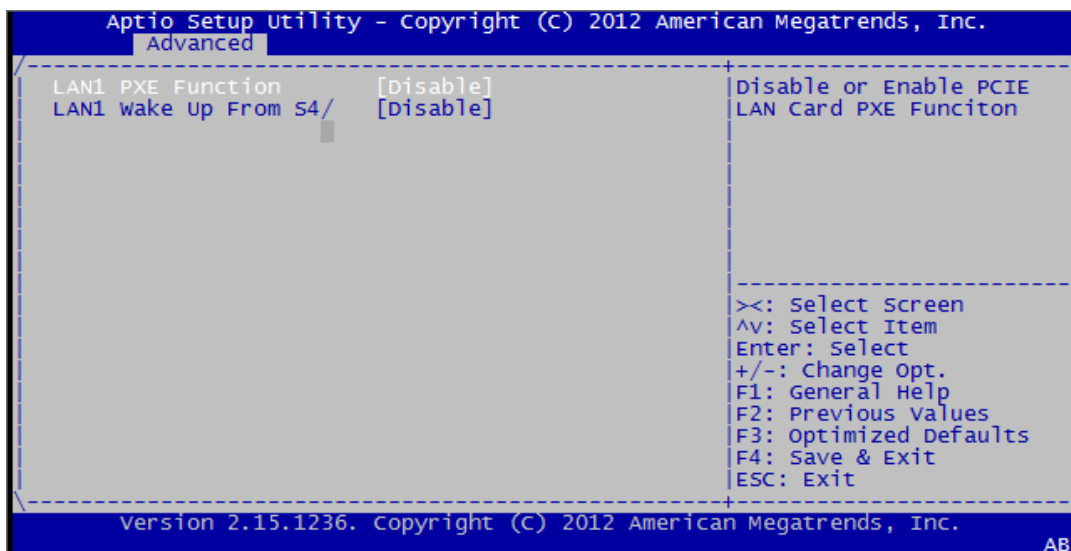


Figure 4.19 PCIE LAN Port Configuration (2)

- **LAN1 PXE Rom**
Enable/disable LAN1 PXE Rom.
- **LAN1 Wake Up From S4/S5**
Enable/disable LAN1 wakeup from S4/S5.

4.2.4 Advanced Chipset Features Setup

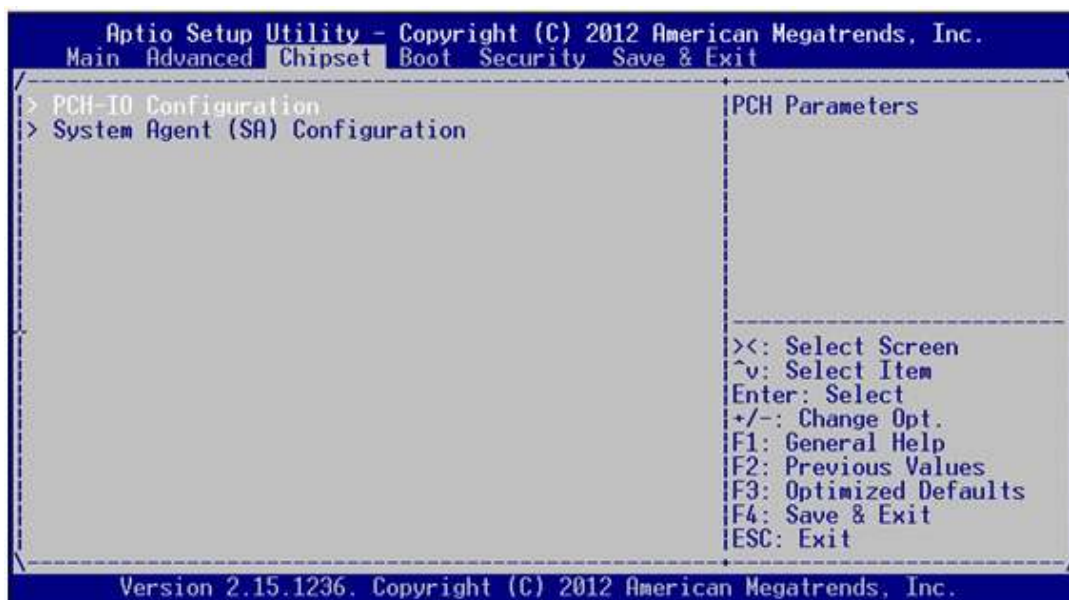


Figure 4.20 Advanced Chipset Features Setup

4.2.4.1 PCH-IO Configuration

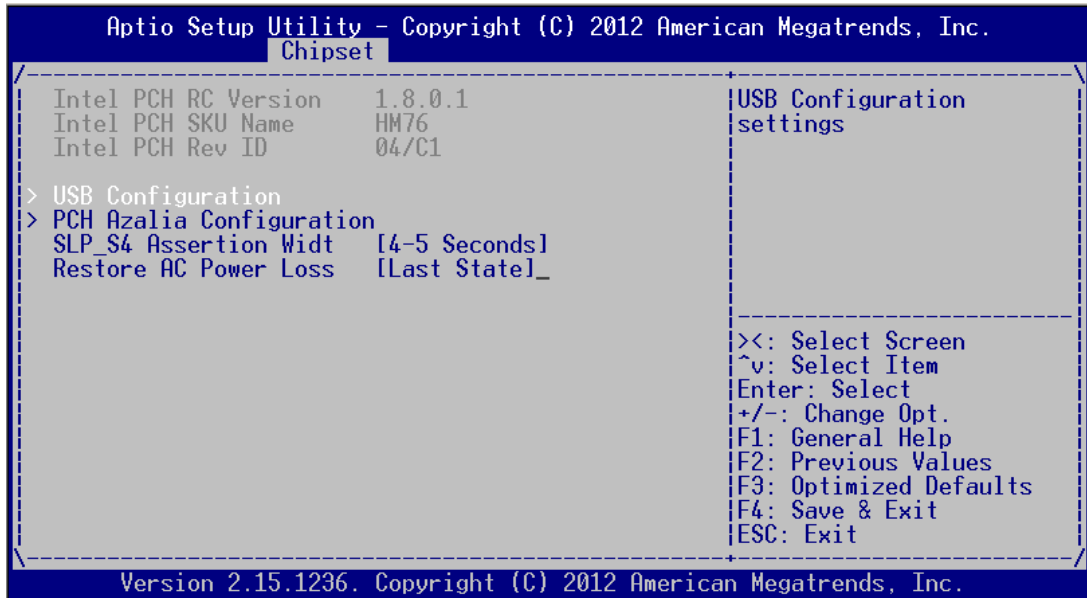


Figure 4.21 PCH-IO Configuration

- **SLP_S4 Assertion Width**
This item is used to set the min. delay of SLP_S4# signal when booting. The default setting is “4-5 Seconds”.
- **Restore AC Power Loss**
This item is used to set power status when the power in on.
Power Off: Power button should be pressed after the power is on.
Power On: No action required after the power is on.
Last State: Resume to the last state before the power is off.

4.2.4.2 USB Configuration

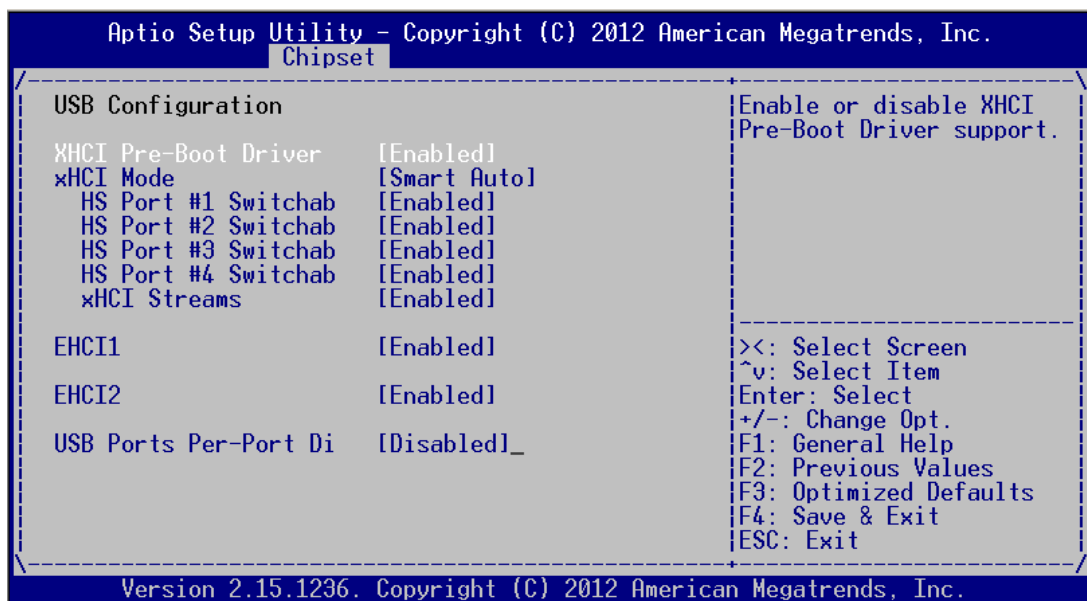


Figure 4.22 Chipset USB Configuration

- **XHCI Pre-Boot Driver**
This item allows users to enable or disable XHCI Pre-Boot Driver. The default setting is “Enable”.
- **xHCI Mode**
This item is used to select xHCI controller mode. The default setting is “Smart Auto”.
- **HS Port #1/#2/#3/#4 Switchable**
Enable: BIOS will let the port connect to EHCI; Disable: BIOS will let the port connect to xHCI. The default setting is “Enable”.
- **xHCI Streams**
This item allows users to enable or disable xHCI Maximum Primary Stream Array Size.
- **EHCI1/EHCI2**
This item allows users to enable or disable EHCI #1/EHCI #2. The default setting is “Enable”.
- **USB Ports Per-Port Disable Control**
This item is used to set disable control of each USB connector.

4.2.4.3 PCH Azalia Configuration

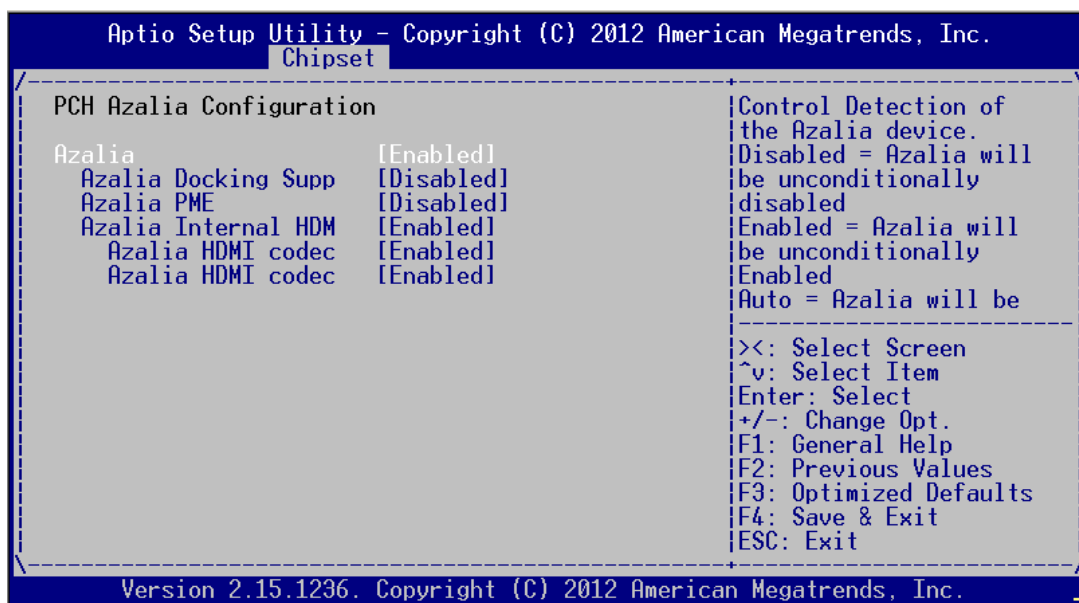


Figure 4.23 PCH Azalia Configuration

- **Azalia**
This item is used to detect Azalia device. The default setting is “Enable”.
 - Disabled?Azalia will be unconditionally disabled
 - Enabled?Azalia will be unconditionally Enabled
 - Auto?Azalia will be enabled if present, disabled otherwise.

4.2.4.4 System Agent (SA) Configuration

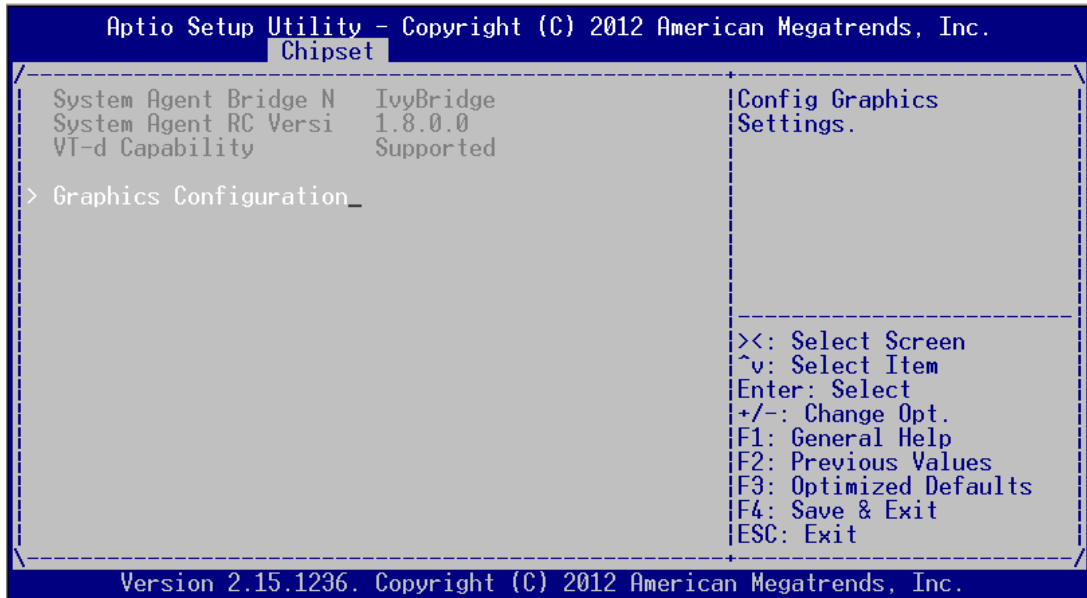


Figure 4.24 System Agent (SA) Configuration

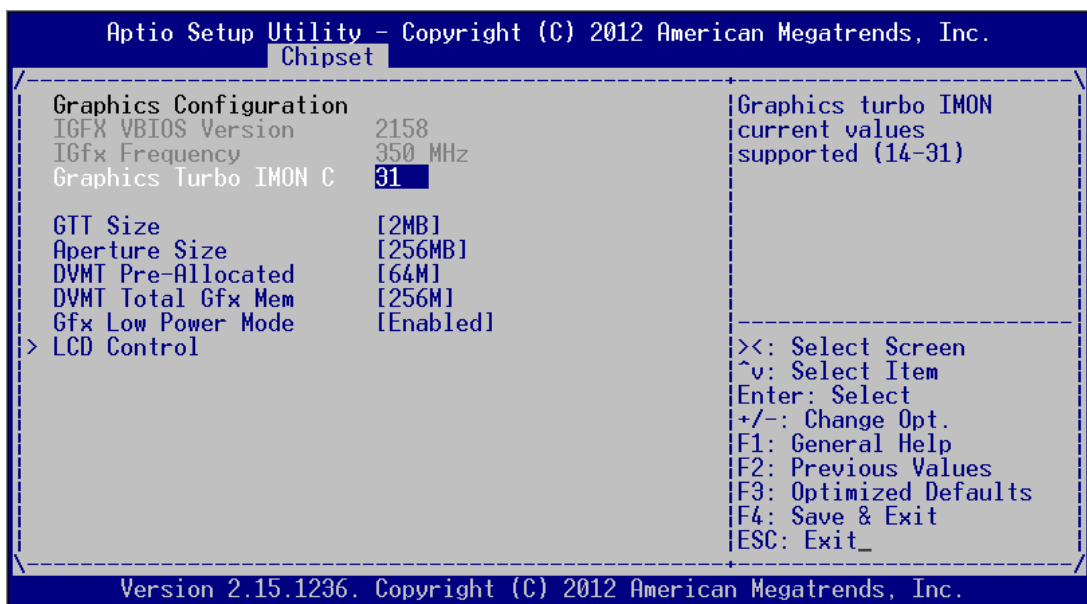


Figure 4.25 Graphics Configuration Menu

- **Graphics Turbo IMON Current**
Graphics turbo IMON current values supported (14-31).
- **GTT Size**
This item is used to select GTT size.
- **DVMT Total Gfx Mem**
This item allows users to select memory size of DVMT Total.
- **Gfx Low Power Mode**
This item allows users to enable of disable Low Power mode.

4.2.4.5 LCD Control

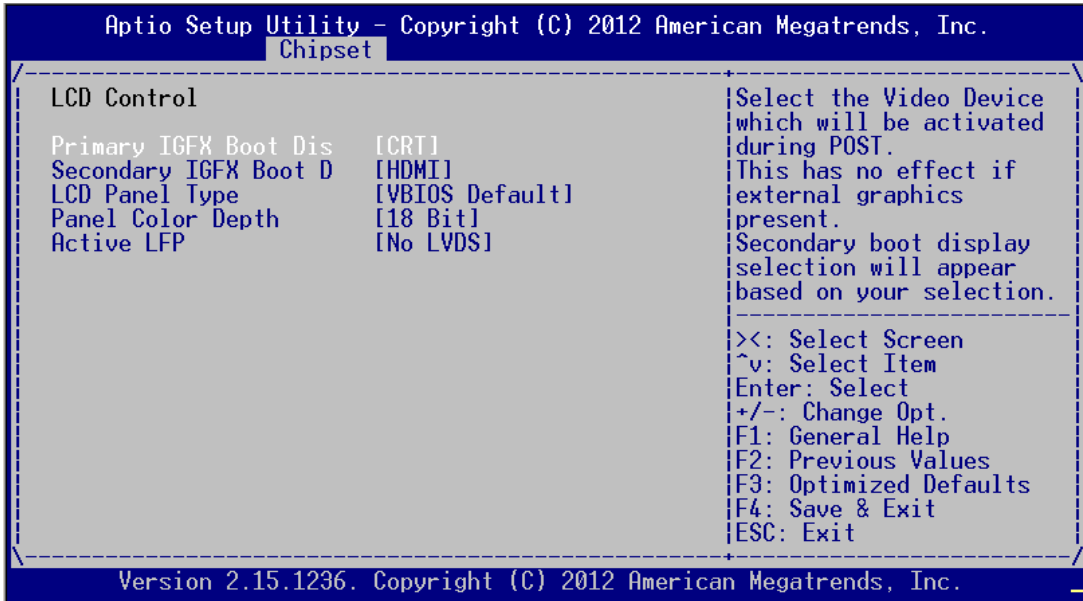


Figure 4.26 LCD Control

- **Primary IGFX Boot Display**
 This item is used to select video device started during POST. The default setting is "CRT".
- **Secondary IGFX Boot Display**
 This item is used to set Second Display Device.
- **LCD Panel Type**
 This item is used to set LCD resolution. The default setting is "1024x768(24bit)".
- **Panel Color Depth**
 This item is used to set LFP Panel Color Depth.
- **Active LFP**
 This item is used to select Active LFP Configuration.

4.2.5 Boot Setup

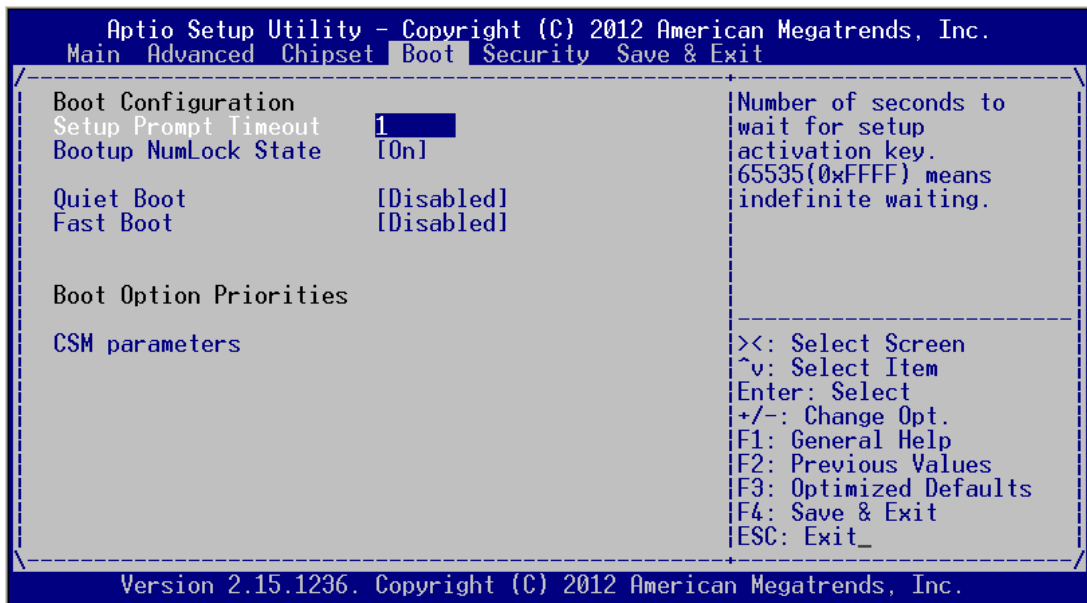


Figure 4.27 Boot Setup

4.2.5.1 Boot Configuration

- **Setup Prompt Timeout**

This item is the waiting time of pressing Setup button. If Setup button is not pressed within the setting time, system will continue to boot.
- **Bootup NumLock State**

This item allows users to active Bootup NumLock State function after the system is power on to DOS. The default setting is “On”.

 - On: NumLock function is on when system boots.
 - Off: Cursor control is activated for keypad when system boots.
- **Quiet Boot**

If it is set to “Disabled”, BIOS will display normal POST information; If it is set to “Enabled”, BIOS will show OEM icon rather than POST information.
- **Fast Boot**

This item allows BIOS to skip some testing procedures during booting so as to reduce system boot-up time. The default setting is “Disabled”.

4.2.5.2 Boot Option Priorities

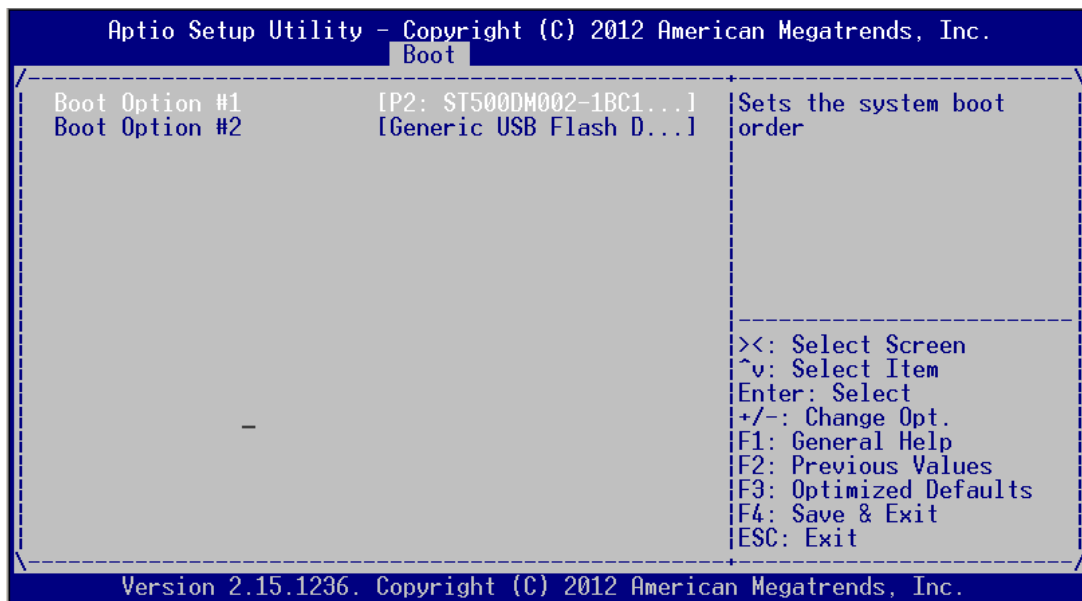


Figure 4.28 Boot Option Priorities

This item is used to set device boot sequence.

4.2.5.3 CSM Parameter

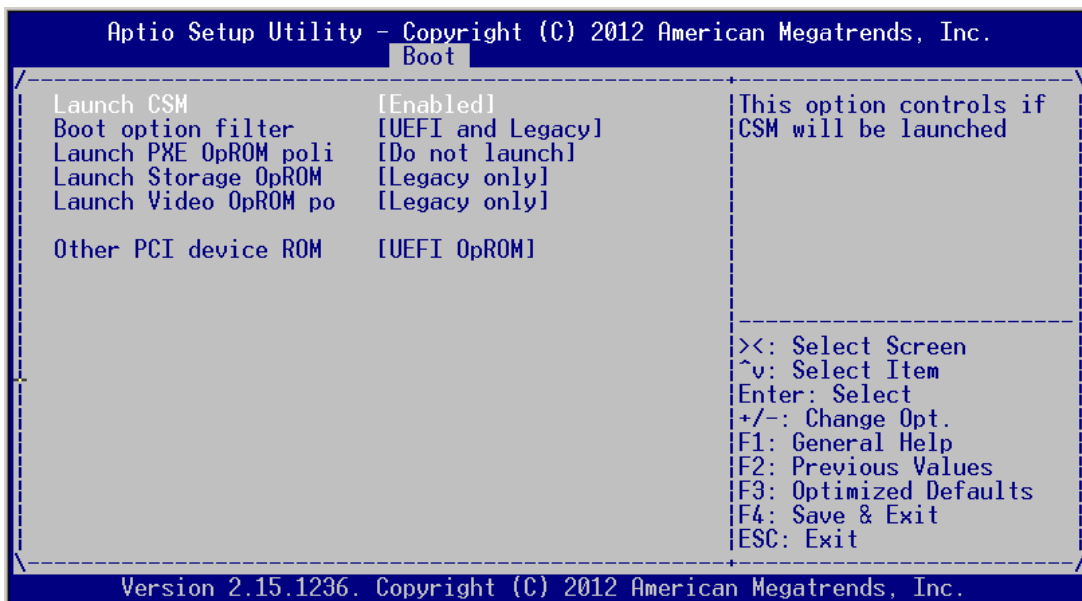


Figure 4.29 CSM Parameter

- **Launch CSM**
This item allows user to enable or disable CSM. The default setting is "Enable".
- **Boot option filter**
This item is used to control boot device system. The default setting is "UEFI and Legacy".
- **Launch PXE OpROM policy**
This item is used to control UEFI execution and backward compatibility of PXE OpROM. The default setting is "Do not Launch".

- **Launch Storage OpROM policy**
This item is used to control UEFI execution and backward compatibility of PXE OpROM. The default setting is “Legacy only”.
- **Launch Video OpROM policy**
This item is used to control UEFI execution and backward compatibility of PXE OpROM. The default setting is “Legacy only”.
- **Other PCI device ROM priority**
- This item is used for PCI device that is not the same as network, which is defined by massive storage or video booted by OpROM.

4.2.6 Security Setup



Figure 4.30 Setup Security Menu

- **Administrator Password**
This item is used to set Administrator Password.
- **User Password**
This item is used to set User Password.

4.2.7 Save & Exit Setup

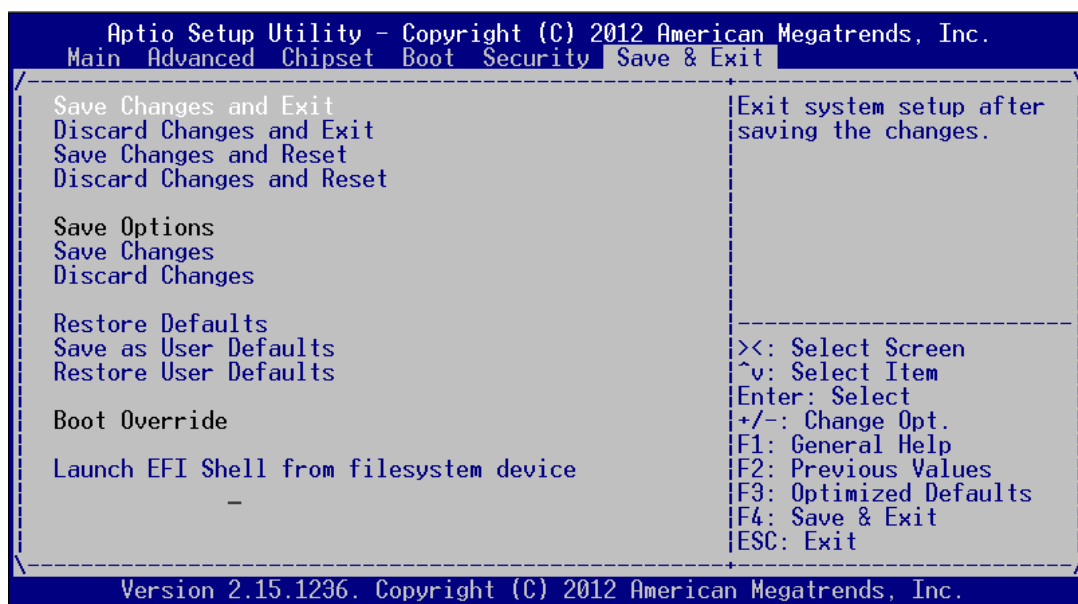


Figure 4.31 Setup Save & Exit Menu

- **Save Changes and Exit**

When you have completed system configuration, select this option to save your changes, exit BIOS setup and reboot the computer so the new system configuration parameters can take effect.

 1. Select Save Changes and Exit from the Exit menu and press <Enter>. The following message appears:
Save Configuration Changes and Exit Now?
[Ok] [Cancel]
 2. Select Ok or Cancel.
- **Discard Changes and Exit**

Select this option to quit Setup without making any permanent changes to the system configuration.

 1. Select Exit Discard Changes and Exit from the Exit menu and press <Enter>. The following message appears:
Discard Changes and Exit Setup Now?
[Ok] [Cancel]
 2. Select Ok to discard changes and exit.
- **Save Changes and Reset**

When you have completed system configuration, select this option to save your changes, exit BIOS setup and reboot the computer so the new system configuration parameters can take effect.

 1. Select Save Changes and Reset and press <Enter>. The following message appears:
Save configuration and Reset?
[Yes] [No]
 2. Select Ok or Cancel.

-
- **Discard Changes and Reset**
Select this option to quit Setup without making any permanent changes to the system configuration.
 1. Select Discard Changes and Reset from the Exit menu and press <Enter>. The following message appears:
Discard Changes and Reset Setup Now?
[Ok] [Cancel]
 2. Select Ok to discard changes and exit.
 - **Save Changes**
This item allows users to save changes done so far to any of the options.
 - **Discard Changes**
This item allows users to discard changes done so far to any of the options.
 - **Restore Defaults**
This item allows users to restore/load default values for all the options.
 - **Save as User Defaults**
This item allows users to save the changes done so far as user defaults.
 - **Restore User Defaults**
This item allows users to restore the user defaults to all the options.
 - **Boot Override**
This item allows users to set boot device.
 - **Launch EFI Shell from file system device**
This item allows to boot EFI shell from system file device

Chapter 5

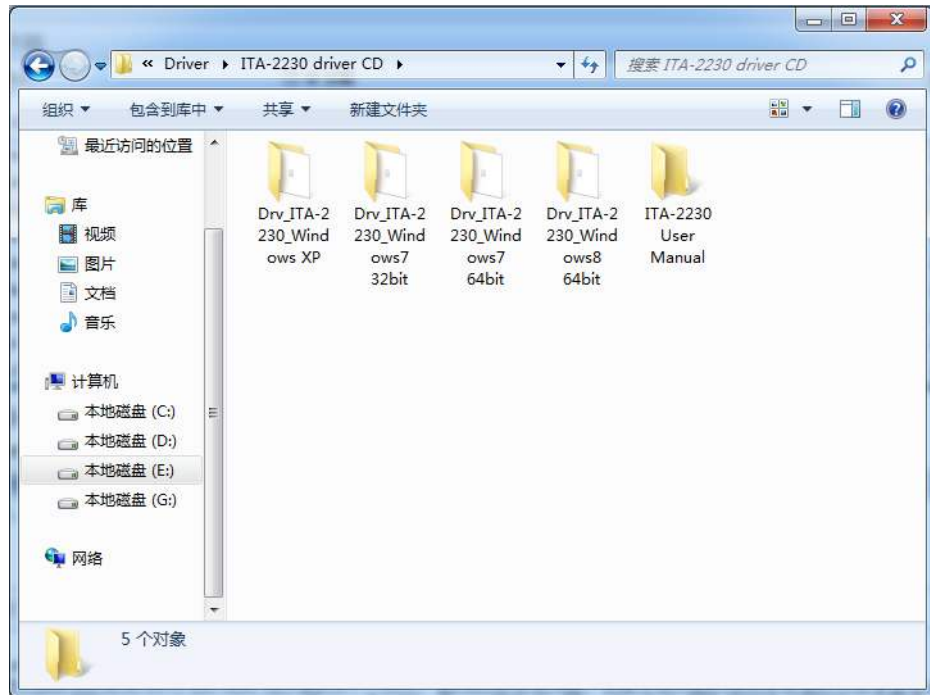
Driver Installation

5.1 Introduction

Advantech offers a complete range of Device Driver and software supports for Windows programming developers. You can apply the Windows Device Drivers to the most popular Windows Programming tools, such as Visual C++, Visual Basic, Borland C++ Builder and Borland Delphi.

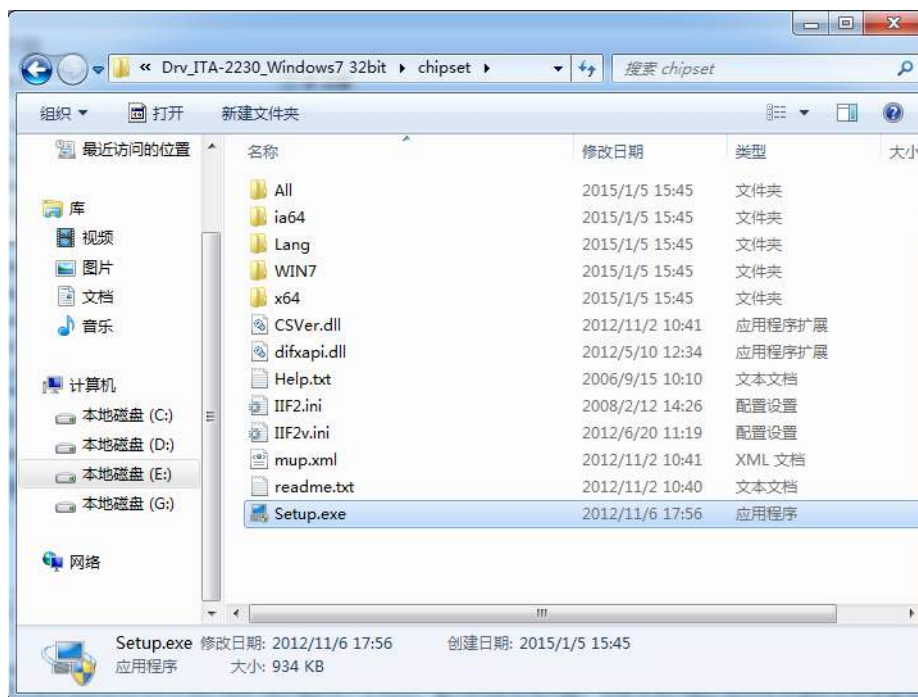
5.2 Driver Installation

Insert the driver CD into your system's CD-ROM drive. You can see the ITA-2230 driver folder items.



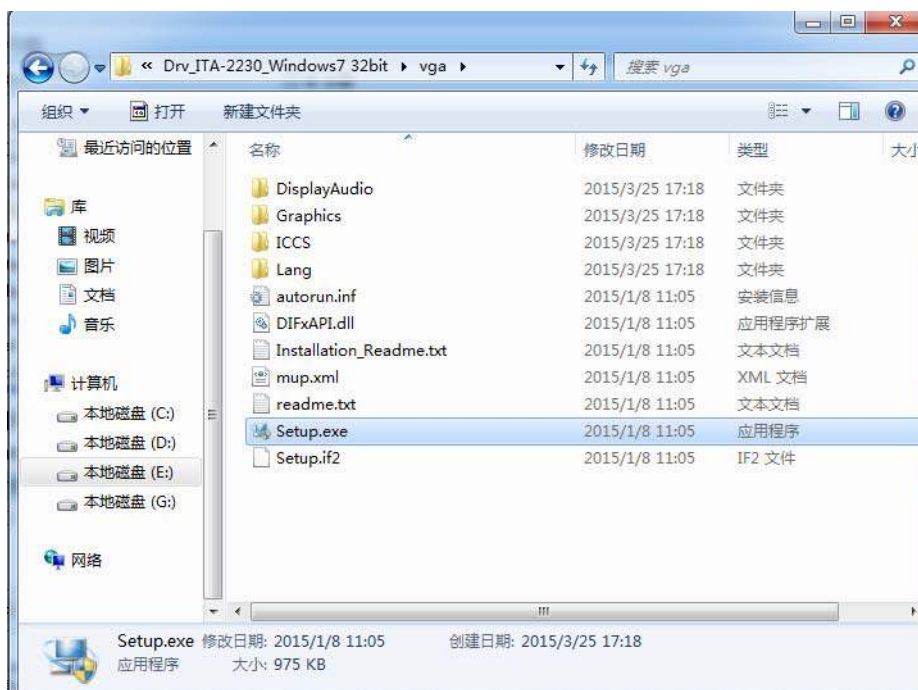
5.2.1 Chipset Windows Driver Setup

Insert the driver CD into your system's CD-ROM drive. You can see the ITA-2230 driver folder. Navigate to the "chipset" folder and click "Setup.exe" to complete the installation of the driver.



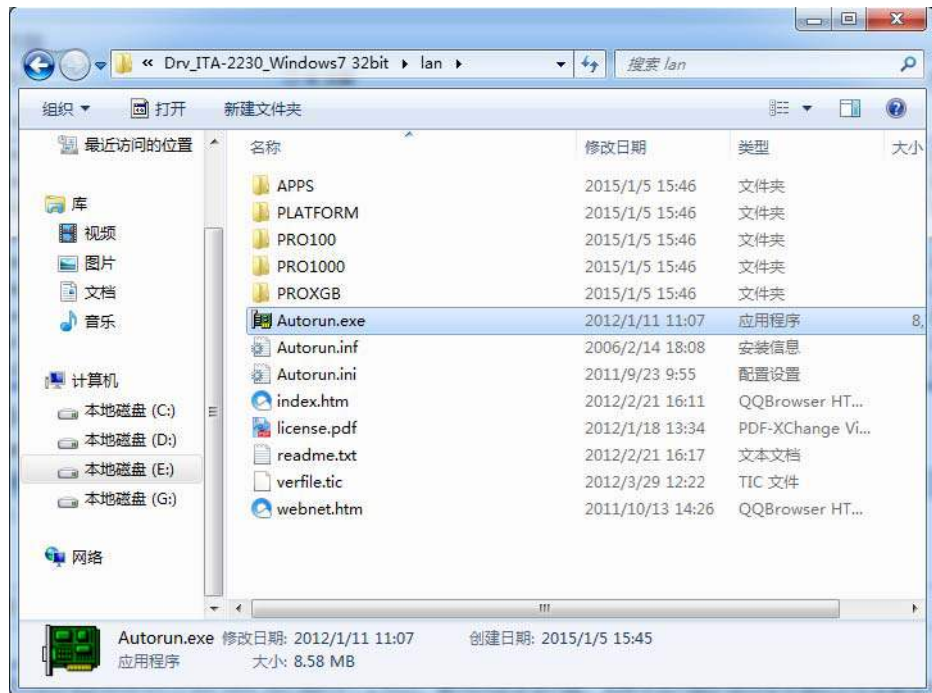
5.2.2 VGA Windows Driver Setup

Insert the driver CD into your system's CD-ROM drive. You can see the ITA-2230 driver folder. Navigate to the "vga" folder and click "Setup.exe" to complete the installation of the driver.



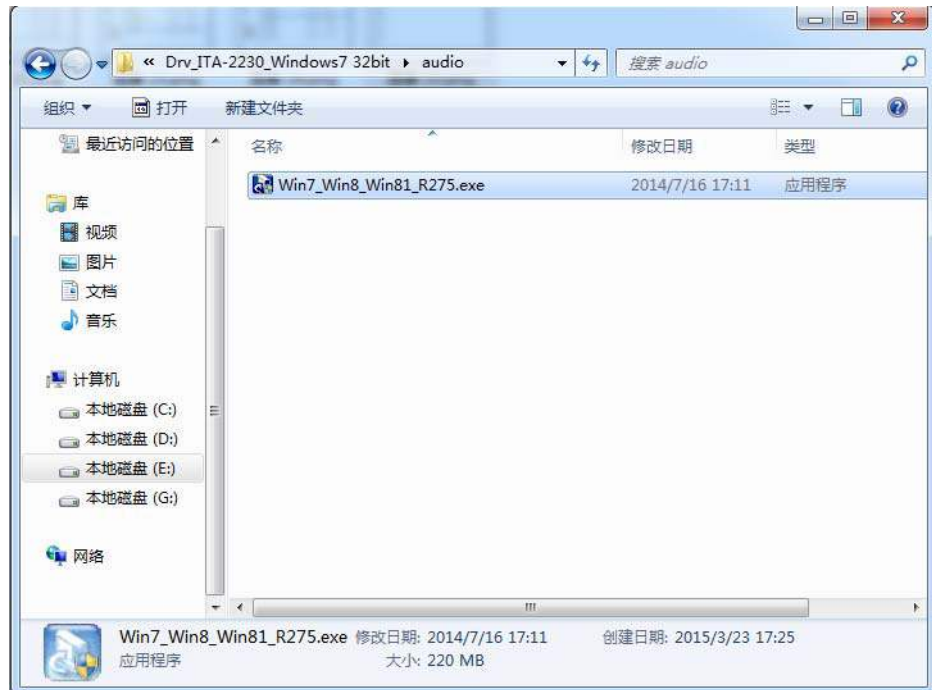
5.2.3 LAN windows Driver Setup

Insert the driver CD into your system's CD-ROM drive. You can see the ITA-2230 driver folder. Navigate to the "lan" folder and click "Autorun.exe" to complete the installation of the driver.



5.2.4 AUDIO windows Driver Setup

Insert the driver CD into your system's CD-ROM drive. You can see the ITA-2230 driver folder. Navigate to the "audio" folder and click "Win7_Win8_Win8_R275.exe" to complete the installation of the driver.



Chapter 6

GPIO Programming Guide

Please carefully read and study the below screenshots and source codes in blue.
Please download specification of NXP Semiconductors PCA9554 for programming.

6.1 ITA-2230 Digital DIO Definition

See Section 2.3.6.

6.2 Configuration Sequence

ITA-2230's GPIO is realized through PCA9554 GPIO IC connected to ICH SMBUS. Therefore, the configuration and access to GPIO IC is completed by IO Space accessing to ICH SMBUS controller.

Below is the diagram of ICH SMBUS IO Space:

SMB_BASE + Offset	Mnemonic	Register Name	Default	Type
00h	HST_STS	Host Status	00h	R/WC, RO, R/WC (special)
02h	HST_CNT	Host Control	00h	R/W, WO
03h	HST_CMD	Host Command	00h	R/W
04h	XMIT_SLVA	Transmit Slave Address	00h	R/W
05h	HST_D0	Host Data 0	00h	R/W
06h	HST_D1	Host Data 1	00h	R/W

For ITA-2230, IO address of the above SMB_BASE is 0xF040.

The detailed SMBUS IO control access code, please refer to Chapter 3.

The corresponding SMBUS slave address of PCA9554 of GPIO 00 - GPIO 07 on ITA-2230 is 0x40 (8bit address):

GPIO 00 – GPIO 07: PCA9554 0x40 (IO0 – IO7)

Below is the sketch of PCA9554:

Table 2. Pin description

Symbol	Pin			Description
	DIP16, SO16, SSOP16, TSSOP16	HVQFN16	SSOP20	
A0	1	15	6	address input 0
A1	2	16	7	address input 1
A2	3	1	9	address input 2
IO0	4	2	10	input/output 0
IO1	5	3	11	input/output 1
IO2	6	4	12	input/output 2
IO3	7	5	14	input/output 3
V _{SS}	8	6 ⁽¹⁾	15	supply ground
IO4	9	7	16	input/output 4
IO5	10	8	17	input/output 5
IO6	11	9	19	input/output 6
IO7	12	10	20	input/output 7
INT	13	11	1	interrupt output (open-drain)

Below is the diagram of PCA9554 register:

6.1.1 Command byte

Table 3. Command byte

Command	Protocol	Function
0	read byte	Input Port register
1	read/write byte	Output Port register
2	read/write byte	Polarity Inversion register
3	read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

PCA9554 has in all 4 registers to control GPIO.

PCA9554 register 0:

6.1.2 Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default 'X' is determined by the externally applied logic level, normally '1' when no external signal externally applied because of the internal pull-up resistors.

Table 4. Register 0 - Input Port register bit description

Bit	Symbol	Access	Value	Description
7	I7	read only	X	determined by externally applied logic level
6	I6	read only	X	
5	I5	read only	X	
4	I4	read only	X	
3	I3	read only	X	
2	I2	read only	X	
1	I1	read only	X	
0	I0	read only	X	

If one GPIO Pin is set to Input, you can read input value from the bit that register 0 corresponds to.

PCA9554 register 1:

6.1.3 Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 5. Register 1 - Output Port register bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	O7	R	1*	reflects outgoing logic levels of pins defined as outputs by Register 3
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

If one GPIO Pin is set to Output, you can read input value from the bit that register 1 corresponds to.

PCA9554 register 2:

6.1.4 Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

Table 6. Register 2 - Polarity Inversion register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	inverts polarity of Input Port register data
6	N6	R/W	0*	0 = Input Port register data retained (default value)
5	N5	R/W	0*	1 = Input Port register data inverted
4	N4	R/W	0*	
3	N3	R/W	0*	
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N0	R/W	0*	

If one GPIO Pin is set to Input, you can control the polarity of input pin from the bit that register 2 corresponds to.

PCA9554 register 3:

6.1.5 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to V_{DD} .

Table 7. Register 3 - Configuration register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	configures the directions of the I/O pins
6	C6	R/W	1*	0 = corresponding port pin enabled as an output
5	C5	R/W	1*	1 = corresponding port pin configured as input
4	C4	R/W	1*	(default value)
3	C3	R/W	1*	
2	C2	R/W	1*	
1	C1	R/W	1*	
0	C0	R/W	1*	

Register 3 is used to set each GPIO as Input or Output:

If the bit is '0', the corresponding GPIO pin is set as Output;

If the bit is '1', the corresponding GPIO pin is set as Input.

Example:

Here take ITA-2230 as an example. Assume GPIO 00 is set as Output and GPIO 7 is set as Input, with two pins interconnected, how to set the corresponding register?

GPIO 00 corresponds to PCA9554 0x40 IO0, while GPIO 07 corresponds to PCA9554 0x40 IO7.

Set GPIO 00 as Output:

1. Read SMBUS slave 0x40 register 3 byte value;
2. Set bit 0 of the value read in step 1 as 0 and write it to SMBUS slave 0x40 register 3;
3. Read SMBUS slave 0x40 register 1 byte value;
4. Set bit 0 of the value read in step 3 as 0 or 1 according to low or high of the output value, then write it back to SMBUS slave 0x40 register 1.

Set GPIO 07 as Input:

1. Read SMBUS slave 0x40 register 3 byte value;
2. Set bit 7 of the value read in step 1 as 1 and write it to SMBUS slave 0x40 register 3;
3. Read SMBUS slave 0x40 register 0 byte value;
4. Decide low or high of the input value through bit7 value read in step3.

6.3 Function call for reference

ICH SMBUS Access Code

(The following code is realized by simulating the access of BIOS to SMBUS. It uses Borand C++ 3.1 for compiling and is successfully tested under DOS (So far, it is not tested under other OSs).

```
#define SMBUS_PORT 0xF040//SMB_BASE?0xF040
```

```
typedef unsigned char BYTE;
```

```
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
```

```
BYTE  smbus_read_byte(BYTE addr, BYTE offset)
```

```
// Read SMBUS Register byte value. Read one byte value each time. addr is slave  
// address (such as 0x40), and offset is register offset.
```

```
{
```

```
    int  i;
```

```
    BYTE data;
```

```
        outportb(SMBUS_PORT + 4, (addr | 1));// Write slave address to  
SMB_BASE + 4 (When reading, bit 0 of slave address should be set as 1, so here  
addr|1 is available)
```

```
        newiodelay();//delay
```

```
        newiodelay();//delay
```

```
        chk_smbus_ready();// Whether SMBUS is ready
```

```
        outportb(SMBUS_PORT + 3, offset);// Write register offset to SMB_BASE +
```

```
3
```



```

        newiodelay();//delay
        newiodelay();//delay

        outportb(SMBUS_PORT + 2, 0x48);// Write SMBUS command to
SMB_BASE + 2. 0x48 means starting byte data transmission
        newiodelay();//delay
        newiodelay();//delay

        for (i = 0; i <= 0x100; i++)
        {
            newiodelay();//longer delay
        }

        chk_smbus_ready();//Whether SMBUS is ready
        return(inportb(SMBUS_PORT + 5));// Byte value read from SMB_BASE + 5
    }

    ///////////////////////////////////////////////////////////////////
void    smbush_write_byte(BYTE addr, BYTE offset, BYTE value)
// Write SMBUS Register byte value. Write one byte value each time. addr is slave
address (such as 0x40), and offset is register offset.
{
    int    i;

        outportb(SMBUS_PORT + 4, addr);// Write slave address to SMB_BASE +
4 (When writing, slave address bit 0 should be set as 0)
        moredelay();//longer delay
        moredelay();//longer delay

        chk_smbus_ready();//Whether SMBUS is ready

        outportb(SMBUS_PORT + 3, offset);// Write register offset to SMB_BASE +
3
        moredelay();//longer delay
        moredelay();//longer delay

        outportb(SMBUS_PORT + 5, value);//Write data value to SMB_BASE + 5
        moredelay();//longer delay
        moredelay();//longer delay

        outportb(SMBUS_PORT + 2, 0x48);// Write SMBUS command to
SMB_BASE + 2.. 0x48 means starting byte data transmission.
        moredelay();//longer delay
        moredelay();//longer delay

        for (i = 0; i <= 0x100; i++)

```

```

    {
        newiodelay();//longer delay
    }

    chk_smbus_ready();//Whether SMBUS is ready
}

/////////////////////////////////////////////////////////////////
int    chk_smbus_ready()
//To decide whether SMBUS is ready or has completed the action, you should wait for
//a long time to check whether SMBUS has successfully transmitted the command.
//Since error may rarely occurs, BIOS code does not make judgement on the return
//value of this function in read and write of SMBUS byte.
{
    int    i, result = 1;
    BYTE data;

    for (i = 0; i <= 0x800; i++)
    {
        //SMB_BASE + 0 is SMBUS status value
        data = inportb(SMBUS_PORT);//Read SMBUS status value once
        data = check_data(SMBUS_PORT);//Read SMBUS status value sev-
        eral timesoutportb(SMBUS_PORT, data);//Write back SMBUS status value which
        will clear status value (Write 1 to the corresponding bit means clearing status)

        if (data & 0x02)
        {
            //If bit 1 is set (which means the command is completed),
            SMBUS is ready
            result = 0;//SMBUS ready
            break;
        }

        if (!(data & 0xBF))
        {
            //If all bits are 0 except bit 2 (which means error occurs on
            SMBUS), SMBUS is ready
            result = 0;//SMBUS ready
            break;
        }

        if (data & 0x04)
        {
            //If bit 2 is set (which means error occurs on SMBUS), error
            occurs on SMBUS which is rarely the case
            result = 1;//SMBUS error
            break;
        }
    }
}

```

```

        returnresult;
    }

    ///////////////////////////////////////////////////////////////////
    BYTE  check_data(WORD addr)
    {
        int  i;
        BYTE data;

        for(i = 0; i <= 6; i++)
        {
            data = inportb(addr);
            if (data != 0)
                break;
        }

        returndata;
    }

    ///////////////////////////////////////////////////////////////////
    void  newiodelay()
    //Shorter delay
    {
        outportb(0xeb, 0); //IO port 0xeb No real device occupies. Write a value to
        this port can realize delay function. You can also choose other method according to
        the real situation.
    }

    ///////////////////////////////////////////////////////////////////
    void  moredelay()
    //Longer delay
    {
        int  i;
        for (i = 0; i < 20; i++)
        {
            outportb(0xeb, 0); //IO port 0xeb No real device occupies. Write a
            value to this port can realize delay function. You can also choose other method
            according to the real situation.
        }
    }
}

```

GPIO Simcodes

(Here GPIO 00 and GPIO 07 in Chapter 2 are taken as examples)

Output High to GPIO 00:

```
data = smbus_read_byte(0x40, 0x03); // Read slave 0x40 register 3 byte
```

```
data &= 0xfe;//bit 0 is set as 0
smbus_write_byte(0x40, 0x03, data)//Write back. GPIO 00 is set for output
data = smbus_read_byte(0x40, 0x01)//Read slave 0x40 register 1
data |= 0x01;//bit 0 is set as 1 which stands for high
smbus_write_byte(0x40, 0x01, data)//Write back. Output high value
```

Read Input Value from GPIO 07:

```
data = smbus_read_byte(0x40, 0x03);//Read slave 0x40 register 3 byte
data |= 0x80;//bit 7??1
smbus_write_byte(0x40, 0x03, data)//Write back. GPIO 07 is set for input
data = smbus_read_byte(0x40, 0x00)//Read slave 0x40 register 0. Then,
the response value of bit 7 should know whether the input is low or high
```

Appendix **A**

Programming the Watchdog Timer

A.1 Programming the Watchdog Timer

The ITA-2230's watchdog timer can be used to monitor system software operation and take corrective action if the software fails to function within the programmed period. This section describes the operation of the watchdog timer and how to program it.

A.1.1 Watchdog Timer Overview

The watchdog timer is built into the super I/O controller SMSC SCH3114. It provides the following user-programmable functions:

- Can be enabled or disabled via user program
- Timer can be set from 1 to 255 seconds or 1 to 255 minutes
- Generates an interrupt or resets signal if the software fails to reset the timer before time-out

A.1.2 Programming the Watchdog Timer

The I/O port address of the watchdog timer is 680h (hex).

Table A.1: Watchdog Timer Registers

Address: 680h (hex)		
Register Shift	Read/Write	Description
65 (hex)	write	Set seconds or minutes as units for the timer. Write 0 to bit 7: set second as counting unit. [default] Write 1 to bit 7: set minutes as counting unit.
66 (hex)	write	0: Stop timer [default] 01~FF (hex): The amount of the count, in seconds or minutes, depends on the value set in register 65 (hex). This number decides how long the watchdog timer waits for strobe before generating an interrupt or reset signal. Writing a new value to this register can reset the timer to count with the new value.
67 (hex)	read/write	Configure watchdog timer Bit 1: Write 1 to enable keyboard to reset the timer, 0 to disable. [default] Bit 2: Write 1 to enable mouse to reset the timer, 0 to disable. [default] Bit 7~4: Set the interrupt mapping of watchdog timer: 1111=IRQ15 0011=IRQ3 0010=IRQ2 0001=IRQ1 0000=Disable [default]
68 (hex)	read/write	Control watchdog timer Bit0: Read watchdog state; 1=Timer timeout Bit2: Write 1 to immediately generate timeout signal, and automatically return to 0 (Write only). Bit3: Write 1 to allow triggering of timer timeout when P20 is effective, 0 to disable. [default]

A.1.3 Example Program

```

;-----
1. Enable watchdog timer and set 10 sec. as timeout interval
;-----
Mov dx,A65h ; Select register 65h, watchdog timer I/O port address 680h+ register
shifts 65h
Mov al,80h ; Set second as counting unit
Out dx,al

Mov dx,A66h ; Select register 66h, watchdog timer I/O port address 680h+ register
shift 66h
Mov al,10 ; Set timeout interval as 10 seconds and start counting
Out dx,al

;-----
2. Enable watchdog timer and set 5 min. as timeout interval
;-----
Mov dx,A65h ; Select register 65h, watchdog timer I/O port address 680h+ register
shifts 65h
Mov al,00h ; Set minute as counting unit
Out dx,al
680h
Mov dx,A66h ; Select register 66h, watchdog timer I/O port address 680h+ register
shifts 66h
Mov al,5 ;Set timeout interval as 5 minutes and start counting
Out dx,al

;-----
3. Enable watchdog timer to be reset by mouse
;-----
Mov dx,A67h ; Select register 67h, watchdog timer I/O port address 680h+ register
shifts 67h
In al,dx
Or al,4h ; Enable watchdog timer to be reset by mouse
Out dx,al

;-----
4. Enable watchdog timer to be reset by keyboard
;-----
Mov dx,A67h ; Select register 67h, watchdog timer I/O port address 680h+ register
shifts 67h
In al,dx
Or al,2h ; Enable watchdog timer to be reset by keyboard
Out dx,al

;-----
5. Generate a time-out signal without timer counting
;-----
Mov dx,A68h ; Select register 68h, watchdog timer I/O port address 680h+ register
shifts 68h
In al,dx
Or al,4h ; Generate a time-out signal
Out dx,al
;-----

```

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