DRV8436 Stepper Driver With Integrated Current Sense, 1/256 Microstepping, STEP/DIR Interface and Smart Tune Technology

1 Features

- PWM microstepping stepper motor driver
  - Simple STEP/DIR interface
  - Up to 1/256 Microstepping indexer
- Integrated current sense functionality
  - No sense resistors required
  - ±7.5% Full-scale current accuracy
- Smart tune decay technology, Fixed slow, and mixed decay options
- 4.5 to 48-V Operating supply voltage range
- Low $R_{DS(ON)}$: 900 mΩ HS + LS at 24 V, 25°C
- High current capacity per bridge: 2.4 A peak, 1.5 A Full-Scale, 1.1 A rms
- Configurable off-time PWM chopping
  - 7-µs, 16-µs, 24-µs, or 32-µs.
- Supports 1.8-V, 3.3-V, 5.0-V logic inputs
- Low-current sleep mode (2 µA)
- Small package and footprint
- Protection features
  - VM undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)
  - Fault condition output (nFAULT)

2 Applications

- Multi-purpose printers and scanners
- 3D printers and laser beam printers
- Automatic teller and money handling machines
- Textile and sewing machines
- Stage lighting equipment
- CCTV, security and dome cameras
- Office and home automation
- Factory automation and robotics

3 Description

The DRV8436 is a stepper motor driver for industrial and consumer end equipment applications. The device is fully integrated with two N-channel power MOSFET H-bridge drivers, a microstepping indexer, and integrated current sensing. The DRV8436 is capable of driving up to 1.1-A rms (dependent on PCB design).

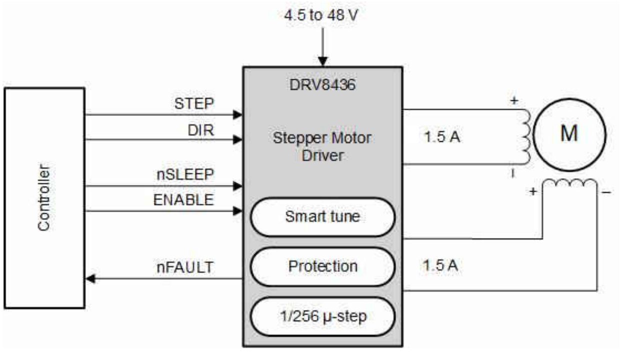
The DRV8436 uses an internal current sense architecture to eliminate the need for two external power sense resistors, saving PCB area and system cost. The device uses an internal PWM current regulation scheme selectable between smart tune, slow and mixed decay options. Smart tune decay technology automatically adjusts for optimal current regulation performance and compensates for motor variation and aging effects.

A simple STEP/DIR interface allows an external controller to manage the direction and step rate of the stepper motor. A low-power sleep mode is provided for very low standby quiescent standby current using a dedicated nSLEEP pin. Protection features are provided for supply undervoltage, charge pump faults, overcurrent, short circuits, and overtemperature. Fault conditions are indicated by the nFAULT pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8436PWPR	HTSSOP (28)	9.7 mm x 4.4 mm
DRV8436RGER	VQFN (24)	4.0 mm x 4.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2020) to Revision B (May 2022)	Page
• Added Application Curves	35
• Updated HTSSOP and QFN layout example	39
• Added Related Documentation section	41

Changes from Revision * (June 2020) to Revision A (August 2020)	Page
• Updated device status to "Production Data"	1

5 Pin Configuration and Functions

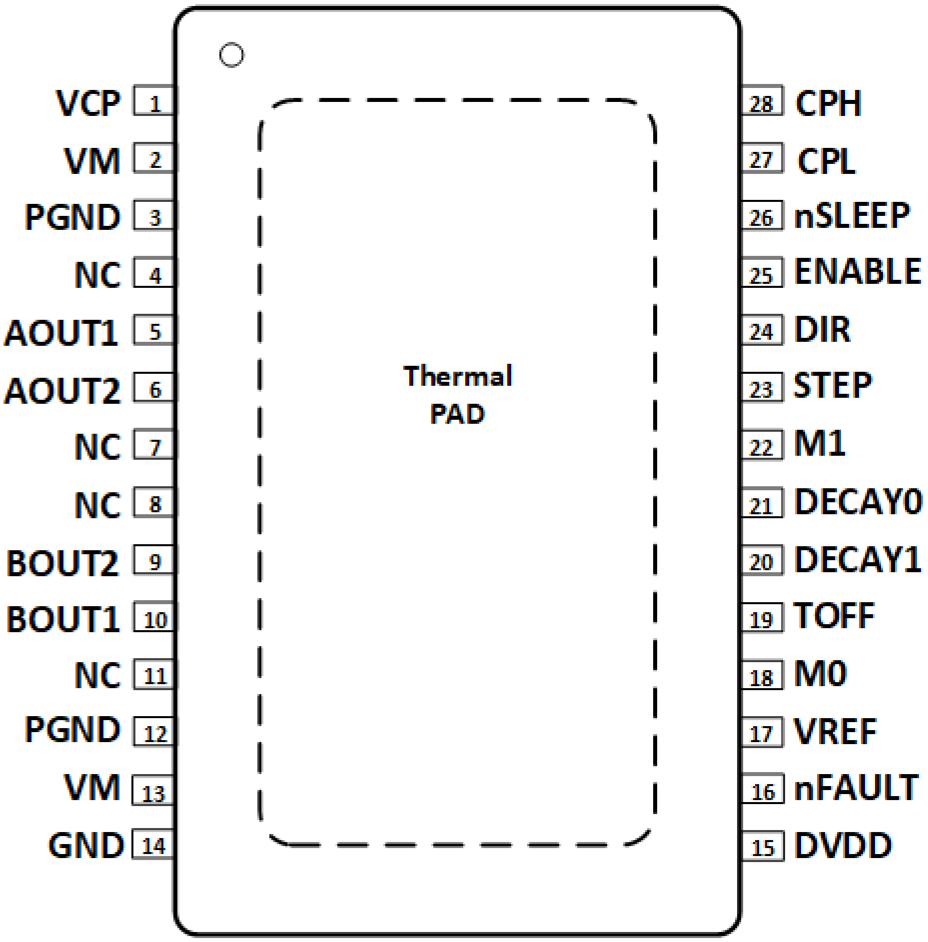


Figure 5-1. PWP PowerPAD™ Package 28-Pin HTSSOP Top View

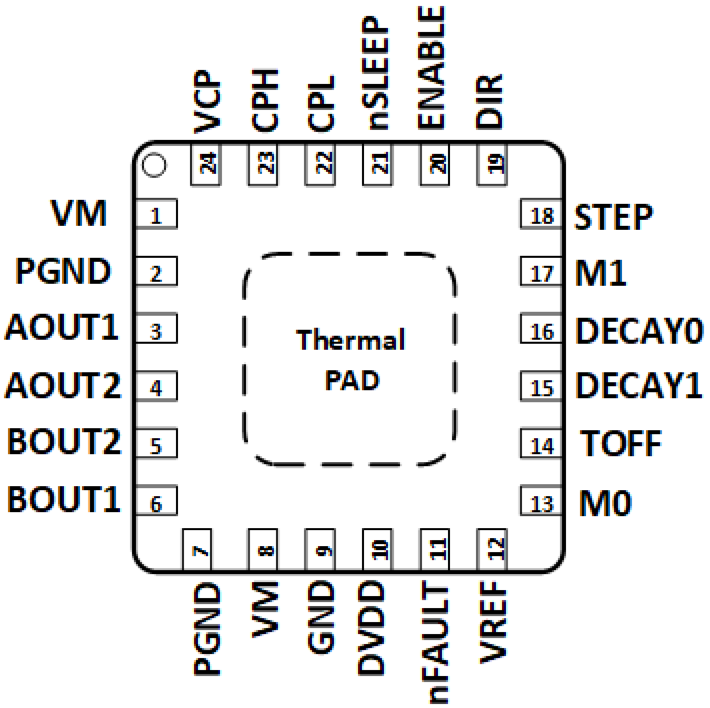


Figure 5-2. RGE Package 24-Pin VQFN with Exposed Thermal PAD Top View

5.1 Pin Functions

PIN			I/O	TYPE	DESCRIPTION
NAME	NO.				
	HTSSOP	VQFN			
AOUT1	5	3	O	Output	Winding A output. Connect to motor winding.
AOUT2	6	4	O	Output	Winding A output. Connect to motor winding.
PGND	3, 12	2, 7	—	Power	Power ground. Both PGND pins are shorted internally. Connect to system ground on PCB.
BOUT2	9	5	O	Output	Winding B output. Connect to motor winding.
BOUT1	10	6	O	Output	Winding B output. Connect to motor winding.
CPH	28	23	—	Power	Charge pump switching node. Connect a X7R, 0.022-μF, VM-rated ceramic capacitor from CPH to CPL.
CPL	27	22			
DIR	24	19	I	Input	Direction input. Logic level sets the direction of stepping; internal pulldown resistor.
ENABLE	25	20	I	Input	Logic low to disable device outputs; logic high to enable; internal pullup to DVDD. Also determines the type of OCP response.
DVDD	15	10		Power	Logic supply voltage. Connect a X7R, 0.47-μF to 1-μF, 6.3-V or 10-V rated ceramic capacitor to GND.
GND	14	9	—	Power	Device ground. Connect to system ground.
VREF	17	12	I	Input	Current set reference input. Maximum value 3.3 V. DVDD can be used to provide VREF through a resistor divider.
M0	18	13	I	Input	Microstepping mode-setting pins. Sets the step mode; internal pulldown resistor.
M1	22	17			
DECAY0	21	16	I	Input	Decay-mode setting pins. Sets the decay mode (see the Section 7.3.6 section).
DECAY1	20	15			
STEP	23	18	I	Input	Step input. A rising edge causes the indexer to advance one step; internal pulldown resistor.
VCP	1	24	—	Power	Charge pump output. Connect a X7R, 0.22-μF, 16-V ceramic capacitor to VM.

PIN			I/O	TYPE	DESCRIPTION
NAME	NO.				
	HTSSOP	VQFN			
VM	2, 13	1, 8	—	Power	Power supply. Connect to motor supply voltage and bypass to GND with two 0.01-μF ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.
TOFF	19	14	I	Input	Sets the Decay mode off time during current chopping; four level pin.
nFAULT	16	11	O	Open Drain	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nSLEEP	26	21	I	Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.
NC	4, 7, 8, 11	-	-	-	No Connect pins. Leave these pins unconnected.
PAD	-	-	-	-	Thermal pad. Connect to system ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	50	V
Charge pump voltage (VCP, CPH)	–0.3	V_{VM} + 7	V
Charge pump negative switching pin (CPL)	–0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
Control pin voltage (STEP, DIR, ENABLE, nFAULT, DECAY0, DECAY1, TOFF, M0, M1)	–0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (VREF)	–0.3	5.75	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3	V_{VM} + 3	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	Corner pins for PWP (1, 14, 15, and 28)	±750	
			Other pins	±500	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	48	V
V_I	Logic level input voltage	0	5.5	V
V_{VREF}	VREF voltage	0.05	3.3	V
f_{PWM}	Applied STEP signal (STEP)	0	500(1)	kHz
I_{FS}	Motor full-scale current (xOUTx)	0	1.5(2)	A
I_{rms}	Motor RMS current (xOUTx)	0	1.1(2)	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load
(2) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC(1)		PWP (HTSSOP)	RGE (VQFN)	UNIT
		28 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.3	41.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.0	32.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	18.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.5	18.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	4.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	ENABLE = 1, nSLEEP = 1, No motor load		5	7	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	μA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	75			μs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	18		35	μs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.6	0.9	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.6	0.9	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 45 V	4.5	5	5.5	V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage			V_{VM} + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		400		kHz
LOGIC-LEVEL INPUTS (STEP, DIR, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	μA
I_{IH}	Input logic-high current	V_{IN} = 5 V			50	μA
TRI-LEVEL INPUTS (M0, DECAY0, DECAY1, ENABLE)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I3}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		μA
QUAD-LEVEL INPUTS (M1, TOFF)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}		330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_{IL}	Output pull-up current			10		μA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.4	V
I_{OH}	Output logic-high leakage	V_{VM} = 24 V	–1		1	μA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ONH)}$	High-side FET on resistance	T_J = 25°C, I_O = -1 A		450	550	mΩ
		T_J = 125°C, I_O = -1 A		700	850	mΩ
		T_J = 150°C, I_O = -1 A		780	950	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance	T_J = 25°C, I_O = 1 A		450	550	mΩ
		T_J = 125°C, I_O = 1 A		700	850	mΩ
		T_J = 150°C, I_O = 1 A		780	950	mΩ
t_{SR}	Output slew rate	V_{VM} = 24 V, I_O = 0.5 A, Between 10% and 90%		150		V/μs
PWM CURRENT CONTROL (VREF)						
K_V	Transimpedance gain	VREF = 3.3V		2.2		V/A

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFF}	PWM off-time	TOFF = 0		7		μs
		TOFF = 1		16		
		TOFF = Hi-Z		24		
		TOFF = 330 kΩ to GND		32		
ΔI_{TRIP}	Current trip accuracy	I_O = 1.5 A, 10% to 20% current setting	–13		10	%
		I_O = 1.5 A, 20% to 67% current setting	–8		8	
		I_O = 1.5 A, 67% to 100% current setting	–7.5		7.5	
$I_{O,CH}$	AOUT and BOUT current matching	I_O = 1.5 A	–2.5		2.5	%
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	4.15	4.25	4.35	V
		VM rising, UVLO rising	4.25	4.35	4.45	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET	2.4			A
t_{OCP}	Overcurrent deglitch time	V_{VM} < 37V		3		μs
		V_{VM} >= 37V		0.5		
t_{RETRY}	Overcurrent retry time			4		ms
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

6.6 Indexer Timing Requirements

Typical limits are at T_J = 25°C and V_{VM} = 24 V. Over recommended operating conditions unless otherwise noted.

NO.			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		500[1]	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	970		ns
3	$t_{WL(STEP)}$	Pulse duration, STEP low	970		ns
4	$t_{SU(DIR, Mx)}$	Setup time, DIR or MODEx to STEP rising	200		ns
5	$t_{H(DIR, Mx)}$	Hold time, DIR or MODEx to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.

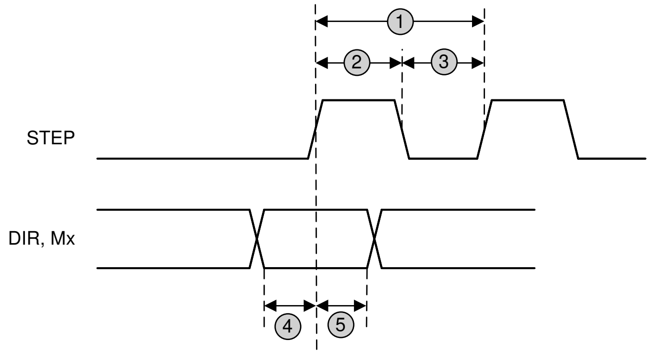


Figure 6-1. Timing Diagram

6.7 Typical Characteristics

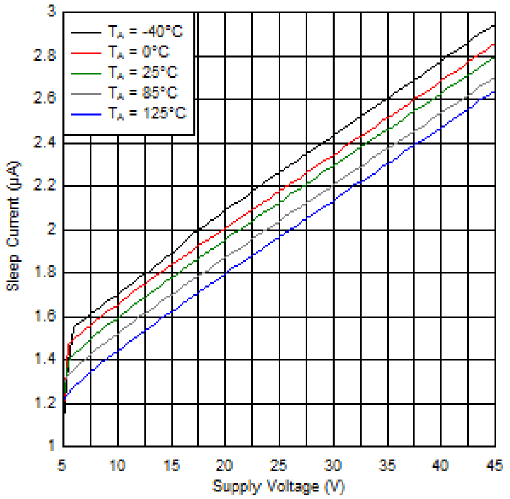


Figure 6-2. Sleep Current over VM

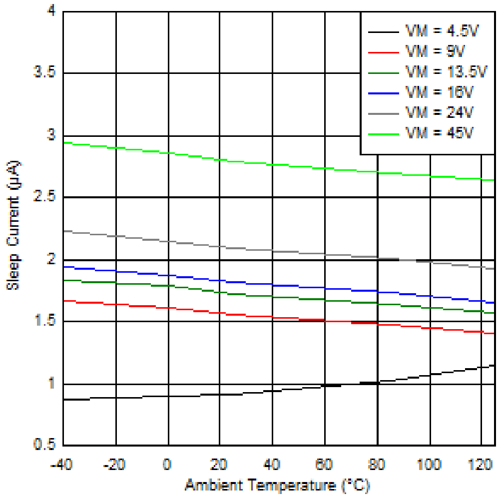


Figure 6-3. Sleep Current over Temperature

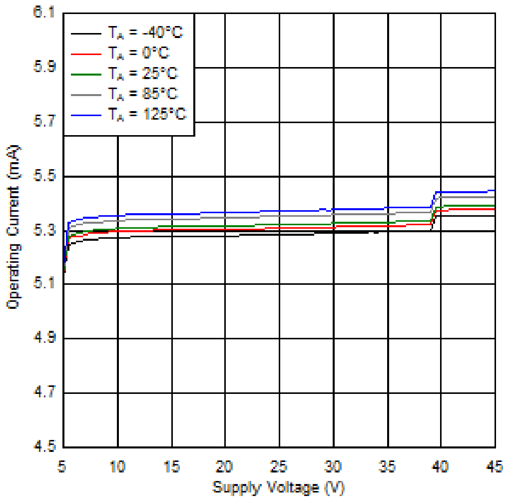


Figure 6-4. Operating Current over VM

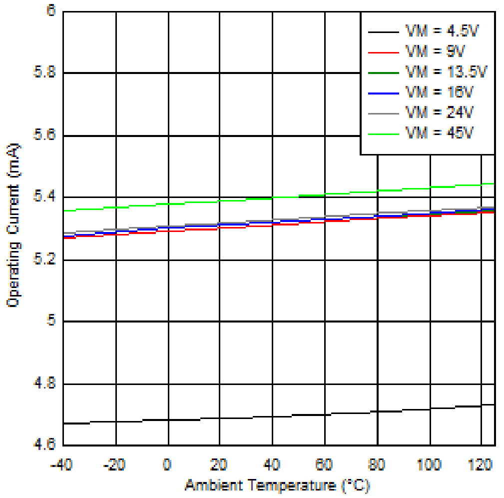


Figure 6-5. Operating Current over Temperature

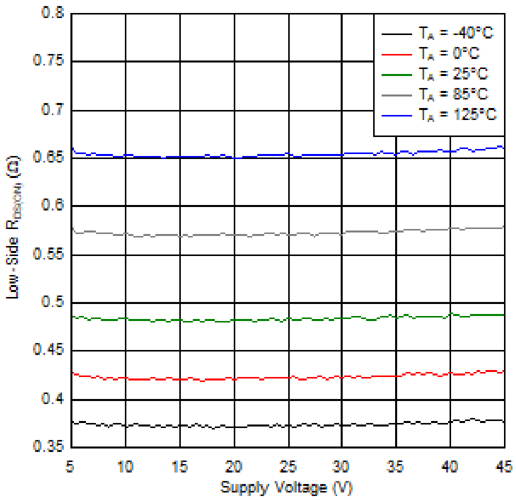


Figure 6-6. Low-Side $R_{DS(ON)}$ over VM

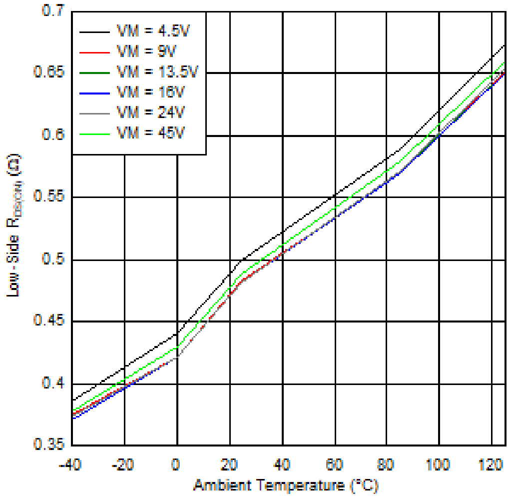


Figure 6-7. Low-Side $R_{DS(ON)}$ over Temperature

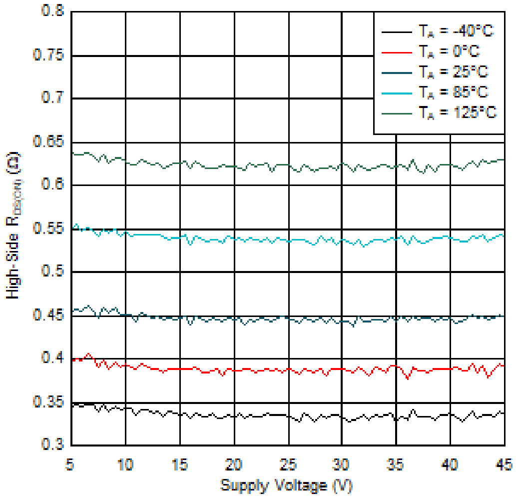


Figure 6-8. High-Side $R_{DS(ON)}$ over VM

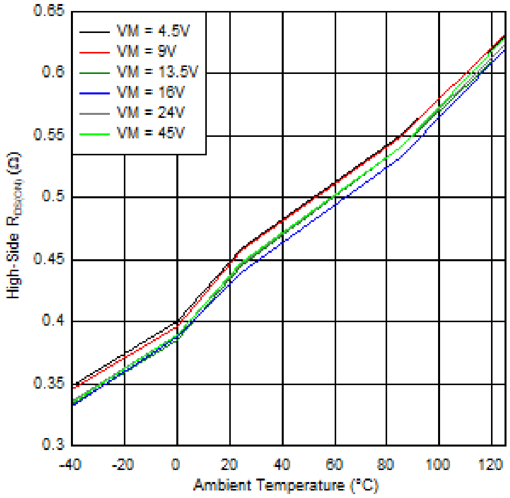


Figure 6-9. High-Side $R_{DS(ON)}$ over Temperature

7 Detailed Description

7.1 Overview

The DRV8436 device is an integrated motor-driver solutions for bipolar stepper motors. The device integrates two N-channel power MOSFET H-bridges, integrated current sense and regulation circuitry, and a microstepping indexer. The DRV8436 device can be powered with a supply voltage from 4.5 to 48 V. The device is capable of providing an output current up to 2.4-A peak, 1.5-A full-scale, or 1.1-A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The DRV8436 device uses an integrated current-sense architecture which eliminates the need for two external power sense resistors. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted by the voltage at the VREF pin. This features reduces external component cost, board PCB size, and system power consumption.

A simple STEP/DIR interface allows for an external controller to manage the direction and step rate of the stepper motor. The internal indexer can execute high-accuracy micro-stepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping. In addition to a standard half stepping mode, a non-circular half stepping mode is available for increased torque output at higher motor RPM.

The current regulation is configurable between several decay modes. The decay mode can be selected as a slow-mixed, mixed decay, smart tune Ripple Control, or smart tune Dynamic Decay current regulation scheme. The slow-mixed decay mode uses slow decay on increasing steps and mixed decay on decreasing steps. The smart tune decay modes automatically adjust for optimal current regulation performance and compensate for motor variation and aging effects. Smart tune Ripple Control uses a variable off-time, ripple control scheme to minimize distortion of the motor winding current. Smart tune Dynamic Decay uses a fixed off-time, dynamic decay percentage scheme to minimize distortion of the motor winding current while also minimizing frequency content.

A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

7.2 Functional Block Diagram

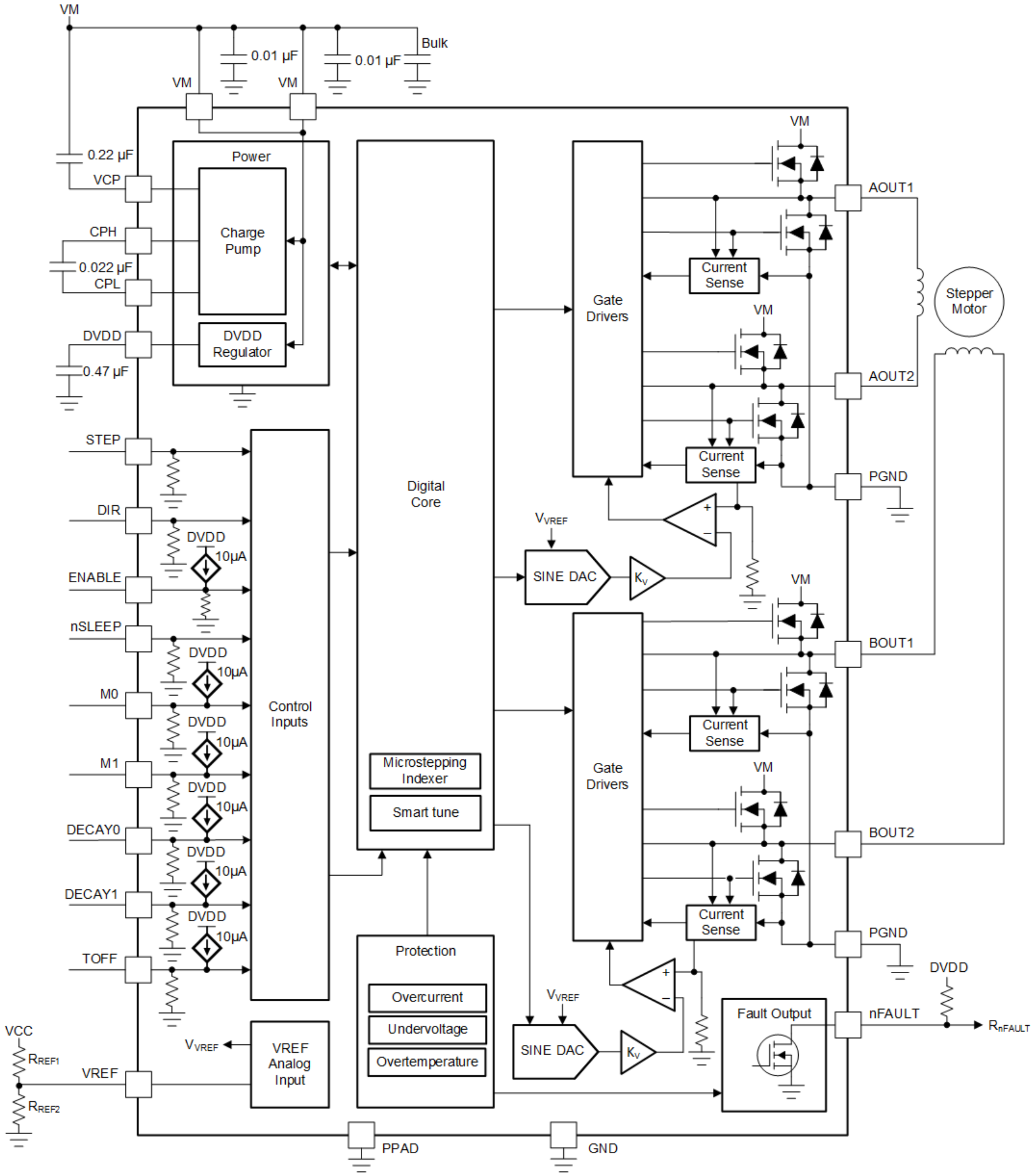


Figure 7-1.

7.3 Feature Description

Table 7-1 lists the recommended external components for the DRV8436 device.

Table 7-1. DRV8436 External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	Two X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	GND	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 0.22-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.022-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47-µF to 1-µF, 6.3-V ceramic capacitor
R_{nFAULT}	VCC (1)	nFAULT	>4.7-kΩ resistor
R_{REF1}	VREF	VCC	Resistor to limit chopping current. It is recommended that the value of parallel combination of R_{REF1} and R_{REF2} should be less than 50-kΩ.
R_{REF2} (Optional)	VREF	GND	

(1) VCC is not a pin on the DRV8436 device, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD

7.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, rms, and full-scale.

7.3.1.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold I_{OCP}. The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver. For the DRV8436 device, the peak current rating is 2.4 A per bridge.

7.3.1.2 rms Current Rating

The rms (average) current is determined by the thermal considerations of the IC. The rms current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The actual operating rms current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8436 device, the rms current rating is 1.1 A per bridge.

7.3.1.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the rms current, the full-scale current is also determined by the thermal considerations of the device. The full-scale current rating is approximately $\sqrt{2} \times I_{RMS}$. For the DRV8436 device, the full-scale current rating is 1.5 A per bridge.

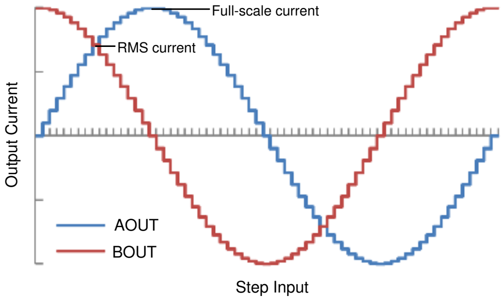


Figure 7-2. Full-Scale and RMS Current

7.3.2 PWM Motor Drivers

The DRV8436 device has drivers for two full H-bridges to drive the two windings of a bipolar stepper motor. Figure 7-3 shows a block diagram of the circuitry.

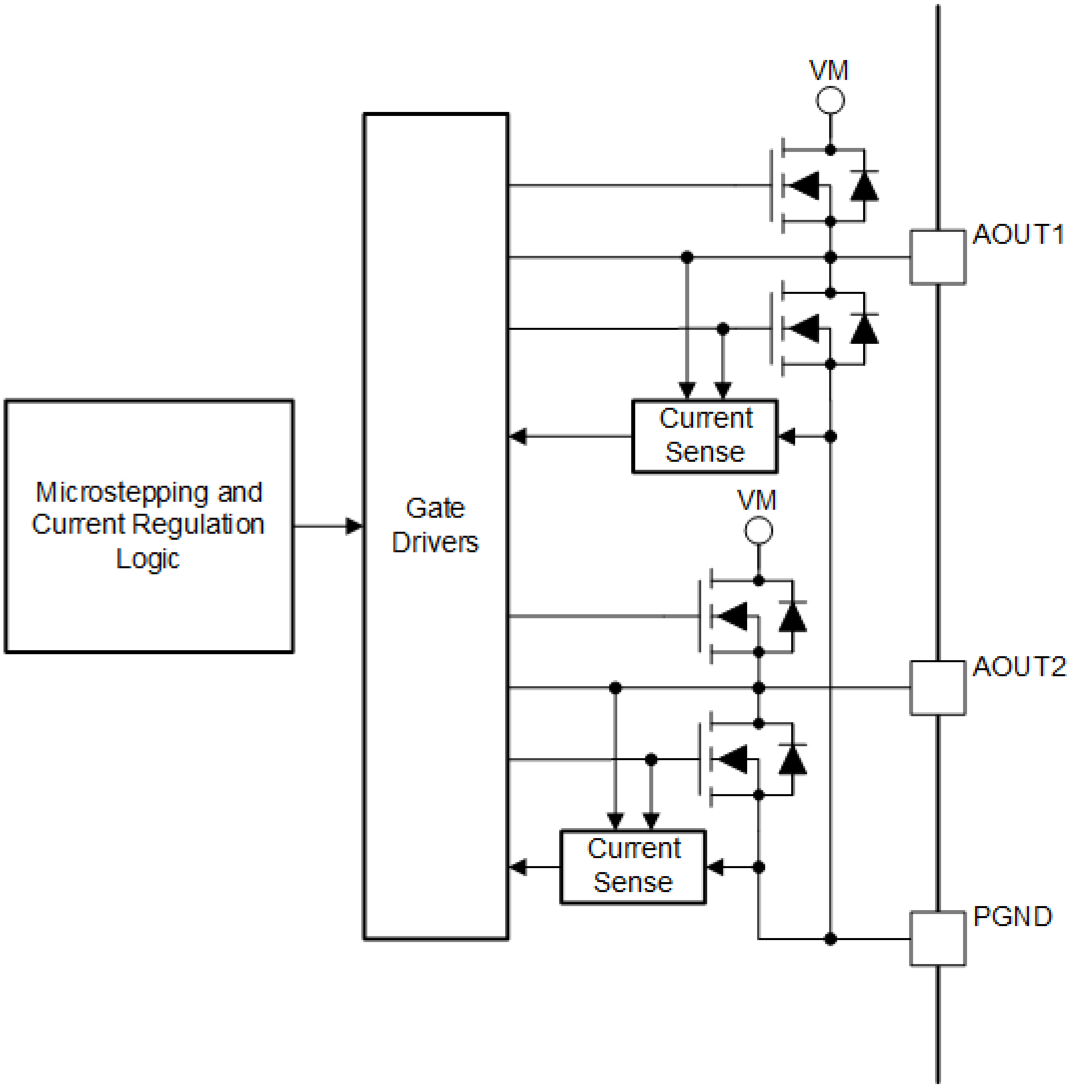


Figure 7-3. PWM Motor Driver Block Diagram

7.3.3 Microstepping Indexer

Built-in indexer logic in the DRV8436 device allows a number of different step modes. The M0 and M1 pins are used to configure the step mode as shown in Table 7-2. The settings can be changed on the fly.

Table 7-2. Microstepping Settings

M0	M1	STEP MODE
0	0	Full step (2-phase excitation) with 100% current
0	330 kΩ to GND	Full step (2-phase excitation) with 71% current
1	0	Non-circular 1/2 step
Hi-Z	0	1/2 step
0	1	1/4 step
1	1	1/8 step

Table 7-2. Microstepping Settings (continued)

M0	M1	STEP MODE
Hi-Z	1	1/16 step
0	Hi-Z	1/32 step
Hi-Z	330 kΩ to GND	1/64 step
Hi-Z	Hi-Z	1/128 step
1	Hi-Z	1/256 step

Table 7-3 shows the relative current and step directions for full-step (71% current), 1/2 step, 1/4 step and 1/8 step operation. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle and the BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from the xOUT1 pin to the xOUT2 pin while driving.

At each rising edge of the STEP input the indexer travels to the next state in the table. The direction is shown with the DIR pin logic high. If the DIR pin is logic low, the sequence is reversed.

Note

If the step mode is changed on the fly while stepping, the indexer advances to the next valid state for the new step mode setting at the rising edge of STEP.

Note

While DIR = 0 and the electrical angle is at a full step angle (45, 135, 225, or 315 degrees), two rising edge pulses on the STEP pin are required in order to advance the indexer after changing from any microstep mode to the full step mode. The first pulse will induce no change in the electrical angle, the second pulse will move the indexer to the next full step angle.

The home state is an electrical angle of 45°. This state is entered after power-up, after exiting logic undervoltage lockout, or after exiting sleep mode.

Table 7-3. Relative Current and Step Directions

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	1	1		0%	100%	0.00
2				20%	98%	11.25
3	2			38%	92%	22.50
4				56%	83%	33.75
5	3	2	1	71%	71%	45.00
6				83%	56%	56.25
7	4			92%	38%	67.50
8				98%	20%	78.75
9	5	3		100%	0%	90.00
10				98%	-20%	101.25
11	6			92%	-38%	112.50
12				83%	-56%	123.75
13	7	4	2	71%	-71%	135.00
14				56%	-83%	146.25
15	8			38%	-92%	157.50
16				20%	-98%	168.75
17	9	5		0%	-100%	180.00

Table 7-3. Relative Current and Step Directions (continued)

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
18				-20%	-98%	191.25
19	10			-38%	-92%	202.50
20				-56%	-83%	213.75
21	11	6	3	-71%	-71%	225.00
22				-83%	-56%	236.25
23	12			-92%	-38%	247.50
24				-98%	-20%	258.75
25	13	7		-100%	0%	270.00
26				-98%	20%	281.25
27	14			-92%	38%	292.50
28				-83%	56%	303.75
29	15	8	4	-71%	71%	315.00
30				-56%	83%	326.25
31	16			-38%	92%	337.50
32				-20%	98%	348.75

Table 7-4 shows the full step operation with 100% full-scale current. This stepping mode consumes more power than full-step mode with 71% current, but provides a higher torque at high motor RPM.

Table 7-4. Full Step with 100% Current

FULL STEP 100%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	100	100	45
2	100	-100	135
3	-100	-100	225
4	-100	100	315

Table 7-5 shows the noncircular 1/2–step operation. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

Table 7-5. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2-STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	–100	135
5	0	–100	180
6	–100	–100	225
7	–100	0	270
8	–100	100	315

7.3.4 Controlling VREF with an MCU DAC

In some cases, the full-scale output current may need to be changed between many different values, depending on motor speed and loading. The voltage of the VREF pin can be adjusted in the system to change the full-scale current.

In this mode of operation, as the DAC voltage increases, the full-scale regulation current increases as well. For proper operation, the output of the DAC should not rise above 3.3 V.

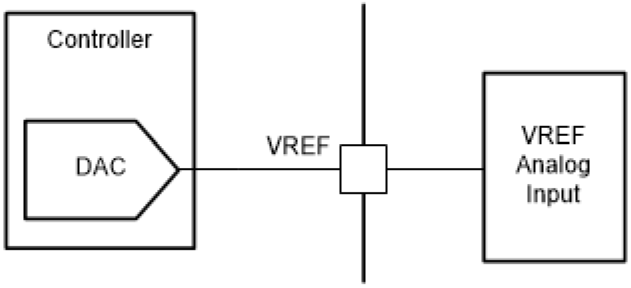


Figure 7-4. Controlling VREF with a DAC Resource

The VREF pin can also be adjusted using a PWM signal and low-pass filter.

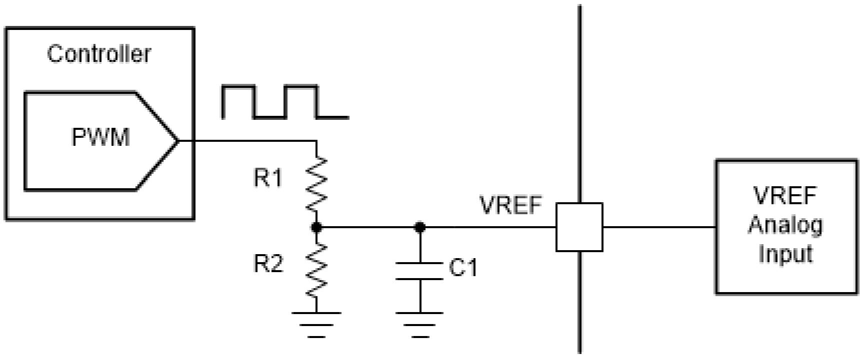


Figure 7-5. Controlling VREF With a PWM Resource

7.3.5 Current Regulation

The current through the motor windings is regulated by an adjustable, off-time PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for a period of time determined by the TOFF pin setting to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

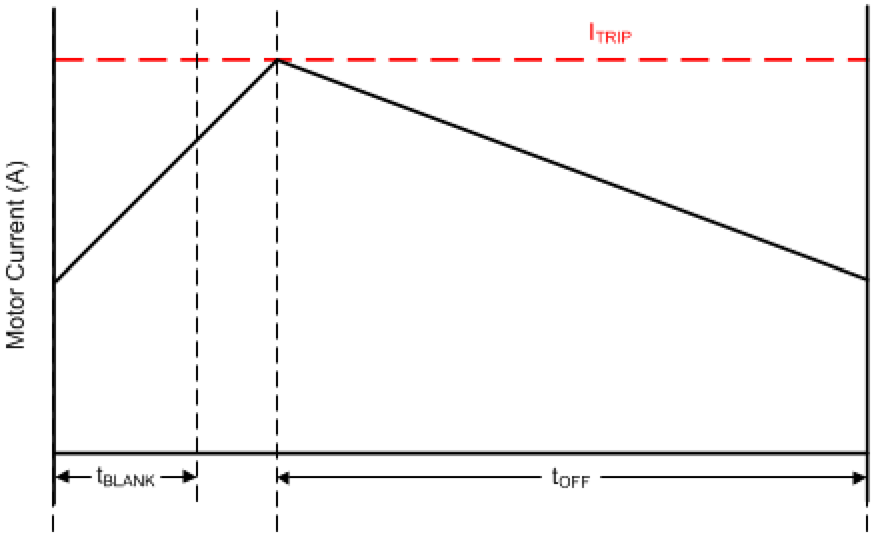


Figure 7-6. Current Chopping Waveform

The PWM regulation current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. The current sense MOSFETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the voltage at the VREF pin.

The full-scale regulation current (I_{FS}) can be calculated as I_{FS} (A) = V_{REF} (V) / K_V (V/A) = V_{REF} (V) / 2.2 (V/A).

7.3.6 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7-7, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. Fast decay mode is shown in Figure 7-7, item 2. In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 7-7, Item 3.

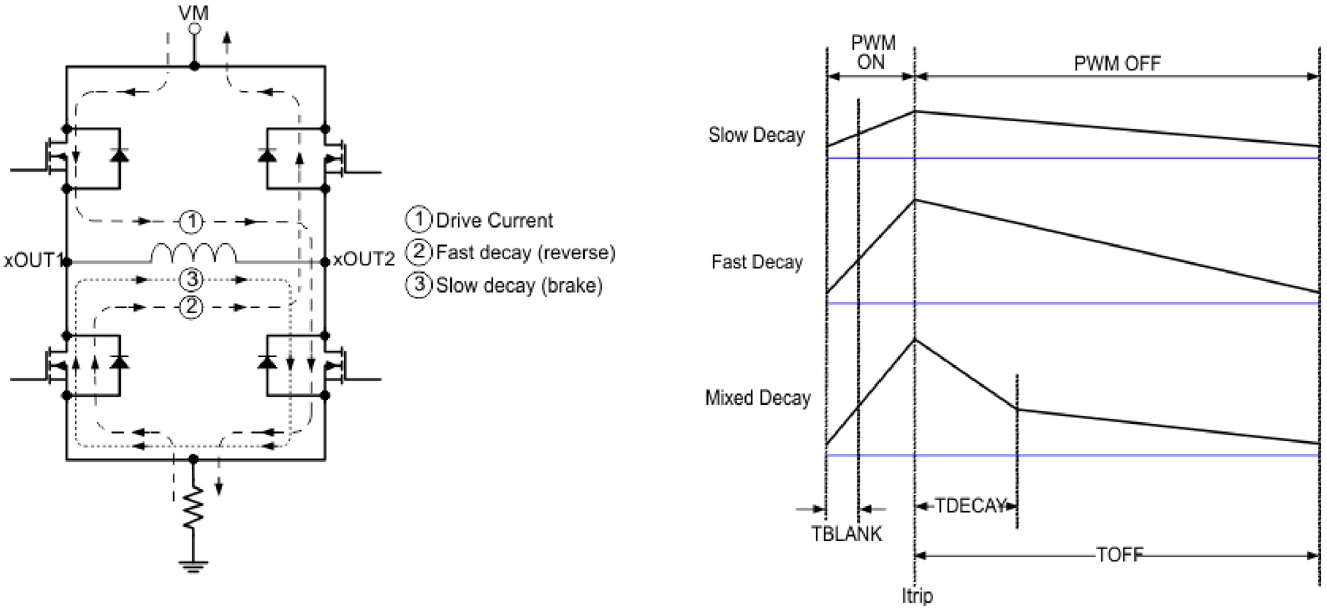


Figure 7-7. Decay Modes

The decay mode of the DRV8436 is selected by the DECAY0 and DECAY1 pins as shown in Table 7-6. The decay modes can be changed on the fly.

Table 7-6. Decay Mode Settings

DECAY0	DECAY1	INCREASING STEPS	DECREASING STEPS
0	0	Smart tune Dynamic Decay	Smart tune Dynamic Decay
0	1	Smart tune Ripple Control	Smart tune Ripple Control
1	0	Mixed decay: 30% fast	Mixed decay: 30% fast
1	1	Slow decay	Mixed decay: 30% fast
Hi-Z	0	Mixed decay: 60% fast	Mixed decay: 60% fast
Hi-Z	1	Slow decay	Slow decay

Figure 7-8 defines increasing and decreasing current. For the slow-mixed decay mode, the decay mode is set as slow during increasing current steps and mixed decay during decreasing current steps. In full step and noncircular 1/2-step operation, the decay mode corresponding to decreasing steps is always used.

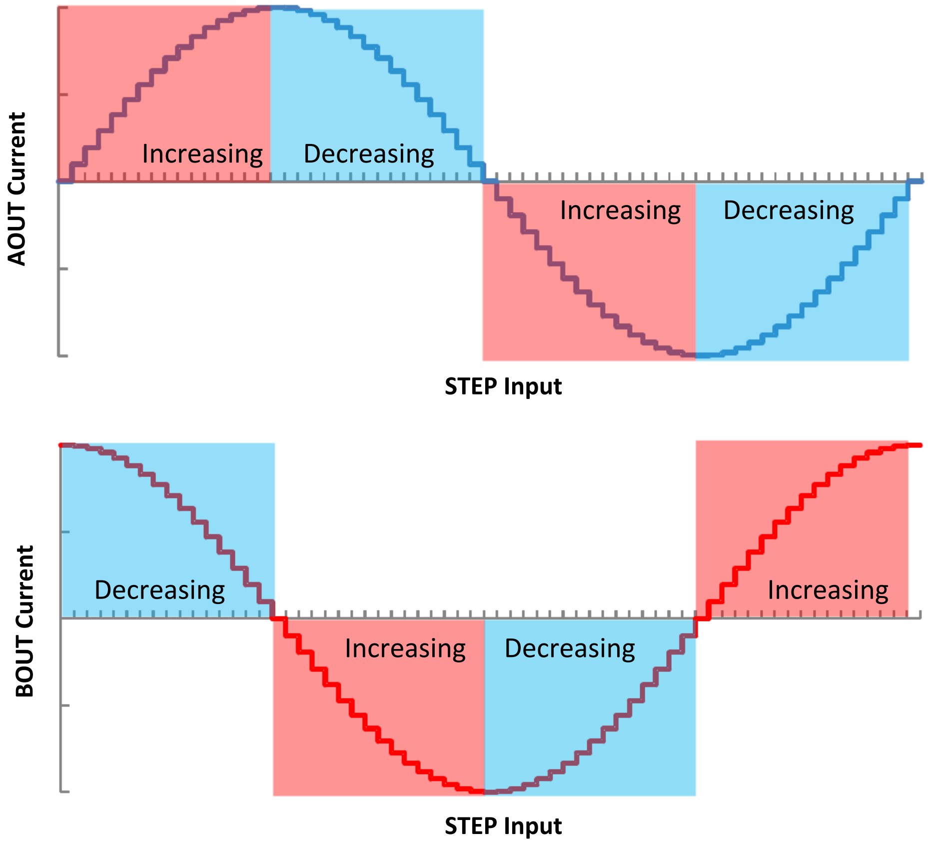


Figure 7-8. Definition of Increasing and Decreasing Steps

7.3.6.1 Slow Decay for Increasing and Decreasing Current

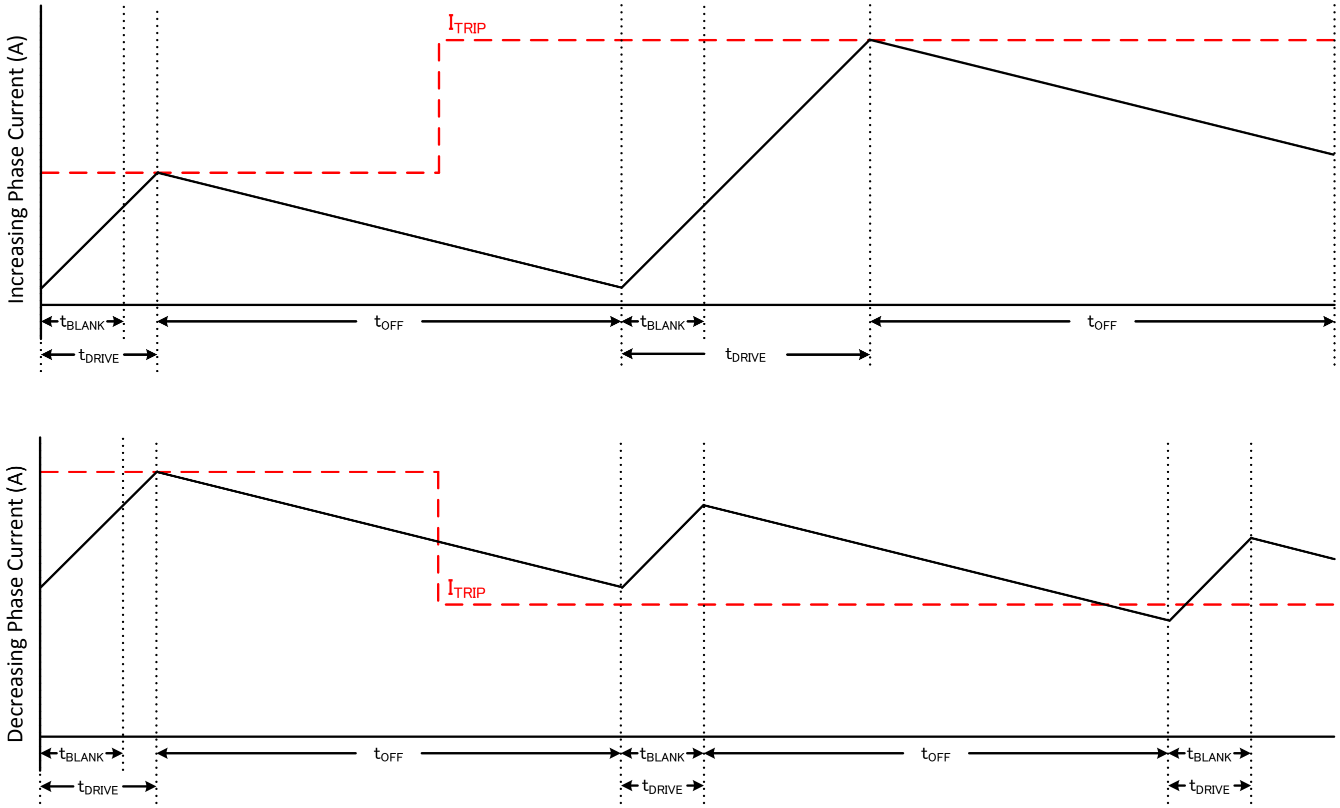


Figure 7-9. Slow/Slow Decay Mode

During slow decay, both of the low-side FETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF}. However on decreasing current steps, slow decay will take a long time to settle to the new ITRIP level because the current decreases very slowly. If the current at the end of the off time is above the ITRIP level, slow decay will be extended for another off time duration and so on, till the current at the end of the off time is below ITRIP level.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and may require a large off-time. In some cases this may cause a loss of current regulation, and a more aggressive decay mode is recommended.

7.3.6.2 Slow Decay for Increasing Current, Mixed Decay for Decreasing Current

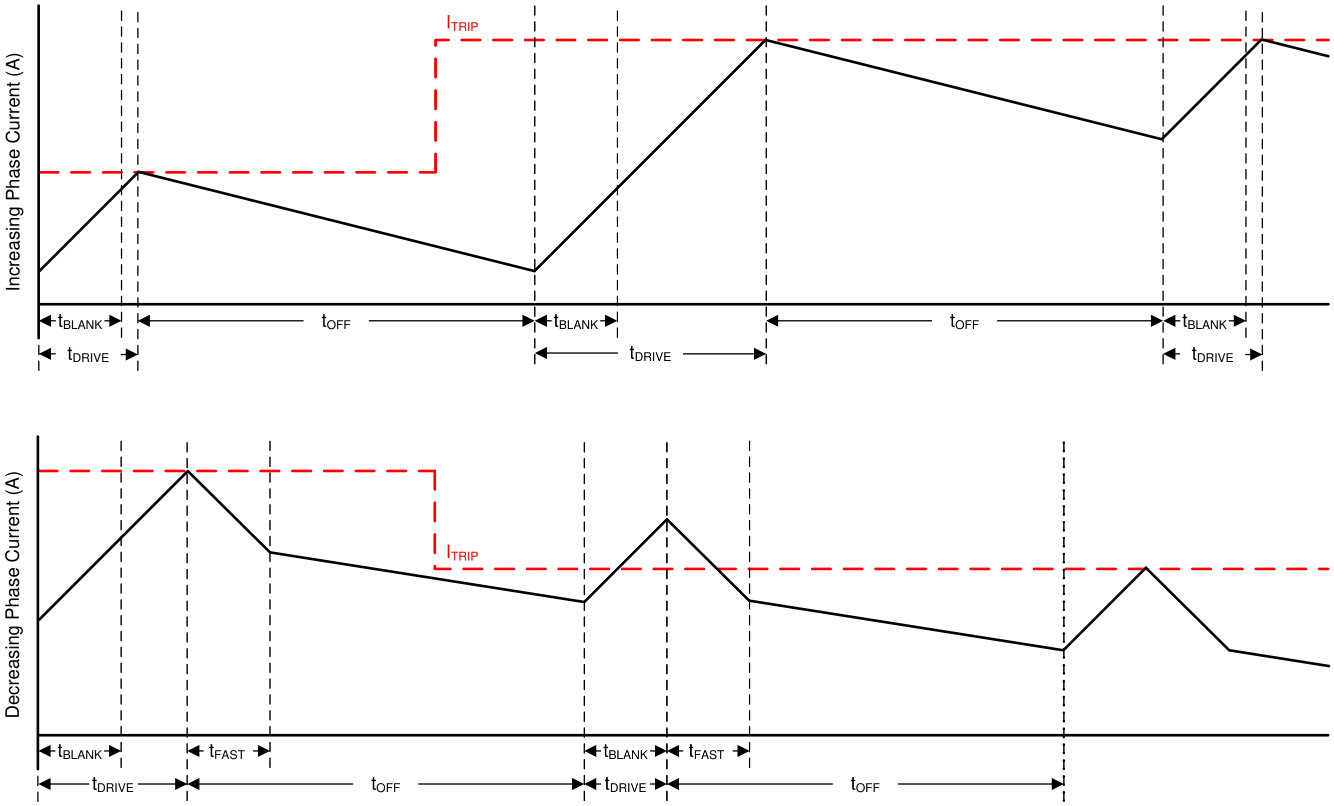


Figure 7-10. Slow-Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of the t_{OFF} time. In this mode, mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This mode exhibits the same current ripple as slow decay for increasing current, because for increasing current, only slow decay is used. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

7.3.6.3 Mixed Decay for Increasing and Decreasing Current

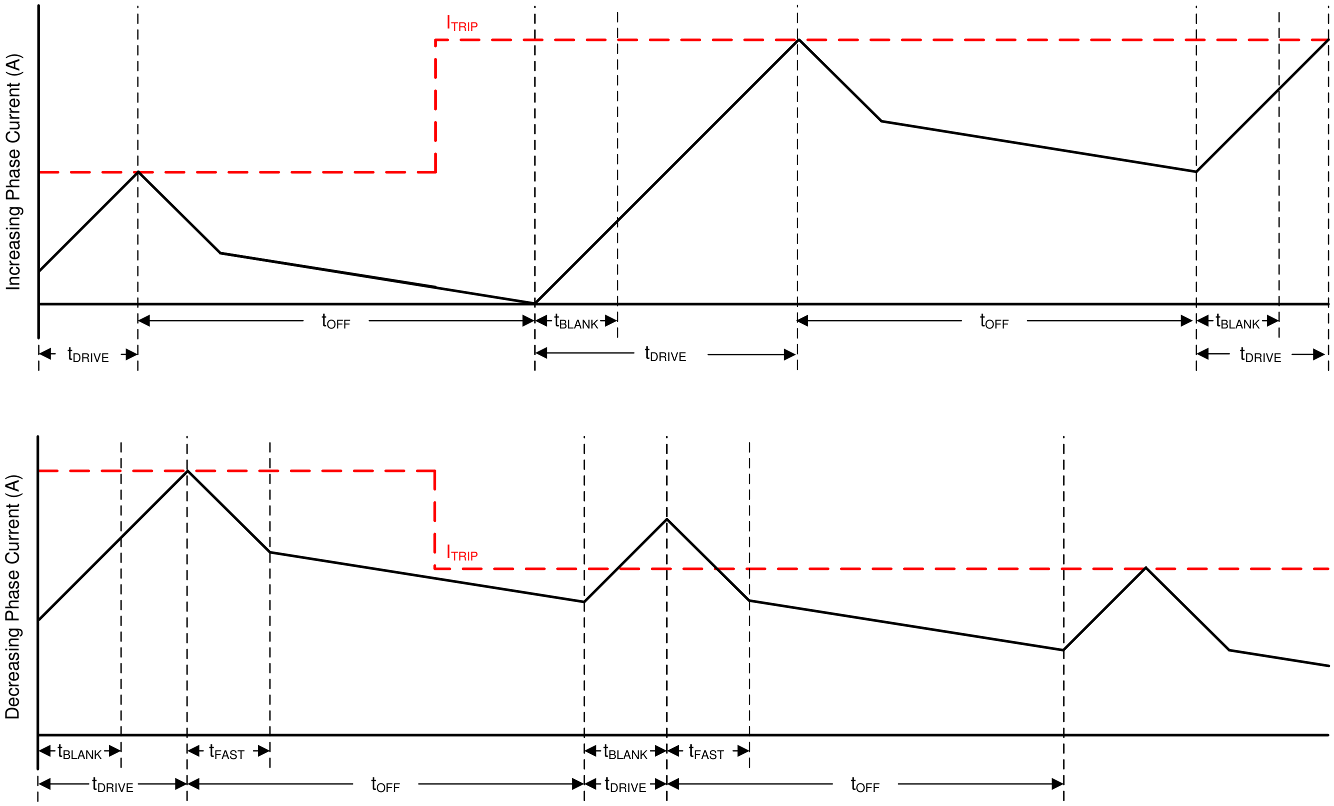


Figure 7-11. Mixed-Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of t_{OFF}. In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and requires an excessively large off-time. Increasing or decreasing mixed decay mode allows the current level to stay in regulation when no back-EMF is present across the motor windings.

7.3.6.4 Smart tune Dynamic Decay

The smart tune current regulation schemes are advanced current-regulation control methods compared to traditional fixed off-time current regulation schemes. Smart tune current regulation schemes help the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Step transitions
- Low-current versus high-current dI/dt

The device provides two different smart tune current regulation modes, named smart tune Dynamic Decay and smart tune Ripple Control.

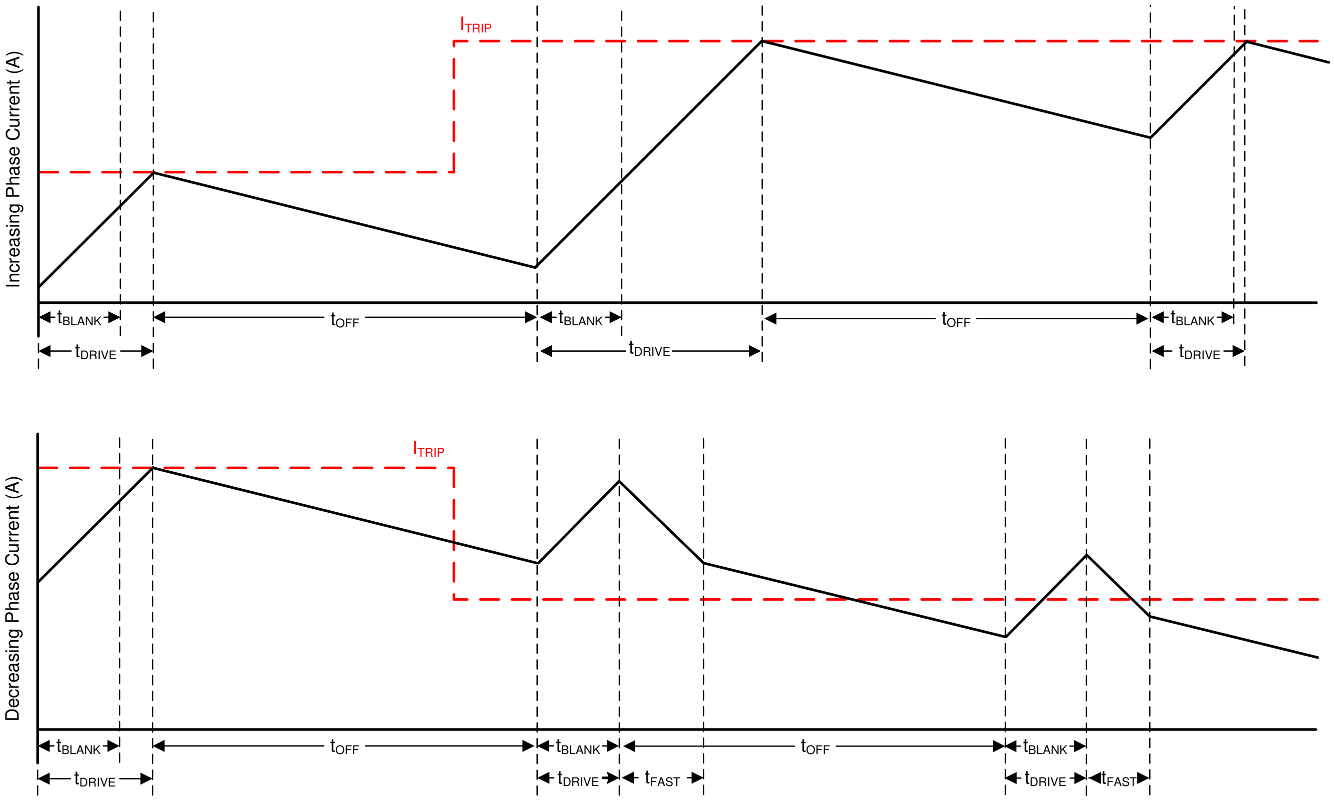


Figure 7-12. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

7.3.6.5 Smart tune Ripple Control

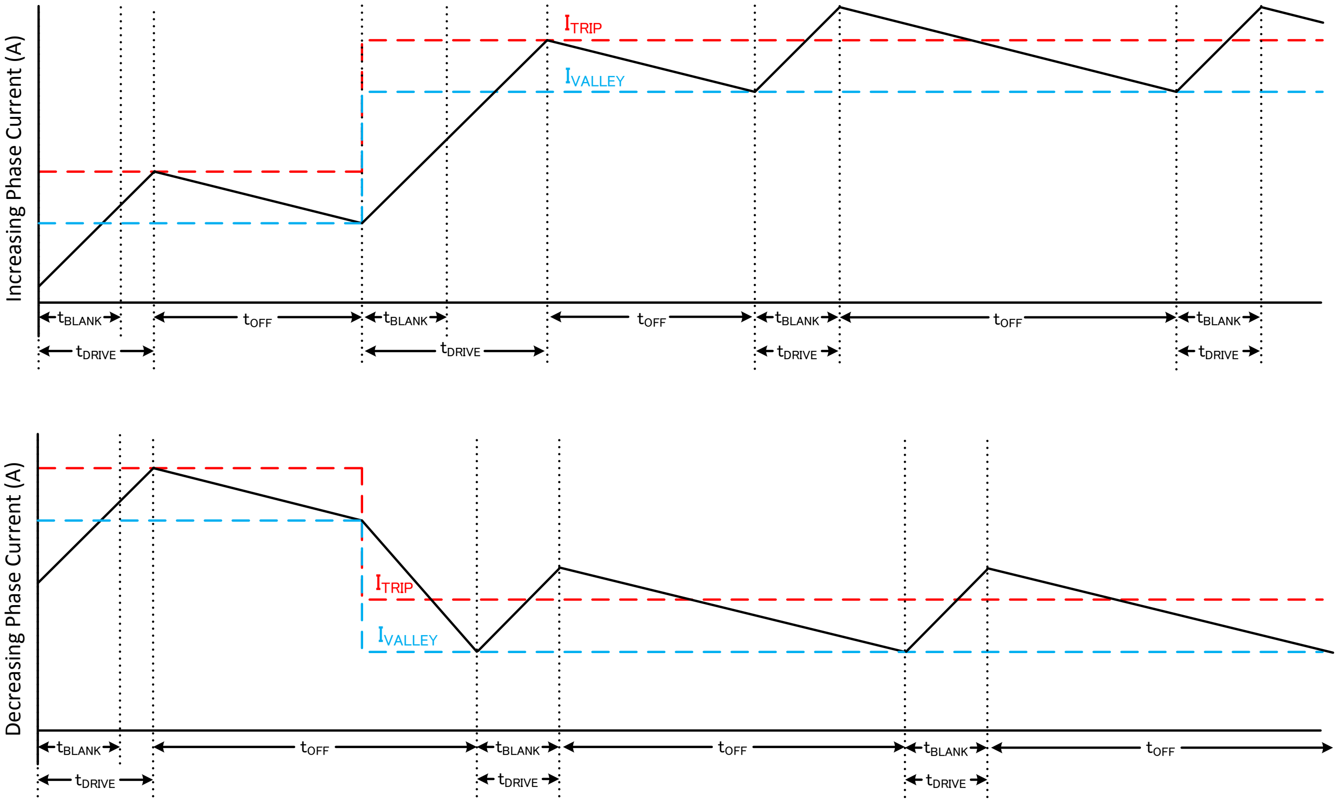


Figure 7-13. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level alongside the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to mode 1 in which both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} varies depending on the current level and operating conditions.

This method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve small current ripple in the current regulation.

7.3.6.6 PWM OFF Time

The TOFF pin configures the PWM OFF time, as shown in Table 7-6. The OFF time settings can be changed on the fly.

Table 7-7. OFF Time Settings

TOFF	OFF Time
0	7 µs
1	16 µs
Hi-Z	24 µs
330 kΩ to GND	32 µs

7.3.6.7 Blanking time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. The blanking time is approximately 860 ns.

7.3.7 Charge Pump

A charge pump is integrated to supply a high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

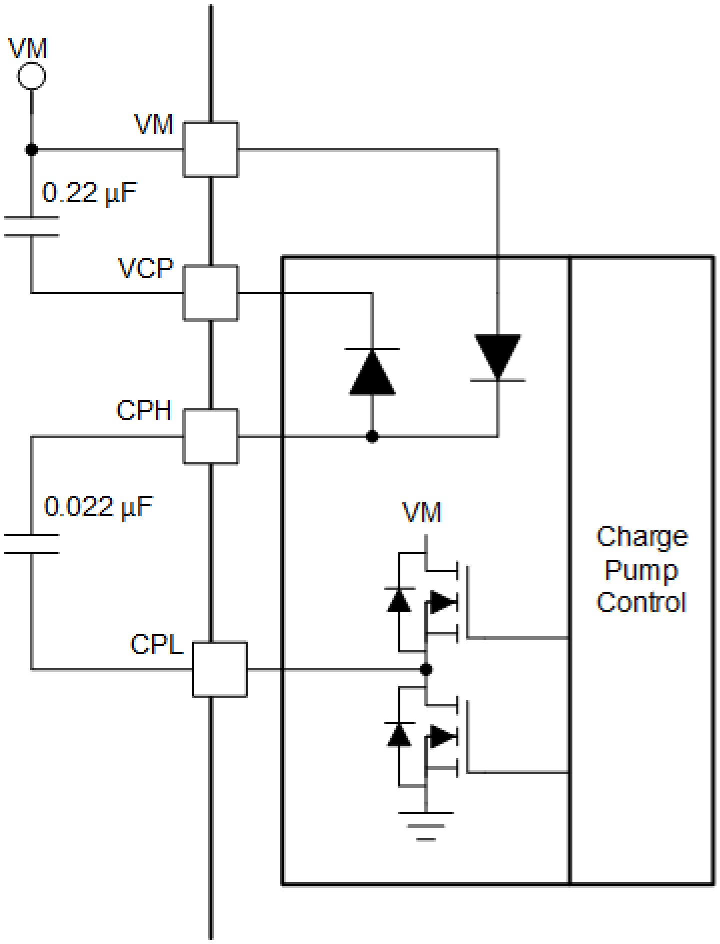


Figure 7-14. Charge Pump Block Diagram

7.3.8 Linear Voltage Regulators

A linear voltage regulator is integrated in the DRV8436 device. The DVDD regulator can be used to provide a reference voltage. DVDD can supply a maximum of 2 mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5-V. When the DVDD LDO current load exceeds 2 mA, the output voltage drops significantly.

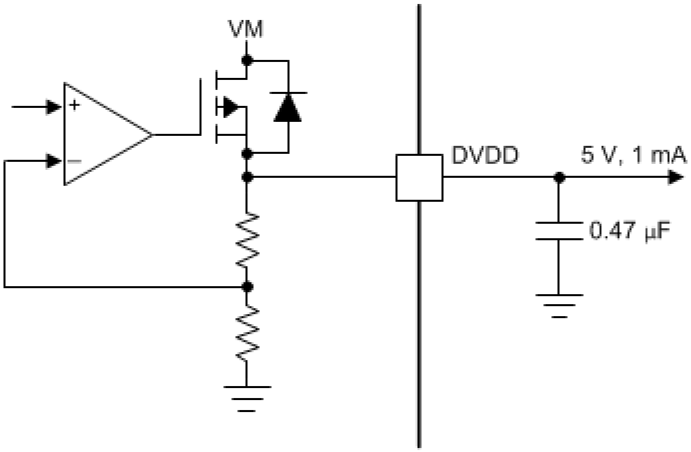


Figure 7-15. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high (that is, Mx, DECAYx or TOFF), tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

7.3.9 Logic Level, tri-level and quad-level Pin Diagrams

Figure 7-16 shows the input structure for M0, DECAY0, DECAY1 and ENABLE pins.

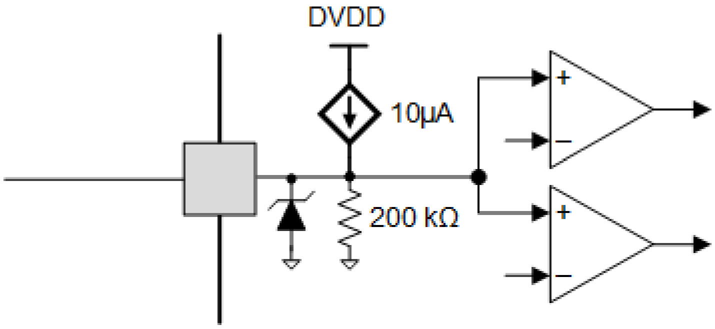


Figure 7-16. Tri-Level Input Pin Diagram

Figure 7-16 shows the input structure for M1 and TOFF pins.

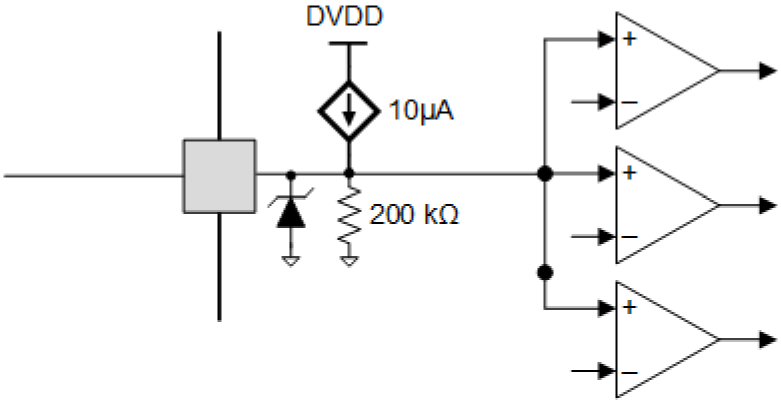


Figure 7-17. Quad-Level Input Pin Diagram

Figure 7-18 shows the input structure for STEP, DIR and nSLEEP pins.

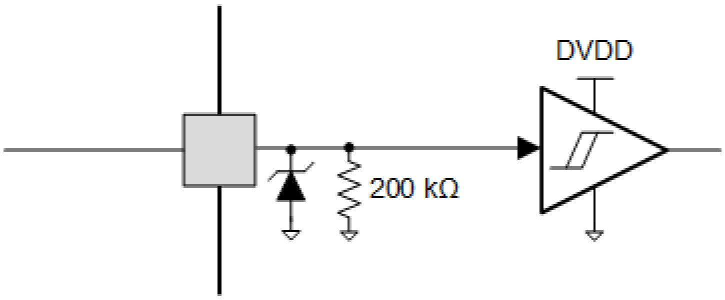


Figure 7-18. Logic-Level Input Pin Diagram

7.3.9.1 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V or 3.3-V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V pullup, an external 3.3-V supply must be used.

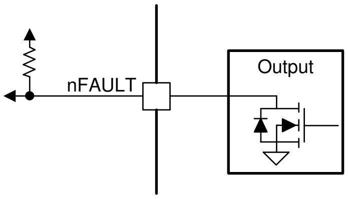


Figure 7-19. nFAULT Pin

7.3.10 Protection Circuits

The DRV8436 device is fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

7.3.10.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage for the voltage supply, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VM undervoltage condition is removed.

7.3.10.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed.

7.3.10.3 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the FETs in that particular H-bridge are disabled and the nFAULT pin is driven low. The charge pump remains active during this condition. The overcurrent protection can operate in two different modes: latched shutdown and automatic retry.

7.3.10.3.1 Latched Shutdown

The ENABLE pin of the DRV8436 has to be made Hi-Z to select latched shutdown mode. In this mode, after an OCP event, the relevant outputs are disabled and the nFAULT pin is driven low. Once the OCP condition is removed, normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

7.3.10.3.2 Automatic Retry

The ENABLE pin of the DRV8436 has to be connected to DVDD to select automatic retry mode. In this mode, after an OCP event the relevant outputs are disabled and the nFAULT pin is driven low. Normal operation resumes automatically (motor-driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

7.3.10.4 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}) all MOSFETs in the H-bridge are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. Normal operation resumes (motor-driver operation and the nFAULT line released) when the OTSD condition is removed.

7.3.10.5 Fault Condition Summary

Table 7-8. Fault Condition Summary

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	—	nFAULT	Disabled	Disabled	Disabled	Reset (V_{DVDD} < 3.9 V)	Automatic: VM > V_{UVLO}
CP undervoltage (CPUV)	CP < V_{CPUV}	—	nFAULT	Disabled	Operating	Operating	Operating	CP > V_{CPUV}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	ENABLE = Hi-Z	nFAULT	Disabled	Operating	Operating	Operating	Latched
		ENABLE = 1	nFAULT	Disabled	Operating	Operating	Operating	Automatic retry: t_{RETRY}
Thermal Shutdown (OTSD)	T_J > T_{OTSD}	—	nFAULT	Disabled	Disabled	Operating	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

The DRV8436 device state is managed by the nSLEEP pin. When the nSLEEP pin is low, the DRV8436 device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The DRV8436 device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Disable Mode (nSLEEP = 1, ENABLE = 0)

The ENABLE pin is used to enable or disable the half bridge in the DRV8436 device. When the ENABLE pin is low, the output drivers are disabled in the Hi-Z state.

7.4.3 Operating Mode (nSLEEP = 1, ENABLE = Hi-Z/1)

When the nSLEEP pin is high, the ENABLE pin is Hi-Z or 1, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.4 nSLEEP Reset Pulse

A latched fault can be cleared through a quick nSLEEP pulse. This pulse width must be greater than 18 μs and shorter than 35 μs. If nSLEEP is low for longer than 35 μs but less than 75 μs, the faults are cleared and the device may or may not shutdown, as shown in Figure 7-20. This reset pulse does not affect the status of the charge pump or other functional blocks.

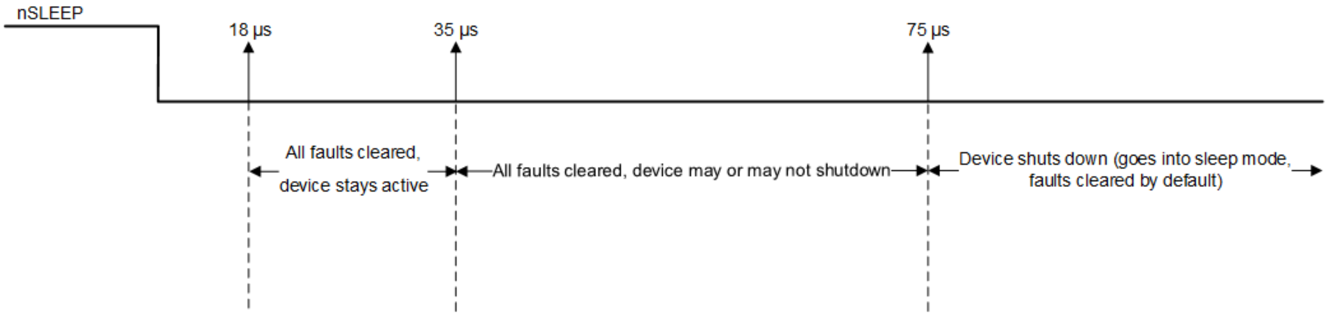


Figure 7-20. nSLEEP Reset Pulse

7.4.5 Functional Modes Summary

Table 7-9 lists a summary of the functional modes.

Table 7-9. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	INDEXER	Logic
Sleep mode	4.5 V < VM < 48 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled	Disabled
Operating	4.5 V < VM < 48 V	nSLEEP pin = 1 ENABLE pin = 1	Operating	Operating	Operating	Operating	Operating
Disabled	4.5 V < VM < 48 V	nSLEEP pin = 1 ENABLE pin = 0	Disabled	Operating	Operating	Operating	Operating

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8436 device is used in bipolar stepper control.

8.2 Typical Application

The following design procedure can be used to configure the DRV8436 device.

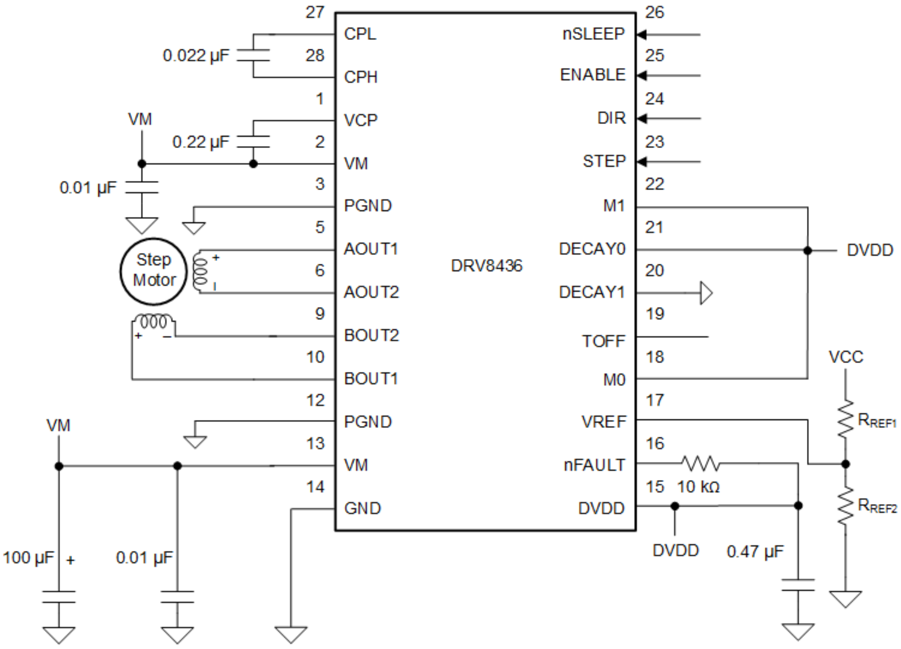


Figure 8-1. Typical Application Schematic (HTSSOP package)

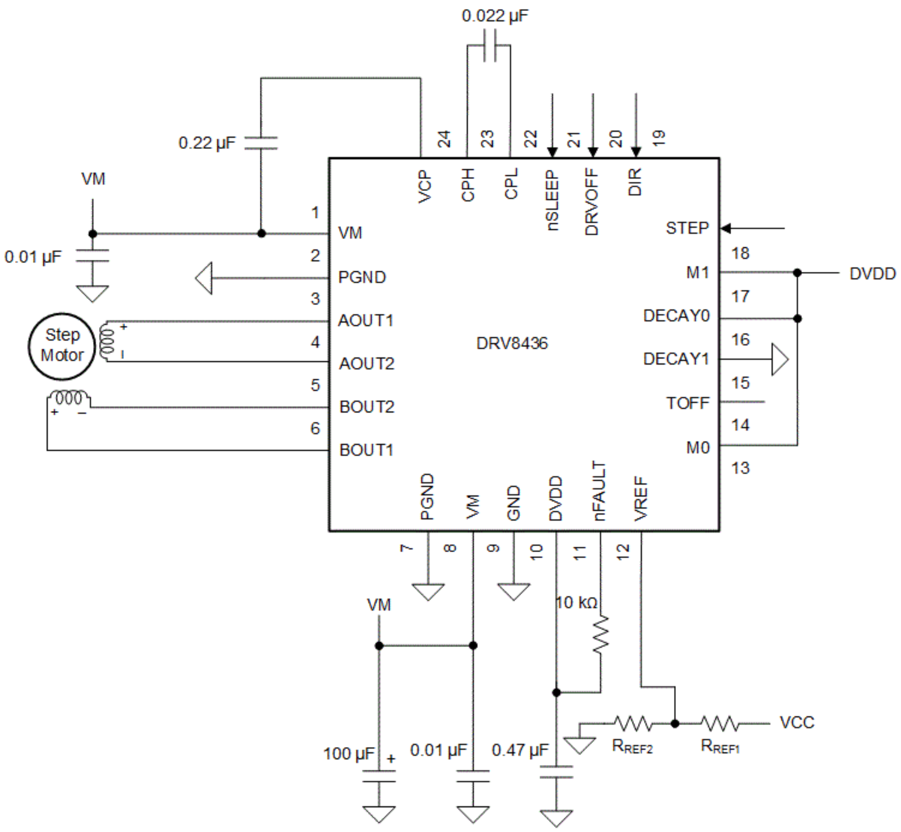


Figure 8-2. Typical Application Schematic (VQFN package)

8.2.1 Design Requirements

Table 8-1 lists the design input parameters for system design.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	2.6 Ω/phase
Motor winding inductance	L_L	1.4 mH/phase
Motor full step angle	$θ_{step}$	1.8°/step
Target microstepping level	n_m	1/8 step
Target motor speed	v	120 rpm
Target full-scale current	I_{FS}	500 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the device requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin. If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target speed.

Use Equation 1 to calculate f_{step} for a desired motor speed (v), microstepping level (n_m), and motor full step angle ($θ_{step}$)

$$f_{step}\ (\mathrm{steps}/\mathrm{s}) = \frac{v\ (\mathrm{rpm}) \times 360\ (°/\mathrm{rot})}{\theta_{step}\ (°/\mathrm{step}) \times n_m\ (\mathrm{steps}/\mathrm{microstep}) \times 60\ (\mathrm{s}/\mathrm{min})} \tag{1}$$

The value of θ_{step} can be found in the stepper motor data sheet, or written on the motor.

For the DRV8436, the microstepping level is set by the M0 and M1 pins and can be any of the settings listed in Table 8-2. Higher microstepping results in a smoother motor motion and less audible noise, but increases switching losses and requires a higher f_{step} to achieve the same motor speed.

Table 8-2. Microstepping Indexer Settings

M0	M1	STEP MODE
0	0	Full step (2-phase excitation) with 100% current
0	330 kΩ to GND	Full step (2-phase excitation) with 71% current
1	0	Non-circular 1/2 step
Hi-Z	0	1/2 step
0	1	1/4 step
1	1	1/8 step
Hi-Z	1	1/16 step
0	Hi-Z	1/32 step
Hi-Z	330 kΩ to GND	1/64 step
Hi-Z	Hi-Z	1/128 step
1	Hi-Z	1/256 step

For example, the motor is 1.8°/step for a target of 120 rpm at 1/8 microstep mode.

$$f_{step}\ (\mathrm{steps}/\mathrm{s}) = \frac{120\ \mathrm{rpm} \times 360°/\mathrm{rot}}{1.8°/\mathrm{step} \times 1/8\ \mathrm{steps}/\mathrm{microstep} \times 60\ \mathrm{s}/\mathrm{min}} = 3.2\ \mathrm{kHz} \tag{2}$$

8.2.2.2 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the VREF voltage. The maximum allowable voltage on the VREF pin is 3.3 V. DVDD can be used to provide VREF through a resistor divider.

During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step. I_{FS} (A) = V_{REF} (V) / 2.2 (V/A)

Note

The I_{FS} current must also follow the equation shown below to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\ (\mathrm{A}) < \frac{\mathrm{VM}\ (\mathrm{V})}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega)} \tag{3}$$

8.2.2.3 Decay Modes

The device supports six different decay modes, as shown in Table 7-6. The current through the motor windings is regulated using an adjustable fixed-time-off scheme which means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the device places the winding in one of the eight decay modes for t_{OFF}. After t_{OFF}, a new drive phase starts.

8.2.3 Application Curves

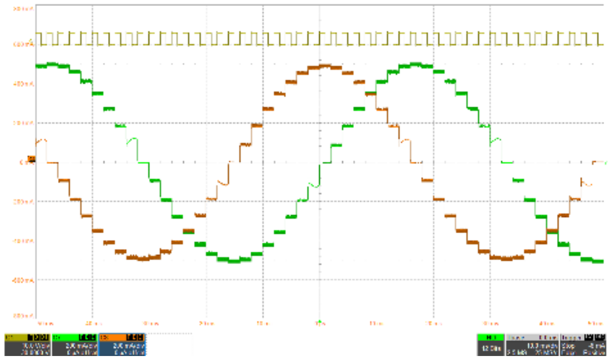


Figure 8-3. 1/8 Microstepping With smart tune Ripple Control Decay

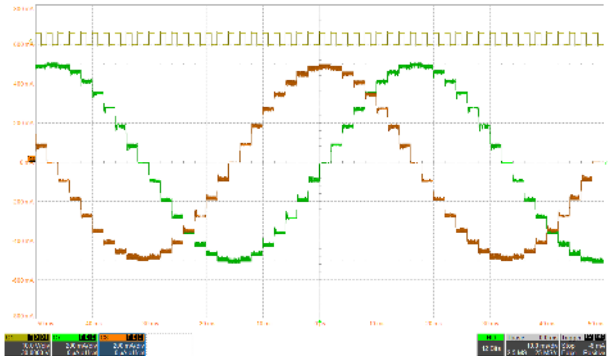


Figure 8-4. 1/8 Microstepping With smart tune Dynamic Decay

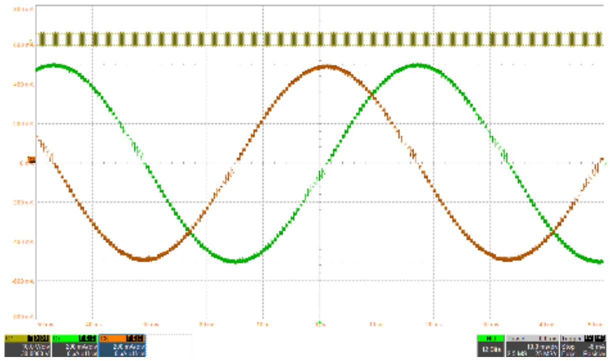


Figure 8-5. 1/32 Microstepping With smart tune Ripple Control Decay

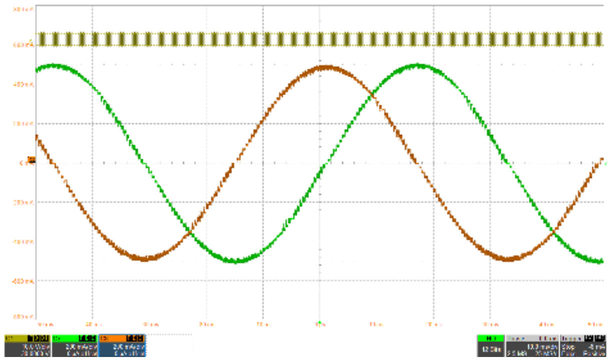


Figure 8-6. 1/32 Microstepping With smart tune Dynamic Decay

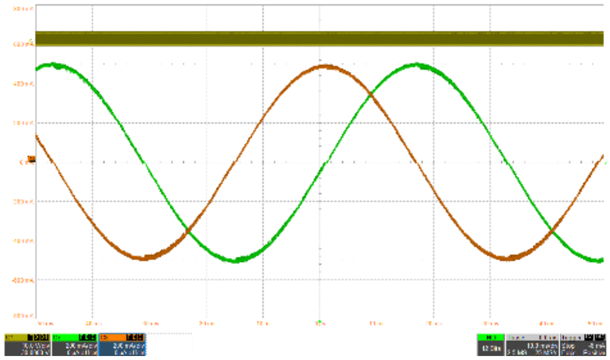


Figure 8-7. 1/256 Microstepping With smart tune Ripple Control Decay

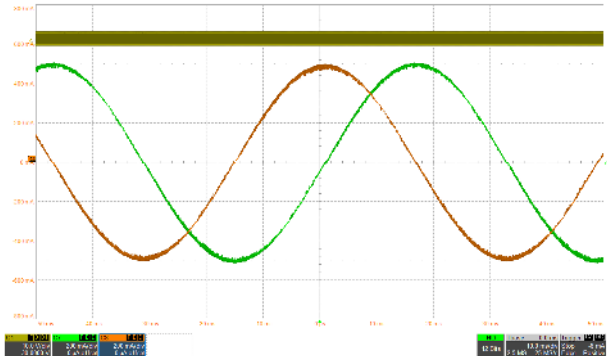


Figure 8-8. 1/256 Microstepping With smart tune Dynamic Decay

9 Thermal Application

This section presents the power dissipation calculation and junction temperature estimation of the device.

9.1 Power Dissipation

The total power dissipation constitutes of three main components - conduction loss (P_{COND}), switching loss (P_{SW}) and power loss due to quiescent current consumption (P_Q).

9.1.1 Conduction Loss

The current path for a motor connected in full-bridge is through the high-side FET of one half-bridge and low-side FET of the other half-bridge. The conduction loss (P_{COND}) depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ONH)}$) and low-side ($R_{DS(ONL)}$) on-state resistances as shown below.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) \tag{4}$$

The conduction loss for the typical application discussed in this section is calculated below.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) = 2 \times (0.5\text{-A} / \sqrt{2})^2 \times (0.45\text{-}\Omega + 0.45\text{-}\Omega) = 0.225\text{-W} \tag{5}$$

Note

This power calculation is highly dependent on the device temperature which significantly effects the high-side and low-side on-resistance of the FETs. For more accurate calculation, consider the dependency of on-resistance of FETs with device temperature.

9.1.2 Switching Loss

The power loss due to the PWM switching frequency depends on the slew rate (t_{SR}), supply voltage, motor RMS current and the PWM switching frequency. The switching losses in each H-bridge during rise-time and fall-time are calculated below.

$$P_{SW\_RISE} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RISE\_PWM} \times f_{PWM} \tag{6}$$

$$P_{SW\_FALL} = 0.5 \times V_{VM} \times I_{RMS} \times t_{FALL\_PWM} \times f_{PWM} \tag{7}$$

Both t_{RISE_PWM} and t_{FALL_PWM} can be approximated as $V_{VM}/\ t_{SR}$. After substituting the values of various parameters, and assuming 30-kHz PWM frequency, the switching losses in each H-bridge are calculated as shown below -

$$P_{SW\_RISE} = 0.5 \times 24\text{-V} \times (0.5\text{-A} / \sqrt{2}) \times (24\text{-V} / 150\ \text{V/µs}) \times 30\text{-kHz} = 0.02\text{-W} \tag{8}$$

$$P_{SW\_FALL} = 0.5 \times 24\text{-V} \times (0.5\text{-A} / \sqrt{2}) \times (24\text{-V} / 150\ \text{V/µs}) \times 30\text{-kHz} = 0.02\text{-W} \tag{9}$$

The total switching loss for the stepper motor driver (P_{SW}) is calculated as twice the sum of rise-time (P_{SW_RISE}) switching loss and fall-time (P_{SW_FALL}) switching loss as shown below -

$$P_{SW} = 2 \times (P_{SW\_RISE} + P_{SW\_FALL}) = 2 \times (0.02\text{-W} + 0.02\text{-W}) = 0.08\text{-W} \tag{10}$$

Note

The rise-time (t_{RISE}) and the fall-time (t_{FALL}) are calculated based on typical values of the slew rate (t_{SR}). This parameter is expected to change based on the supply-voltage, temperature and device to device variation.

The switching loss is directly proportional to the PWM switching frequency. The PWM frequency in an application will depend on the supply voltage, inductance of the motor coil, back emf voltage and OFF time or the ripple current (for smart tune ripple control decay mode).

9.1.3 Power Dissipation Due to Quiescent Current

The power dissipation due to the quiescent current consumed by the power supply is calculated as shown below -

$$P_Q = V_{VM} \text{ x } I_{VM} \tag{11}$$

Substituting the values, quiescent power loss can be calculated as shown below -

$$P_Q = 24\text{-V x } 5\text{-mA} = 0.12\text{-W} \tag{12}$$

Note

The quiescent power loss is calculated using the typical operating supply current (I_{VM}) which is dependent on supply-voltage, temperature and device to device variation.

9.1.4 Total Power Dissipation

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss as shown below.

$$P_{TOT} = P_{COND} + P_{SW} + P_Q = 0.225\text{-W} + 0.08\text{-W} + 0.12\text{-W} = 0.425\text{-W} \tag{13}$$

9.2 Device Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as $T_J = T_A + (P_{TOT} \text{ x } R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 31.3 °C/W for the HTSSOP package and 41.3 °C/W for the VQFN package.

Assuming 25°C ambient temperature, the junction temperature for the HTSSOP package is calculated as shown below -

$$T_J = 25°\text{C} + (0.425\text{-W x } 31.3°\text{C/W}) = 38.3\ °\text{C} \tag{14}$$

The junction temperature for the VQFN package is calculated as shown below -

$$T_J = 25°\text{C} + (0.425\text{-W x } 41.3°\text{C/W}) = 42.55\ °\text{C} \tag{15}$$

Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.5 V to 48 V. A 0.01-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the device as possible. In addition, a bulk capacitor must be included on VM.

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

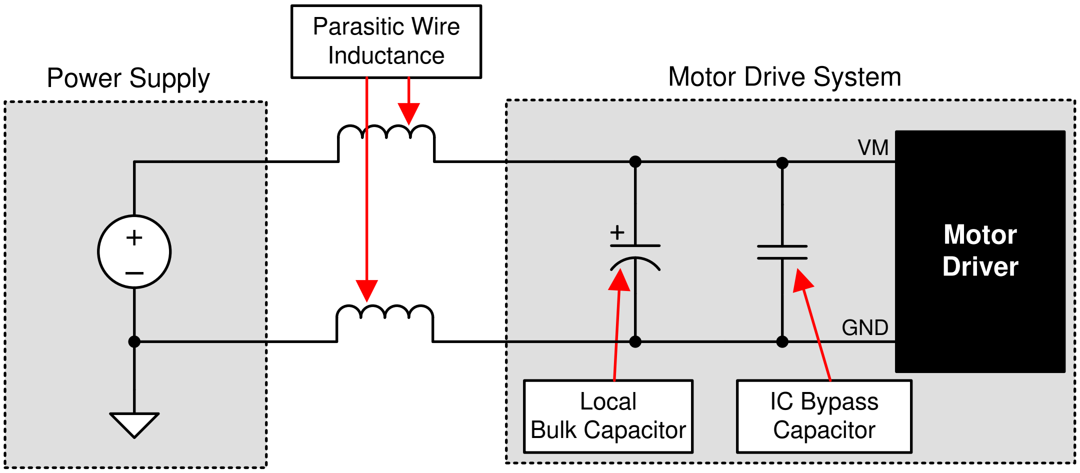
The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.



Copyright © 2016, Texas Instruments Incorporated

Figure 10-1. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.022 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.

The thermal PAD must be connected to system ground.

10.2 Layout Examples

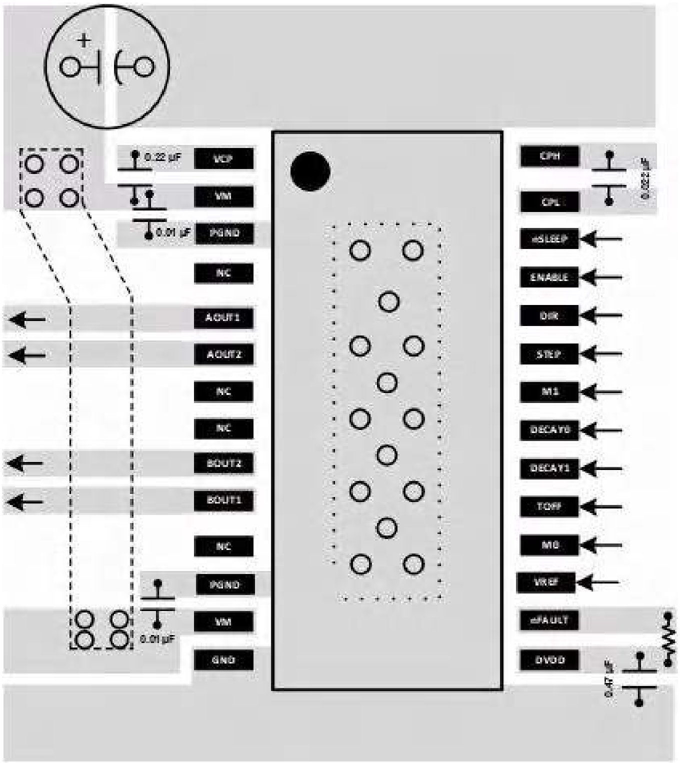


Figure 10-1. HTSSOP Layout Example

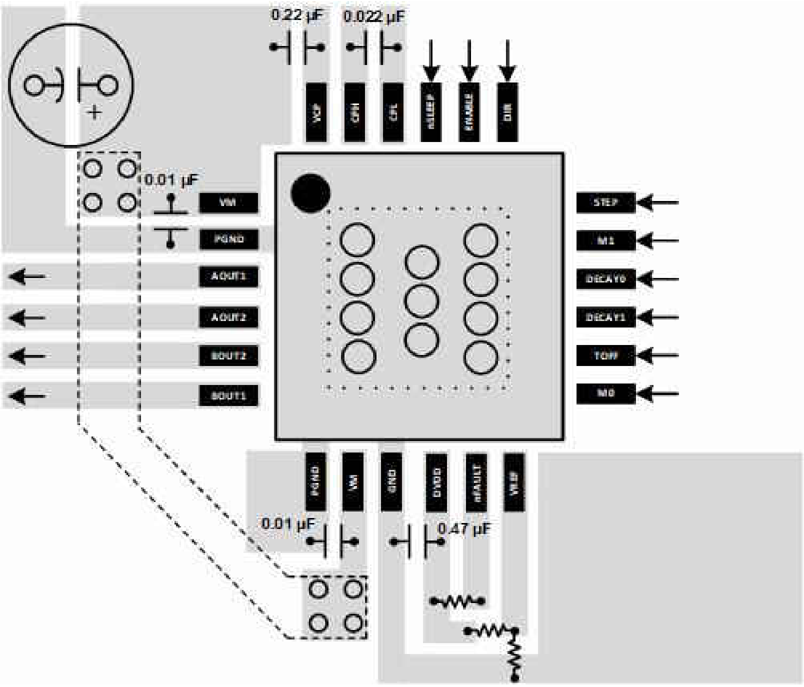


Figure 10-2. QFN Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *How to Reduce Audible Noise in Stepper Motors* application report
- Texas Instruments, *How to Improve Motion Smoothness and Accuracy* application report
- Texas Instruments, *How to Drive Unipolar Stepper Motors with DRV8xxx* application report
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Motor Drives Layout Guide* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

11.4 Trademarks

All trademarks are the property of their respective owners.

12 Mechanical, Packaging, and Orderable Information

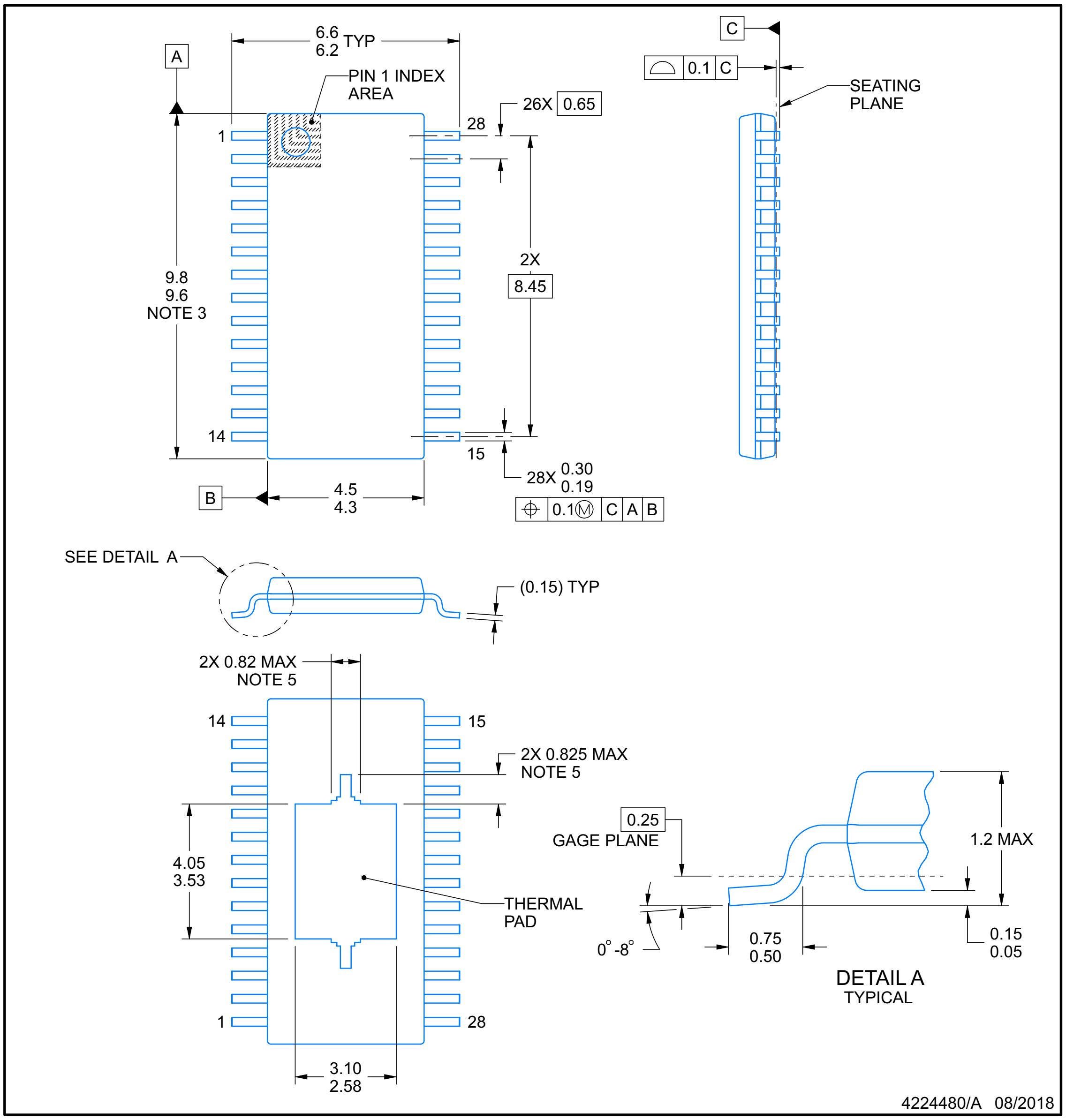
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

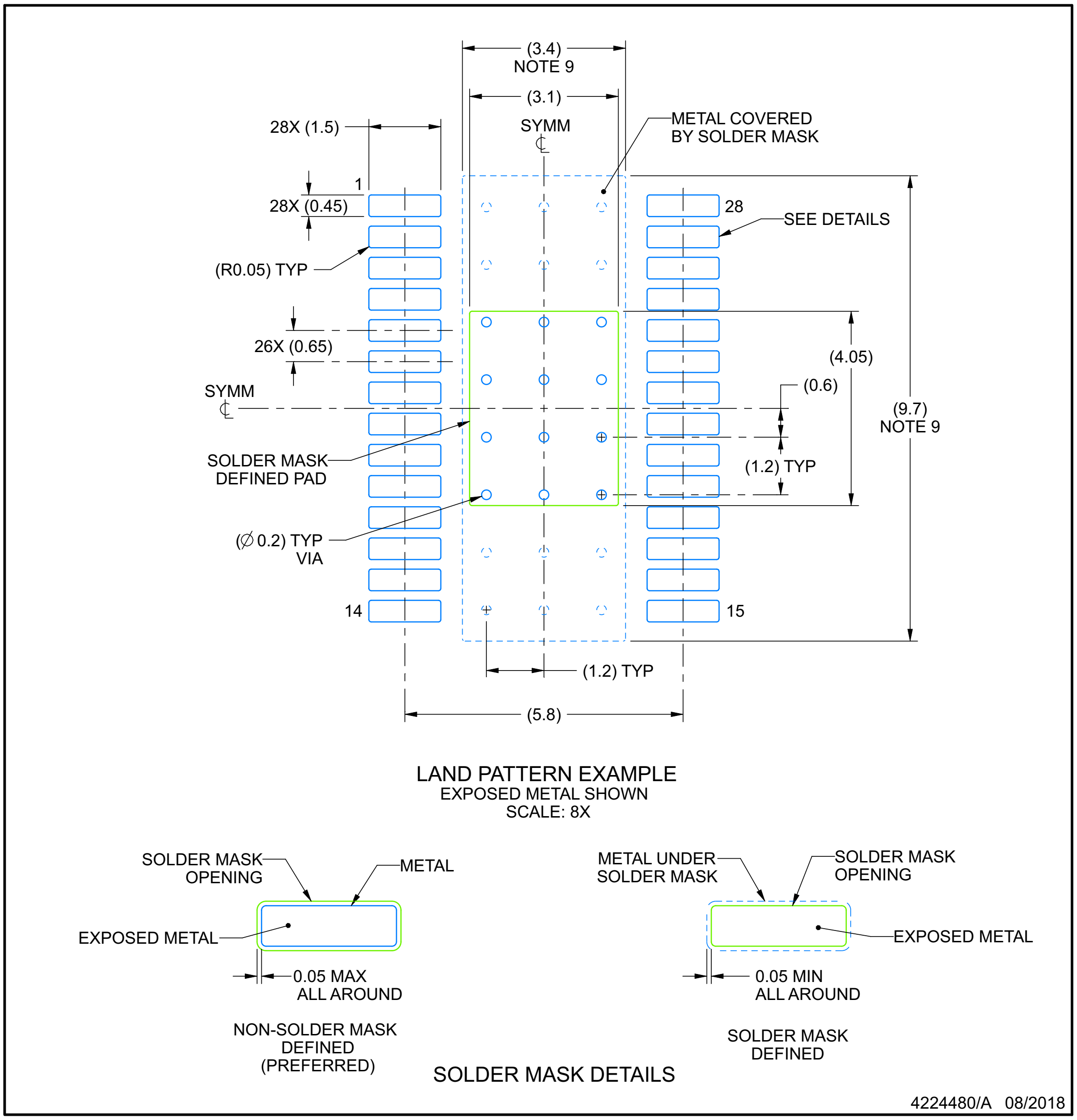
www.ti.com

EXAMPLE BOARD LAYOUT

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4224480/A 08/2018

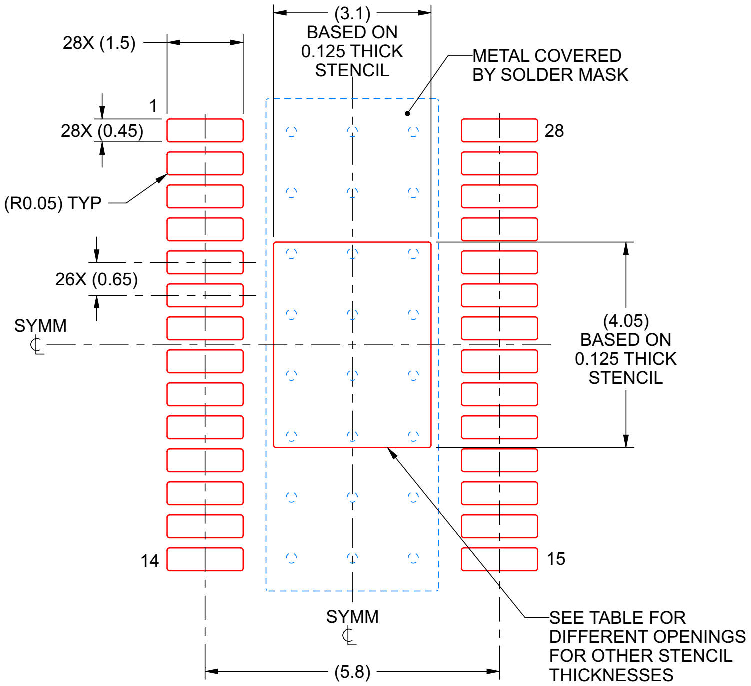
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0028M **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 4.53
0.125	3.10 X 4.05 (SHOWN)
0.15	2.83 X 3.70
0.175	2.62 X 3.42

4224480/A 08/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

www.ti.com

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8436PWPR	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8436	Samples
DRV8436RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8436	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

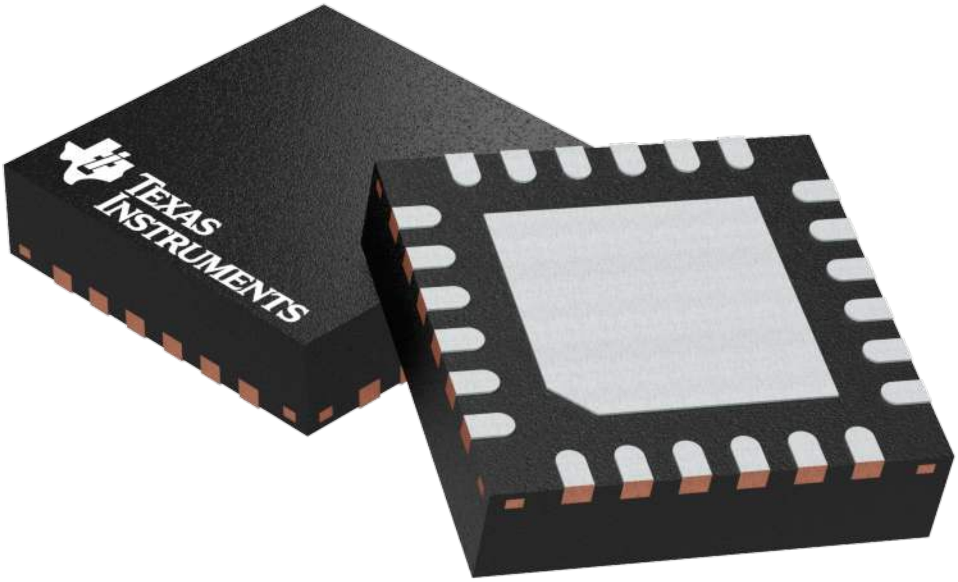
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

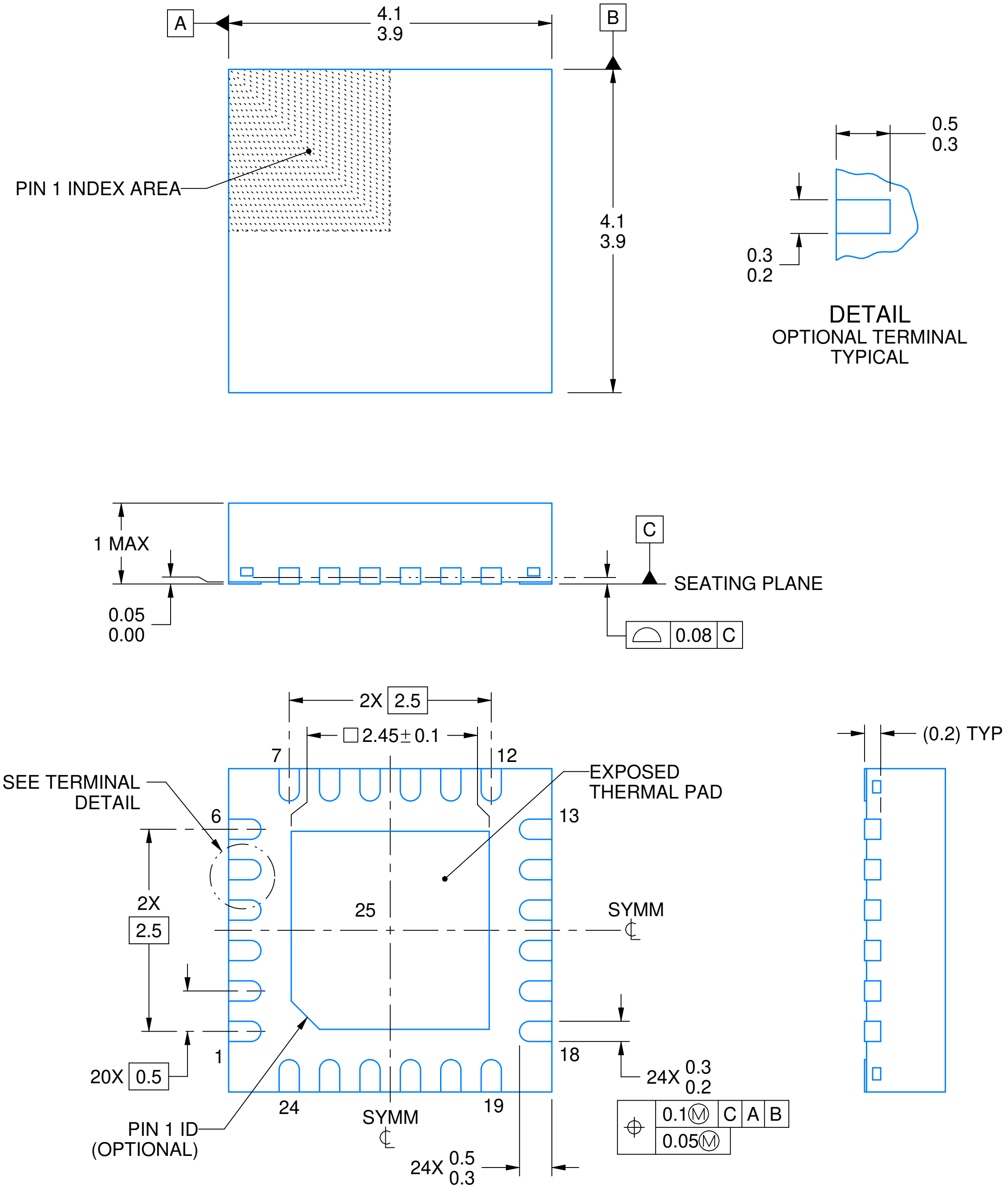
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



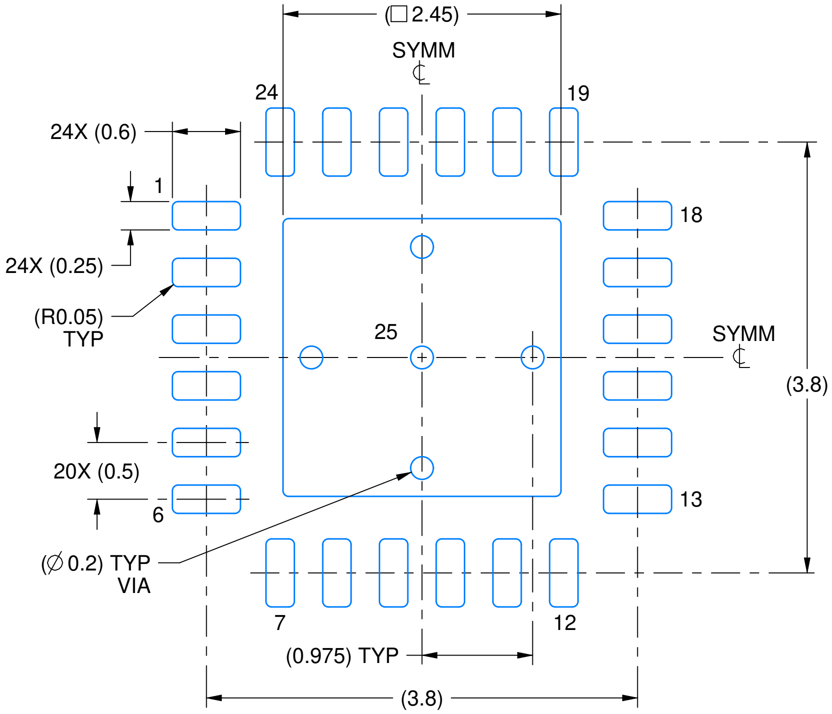
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



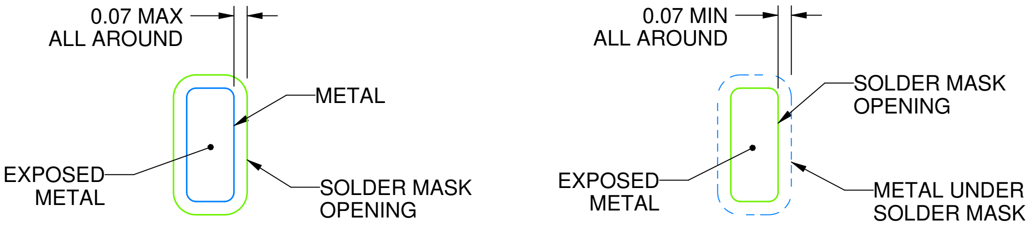
4219013/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



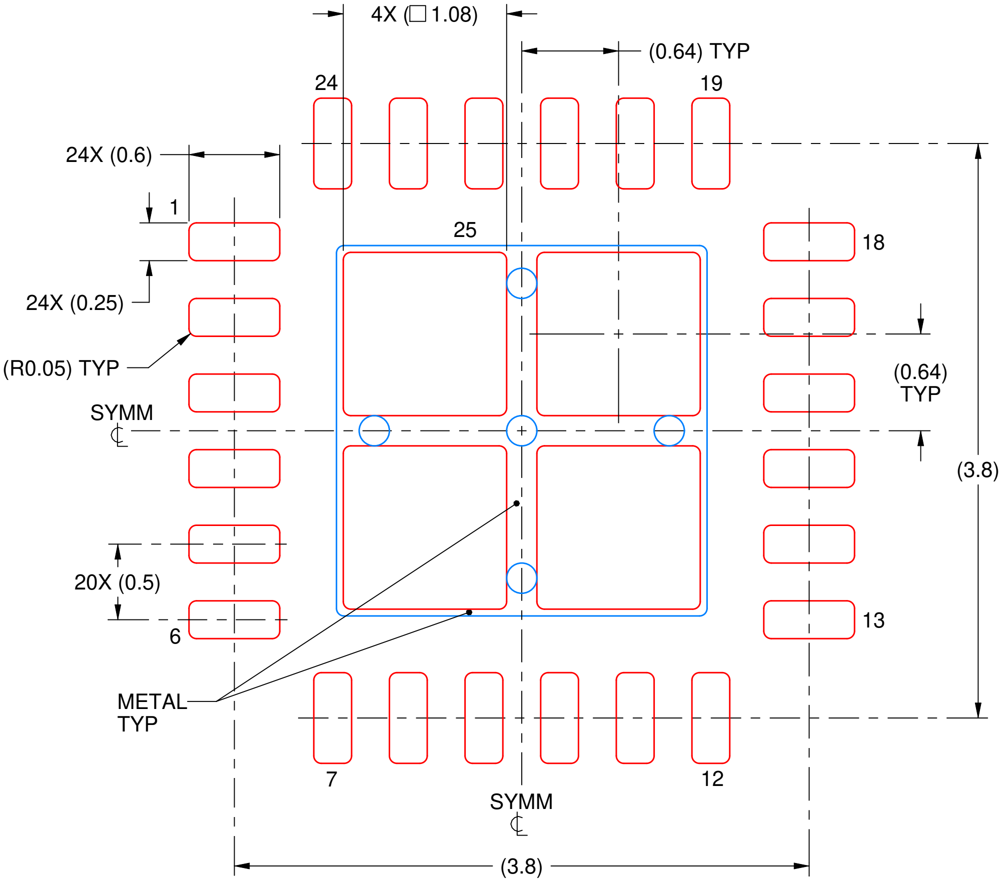
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

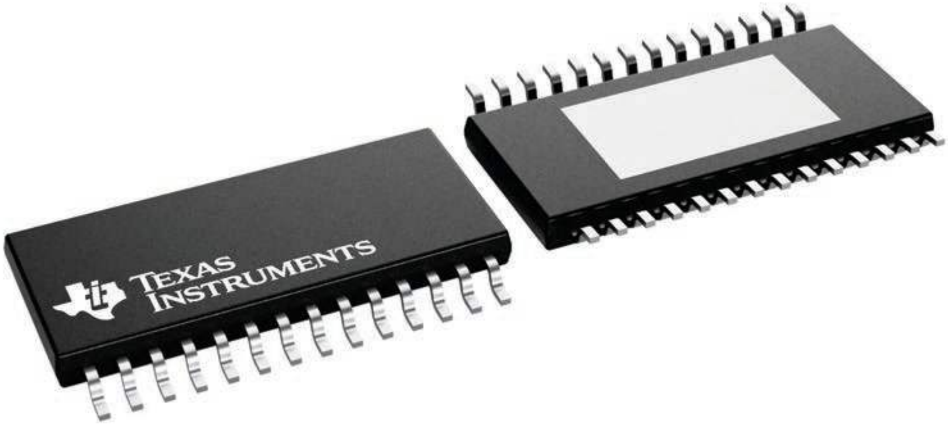
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated