

N-Channel 100-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY		
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.0105 at $V_{GS} = 10$ V	85 ^a
	0.012 at $V_{GS} = 4.5$ V	

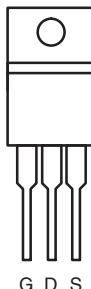
FEATURES

- TrenchFET® Power MOSFET
- 175 °C Maximum Junction Temperature



RoHS*
COMPLIANT

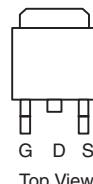
TO-220AB



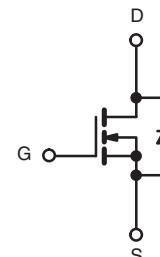
DRAIN connected to TAB

Top View
SUP85N10-10

TO-263



Top View
SUP85N10-10



N-Channel MOSFET

ORDERING INFORMATION

Package	Tin/Lead Plated	Lead (Pb)-free
TO-220AB	SUP85N10-10	SUP85N10-10-E3
TO-263	SUB85N10-10	SUB85N10-10-E3

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	85 ^a	A
		60 ^a	
Pulsed Drain Current	I_{DM}	240	
Avalanche Current	I_{AS}	75	
Single Pulse Avalanche Energy ^b	E_{AS}	280	mJ
Maximum Power Dissipation ^b	P_D	250 ^c	W
		3.75	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R_{thJA}	40	°C/W
		62.5	
Junction-to-Case	R_{thJC}	0.6	

Notes:

- Package limited.
- Duty cycle $\leq 1\%$.
- See SOA curve fo voltage derating.
- When mounted on 1" square PCB (FR-4 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply.

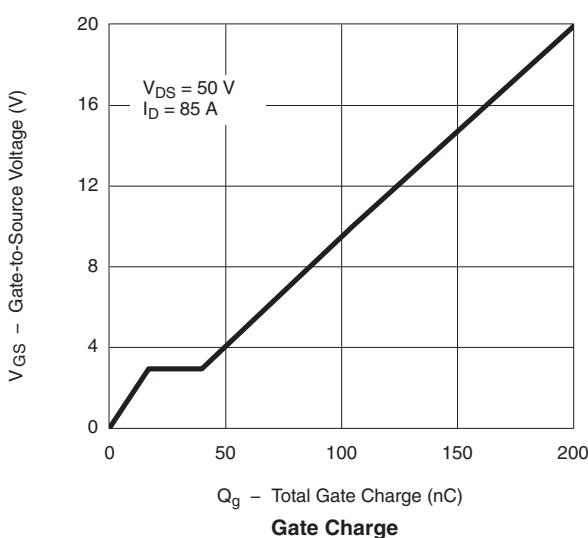
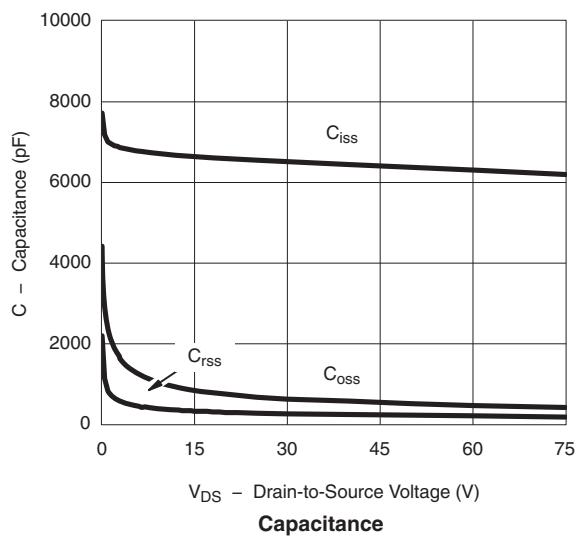
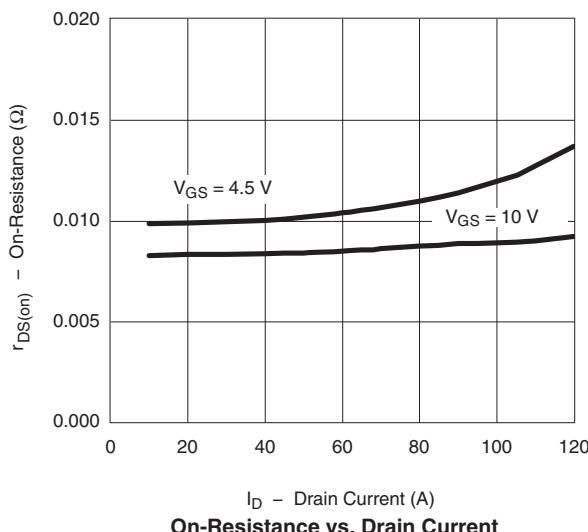
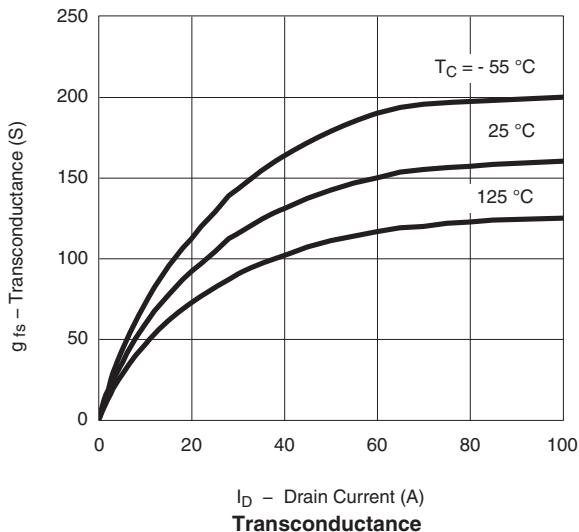
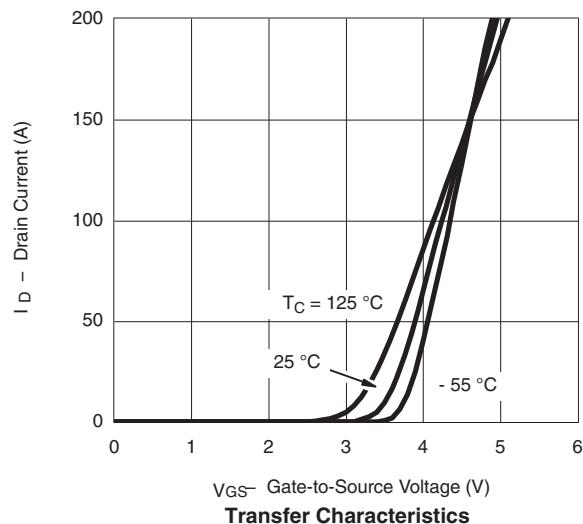
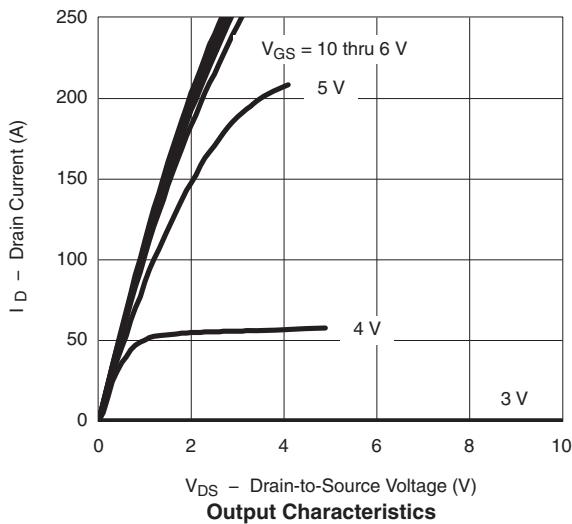
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V
Gate-Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1		3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$			1	
		$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125^\circ\text{C}$			50	
		$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 175^\circ\text{C}$			250	μA
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} = \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	120			A
Drain-Source On-State Resistance ^a	$r_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}$		0.0085	0.0105	
		$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$		0.010	0.0012	
		$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}, T_J = 125^\circ\text{C}$			0.017	Ω
		$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}, T_J = 175^\circ\text{C}$			0.022	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 30 \text{ A}$	25			S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		6550		
Output Capacitance	C_{oss}			665		
Reverse Transfer Capacitance	C_{rss}			265		pF
Total Gate Charge ^c	Q_g	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 85 \text{ A}$		105	160	
Gate-Source Charge ^c	Q_{gs}			17		nC
Gate-Drain Charge ^c	Q_{gd}			23		
Turn-On Delay Time ^c	$t_{d(\text{on})}$			12	25	
Rise Time ^c	t_r	$V_{DD} = 50 \text{ V}, R_L = 0.6 \Omega$ $I_D \geq 85 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 2.5 \Omega$		90	135	
Turn-Off Delay Time ^c	$t_{d(\text{off})}$			55	85	ns
Fall Time ^c	t_f			130	195	
Source-Drain Diode Ratings and Characteristics ($T_C = 25^\circ\text{C}$)^b						
Continuous Current	I_S	$I_F = 85 \text{ A}, V_{GS} = 0 \text{ V}$ $I_F = 50 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$			85	
Pulsed Current	I_{SM}				240	A
Forward Voltage ^a	V_{SD}			1.0	1.5	V
Reverse Recovery Time	t_{rr}			85	140	ns
Peak Reverse Recovery Current	$I_{RM(\text{REC})}$			4.5	7	A
Reverse Recovery Charge	Q_{rr}			0.17	0.35	μC

Notes:

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

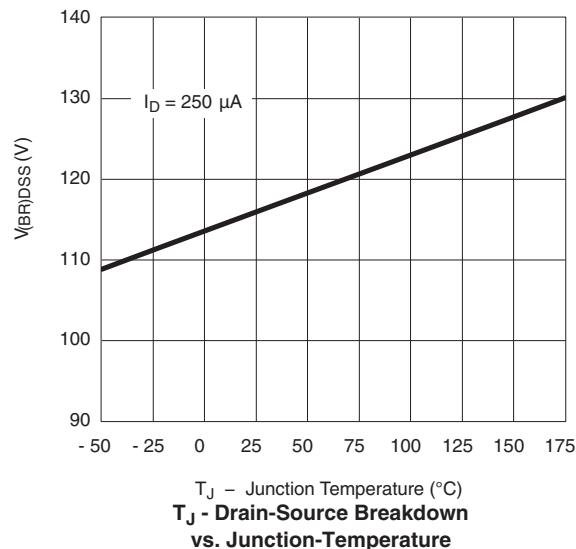
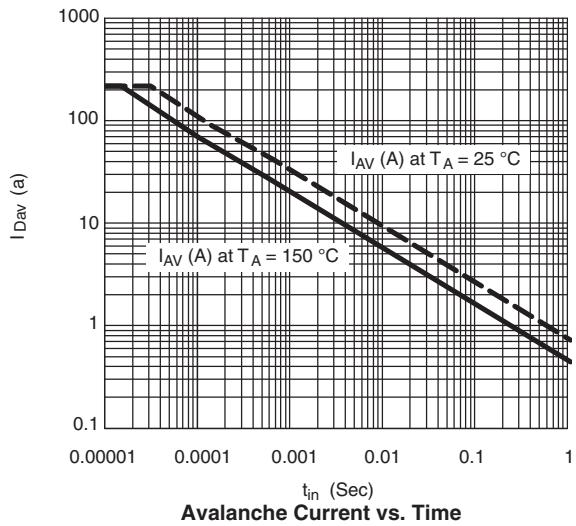
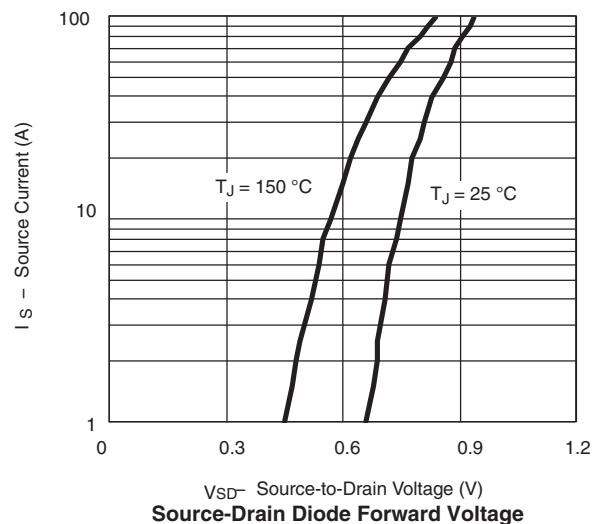
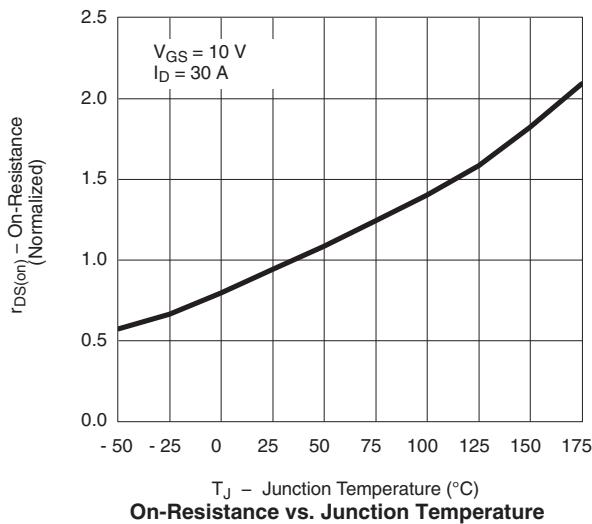
TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted


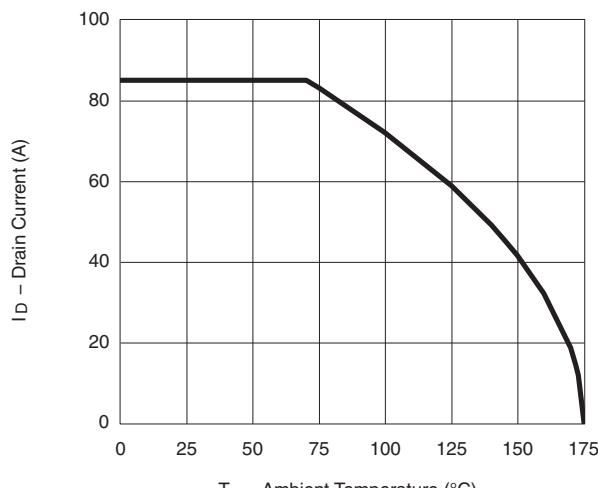
SUP/SUB85N10-10

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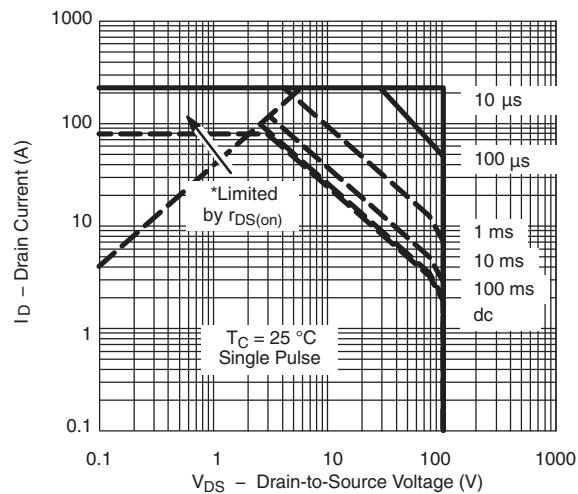


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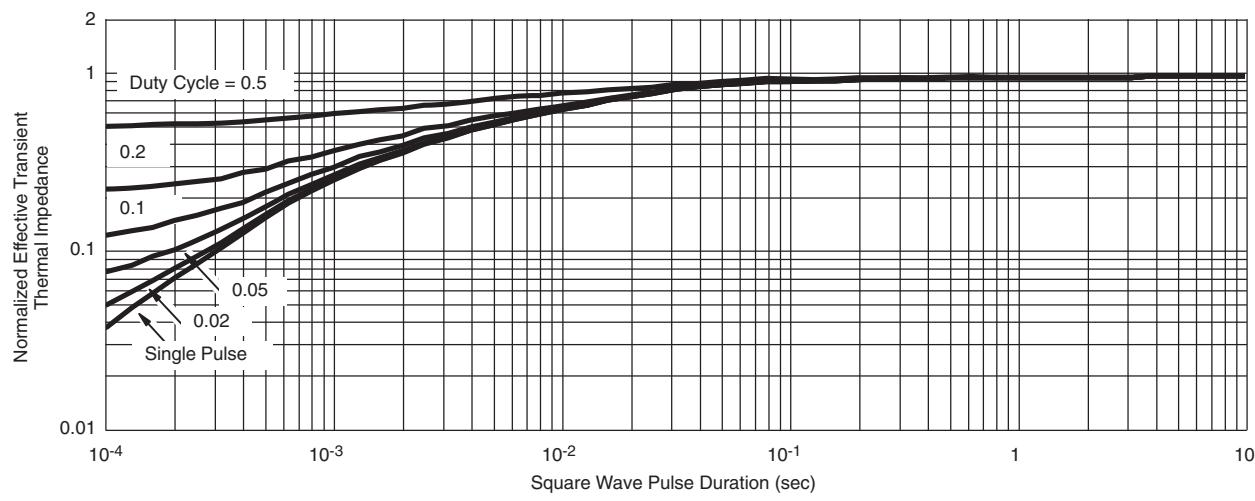
THERMAL RATINGS


Maximum Avalanche and Drain Current
vs. Case Temperature



* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?71141>.



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