TLE82453-3SA

3 Channel High-Side and Low-Side Linear Solenoid Driver IC

Dragon IC

Data Sheet

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Automotive Power

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3 Channel High-Side and Low-Side Linear Solenoid Driver IC
Dragon IC

TLE82453-3SA

1 Overview

PG-DSO-36

Features

- Three independent low side / high side configurable channels
- Integrated half-bridge power stages
- R_{ON}(max) = 250 mΩ @ Tj = 150 °C
- Integrated sense resistor with internal TCR compensation
- Load current measurement range = 0 mA to 1500 mA (typical)
- Current setpoint resolution = 11 bits
- Current control accuracy
  - +/- 5mA for load currents less than 500 mA
  - +/- 1% for load currents greater than 500 mA
- Excellent immunity to large load supply voltage changes
- Integrated dither generator with programmable amplitude & frequency
- SPI interface for output control, diagnosis, and configuration
- Independent thermal shutdown for each channel
- Open load, switch bypass, and overcurrent protection and diagnosis for each channel
- Programmable slew rate control for reduced EMI
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE82453-3SA is a flexible, monolithic solenoid driver IC designed for the control of linear solenoids in automatic transmission, electronic stability control, and active suspension applications. The three channels can be used as either lowside or highside drivers in any combination. The device includes the drive transistor, recirculation transistor, and current sensing resistor; minimizing the number of required external components.

This device is capable of regulating the average current flow in a load up to 1500 mA, depending on the dither settings and the load characteristics, with 11 bits resolution. A triangular dither waveform generator, when enabled, superimposes a triangular waveform with programmable amplitude and frequency on the programmed current setpoint.

A 32 bit SPI interface is used to control thethree channels and to monitor the status of the diagnostic functions.

An active low reset input, RESN, is used to disable all of the channels and reset the internal registers to the default values. An active high enable pin, EN, is used to enable or disable the operation of the output channels. When the EN pin is low, the channels are disabled, and the SPI interface is fully functional. A fault output pin is provided to generate a signal that can be used as an external interrupt to the microcontroller whenever a fault is detected.

Type	Package	Marking
TLE82453-3SA	PG-DSO-36	TLE82453-3SA

2 Block Diagram

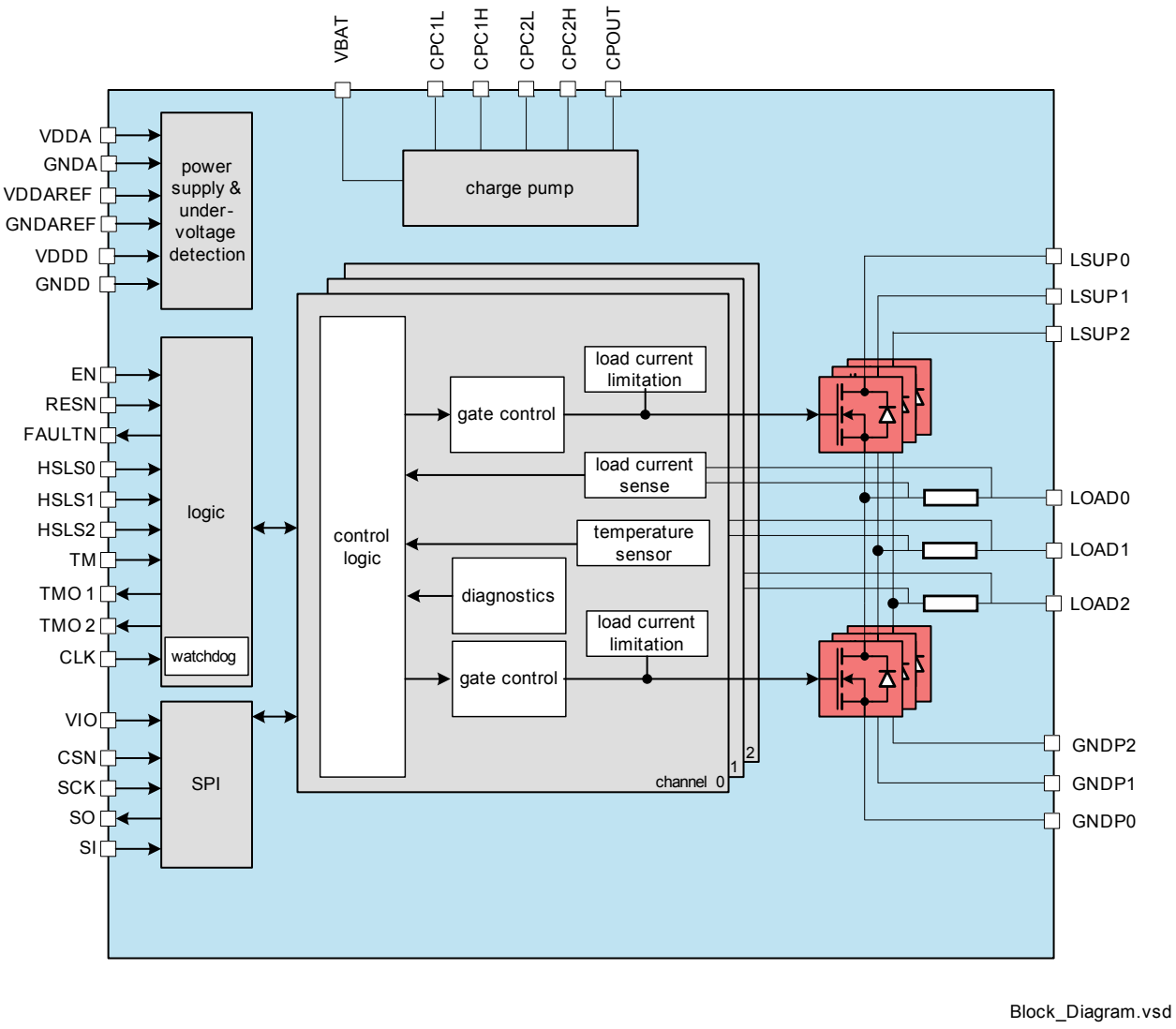

Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

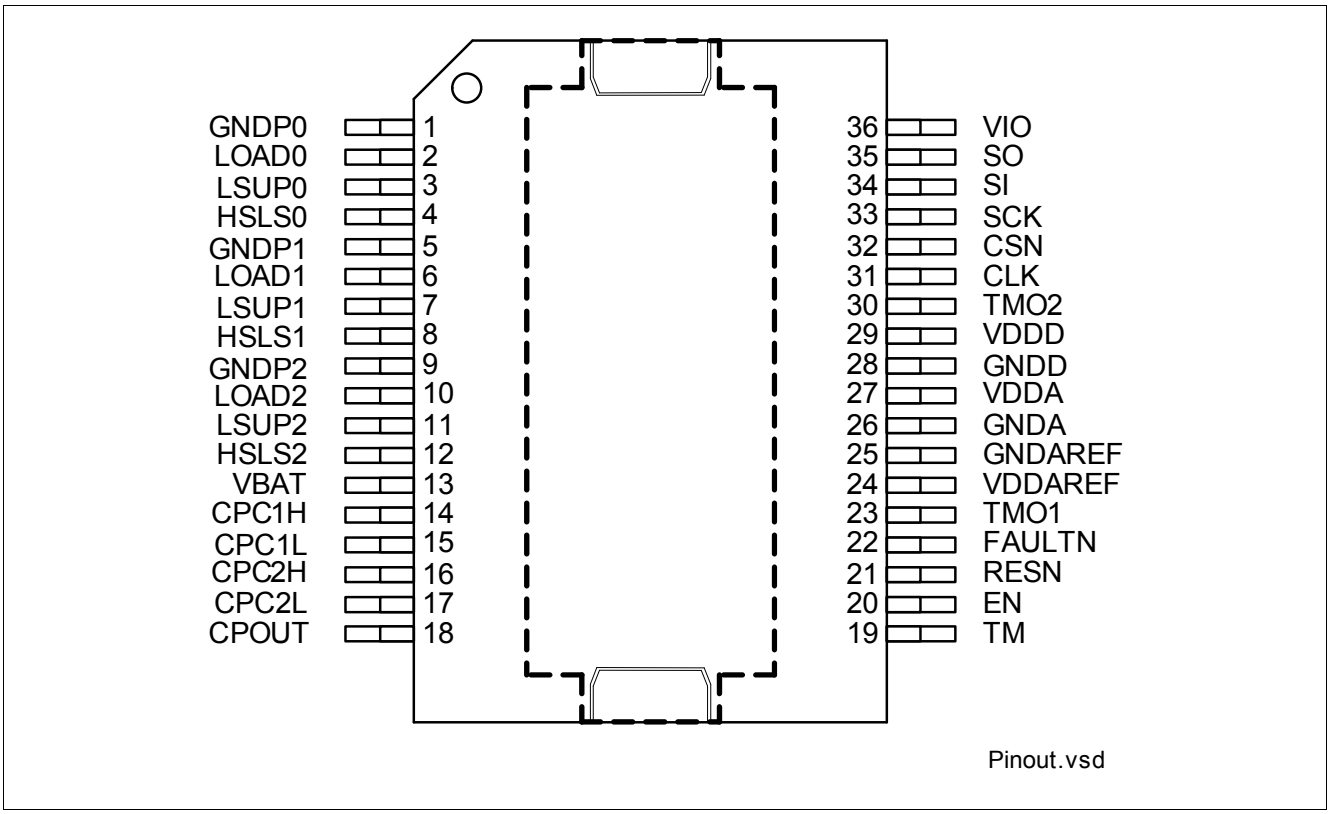

Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GNDP0	**Ground;** Ground connection for channel 0 power stage. Chip damaged if connection lost.
2	LOAD0	**Output** Connect a ceramic capacitor <= 10 nF to GND for ESD protection.
3	LSUP0	**Supply Voltage;** Supplies channel 0. Connect to Switched Battery Voltage with reverse protection diode and filter against EMC.
4	HSLS0	**Control Input;** Digital input. Connect to ground for high-side configuration. Connect to +5V or VBAT for low-side configuration.
5	GNDP1	**Ground;** Ground connection for channel 1 power stage. Chip damaged if connection lost.
6	LOAD1	**Output** Connect a ceramic capacitor of <= 10 nF to GND for ESD protection.

Pin	Symbol	Function
7	LSUP1	**Supply Voltage;** Supplies channel 1. Connect to Switched Battery Voltage with Reverse protection diode and filter against EMC.
8	HSLS1	**Control Input;** Digital input. Connect to ground for high-side configuration. Connect to +5V or VBAT for low-side configuration.
9	GNDP2	**Ground;** Ground connection for channel 2 power stage. Chip damaged if connection lost.
10	LOAD2	**Output;** Connect a ceramic capacitor of <= 10 nF to GND for ESD protection.
11	LSUP2	**Supply;** Supplies channel 2. Connect to Switched Battery Voltage with reverse protection diode and filter against EMC.
12	HSLS2	**Control Input;** Digital input. Connect to ground for high-side configuration. Connect to +5V or VBAT for low-side configuration.
13	VBAT	**Supply Voltage;** Connected to Battery Voltage with reverse protection diode and filter against EMC.
14	CPC1H	**Charge Pump;** For internal charge pump; connect a ceramic capacitor between CPC1H and CPC1L.
15	CPC1L	**Charge Pump;** For internal charge pump; connect a ceramic capacitor between CPC1H and CPC1L.
16	CPC2H	**Charge Pump;** For internal charge pump; connect a ceramic capacitor between CPC2H and CPC2L.
17	CPC2L	**Charge Pump;** For internal charge pump; connect a ceramic capacitor between CPC2H and CPC2L.
18	CPOUT	**Charge Pump Output** For internal charge pump; connect a ceramic storage capacitor from this pin to VBAT. This pin should not be connected to other external components or used as a supply for other circuits.
19	TM	**Test Pin;** connect to GND.
20	EN	**Control Input;** Digital input: 3.3V or 5.0V logic levels. Active high enable input.
21	RESN	**Control Input;** Digital input: 3.3V or 5.0V logic levels. Active low reset input.
22	FAULTN	**Status Output;** Open Drain output. In case not used, keep open.
23	TMO1	**Test Pin;** connect to GND.
24	VDDAREF	**Supply Voltage;** Supplies analog circuits. Connect to 5.0V supply voltage.
25	GNDAREF	**Ground;** Ground connection for analog circuits.
26	GNDA	**Ground;** Ground connection for analog circuits.
27	VDDA	**Supply Voltage;** Supplies analog circuits. Connect to 5.0V supply voltage.
28	GNDD	**Ground;** Ground connection for digital circuits.
29	VDDD	**Supply Voltage;** Supplies digital circuits. Connect to 5.0V supply voltage
30	TMO2	**Test Pin;** connect to GND.
31	CLK	**Clock Input;** Main system clock.
32	CSN	**SPI Chip Select Input;** Digital input: 3.3V or 5.0V logic levels.
33	SCK	**SPI Clock Input;** Digital input: 3.3V or 5.0V logic levels.

Pin	Symbol	Function
34	SI	**SPI Input;** Digital input: 3.3V or 5.0V logic levels.
35	SO	**SPI Output;** Push Pull output compatible to 3.3 V and 5.0 V logic levels.
36	VIO	**IO Supply;** Connected to 3.3 V or 5.0 V supply.
Cooling Tab	GND	Cooling Tab; internally connected to GND.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply Voltage	V_{BAT}	-0.3	–	45	V	–	P_4.1.1
Load Supply Voltage	V_{LSUP}	-0.3	–	45	V	–	P_4.1.2
Digital, Analog, and IO Supply Voltage	V_{DDD}, V_{DDA}, V_{DDAREF}, V_{IO}	-0.3	–	5.5	V	with respect to GNDD, GNDA, GNDAREF, and GNDPx	P_4.1.3
Input Voltage; SCK, CSN, SI, RESN, EN, TM, CLK	V_{INLV}	-0.3	–	V_{DDD}+ 0.3[2)]	V	–	P_4.1.4
Input Voltage; HSLS0, HSLS1, and HSLS2	V_{HSLSX}	-0.3	–	V_{BAT}+ 0.3[3)]	V	–	P_4.1.5
Open Drain Output; FAULTN	V_{FAULTN}	-0.3	–	V_{IO}+ 0.3[2)]	V	–	P_4.1.9
Push Pull Output; SO	V_{SO}	-0.3	–	V_{IO}+ 0.3[2)]	V	–	P_4.1.10
Voltage; LOADx	V_{LOAD}	-2	–	V_x+ 5 [4)]	V	$\|I_l\|$ < 1.6 A	P_4.1.11
Voltage; CPOUT	V_{CPOUT}	V_{BAT} - 0.3	–	50	V	–	P_4.1.12
Maximum Voltage; CPC1L, CPC2L	V_{CPCxL}	-0.3	–	50	V	–	P_4.1.13
Maximum Voltage; CPC1H, CPC2H	V_{CPCxH}	-0.3	–	50	V	–	P_4.1.14
Maximum Voltage; GNDPx	V_{GNDP}	-0.3	–	1.0	V	with respect to GNDD	P_4.1.15
Maximum Voltage; GNDA, GNDAREF	V_{GND}	-0.3	–	0.3	V	with respect to GNDD	P_4.1.16
Currents							
Output Current	I	-1.6	–	1.6	A	DC[5)]	P_4.1.17
Output Current, FAULTN Pin	I_{FAULTN}	0	–	20	mA	DC	P_4.1.18
Output Current, SO Pin	I_{SO}	-20	–	20	mA	DC	P_4.1.19

Table 1 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40 °C to +150 °C; all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Current; SCK, CSN, SI, RESN, EN, TM, CLK	I_{IN}	-5	–	5	mA	maximum allowable forward and reverse current through the ESD structure	P_4.1.20
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	continuous operation	P_4.1.21
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.22
ESD Susceptibility							
ESD Resistivity to GND	V_{ESD}	-2	–	2	kV	HBM[6)]	P_4.1.23
ESD Resistivity all pins[7)]	V_{ESD}	-2	–	2	kV	HBM[6)]	P_4.1.24
ESD Resistivity to GND	V_{ESD}	-500	–	500	V	CDM[8)]	P_4.1.25
ESD Resistivity Pin 1, 18, 19, 36 (corner pins)	$V_{ESD1,18,19,36}$	-750	–	750	V	CDM[8)]	P_4.1.26

1) Not subject to production test, specified by design.
2) Voltage must not exceed 5.5V.
3) Voltage must not exceed 45.0V.
4) VLOADx - VGNDPx and VLSUPx-VLOADx must not exceed 45.0V.
5) Compliant to short circuit requirements according to AEC-Q100-012.
6) ESD susceptibility, HBM according to EIA/JESD 22-A114B.
7) Pin VBAT vs. Pin CPC1H : +/- 1.5kV.
8) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Nominal Operation	V_{BATnom}	8	–	17	V	–	P_4.2.1
Extended Supply Voltage Range for Operation	$V_{BAT(ext)}$, $V_{LSUP\_UV(ext)}$	V_{LSUP_UV}	–	8	V	Parameter deviations possible	P_4.2.2
Extended Supply Voltage Range for Operation	$V_{BAT(ext)}$, $V_{LSUP(ext)}$	17	–	40	V	Parameter deviations possible	P_4.2.3
VBAT Supply Voltage transients slew rate	dV_{BAT}/dt	-1	–	1	V/µs	[1] –	P_4.2.4
Load Supply Voltage	V_{LSUP}	8	–	V_{BAT}+0.3 [2]	V	–	P_4.2.5
Load Supply Voltage transients slew rate	dV_{LSUP}/dt	-1	–	1	V/µs	[1] –	P_4.2.6
Digital Supply Voltage	V_{VDDD}	4.75	–	5.25	V		P_4.2.7
Analog Supply Voltage	V_{VDDA}, $V_{VDDAREF}$	4.75	–	5.25	V		P_4.2.8
Ground Offset Voltage; GNDA, GNDAREF	V_{GND}	-0.1	–	0.1	V	with respect to GNDD	P_4.2.9
IO Supply Voltage	V_{IO}	3.0	–	5.25	V	–	P_4.2.10
Voltage (static); LOADx	V_{LOADx}	-0.3	–	V+ 0.3	V	–	P_4.2.11
Voltage (dynamic); LOADx	V_{LOADx}	-2	–	V+ 5	V	$\|I_l\|$ < 1.6 A	P_4.2.12
System Clock Frequency	F_{SYS}	4	–	6	MHz	$F_{SYS} = F_{CLK} / F_{SYS\_div}$	P_4.2.13
CLK pin Frequency	F_{CLK}	8	–	40	MHz	–	P_4.2.14
SPI Clock Frequency	F_{SCK}	–	–	8	MHz	–	P_4.2.15
LOADx PWM Frequency	F_{LOAD}	100	–	4000	Hz	dependent on solenoid characteristics	P_4.2.16
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.17

1) Not subject to production test, specified by design.

2) VLSUPx - GNDD must not exceed 45.0V.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case[1)]	R_{thJC}	–	–	2	K/W	–	P_4.3.1
Junction to Ambient	R_{thJA}	–	15	–	K/W	[2)]	P_4.3.2

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

5 Input / Output

5.1 I/O Description

The CLK pin must be connected to a precise clock signal. This clock is used by the internal analog to digital converters and by the internal logic. A small internal pull down current will keep the voltage on this pin near ground when the pin is open. The device includes a programmable divider to generate the internal system clock from the CLK pin signal. This divider ratio is programmed in the CLK-DIVIDER register by the SPI interface. The output stages cannot be enabled until this field has been written.

An internal watchdog circuit will hold the device in an internal reset state if the delay between rising edges on the CLK pin is greater than the threshold time, T_{CLK_MSS}. The watchdog is initially disabled when the device exits the reset state. The watchdog is enabled by setting the WDEN bit in the CLK-DIVIDER register. If the watchdog is enabled, there are no settings which can prevent the fault pin being pulled low during a WD event.

Until the watchdog is enabled, the output stages are disabled. Once the watchdog function is enabled, a missing CLK signal will set the Watchdog Status Bit in the IC VERSION register, set the FAULTN pin to a logic low state, disable the output stages, and cause the device to enter an internal reset state. If the CLK signal is missing, the SPI response from the device will always be the response to an IC VERSION register read command. If the CLK signal returns after the watchdog function has triggered, the SPI response to a specific register read command will be the reset value of the specific register, except of the ICVID Register that is indicating the Watchdog timeout fault. Be aware that the CLK-DIVIDER is reset to 8 when the CLK is lost and than returns, which affects the system clock frequency (F_{SYS} = F_{CLK}/8) and thus the transfer delay time (see P_11.3.6).

In both cases it is not possible to write to any SPI register. To return to normal operation and exit this internal reset state the device must be reset externally by the RESN pin or an power on reset must be performed.

The EN pin is used to enable / disable the output stages. If the EN pin is low, all of the channels are disabled and (when the fault mask bit FME = 1) the FAULTN pin is pulled low. The SPI interface remains functional. However, when the EN pin is low, the EN bits in the SET-POINT registers are cleared. The EN pin can be connected to a general purpose output pin of the microcontroller or to an output of a safing circuit. However, all other SPI register settings remain unchanged. After the EN pin goes high the EN bits in the set point registers remain 0 until they are changed to 1. The EN bits will immediately return to 0 if the EN pin is low.

The RESN pin is the reset input for the device. If the RESN pin is low, the device is held in an internal reset state, the FAULTN pin is held low, and the SPI interface is disabled. An internal pull down current source will hold the RESN pin low in case the pin is open.

The FAULTN pin is an open drain output. This pin is pulled low when a fault is detected by the diagnosis circuit or when the device is in an internal reset state. An external resistor should be connected between this pin and the VIO supply.

The SI, SO, CSN, and SCLK pins comprise the SPI interface. See **Chapter 11**and **Chapter 12** for details.

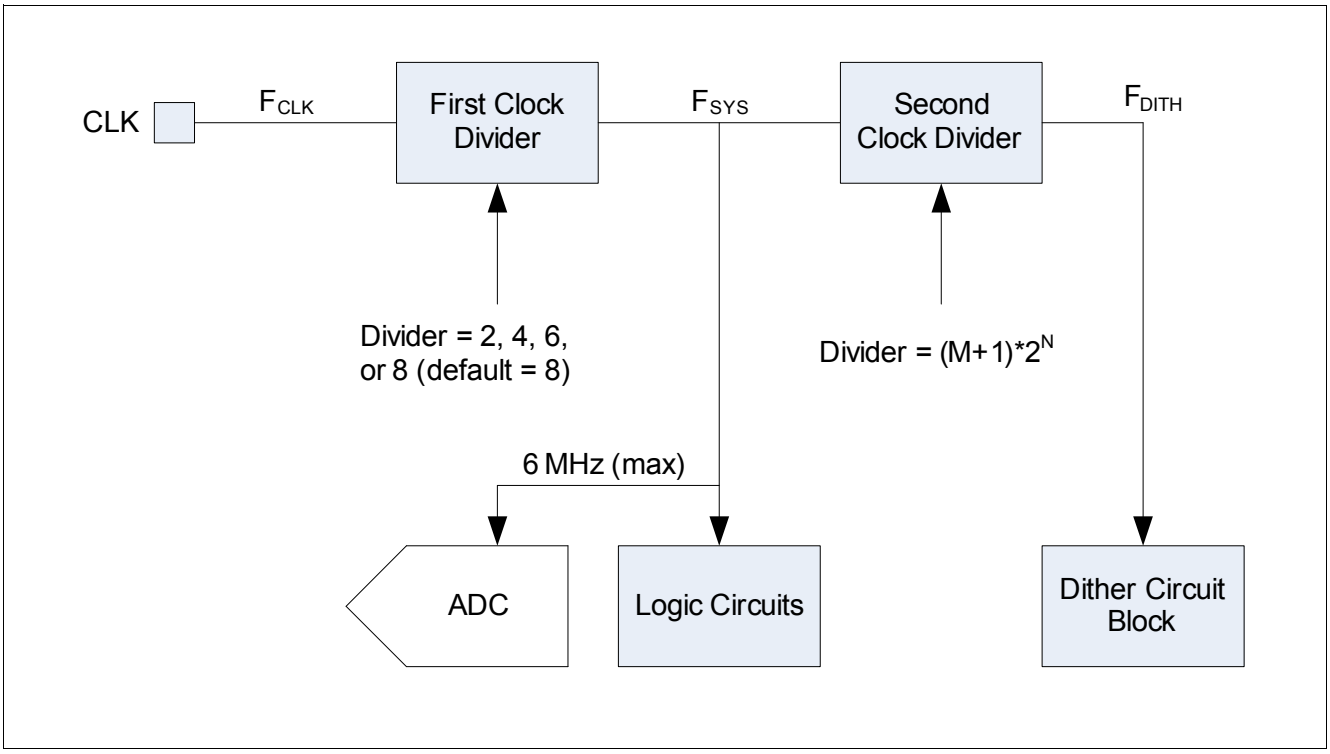

Figure 3 Clock Divider

5.2 Electrical Characteristics I/O

Table 4 Electrical Characteristics:

V_{BAT} = 8 V to 17 V, V_{DDx} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C, all voltages with respect to ground (GNDD), positive current flowing into pin
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Control Inputs EN, RESN, CSN, SI, SCK, CLK							
Input threshold - low	V_{IN_L}	0.8	–	–	V	V_{IN} increasing	P_5.2.1
Input threshold - high	V_{IN_H}	–	–	2.0	V	V_{IN} decreasing	P_5.2.2
Input hysteresis	V_{IN_HYS}	–	50		mV		P_5.2.3
Pull up current - CSN	I_{PU}	-50	–	-10	µA		P_5.2.4
Pull down current - EN, SI, SCK, CLK, RESN	I_{PD}	10	–	50	µA		P_5.2.5
Output SO							
Output low-level voltage	V_{SO_L}	0	–	0.5	V	I_{SO} = 0.5mA	P_5.2.6
Output high-level voltage	V_{SO_H}	V_{IO} - 0.5	–	V_{IO}	V	I_{SO} = -0.5mA, 3.0V < V_{IO} < 5.5V	P_5.2.7
Output tri-state leakage current	I_{SO_OFF}	-10	–	10	µA	V_{CSN}=V_{IO}	P_5.2.8
Output FAULTN							
Output low-level voltage	V_{FLT_L}	0	–	0.4	V	I_{FLT} = 2mA	P_5.2.9
Output tri-state leakage current	V_{FLT_OFF}	-10	–	10	µA		P_5.2.10

6 Power Supply

6.1 Overview

The TLE82453-3SA has multiple supply pins. The internal circuits are powered by three +5.0 V supply pins; VDDD, VDDA, and VDDAREF; and by one battery pin, VBAT. A separate supply pin, VIO, can be connected to either a 3.3 V or 5 V supply depending on the logic levels of the interfaced microcontroller I/O signals. The device includes a charge pump circuit which generates a supply voltage greater than VBAT.

6.2 Battery Supply (VBAT)

This pin is the supply for the internal charge pump and must be connected to the reverse polarity protected battery voltage supply. For correct operation the voltage on this pin must not be lower than the voltage on any of the LSUPx pins. This pin is also used by the overvoltage detection circuit.

6.3 Load Supplies (LSUP2, LSUP1, LSUP0)

These pins are the supply pins for thethree output stages. If the voltage on one of these pins is lower than the LSUP under voltage threshold, the respective power stage is disabled and the respective UVx fault bit is set in the DIAGNOSIS register. The LSUP pins of unused channels must be connected to VBAT.

6.4 Analog Supplies (VDDA and VDDAREF)

The VDDA pin is the supply for the internal analog circuits such as the amplifiers and analog-to-digital converters. The VDDAREF pin is the supply for the internal bandgap references. An externally regulated 5.0 VDC +/- 5% supply must be connected to these pins. A ceramic capacitor with a value of 100nF must be connected between each of these pins and ground near the IC.

These pins are monitored by a pair of internal comparators. The internal logic circuits are held in a reset state if the voltage on either of these pins is less than the threshold V_{DDA_UV} and V_{DDAREF_UV}.

6.5 Digital Supply (VDDD)

This pin is the supply for all of the internal logic circuitry. An externally regulated 5.0 VDC +/- 5% supply must be connected to this pin. A ceramic capacitor with a value of 100nF must be connected between this pin and ground near the IC.

This pin is monitored by an internal comparator. The internal logic circuits are held in a reset state if the voltage on this pin is less than the threshold V_{DDD_UV}.

6.6 I/O Supply (VIO)

This pin is used to supply the pins that interface with the external microcontroller. This pin must be connected to a supply with the same voltage, 3.3V or 5.0V, that is used to supply the peripherals of the microcontroller.

6.7 Power On Reset

An internal power on reset circuit holds the device in a reset state if any of the supplies VDDD, VDDA, or VDDAREF is below the respective undervoltage detection threshold. The device is also held in reset if the clock signal on the CLK pin is missing or the clock frequency is too low when the CLK pin watchdog is enabled. The power on reset is released after the following conditions. All of the supplies are above their respective threshold voltages then a fixed power on reset time (T_{POR}) elapses. The SPI interface can be accessed after the power on reset time.

The fault bit “RST” in the DIAGNOSIS register is set whenever the device exits the reset state. This bit is cleared automatically whenever the DIAGNOSIS register is accessed. The microcontroller can use this bit to determine if an internal or external reset has occurred.

6.8 Charge Pump

In order to provide low Rdson of the high-side mosfet transistors, a charge pump is used to drive the internal gate voltage above VBAT. The device uses a common charge pump for all channels. The charge pump uses the battery voltage supply connected to the VBAT pin. The charge pump output voltage at the CPOUT pin is regulated to typically 11V above the voltage at the VBAT pin.
The charge pump circuit requires three external capacitors. A reservoir capacitor with a recommended value of 220nF must be connected between the CPOUT pin and the VBAT pin. Two pump capacitors with recommended values of 27nF must be connected between the CPC1L and CPC1H pins and also between the CPC2L and CPC2H pins. A built in supervisor circuit checks if the charge pump output voltage is sufficient to control the high-side mosfet transistors. If the VCPOUT voltage is less than the charge pump undervoltage threshold, the output transistors are disabled and the CPUV fault flag is set in the DIAGNOSIS register. A separate CPW (Charge Pump Warning) fault bit in the DIAGNOSIS register is set if the VCPOUT voltage is below the CP warning threshold voltage. The device will continue to operate normally when the VCPOUT voltage is between the CPW threshold and the CPUV threshold, however the current control accuracy may be outside of the specification limits.

6.9 Sleep Mode

If any one of the VDDD, VDDA, and VDDAREF voltage supplies is below the respective undervoltage threshold, the device enters sleep mode. The current drawn into the VBAT pin is reduced during this mode of operation. Sleep mode is automatically exited when all of the VDDD, VDDA, and VDDAREF supply pins are above the respective undervoltage threshold. The sleep mode has the same effect as a reset and follows the Initialization Sequence.

6.10 Power Supply Modes

The following table describes the operation of the device with all possible power supply modes of VBAT, VCPOUT, VDDD, VDDA, VDDAREF, and VIO. The “X” symbol means that the state of this supply does not effect the result (can be either supplied or not supplied) in the specific case.

VDDD	< VDDx_UV	X	X	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV
VDDA	X	< VDDx_UV	X	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV
VDDAREF	X	X	< VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV
RESN	X	X	X	LOW	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CLK	X	X	X	X	TCLK > TCLK_MSS	TCLK > TCLK_MSS	TCLK < TCLK_MSS	TCLK < TCLK_MSS	TCLK < TCLK_MSS	TCLK < TCLK_MSS	TCLK < TCLK_MSS	TCLK < TCLK_MSS
VIO	X	X	X	X	> 3.0V	> 3.0V	0V	> 3.0V	> 3.0V	> 3.0V	> 3.0V	> 3.0V
WDEN	X	X	X	X	LOW	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
EN	X	X	X	X	X	X	HIGH	LOW	HIGH	HIGH	HIGH	HIGH
VCPOUT - VBAT	X	X	X	X	X	X	> CPUV	X	< CPUV	> CPUV	> CPUV	> CPUV
VBAT	X	X	X	X	X	X	< VBATOV	X	X	> VBATOV	< VBATOV	< VBATOV
VLSUP$_x$	X	X	X	X	X	X	> VLSUPUV	X	X	X	< VLSUPUV	> VLSUPUV
Sleep Mode	YES	YES	YES	NO	NO	NO	NO	NO	NO	NO	NO	NO
Watchdog Fault	NO	NO	NO	NO	NO	YES	NO	NO	NO	NO	NO	NO
Channel Operational	NO	NO	NO	NO	NO	NO	YES	NO	NO	NO	NO (Channel X only)	YES
SPI Functional	NO	NO	NO	NO	YES	NO Response is ICVID	INPUT – YES Response is 0000$_H$	YES	YES	YES	YES	YES
Diagnostics Functional	NO	NO	NO	NO	NO	NO	YES	NO Load faults are detected	YES	YES	YES	YES
FAULTN	LOW	LOW	LOW	LOW	LOW	LOW	Undefined	LOW (1)	LOW	LOW	LOW (4)	HIGH
RST bit	HIGH (2)	HIGH (2)	HIGH (2)	HIGH (2)	HIGH (3)	HIGH (3)	unchanged	unchanged	unchanged	unchanged	unchanged	unchanged

Figure 4 Power Supply Mode Diagram

The X's indicate a don't care condition for all the states below the double line.

1. The FAULTN pin is LOW if the FME fault mask bit is set to 1
2. The RST bit in the DIAGNOSIS register will be set after the device exits the reset state
3. A missing CLK signal will result in a reset only if the CLK Watchdog has been enabled
4. The FAULTN pin is LOW if the FMx fault mask bit is set to 1

6.11 Initialization

The following figure illustrates the initialization sequence for the device after power-up. The T_{POR} cycle begins on the first CLK clock cycle after the RESN pin transitions from low to high.

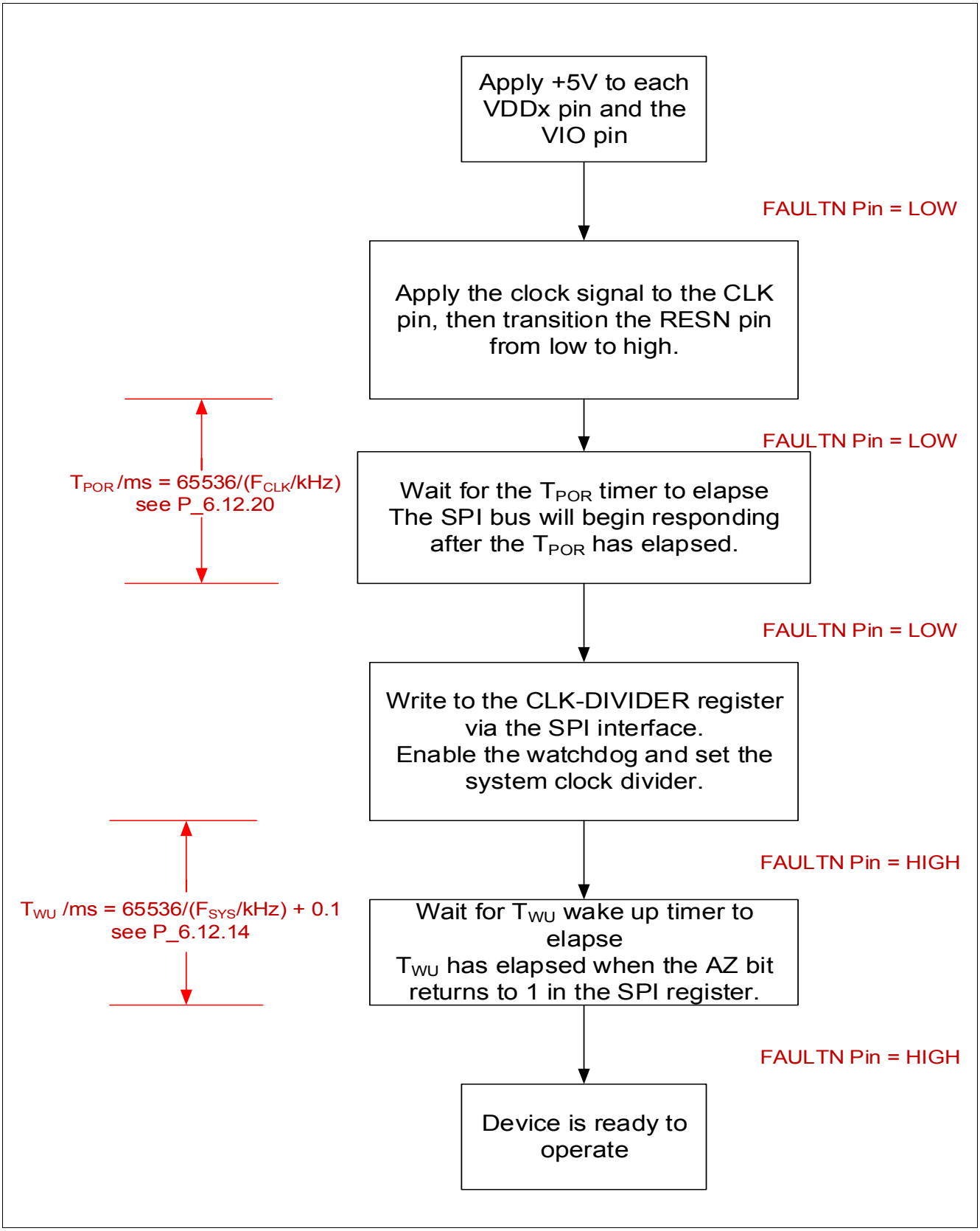

Figure 5 Initialization Sequence

6.12 Reset

If the device needs to be shut down during operation the RESN pin can be pulled low. The RESN pin should be held low until the current flowing in the solenoid decays to zero. If the device is restarted with current flowing in the solenoid the auto zero function will enter the value as an offset, causing an error in the current control.

6.13 Electrical Characteristics

Table 5 Electrical Characteristics: Power Supply

V_{BAT} = 8 V to 17 V, V_{DDx} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C, CPC1 and CPC2 = 27nF CPCOUT = 220nF, all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
VBAT Current Consumption normal mode	I_{VBAT}	–	–	10	mA	all channels active	P_6.12.1
VBAT Current Consumption sleep mode	I_{VBAT_SLP}	–	–	8	µA		P_6.12.2
VDDD Current Consumption	I_{VDDD}	–	–	20	mA		P_6.12.3
VDDA Current Consumption	I_{VDDA}	–	–	13	mA		P_6.12.4
VDDAREF Current Consumption	$I_{VDDAREF}$	–	–	4	mA		P_6.12.5
VIO Current Consumption	I_{VIO}	–	–	1	mA	CSN=V_{IO}=5.25V	P_6.12.6
Undervoltage reset (internally generated) - VDDA	V_{DDA_UV}	3.8	–	4.3	V	V_{DDA} decreasing	P_6.12.7
Undervoltage reset (internally generated) - VDDAREF	V_{DDAREF_UV}	3.8	–	4.3	V	V_{DDAREF} decreasing	P_6.12.8
Undervoltage reset (internally generated) - VDDD	V_{DDD_UV}	3.8	–	4.3	V	V_{DDD} decreasing	P_6.12.9
Undervoltage hysteresis	V_{UV_HYS}		150		mV		P_6.12.10
LSUP undervoltage threshold	V_{LSUP_UV}	4.5		5.5	V		P_6.12.11
Missing CLK clock detection time	T_{CLK_MSS}	2	–	10	µs		P_6.12.12
Power On Reset time initialized with RESN	T_{POR}	–	–	0.1	ms	[1)]Logic circuits are functional after T_{POR} timer	P_6.12.13
Power On Reset time initialized with undervoltage reset	T_{POR}	–	–	T_{POR} =65536/ (F_{CLK}/kHz)	ms	[1)]Logic circuits are functional after T_{POR} timer	P_6.12.20

Table 5 Electrical Characteristics: Power Supply (cont'd)

V_{BAT} = 8 V to 17 V, V_{DDx} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C, CPC1 and CPC2 = 27nF CPCOUT = 220nF, all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power-on wake-up time	T_{WU}	–	–	T_{WU} =65536/ (F_{SYS}/kHz) + 0.1	ms	1)Timer starts after writing to the CLK-DIV register, (CSN goes high) all supplies are above the UV thresholds and RESN pin is high. Output stages are functional after T_{WU} 2)	P_6.12.14
Charge Pump							
Charge pump voltage	V_{CP_OUT}	V_{BAT}+8	–	V_{BAT} +13 3)	V		P_6.12.15
Charge pump clock frequency	F_{CP}	–	65	–	KHz	F_{SYS} = 6 MHz 4)	P_6.12.16
Charge pump warning threshold voltage	V_{CPOUT_W}	V_{BAT}+7	–	V_{BAT}+ 8.5	V		P_6.12.17
Charge pump undervoltage threshold voltage	V_{CPOUT_UV}	V_{BAT} +4.5	–	V_{BAT} +5.5	V		P_6.12.18
Charge pump overvoltage clamp	V_{CPOUT_OV}	–	48.5	–	V		P_6.12.19

1) Not subject to production test, specified by design.
2) To guarantee a proper Autozero result there must not be any I_{LOAD} during power-on wake-up (**Chapter 8.7**).
3) Will not exceed V_{CPOUT_OV}.
4) Parameter not subject to production test, specified by design.

Attention: Voltage Ratings for Charge Pump caps: CPC1/CPC2: Vmin=VBATmax + 10V, CCPOUT: Vmin=16V

7 Power Stages

7.1 Overview

There are three output channels implemented in this device. The output power stages of each channel consists of a half bridge made up of two n-channel DMOS transistors and a current sensing resistor. An internal charge pump generates the voltage required to switch the n-channel DMOS high-side switches. The switches are protected from external failures by built in overcurrent and overtemperature detection circuits.

The half bridge arrangement allows the use of active freewheeling, which reduces the power dissipation of the device.The arrangement also allows each channel to be individually programmed for lowside or highside drive. The output current slew rate of the power stages can be programmed to one of three values by programming the CONFIGURATION register by SPI.

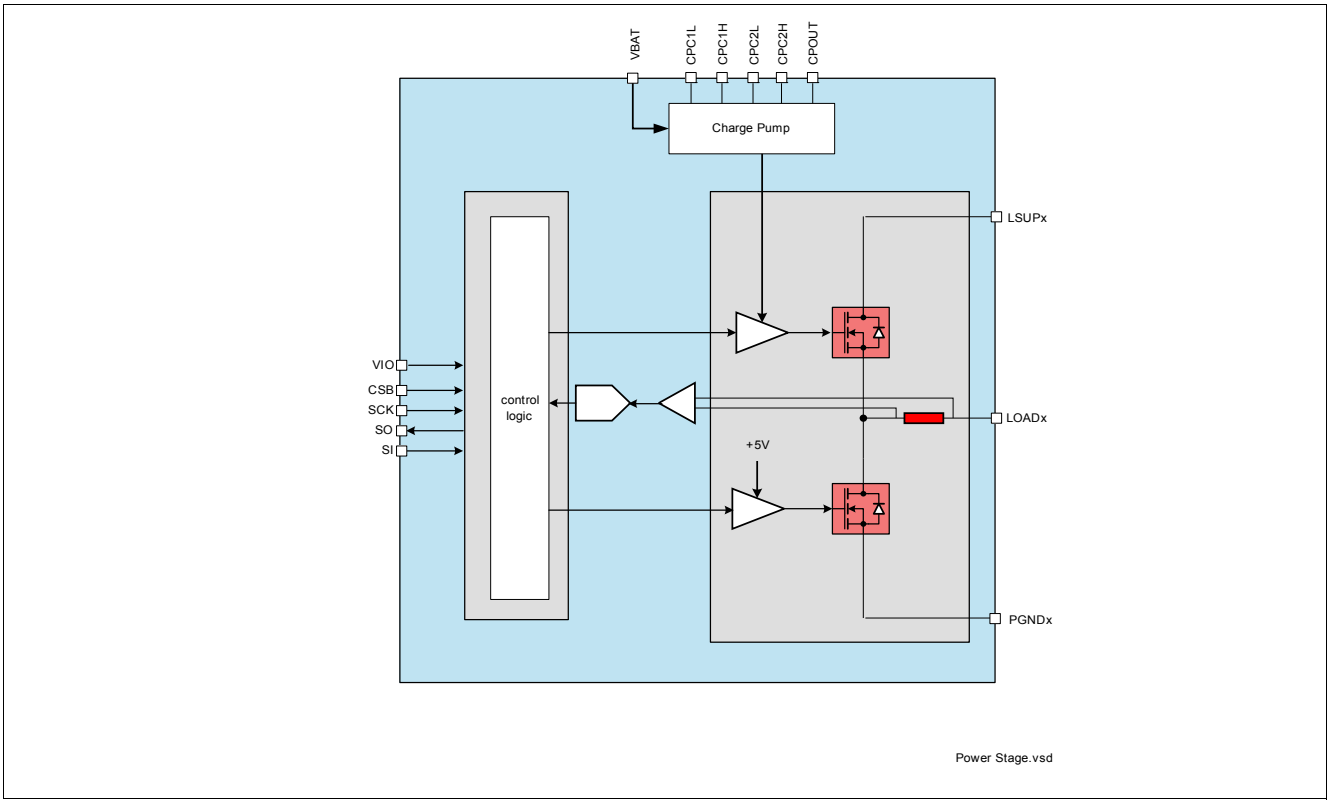

Figure 6 Power Stages

7.2 Channel Disabled

When the channel is disabled, both transistors of the half bridge are turned off. The output stage is in a high output impedance state in this condition. The channel is disabled if the EN pin is 0, or the EN bit is 0, or the set point = 0.

7.3 Channel Enabled

When a channel is configured for lowside operation, the lowside DMOS switch is the “drive” switch and the highside DMOS switch is the “recirculation” switch. Likewise, when a channel is configured for highside operation, the highside DMOS switch is the “drive” switch and the lowside switch is the “recirculation” switch. In normal operation, the “drive” switch is turned on and off with the duty cycle needed to regulate the solenoid current at the target value. During the time that the “drive” switch is turned off, the device is in active freewheeling mode. The “recirculation” switch is turned on in this mode to reduce the voltage drop across the device during recirculation.

The transistors are controlled in a way that prevents shoot through current during switching, that is the control logic prevents the simultaneous activation of both the “drive” switch and the “recirculation” switch. If the EN pin is low, the EN bit is pulled to 0. If the EN pin changes from low to high, the EN bit remains unchanged.

7.4 Configuration of Channels

The pins HSLS0, HSLS1, and HSLS2 are used to configure each channel for highside or lowside operation. The pin must be connected to ground for highside operation and to VBAT or + 5V for lowside operation. The configuration of each channel can be verified by reading the CONFIGURATION register via SPI.

7.5 Electrical Characteristics Power Stages

Table 6 Electrical Characteristics: Power Stages

V_{BAT} = 8 V to 17 V, V_{DDx} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C, all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
LSUPx leakage current	I_{LSUP_LKG}	-150	–	150	µA	set-point = 0mA 8V < V_{LSUP} < V_{BAT} + 0.3V	P_7.6.1
LSUPx leakage current in sleep mode	$I_{LSUP\_LG\_SLP}$	-50	–	50	µA	Sleep mode All VDDx=0V	P_7.6.2
On-State Resistance - high side FET	$R_{DS(ON)\_HS}$	–	–	250	mΩ	T_j = 150°C; I_{LOAD} = -1.6A	P_7.6.3
On-State Resistance - low side FET	$R_{DS(ON)\_LS}$	–	–	250	mΩ	T_j = 150°C; I_{LOAD} = 1.6A	P_7.6.4
LOADx leakage current	I_{LOAD_LKG}	-300	–	0	µA	set-point = 0mA 8V < V_{LSUP} < V_{BAT} + 0.3V; 0V < V_{LOAD} < V_{LSUP}	P_7.6.5
LOADx leakage current in sleep mode	$I_{LOAD\_LKG\_SLP}$	-80	–	80	µA		P_7.6.6
Current rise and fall times - SR0	$T_{R0,}$ $T_{F0,}$	–	1[1)]	–	µs	I_{LOAD} = 1.4A; 8V < V_{LSUP} < V_{BAT} + 0.3V; 20% to 80% ΔI_{LSUP} & ΔI_{GNDP}	P_7.6.7
Current rise and fall times - SR1	$T_{R1,}$ T_{F1}	–	0.5[1)]	–	µs	I_{LOAD} = 1.4A; 8V < V_{LSUP} < V_{BAT} + 0.3V; 20% to 80% ΔI_{LSUP} & ΔI_{GNDP}	P_7.6.8
Current rise and fall times	$T_{R2,}$ T_{F2}	–	2[1)]	–	µs	I_{LOAD} = 1.4A; 8V < V_{LSUP} < V_{BAT} + 0.3V; 20% to 80% ΔI_{LSUP} & ΔI_{GNDP}	P_7.6.9
Voltage slew rate SR0		–	5	–	V/µs		P_7.6.10
Voltage slew rate SR1		–	10	–	V/µs		P_7.6.11
Voltage slew rate SR2		–	2.5	–	V/µs		P_7.6.12
Current Sense Resistor							
Sense resistor resistance	R_{SENSE}	–	250	380	mΩ		P_7.6.13

1) Not subject to production test, specified by design.

8 Current Control

8.1 Overview

The device has independent controller blocks for each channel. Each control loop consists of the average current setpoint input, the dither generator, the load current feedback path, the controller block, and the output stage.

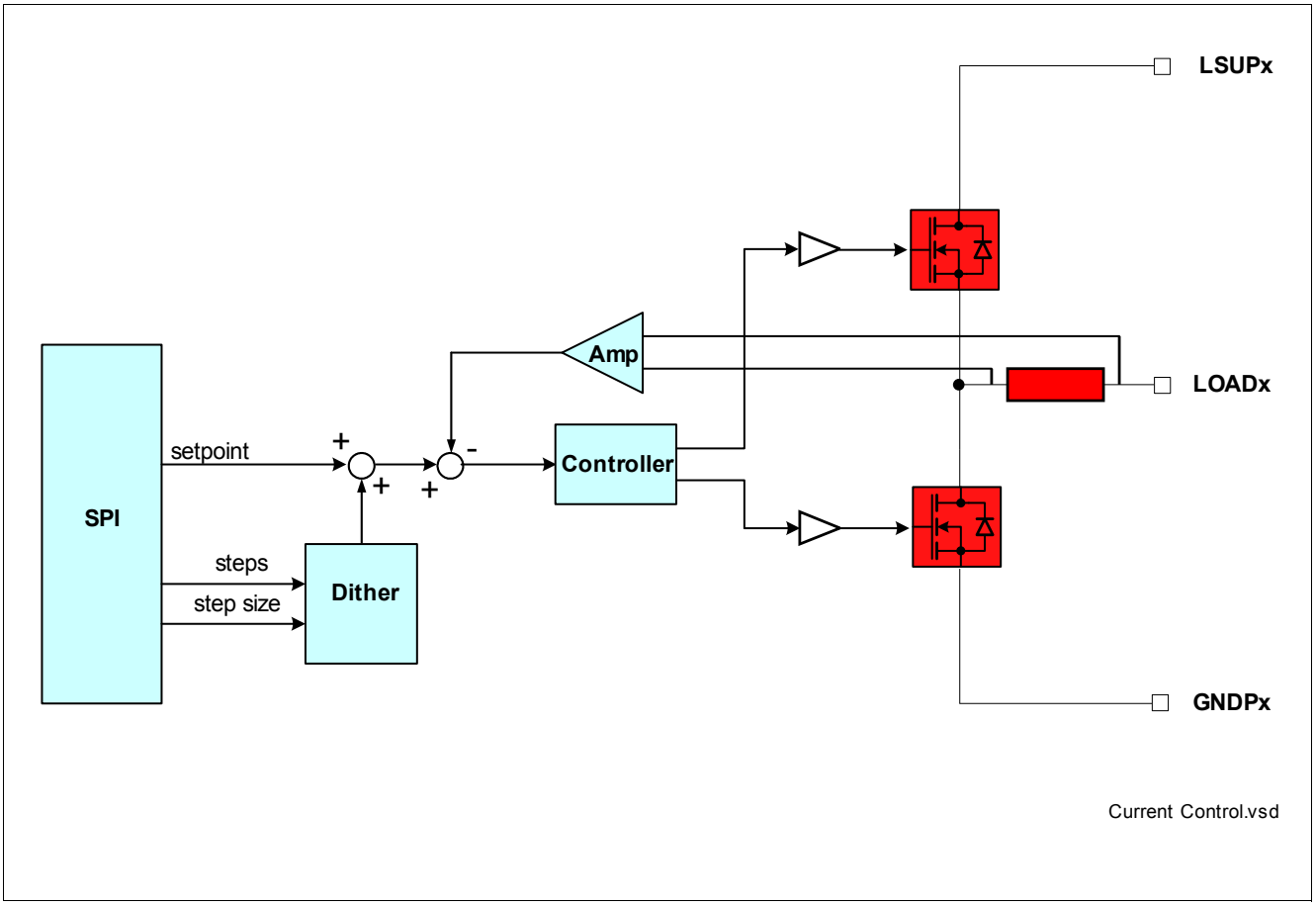

Figure 7 Controller Block Diagram

8.2 Average current setpoint

The average current setpoint value is determined by the contents of the SETPOINT register. The relationship between the value of the setpoint register and the average load current is shown in **Figure 8**.The accuracy band of the current regulation is also shown in **Figure 8**. The accuracy is specified over the normal operating range of the device (including the full normal operating junction temperature range). An automatic auto-zero feature is included in the device. The auto-zero feature will automatically measure the offset of the current measurement circuits of each channel after power-up. When a channel is programmed to regulate current, the offset is compensated by an automatic modification of the setpoint. The content of the SPI accessed average current setpoint register is not influenced by the autozero circuit.

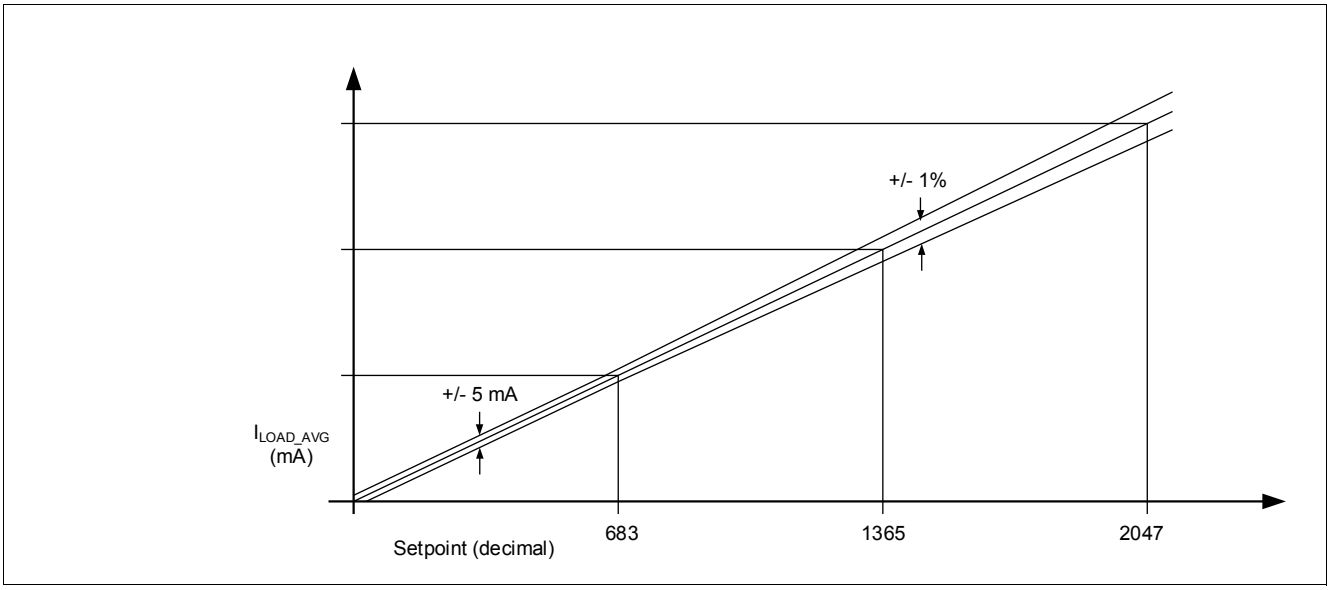

Figure 8 Output current transfer function and accuracy

8.3 Dither waveform

A triangular dither waveform can be added to the average current setpoint in order to reduce the hysteresis of the driven solenoid valve. The dither waveform is shown in **Figure 9**. The frequency of the dither waveform is set by programming the STEPS field in the DITHER register. The value of the STEPS field determines the number of dither steps in one quarter of the dither waveform. The time duration of each step is set by programming the N and M fields in the CLOCK-DIVIDER register. The amplitude of the signal is determined by the contents of the STEPS field and the contents of the STEP SIZE field of the DITHER register (see **Figure 9**). The application software must take care that the product of the steps and stepsize does not exceed 0x03FF hex. When dither is disabled or a new value is entered, the current dither period will be completed.

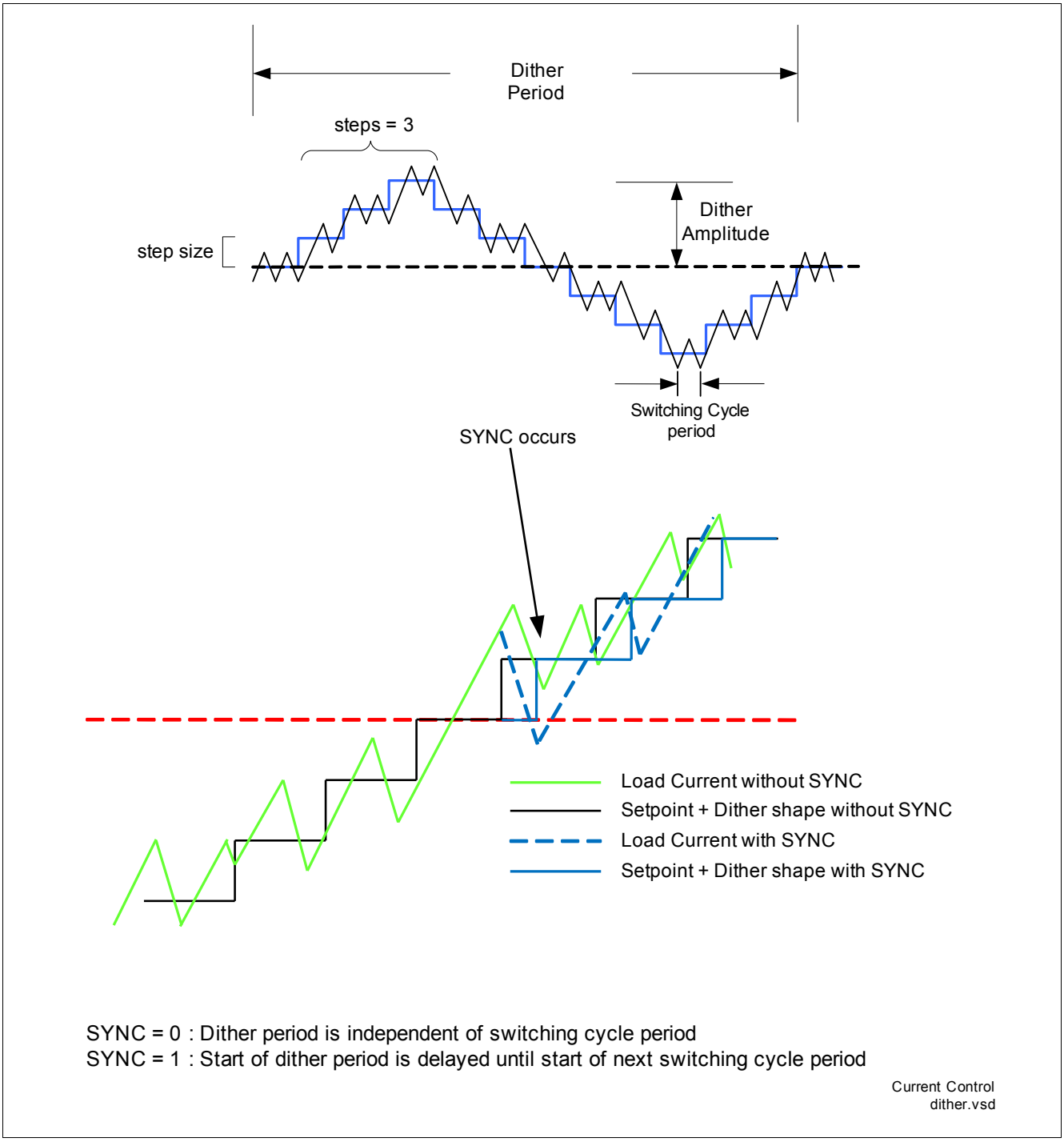

Figure 9 Dither Waveform

The dither waveform can be synchronized to the PWM frequency by setting the SYNC bit in the DITHER register. When the SYNC bit is set to 0, the triangular dither waveform is free-running and is asynchronous to the PWM frequency. When the SYNC bit is set to 1, a new dither period will not start until the start of the next PWM cycle. The start of a PWM cycle period is defined to be when the output stage turns on. The start of a dither period is defined to be when the dither increases one step above zero on this rising slope of the waveform.

8.4 Sense Resistor

The current sense resistor is integrated into the device. The initial error and the temperature drift of this resistor are measured and trimmed during the device manufacturing process.The internal protection circuits are built in a way, that repeated shorts to VBAT/GND will not destroy the internal shunt.

8.5 Current Controller

The current controller regulates the load current by alternatively turning on the drive switch and the recirculation switch. The on time of the drive switch is determined by the integrated PWM period controller. The off time of the transistor is determined by the average current controller. When the average load current over the current PWM period is equal to the setpoint during freewheeling, the drive transistor is turned on again and the next PWM cycle is started.

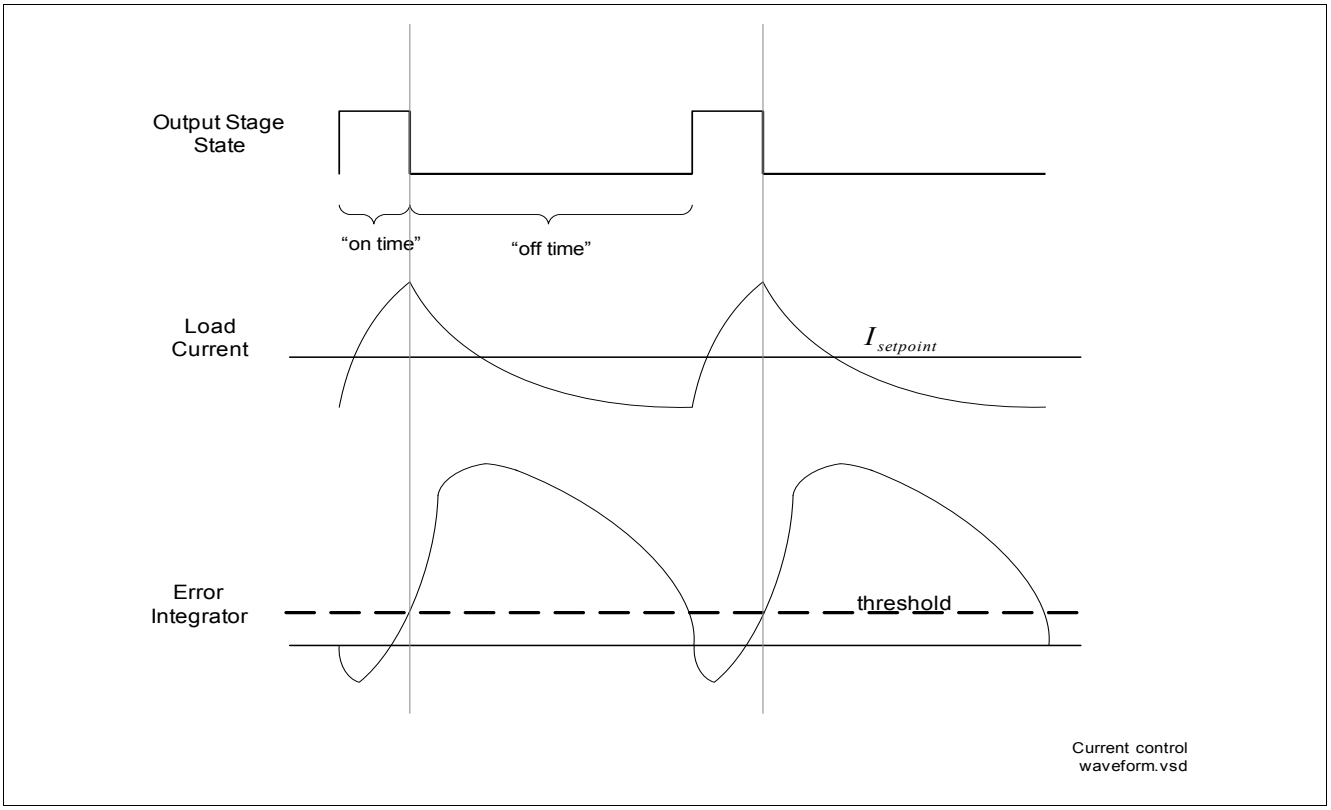

Figure 10 Controller waveforms

The controller includes an integrator which integrates the difference between the average load current and the setpoint over the time duration of the PWM cycle. At the start of a PWM cycle, the driving FET is turned on and the recirculation FET is turned off. In this phase of operation, the load current will increase. When the value of the error integrator exceeds the integrator threshold, the driving FET is turned off and the recirculation FET is turned on. The load current will decrease in this phase of operation. The integrator threshold is adjusted automatically by the internal PWM period controller until the desired PWM period is reached. When the error integrator decreases to 0, the recirculation FET is turned off and the driving FET is turned on to start the next PWM cycle.

The integrator can be automatically limited by the device after a change in setpoint by setting the Auto-Limit bit in the SETPOINT register. The device will limit the integrator output to a small value (+/- 20d) during the setpoint change and then automatically revert back to the normal integrator limit values after the setpoint change has been achieved when this bit is set. The bit remains set until changed, or a reset occurs.
A "Regulator Error" fault bit in the DIAGNOSIS register is set when the programmed setpoint current is not reached after 8 PWM cycles after the SETPOINT register is written.

8.6 PWM Frequency Controller

The integrated PWM Frequency controller regulates the PWM Frequency using an “Integral” control loop with a programmable gain, KI. This control loop monitors the actual PWM period and compares it to the PWM period setting in the PWM Period Register. The error in the PWM period is multiplied by the gain KI and then integrated at each PWM cycle. The output of the controller adjusts the “on time” of the PWM signal until the actual PWM period matches the programmed PWM period.

KI gains of 1, 1/2, 1/4, 1/8, 1/16, 1/32, and 1/64 can be selected in the PWM Period Register. The KI value of 1, KI_index =0, has the fastest response time, the KI value of 1/64, KI_index=6, has the slowest response time, but with less overshoot and less ringing. KI_index = 6 is the recommended setting for initial evaluation.

8.7 Autozero

Each channel has an autozero function which measures and compensates for the offset of analog current measurement circuits. The autozero function is automatically initiated during power-up after the first write to the CLK-DIVIDER register, or with a reset “RESN” after the first write to the CLK-DIVIDER register. The function can also be initiated by the user by setting the AZ start bit in the AUTOZERO SPI message. The EN bit in the SETPOINT register must be set to 0 to initiate the auto-zero function. This AZ START bit is automatically cleared by the device when the autozero sequence is complete. The measured offset of current measurement circuits can be read by the micro controller via the SPI message AUTOZERO. Autozero functions with the EN pin in the high or low state.

Care must be taken if the device enters Autozero while current is flowing in the solenoid. This can occur if the device is reset or the Autozero bit is set, while current is flowing in the solenoids. The current will create an unintended offset. During initialization or if a reset occurs during operation the device should be held in reset until the current decays to zero. During normal operation an Autozero should not be initiated until the solenoid current decays to zero. The time is determined by the inductance of the solenoid, which can be calculated or measured.

8.8 Measurement Functions

The SPI register FEEDBACK can be read to access the value of the load current measured by the device and the value of the output PWM period. The CFB bit in the DITHER register selects between two measurement types. When CFB=0, the average current and the switching period are measured over each switching cycle. When CFB=1, the maximum current and minimum currents are measured over a dither cycle. Also the number of switching cycles occurring in the last dither cycle is measured.

When the CFB bit = 0 and the device is not in calibration mode, the FEEDBACK register contains a 12 bit Current Feedback field. The content of this field represents the integration of the load current measured by the analog current measurement circuit blocks over the most recent switching period. The average load current can be calculated according to the equation I_load_avg = 1.5* Current Measurement_Feedback / Period Measurement Feedback.

When the CFB bit = 0 and the device is not in calibration mode, the actual output frequency of each channel can be determined by reading the 12 bit Period Feedback field in the FEEDBACK register. This field contains the number of system clocks (Fsys) counted during the most recently completed PWM period divided by 16, this is the same resolution as the PWM set register.

When the CFB bit = 1 and the device is not in calibration mode, the FEEDBACK register contains two 8 bit Current Feedback (CFB) fields. The contents of these fields represent the minimum and maximum load current measured by the analog current measurement circuit blocks over the most recent dither cycle when dither is enabled. Otherwise, these fields contain the minimum and maximum load current values since the last read of the FEEDBACK register. I min and I max = 1.5* readout / 127.

When the CFB bit = 1 and the device is not in calibration mode, the FEEDBACK register contains an 8 bit field which contains the number of full switching cycles in the last dither cycle. This information can be used by the

microcontroller to calculate the average switching cycle period over a dither period. If dither is disabled, the contents of this register is 0.

The contents of the feedback registers are 0 when the respective channel is not operating. The number of PWM cycles per dither cycle value is 0 if dither is disabled.

8.9 Calibration Mode

In case the accuracy of the current regulation must be improved by module calibration, the TLE82453-3SA device includes a calibration mode of operation. In order to enter calibration mode, the CM bit in the CALIBRATION register must be set by writing a 1 to this bit location. Calibration mode will not be entered unless the setpoint for all three channels are zero and the EN enable bit (in the SETPOINT register) is set to 1. If one or more of the channels is not off and a 1 is written to the CM bit, the write command is ignored and the CM bit will remain at 0. In the Calibration Mode of operation, the individual transistors of the output stages can be controlled by writing to the CALx bits in the CALIBRATION register. The resulting output current will be measured by the device and can be monitored by reading the FEEDBACK register. When the device is in calibration mode, the FEEDBACK register contains a 16 bit field which represents the average load current measured during the calibration. Ical = 1.5 * readout / 65535. The Current Feedback Register is not valid if the PWM period is set to 0x00 hex in the PWM Register.

Current limitation is not active during calibration mode. Exceeding 1.5 A may damage the device.

8.10 Electrical Characteristics

Table 7 Electrical Characteristics: Current Control

V_{BAT} = 8 V to 17 V, V_{DDx} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Average Current Regulation							
Current measurement range	I_{MEAS}	0	–	1500[1]	mA	target	P_8.10.1
Current setpoint resolution	I_{SPRES}	–	1500 / 2047	–	mA		P_8.10.2
Output current accuracy	$I_{SPACCL1}$	-5	–	5	mA	0A < I_{LOAD} < 0.5A -40°C < T_j < 125°C	P_8.10.3
Output current accuracy	$I_{SPACCH1}$	-1	–	1	%	0.5A<I_{LOAD} <1.5A -40°C < T_j < 125°C	P_8.10.4
Output current accuracy	$I_{SPACCL2}$	-7.5	–	7.5	mA	0A < I_{LOAD}< 0.5A -40°C < Tj < 150°C	P_8.10.5
Output current accuracy	$I_{SPACCH2}$	-1.5	–	1.5	%	0.5A< I_{LOAD}<1.5A -40°C < Tj < 150°C	P_8.10.6
Accuracy Lifetime Drift	–	–	0.25%	–	–	[2]	P_8.10.7
PWM period control							
PWM period range	t_{PWM_RNG}	16	–	65535	cycles	F_{SYS} cycles[3]	P_8.10.8
PWM period resolution	t_{PWM_RES}	–	16	–	cycles /lsb	F_{SYS} cycles	P_8.10.9
Dither							
Dither amplitude range	I_{DARNG}	0	–	46	mA	steps = 1	P_8.10.10
Dither amplitude resolution	I_{DARES}	–	0.73	–	mA	steps = 1	P_8.10.11
Dither period range	T_{DRNG}	0.007	–	100,000	ms		P_8.10.12

1) The maximum obtainable average current value is dependent on the chosen PWM frequency, the chosen dither amplitude, and the load impedance.
2) This value corresponds to the maximum evaluated life time drift according to AEC-Q100 grade 1.
3) The minimum and maximum achievable PWM frequencies depend on the load characteristics.

9 Protection Functions

9.1 Overview

The device provides embedded protection functions which are designed to prevent IC destruction under fault conditions described in this datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are neither designed for continuous nor for repetitive operation. There are overload, overtemperature, and overvoltage protection circuits implemented in this device.

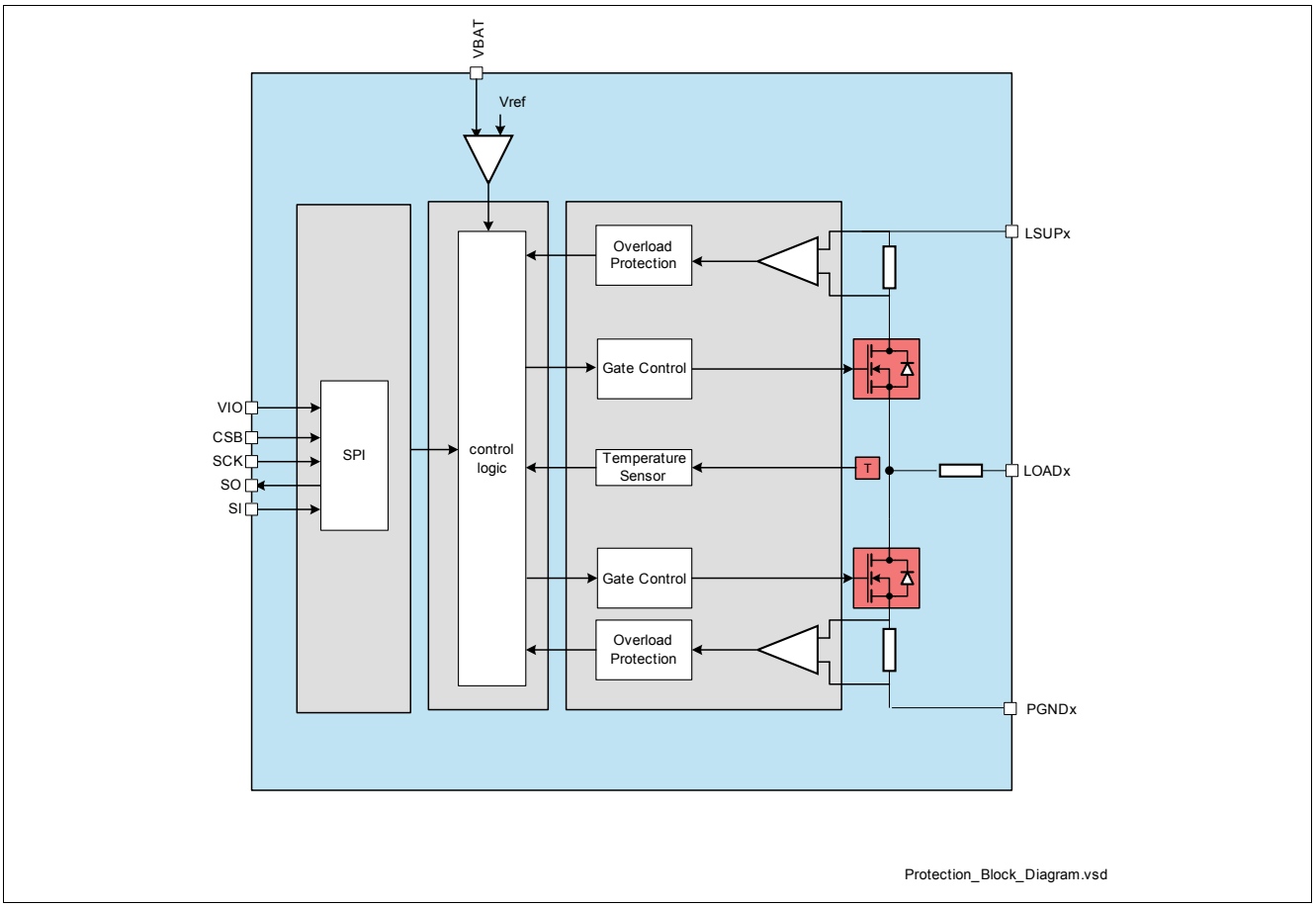

Figure 11 Protection Functions Block Diagram

9.2 Overcurrent Protection

The load current is limited by the device itself in case of overload. An overload can be caused by a short to ground when the channel is configured for high-side operation, or by a short to battery when the channel is configured for low-side operation. The channel is switched off when the overload condition is detected, the setpoint and EN bit are cleared to 0, and the fault bit is latched in the DIAGNOSIS register. The fault bit is cleared when the DIAGNOSIS register is read by an SPI access. The channel can be turned on again by re-activating the channel by setting a nonzero average current setpoint. See the Diagnostic Functions Section (Section 10) for further description.

Conditions for an overcurrent fault detection

1. $I_{load} > I_{load\_lim\_H}$
   - power stage is disabled immediately, independent of OCDT filter
2. $I_{load\_lim\_L} < I_{load\_lim\_H}$
   - NO quick shutoff
   - Overcurrent condition needs to persist for t > t_{OCDT}
   OR
   - power stage changes its state if t < t_{OCDT}
   to disable the power stage and issue a fault according to the fault assignment matrix

Table 8 Fault assignment matrix

Configuration of Channel	Location of detected overcurrent	OLSB	OVC
LS	HS FET	X	
LS	LS FET		X
HS	HS FET		X
HS	LS FET	X	
X	Open load in ON	X	

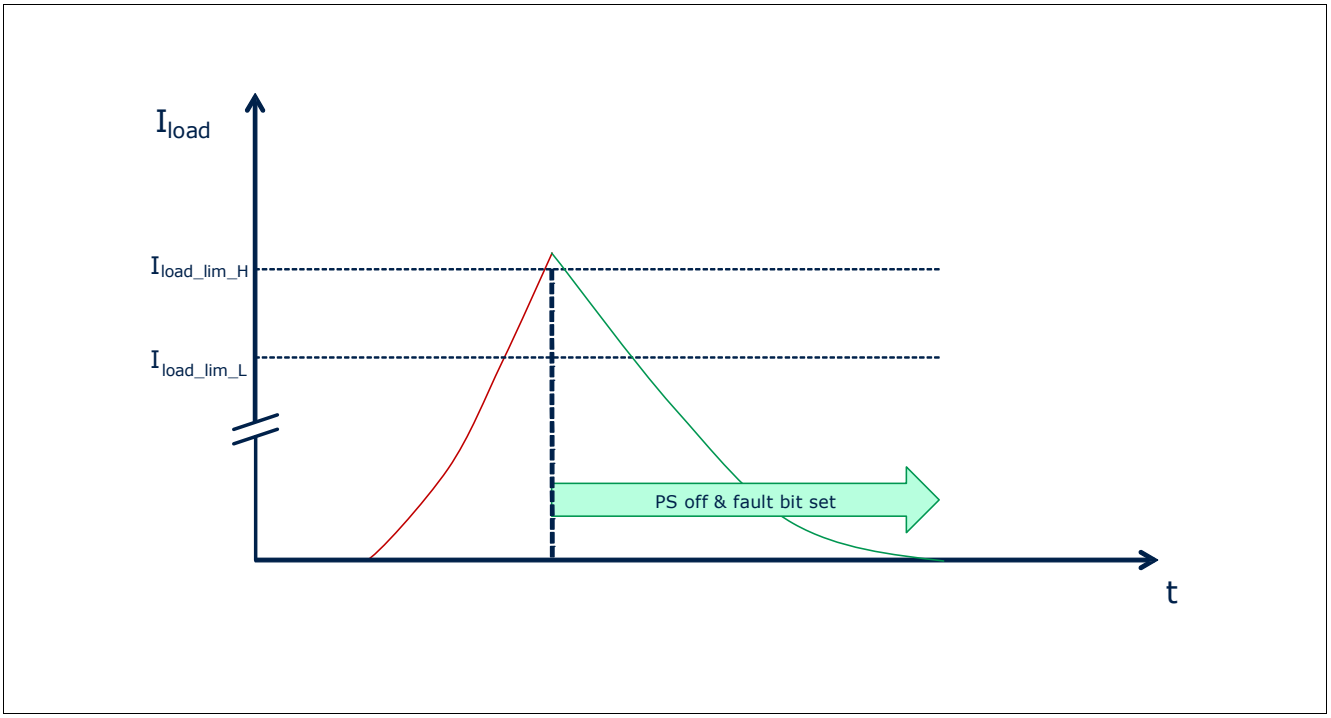

Figure 12 High-level short circuit ($I_L > I_{load\_lim\_H}$)

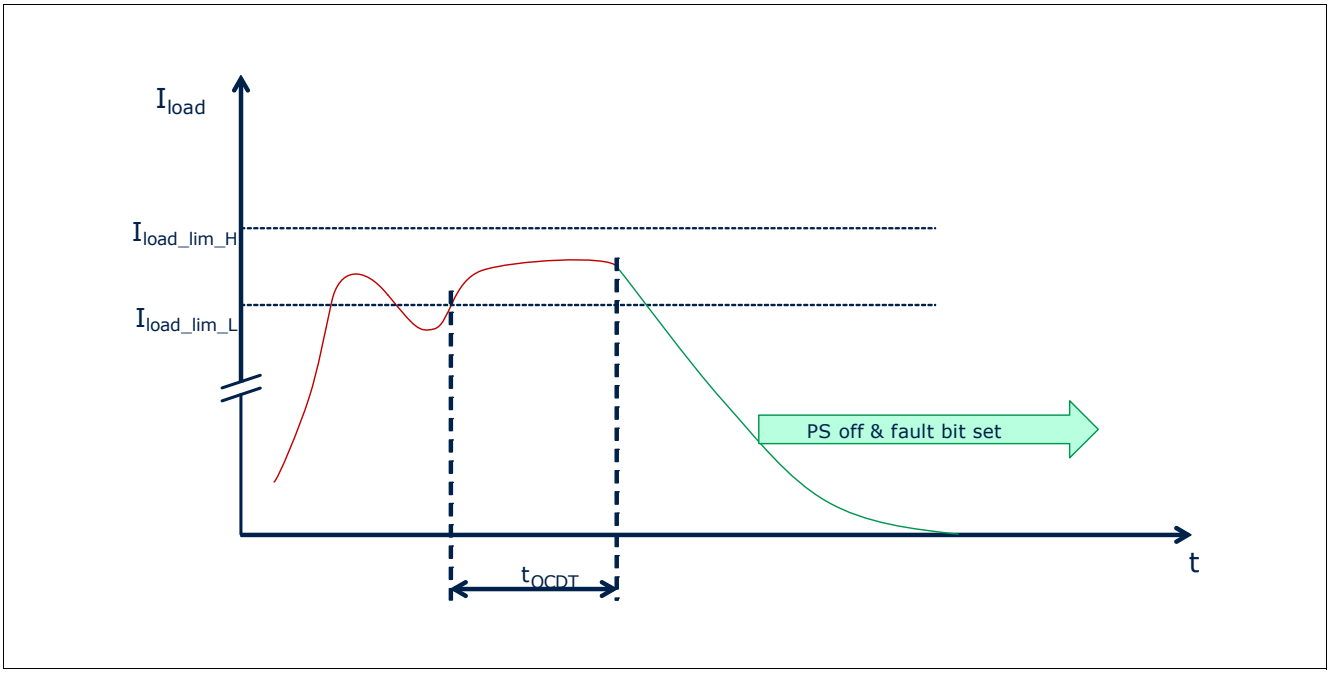

Figure 13 OCDT expiration overcurrent detection timer ($I_{load\_lim\_L} < I_{load} < I_{load\_lim\_H}$)

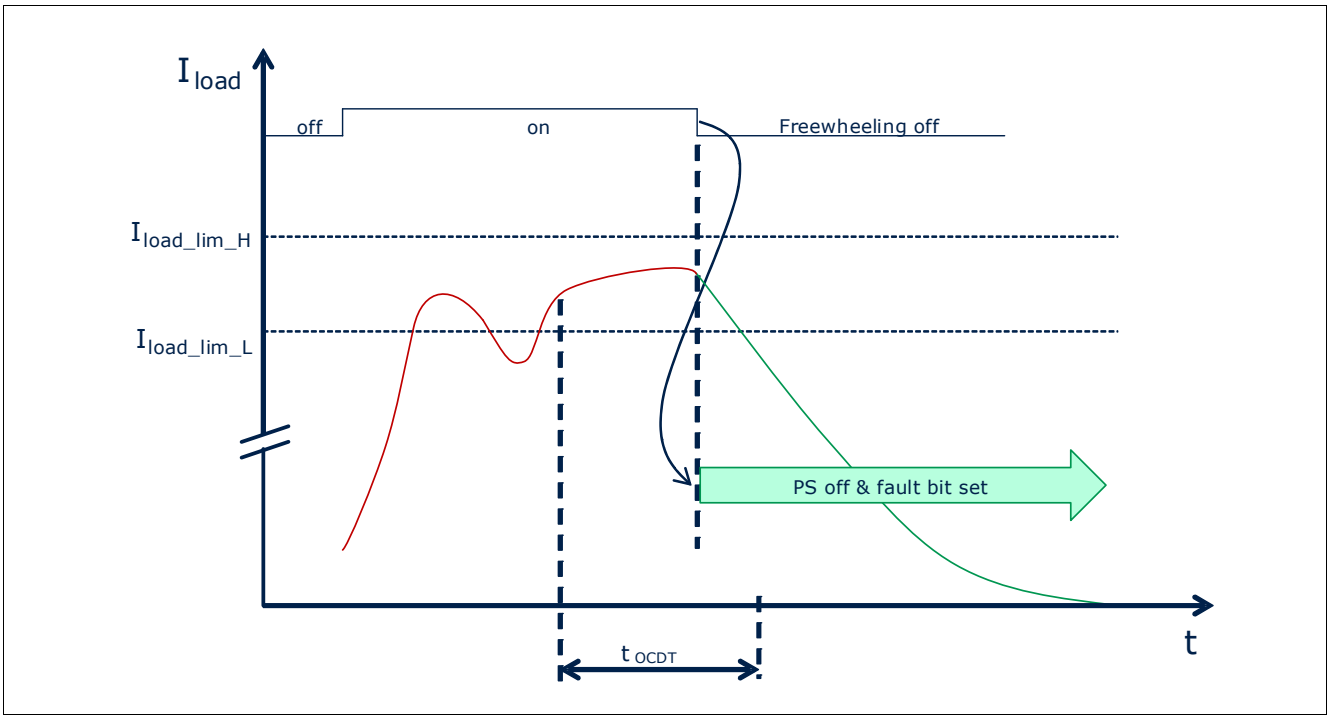

Figure 14 State change of power change before OCDT detection ($I_{load\_lim\_L} < I_{load} < I_{load\_lim\_H}$)

9.3 Overtemperature Protection

A temperature sensor for each channel is used to switch off an overheated channel to prevent destruction. When an overtemperature fault is detected, the channel is automatically turned off and the setpoints and EN bits of all the overtemperature channels are cleared to 0, and the fault bit is latched in the DIAGNOSIS register. The channel remains off until the channel temperature has decreased by the thermal hysteresis value ΔTSD. The channels will remain disabled until the diagnostic register is read and the EN bit is set back to 1 and the setpoint is set to >0. A fault bit is latched in the DIAGNOSIS register when the overtemperature fault is detected. The fault remains latched until the DIAGNOSIS register has been read and the fault condition is no longer present.

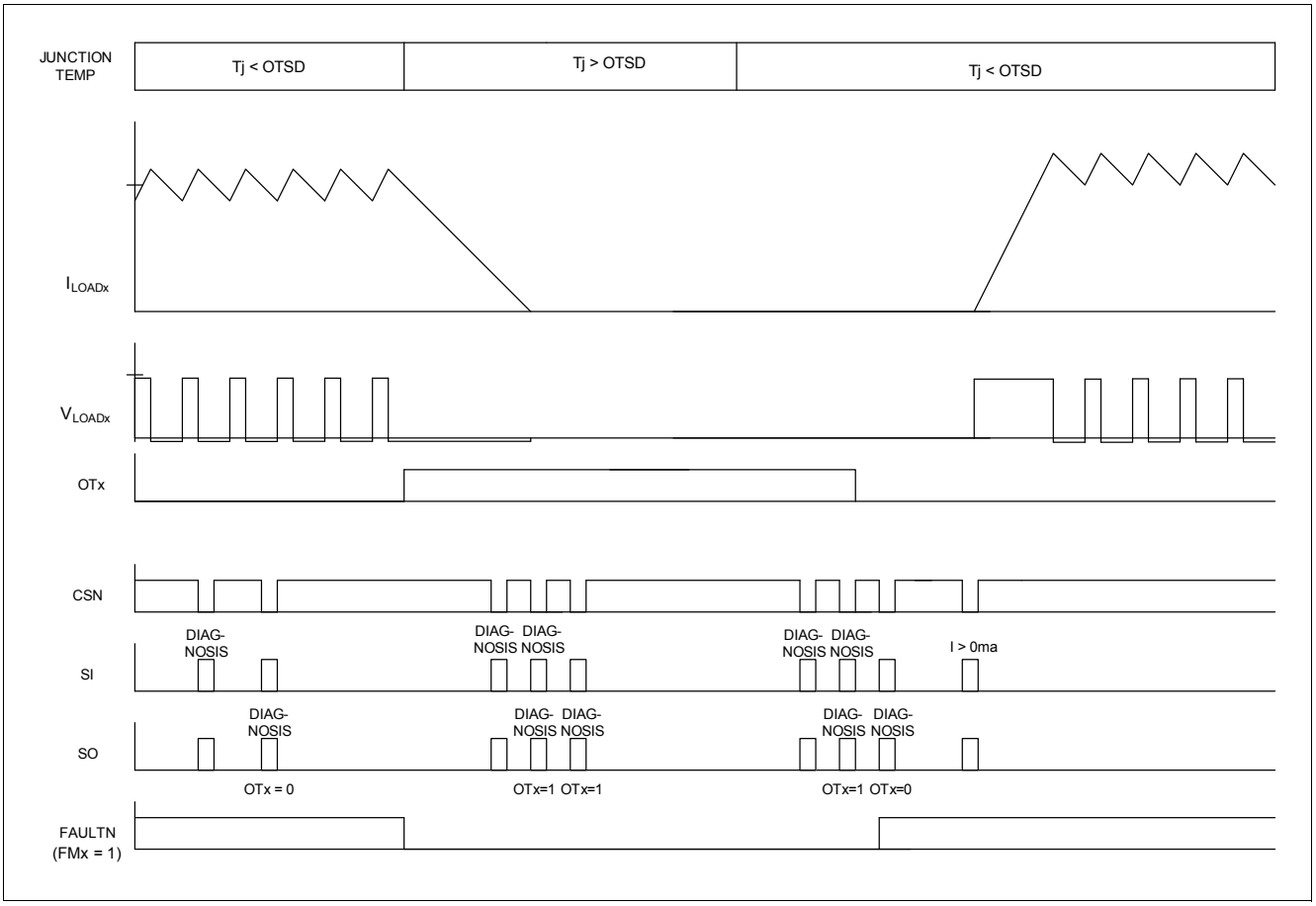

Figure 15 Overtemperature Timing Diagram (High-Side Configuration)

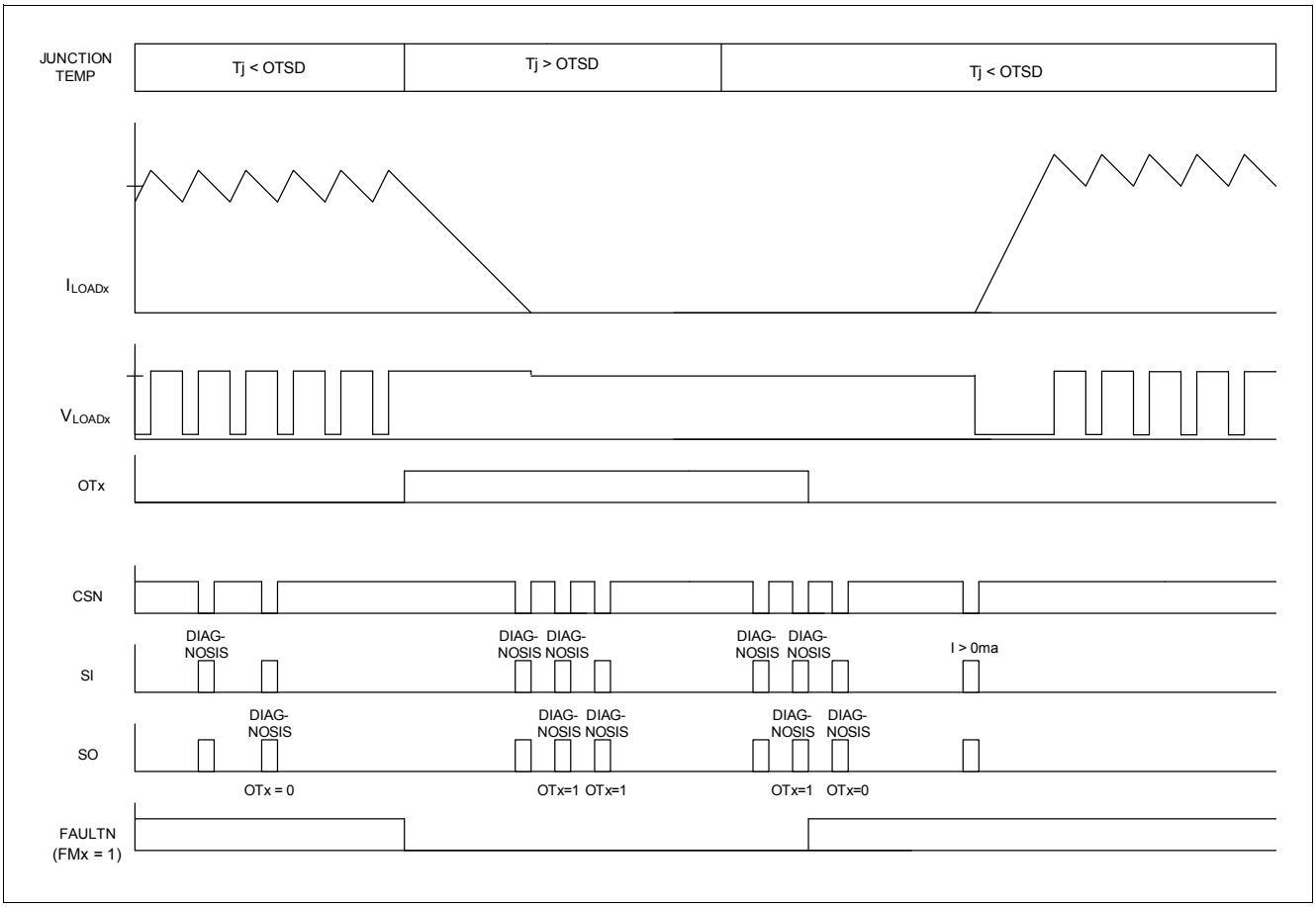

Figure 16 Overtemperature Timing Diagram (Low-Side Configuration)

9.4 Overvoltage Shutdown

This feature is implemented to protect the internal power transistors from damage due to overvoltage on the VBAT pin. If the voltage on the VBAT pin exceeds the VBAT overvoltage threshold an overvoltage fault bit will be set in the diagnostic register. This fault bit will be latched until the diagnostic register is read by SPI and the overvoltage condition no longer exists. All channels are disabled while the overvoltage condition exists and the setpoints and EN bits of all the channels are cleared to 0, and the fault bit is latched in the diagnostic register. The channel will remain disabled until the diagnostic register is read and the EN bit is set back to 1 and the setpoint is set to >0.

The charge pump output voltage is clamped to approximately 50V. The charge pump undervoltage fault (CPUV) may be set before the VBAT overvoltage fault bit is set depending on the rise time of the VBAT voltage.

9.5 Electrical Characteristics

Table 9 Electrical Characteristics: Protection Functions

V_{BAT} = 8 V to 17 V, V_{DDx} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Overload Protection							
Load current limit	$\|I_{LIM\_low}\|$ 1) $\|I_{LIM\_high}\|$ 2)	1.8 2.6	3 4.3	4.2 6	A	note: operates over range V_{LSUP_UV} < V_{LSUP} < V_{BAT}+0.3V, V_{DDx_UV} < V_{DDx} < 5.5V	P_9.5.1
Load current limit hysteresis	$\|I_{LIM\_high}\|$ - $\|I_{LIM\_low}\|$ 3)	0.8	1.4	2	A		P_9.5.6
Overcurrent detection filter time	T_{OCDT}	20	–	40	cycles	F_{SYS} cycles	P_9.5.2
Overtemperature Protection							
Thermal shut down temperature	T_{SD}	170	–	190	°C	4)	P_9.5.3
Thermal hysteresis	ΔT_{SD}	–	10	–	°C	4)	P_9.5.4
Overvoltage Protection							
Overvoltage threshold on VBAT	V_{BAT_OV}	40	–	44	V		P_9.5.5

1) If this limit is exceeded the OCDT counter starts.
2) This is the quick shutoff limit.
3) This is the difference between the high and low threshold value. It is guaranteed that the high threshold always is higher than the low threshold.
4) Not subject to production test, specified by design.

10 Diagnosis Functions

10.1 Overview

For diagnosis purposes, the device provides a FAULTN pin and a DIAGNOSIS register accessed through the SPI interface. The following table lists the types of load faults which are detected in each mode of operation.

	HIGH_SIDE CONFIG		LOW_SIDE CONFIG	
	OFF (0 mA)	ON	OFF (0 mA)	ON
OPEN LOAD	YES	YES	YES	YES
SHORT TO BATTERY	YES	YES	NO	YES
SHORT TO GROUND	NO	YES	YES	YES

Figure 17 Fault Conditions Detected in Each Mode of Operation

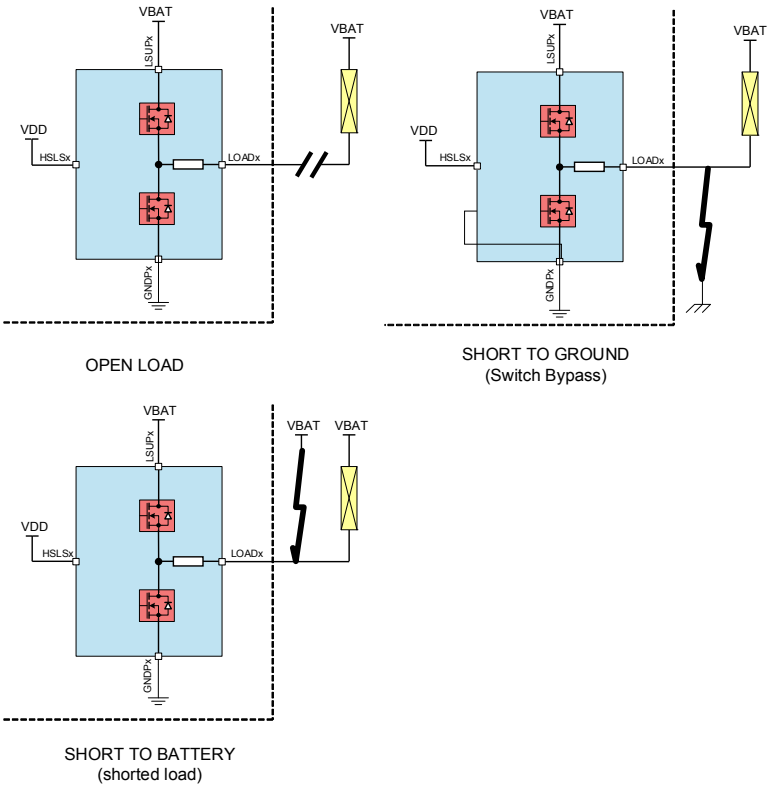

Figure 18 Fault Conditions for Low-Side Configuration

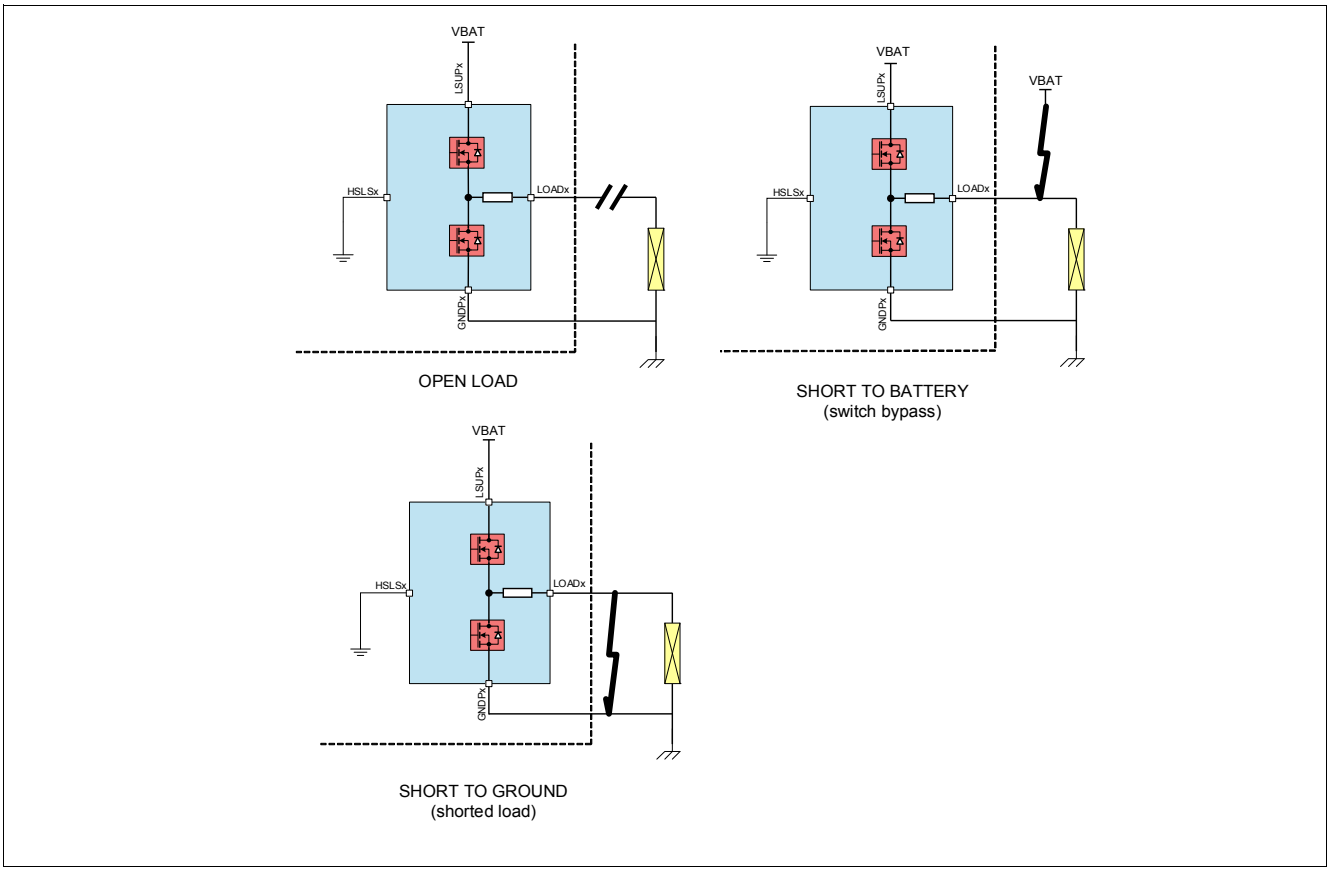

Figure 19 Fault Conditions for High-Side Configuration

10.2 FAULTN pin

The FAULTN pin is an open drain output pin. The FAULTN pins of multiple devices can be connected to form a “wired AND” circuit. The FAULTN pin can be used to generate an external interrupt to the microcontroller whenever a fault is detected. The microcontroller must then interrogate the device by the SPI interface to determine the type of the fault and the faulted channel number.

The FAULTN pin is pulled low when one of following unmasked faults is detected.

- overcurrent
- overtemperature
- open load in on state
- switch bypass in on state
- RESN pin is in low state
- EN pin is in low state
- internal reset is active due to VDDx undervoltage
- CLK pin signal fault
- VBAT pin overvoltage
- LSUPx pin undervoltage
- WD event

Certain faults can be masked by setting the appropriate mask bits in the configuration SPI register. A masked fault has no effect on the FAULTN pin.

During power-up, the FAULTN pin is held low until the device is ready to operate. The FAULTN pin will transition from low to high automatically after power-up.

10.3 FAULT mask bits

The CONFIGURATION register includes fault mask bits which can be used to allow or prevent a fault from activating the FAULTN pin. Setting the FME bit to 1 will cause the FAULTN pin to be held low whenever the EN pin is low. If the FME bit is set to 0, the FAULTN pin is not affected by the state of the EN pin voltage. Setting the FMx bit to 1 will cause the FAULTN pin to be held low whenever a OTx, OVCx, UVx, or OLSBx fault is detected on the respective channel. If the FMx bit is set to 0, the state of the OTx, OVCx, UVx, and OLSBx fault bits will not affect the state of the FAULTN pin.

10.4 Overcurrent fault

The device is protected from a short across the load by an overcurrent shutdown feature when the channel is enabled and the setpoint is >0. When a fault is detected the EN bit is set to 0, the setpoint is cleared to 0 and the overcurrent fault bit OVCx is set. The channel will remain disabled until the diagnostic register is read and the EN bit is set back to 1 and the setpoint is set to >0. When an overcurrent fault is detected, the OVCx fault bit is latched. The fault bit is cleared when the DIAGNOSIS register is read. The functional range for the short circuit detection depends on the setpoint and the PWM period.

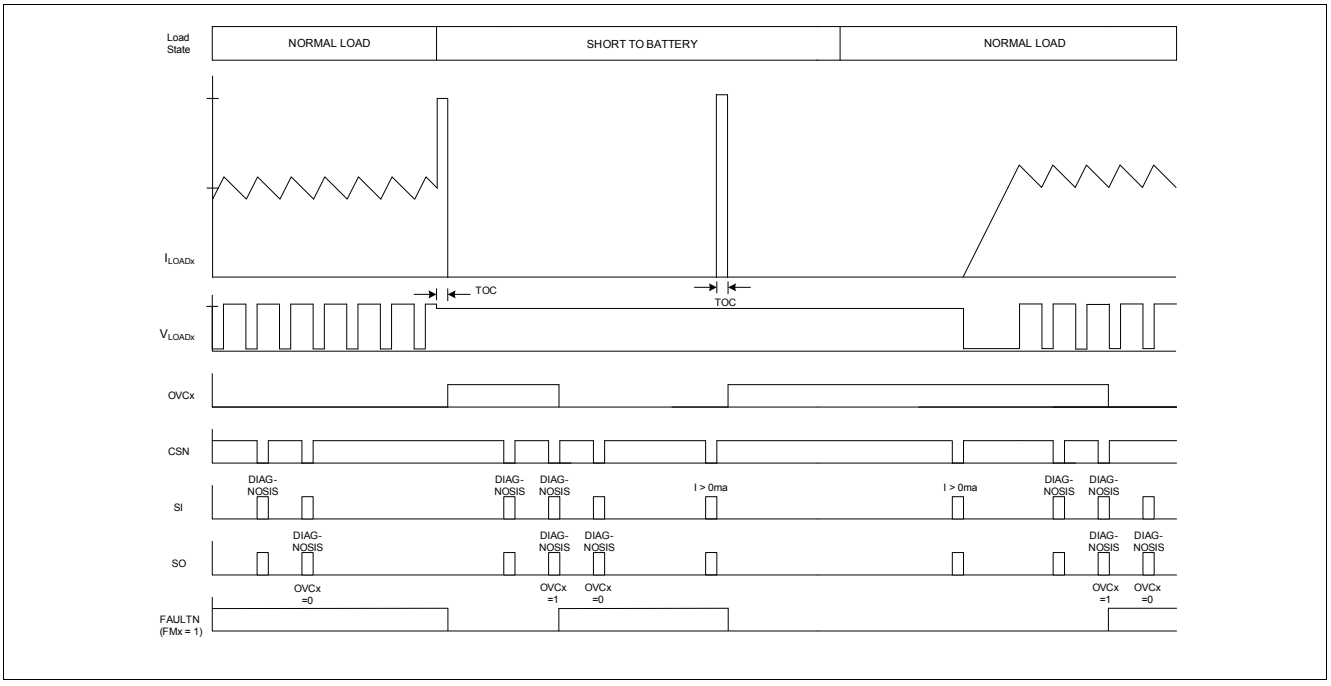

Figure 20 Overcurrent Fault in Low-Side Configuration

10.5 Open Load / Switch Bypass Fault

An open load fault and a switch bypass fault can be detected, but not distinguishable, via the OLSB bit alone. An OLSB fault can be detected when the setpoint of the faulted channel is equal to 0 mA (channel off) or when the setpoint is greater than 0 mA (channel operating). While the output is off, both faults can be distinguished using the OLOFF bit. The switch bypass fault is a short to battery fault when the channel is configured as a high-side driver and a short to ground when the channel is configured as a low-side driver.

The device detects an open load or switch bypass fault in the operating condition by monitoring the load current. If the load current is below the OLSB threshold current for a time greater than the OLSB delay time (on state), then the OLSBx fault bit is set and the channel is disabled. The OLSBx fault bit is latched when the fault occurs, and it is cleared when the DIAGNOSIS register is read and the fault is no longer present. The channel will remain disabled until the diagnostic register is read and the EN bit is set back to 1 and the setpoint is set to >0. Additional information can be found in the Diagnostic and Protection functions applications note.

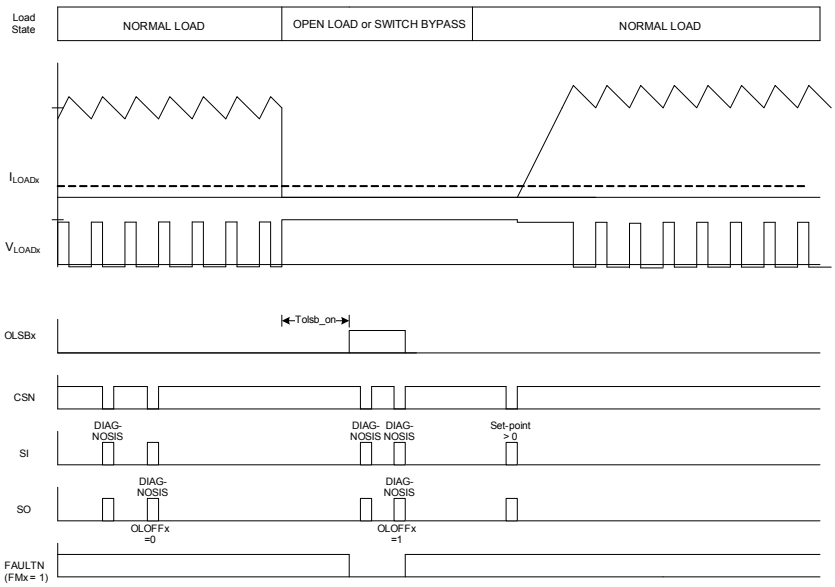

Figure 21 OLSB Fault - On State Timing Diagram (High-Side Configuration)

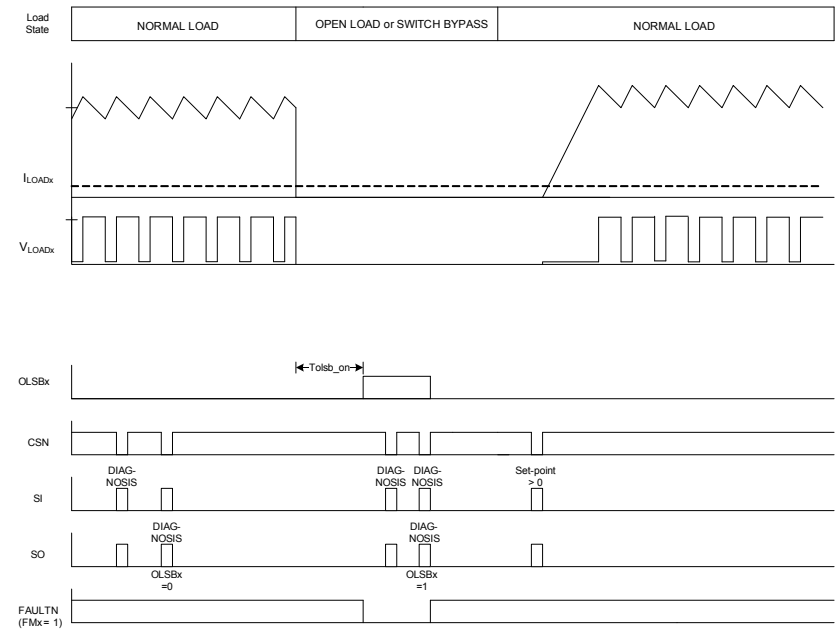

Figure 22 OLSB Fault - On State Timing Diagram (Low-Side Configuration)

The device detects an open load / switch bypass fault when the channel is turned off by applying a weak current source to the LOADx pin and comparing the LOADx pin voltage to VLSUPx/2. A pull up current source or a pull down current sink can be activated by setting the IDIAGx Select field of the CONFIGURATION register. The programmed current source is automatically enabled when the setpoint is set to 0 and the EN bit in the setpoint register is set to 1. It is disabled when the setpoint is set to a value greater than 0 or the EN bit is set to 0. A simplified block diagram of the OLOFF detection circuit when the channel is disabled is shown in **Figure 23**. The OLOFF fault bit is never latched. The fault bit will be cleared when the fault is no longer present.

When the channel is disabled and an OLOFF fault is detected, it is possible to discriminate between an open load fault and a switch bypass fault by changing the IDIAG current source. For a high-side configured channel, the pull

up current source must be initially enabled in order to detect the OLOFF fault. Once this fault is detected, the pull up current source current can be disabled and the pull down current can be enabled by SPI in order to determine if the fault is an open load or a short to battery.

The diagnostic currents used are weak, a wait time is needed before the OLOFF bit is read.
t_{wait} = (V_{LSUP} /2) * C_{load}/ |$I_{DIAGMIN}$|. $I_{DIAGMIN}$ is the absolute value of the I_{DIAG_UPMax} or I_{DIAG_DNMin} depending on which is selected.

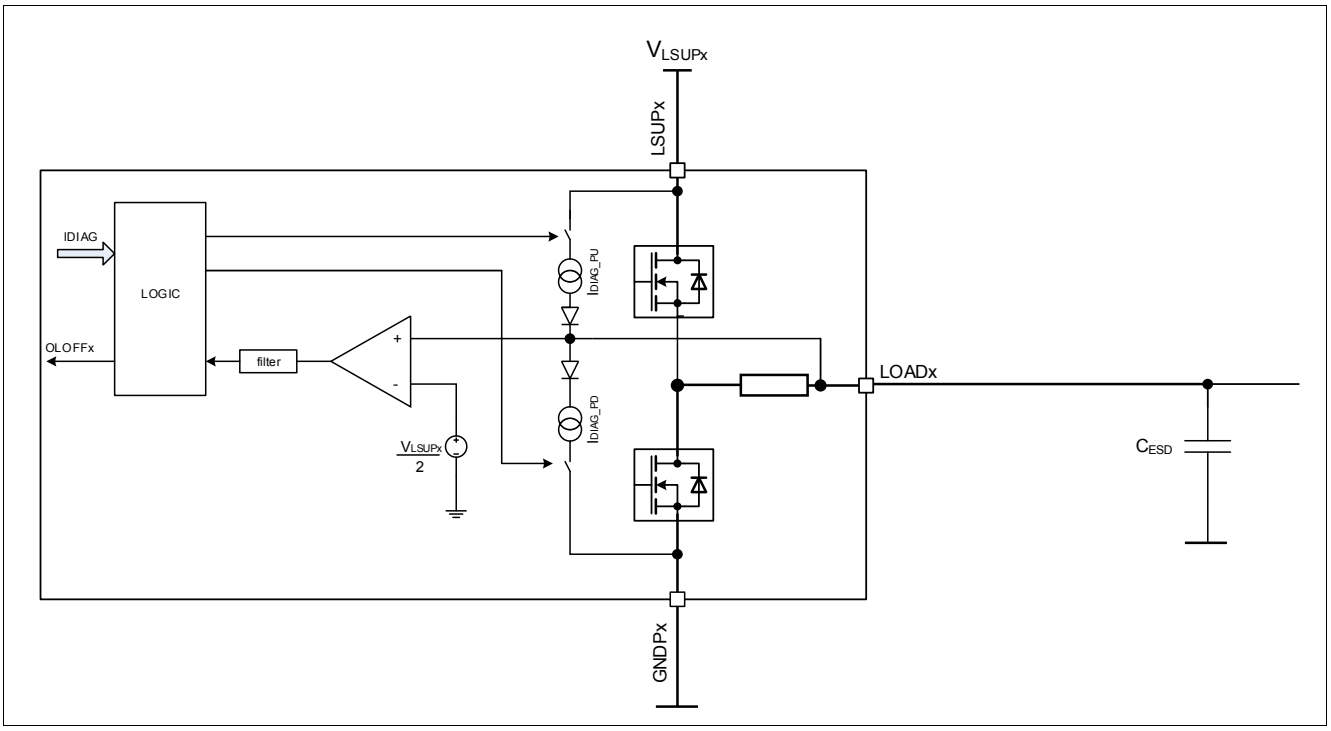

Figure 23 OLSB Fault - Off State Block Diagram

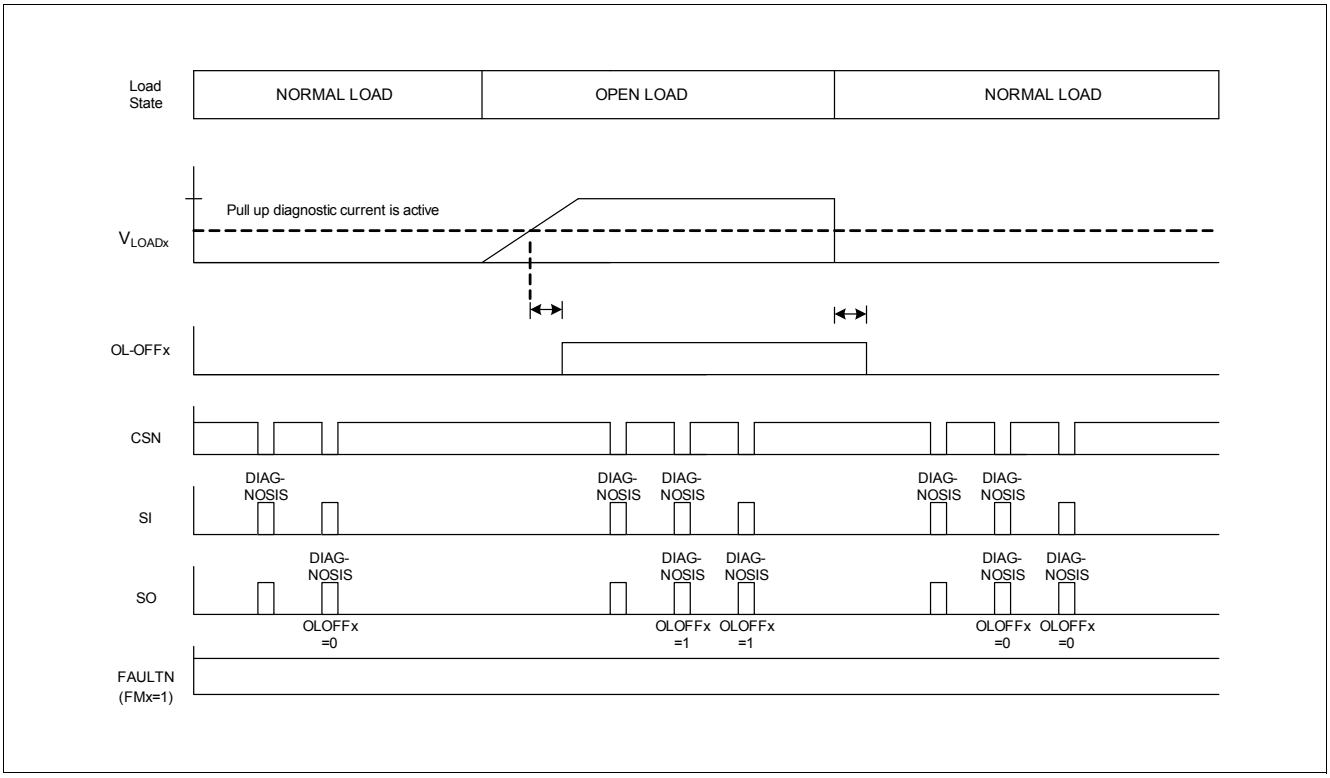

Figure 24 Open Load Fault - Off State Timing Diagram (High-Side Configuration)

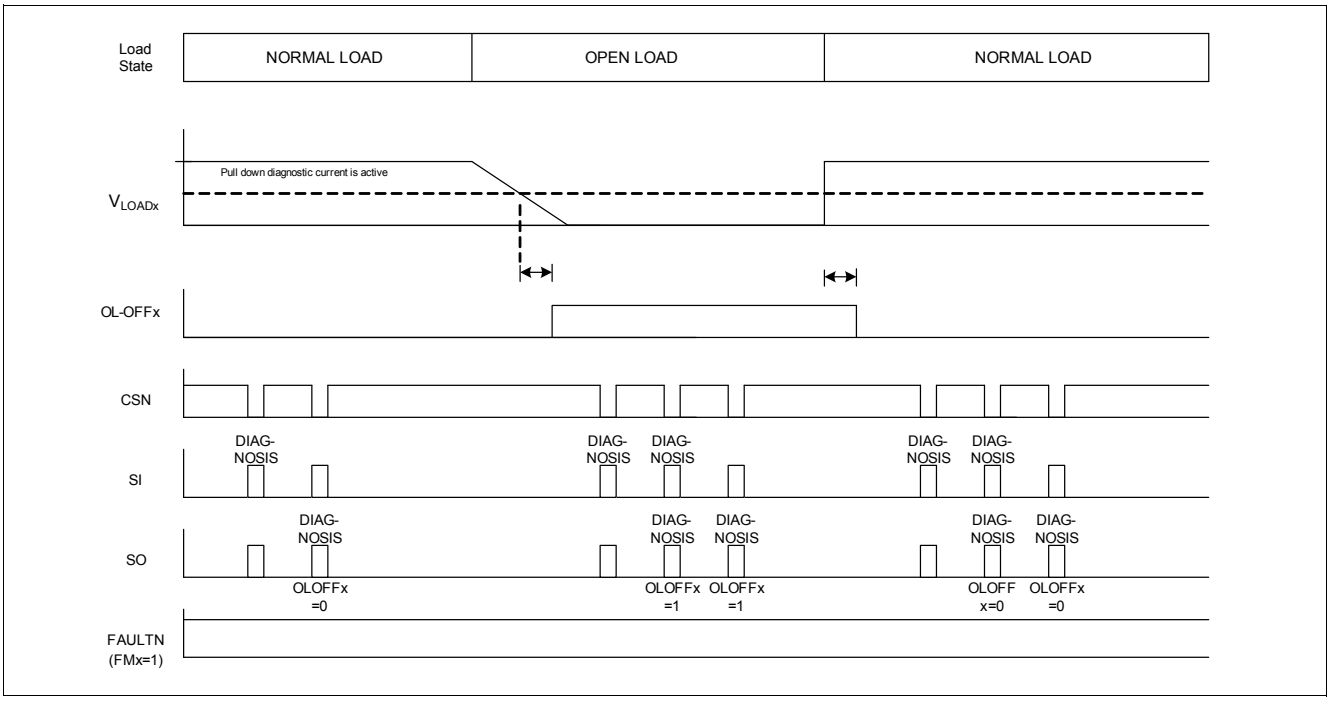

Figure 25 Open Load Fault - Off State Timing Diagram (Low-Side Configuration)

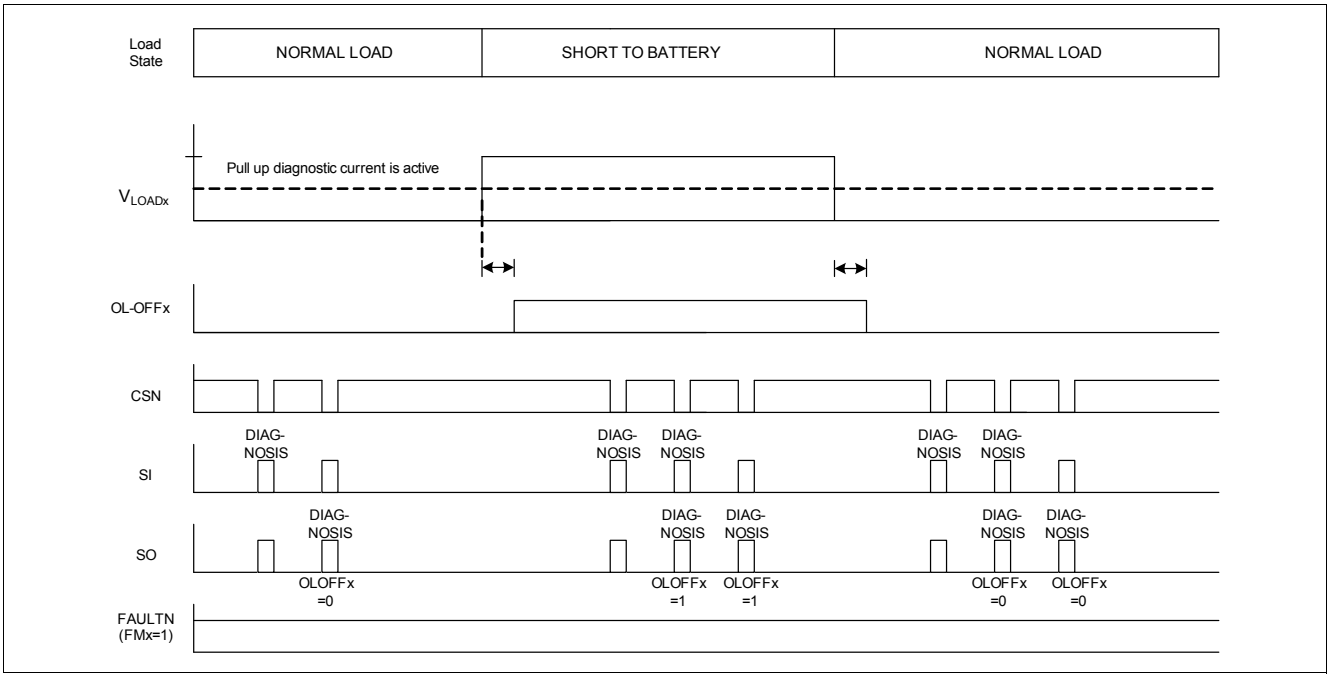

Figure 26 Switch Bypass Fault - Off State Timing Diagram (High-Side Configuration)

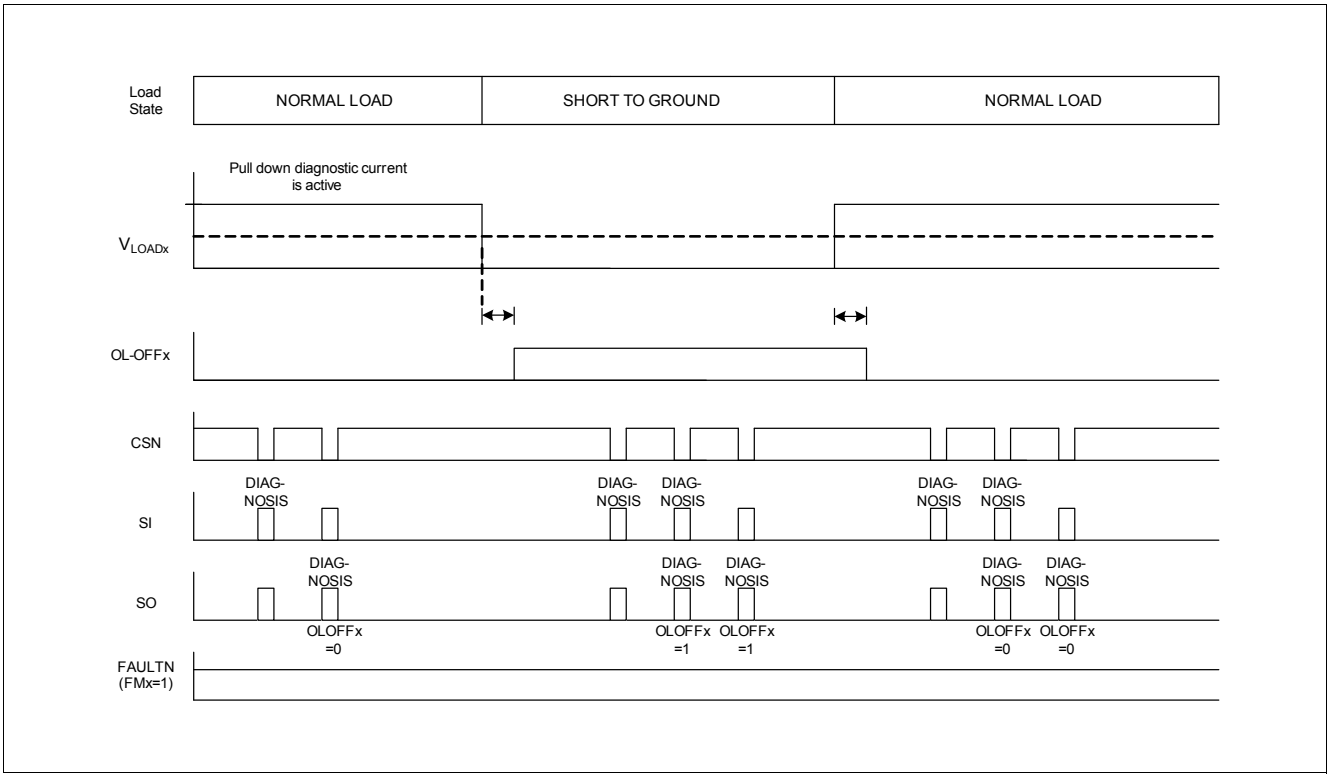

Figure 27 Switch Bypass Fault - Off State Timing Diagram (Low-Side Configuration)

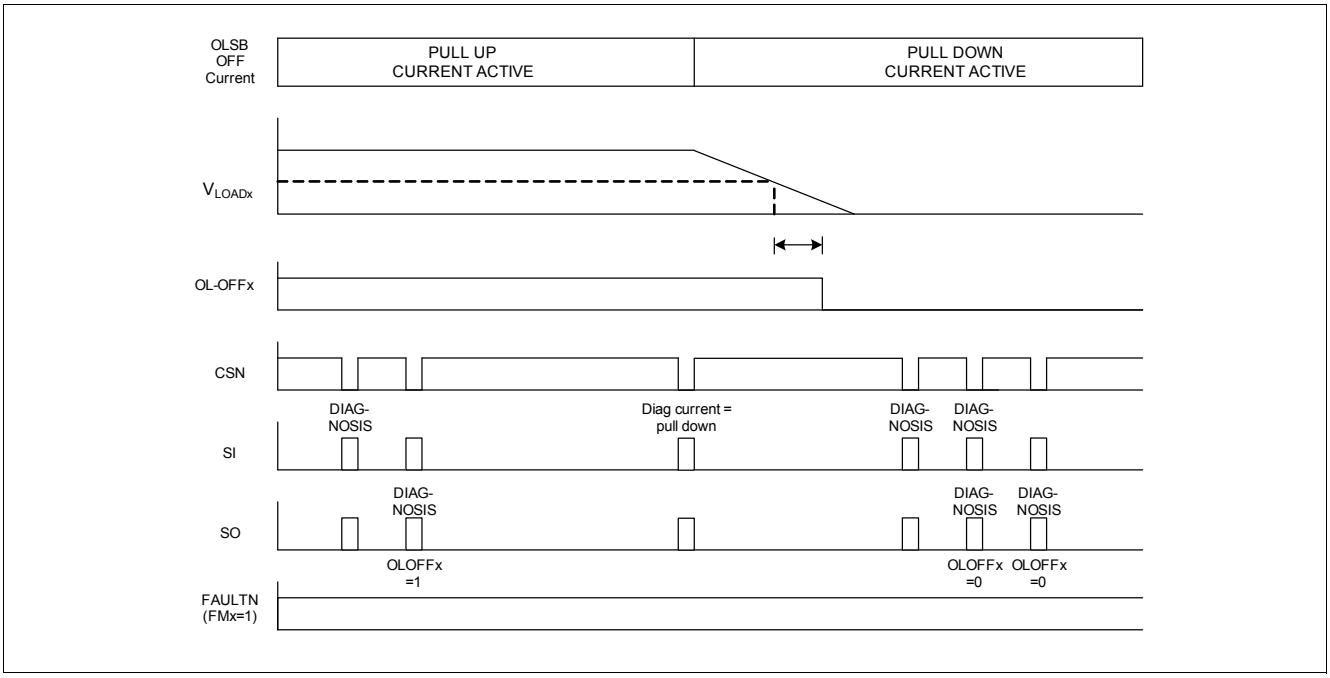

Figure 28 Open Load Fault - Off State Discrimination Timing Diagram (High-Side Configuration)

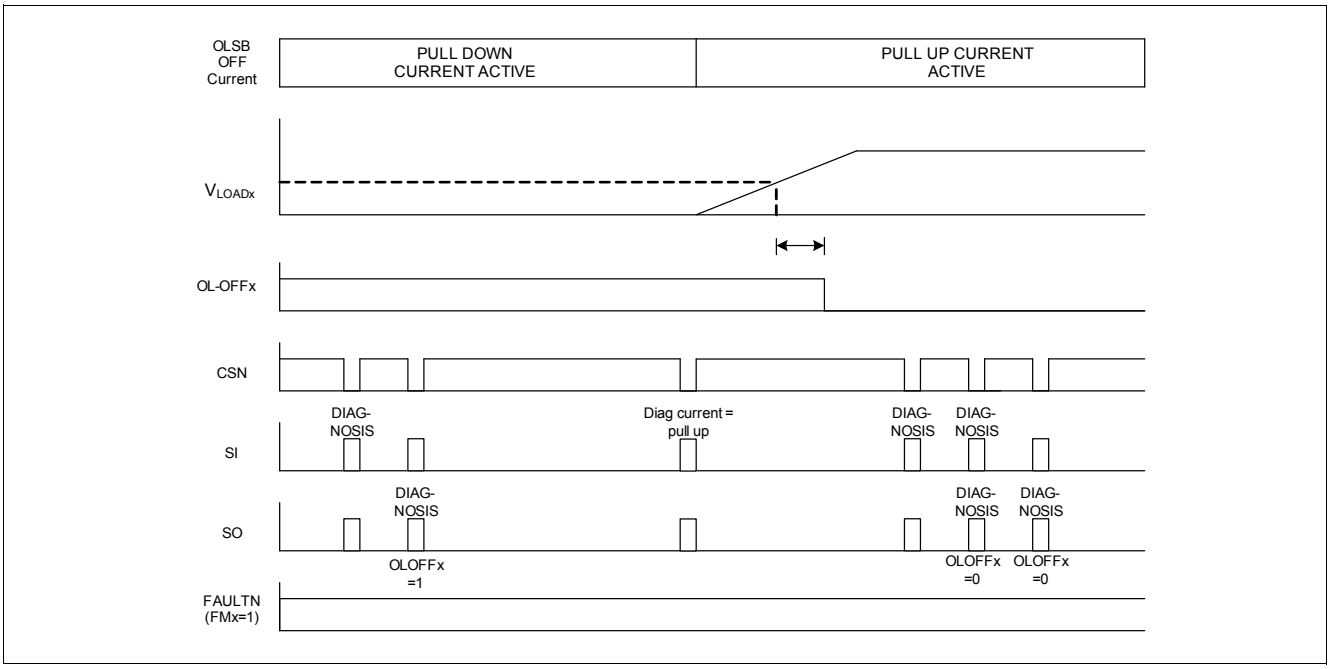

Figure 29 Open Load Fault - Off State Discrimination Timing Diagram (Low-Side Configuration)

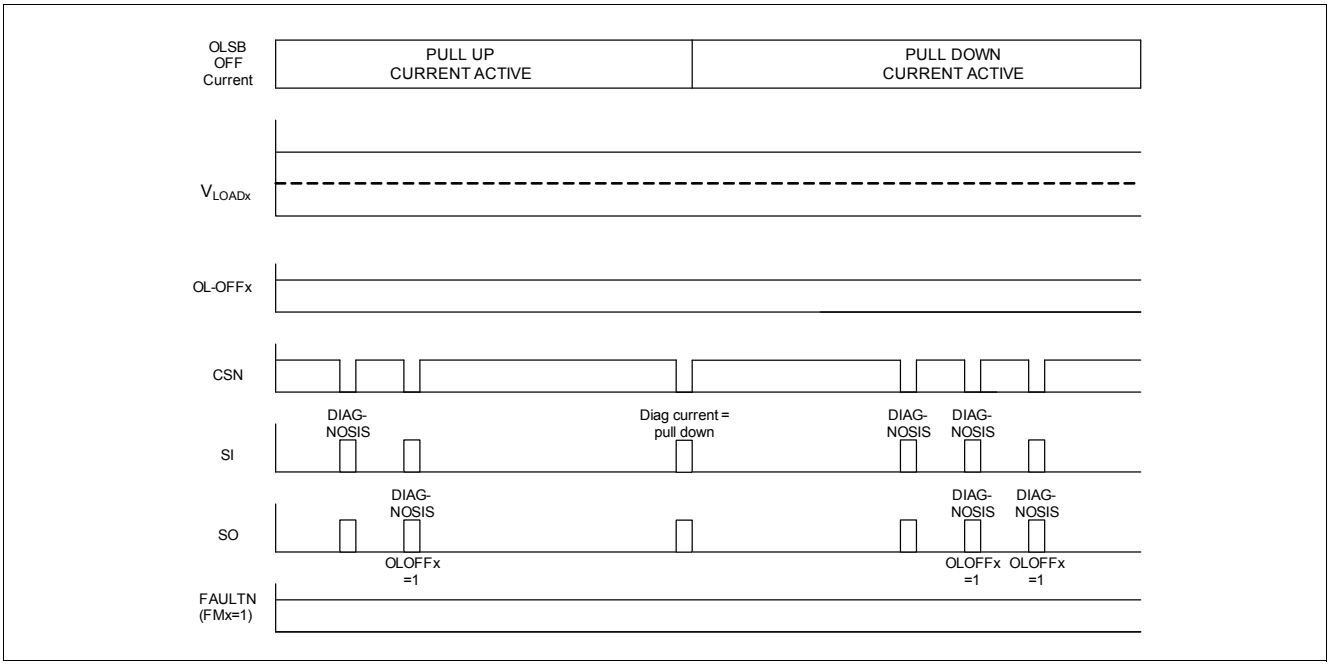

Figure 30 Switch Bypass Fault - Off State Discrimination Timing Diagram (High-Side Configuration)

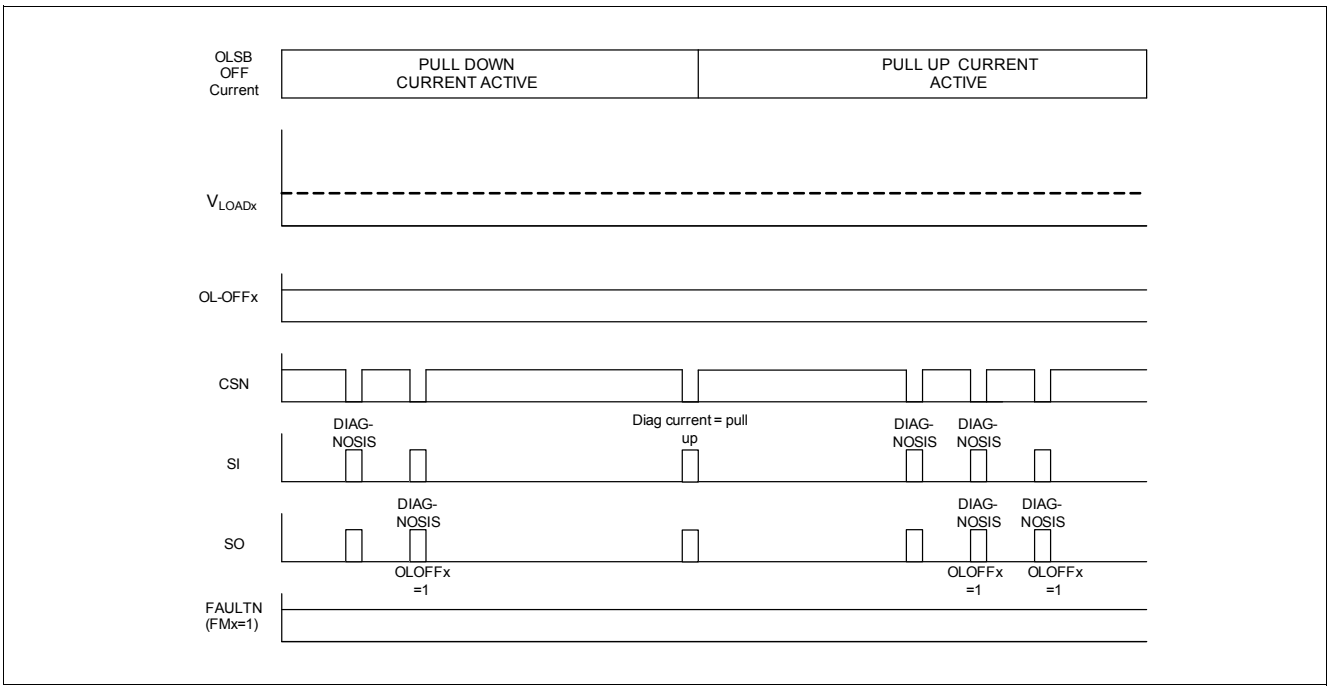

Figure 31 Switch Bypass Fault - Off State Discrimination Timing Diagram (Low-Side Configuration)

10.6 Supply Out of Range Fault

The LSUPx pins, the CPOUT pin, and the VBAT pin are connected to internal monitor circuits which disable the output channels if the pin voltage is out of range. The VBAT pin is connected to an overvoltage detection circuit block. The CPOUT and LSUPx pins are connected to undervoltage detection circuits. When the voltage on these pins exceeds the shutdown threshold, a fault bit is set and the channel is disabled. The fault bits are latched until the DIAGNOSIS register is read and the voltage is in the correct range. The EN bits and setpoint are cleared to 0. When a CPUV fault occurs, all channels are disabled, the EN bits and setpoints are cleared to 0. The channels

can be reactivated when the CPUV fault is not present by reading the DIAGNOSIS register and setting the EN bits to 1 and set the setpoint to > 0.

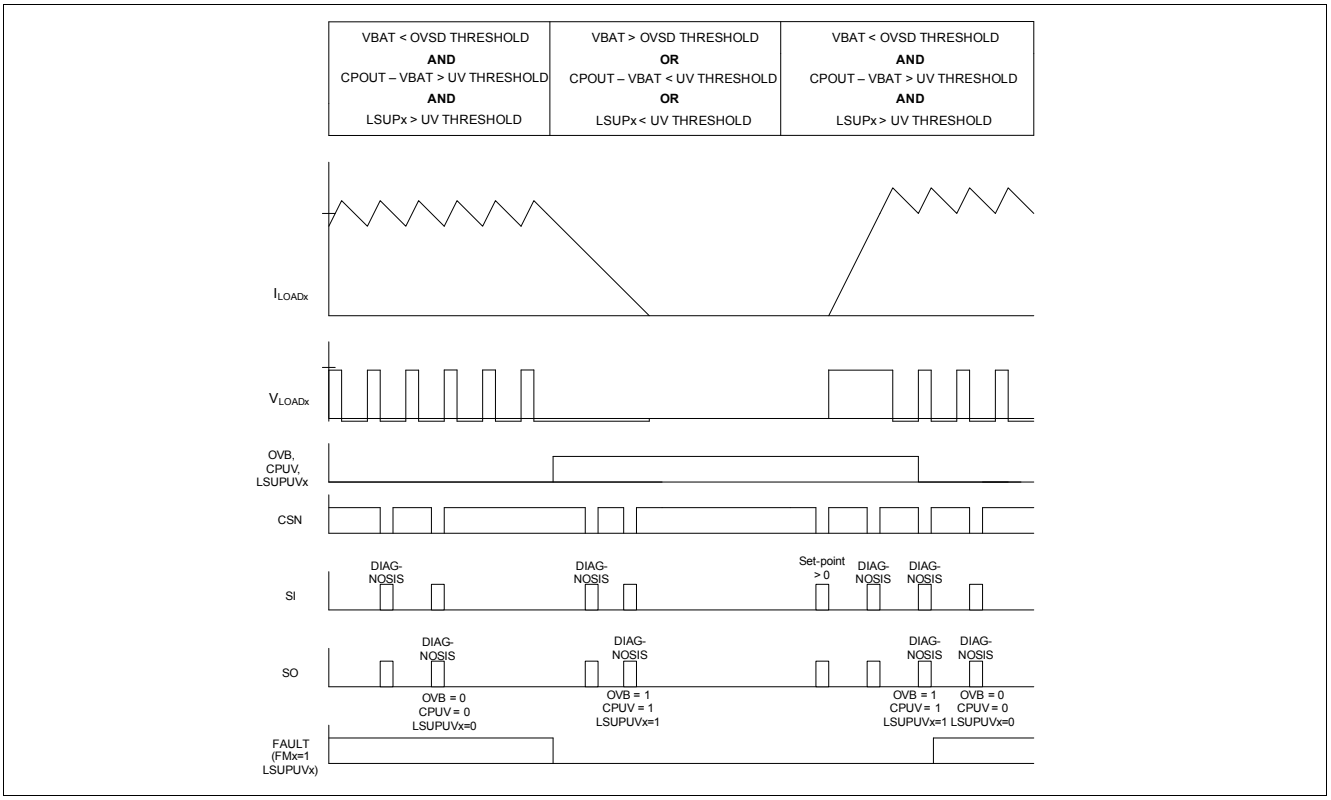

Figure 32 Supply Out of Range Fault in High-Side Configuration

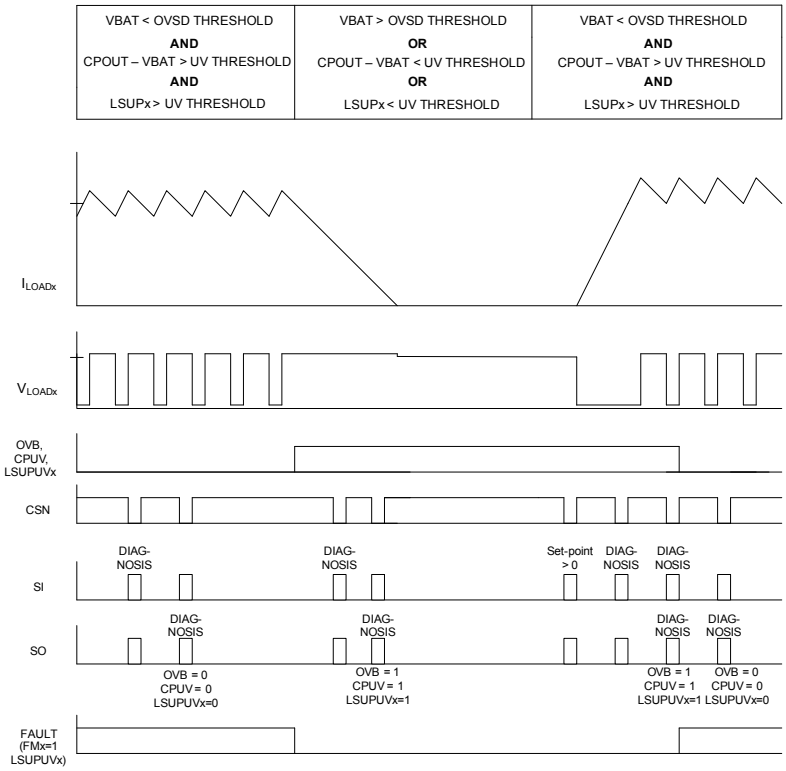

Figure 33 Supply Out of Range Fault in Low-Side Configuration

10.7 CRC Fault

The device contains EEPROM cells for storing calibration data. These cells are accessed during start up and periodically during operation of the device. A Cyclical Redundancy Checking (CRC) feature is included to detect errors in the reading of the EEPROM. If an error is detected, the CRC error bit will be set in the DIAGNOSIS register. All channels will remain operational, but the accuracy of the current control may be degraded. The CRC fault bit is cleared upon reading the Diagnosis Register.

10.8 Regulator Error Fault (REx)

The DIAGNOSIS register includes a regulator error bit for each channel. This bit is set when the controller is not able to regulate the load current to the setpoint value for more than 8 consecutive PWM cycles. The RE bit is set if the integrator output exceeds the upper or lower limit for more than 8 PWM cycles. The REx fault bits are cleared upon reading the Diagnosis Register.

10.9 Electrical Characteristics

Table 10 Electrical Characteristics: Diagnosis

V_{BAT} = 8 V to 17 V, V_{DDx} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Shorted load resistance threshold	R_{SL_ON}	0.5	–	–	Ω	1)	P_10.9.1
Open load - switch bypass threshold current range (on state)	I_{OLSB_ON}	0	–	375	mA	Configurable	P_10.9.2
Open load - switch bypass delay time (on state)	T_{OLSB_ON}	–	8192	–	cycles	F_{SYS} cycles	P_10.9.3
Off-State pull up current	I_{DIAG_UP}	-600	–	-100	µA	V_{LOAD} < V_{LSUP} - 4V	P_10.9.4
Off-State pull down current	I_{DIAG_DN}	100	–	600	µA	V_{LOAD} > 4V	P_10.9.5
Off-State LOADx threshold voltage	V_{LOAD_DIAG}	0.42* V_{LSUP}	–	0.58* V_{LSUP}	V	independent of V_{BAT} voltage	P_10.9.6

1) Not subject to production test, specified by design.

11 Serial Peripheral Interface (SPI)

11.1 Description of Interface

The diagnosis and control communication interface is based on the standard serial peripheral interface (SPI). The SPI is a full duplex synchronous serial slave interface which uses four signal lines: SO, SI, SCK, and CSN. Data is transferred by the lines SI and SO at the data rate given by SCK. The falling edge of CSN indicates the beginning of a data access. Data is sampled in on line SI at the falling edge of SCK and shifted out on line SO at the rising edge of SCK. Each access must be terminated by a rising edge of CSN. A counter ensures that data is taken only when 32 bits have been transferred. If in one transfer cycle the number of bits transferred is not 32, the data frame is ignored

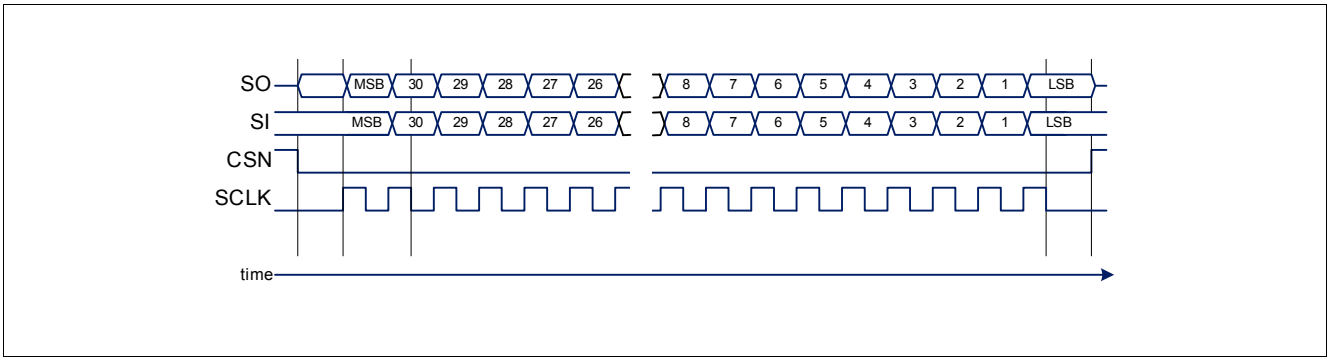

Figure 34 SPI Interface Signal Overview

11.2 Timing Diagrams

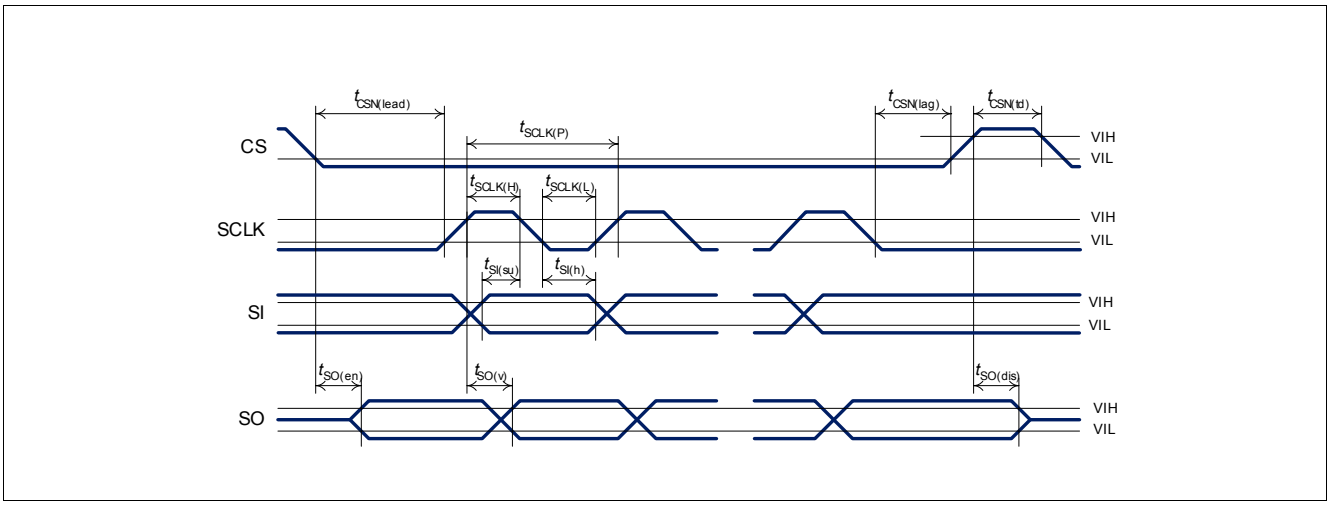

Figure 35 SPI Signal Timing Diagram - Thresholds = 20% / 80%

11.3 Electrical Characteristics SPI Interface

Table 11 Electrical Characteristics: SPI

V_{BAT} = 8 V to 17 V, V_{DDx} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Serial clock frequency	f_{SCLK}	–	–	8	MHz	1) 2)	P_11.3.1
Serial clock high time	t_{SCLKH}	50	–	–	ns	1)	P_11.3.2
Serial clock low time	t_{SCLKL}	50	–	–	ns	1)	P_11.3.3
Enable lead time (falling CSN to rising SCLK)	t_{CSN_LEAD}	250	–	–	ns	1)	P_11.3.4
Enable lag time (falling SCLK to rising CSN)	t_{CSN_LAG}	250	–	–	ns	1)	P_11.3.5
Transfer delay time (rising CSN to falling CSN)	t_{CSN_TD}	5	–	–	cycles	F_{sys} cycles 1)	P_11.3.6
Data setup time (required time SI to falling SCLK)	t_{SI_SU}	20	–	–	ns	1)	P_11.3.7
Data hold time (required time falling SCLK to SI)	t_{SI_H}	20	–	–	ns	1)	P_11.3.8
Output enable time (falling CSN to SO valid)	t_{SO_EN}	–	–	200	ns	C_L = 200 pF 1)	P_11.3.9
Output disable time (rising CSN to SO tri-state)	t_{SO_DIS}	–	–	200	ns	C_L = 200 pF 1)	P_11.3.10
Output data valid time with capacitive load	t_{SO_V}	–	–	100	ns	C_L = 200 pF 1)	P_11.3.11
SO rise time	t_{SO_R}	–	–	50	ns	C_L = 200 pF 1)	P_11.3.12
SO fall time	t_{SO_F}	–	–	50	ns	C_L = 200 pF 1)	P_11.3.13
Input pin capacitance: CSN, SCLK, SI, CLK	C_{IN}	–	–	20	pF	1)	P_11.3.14
SO pin capacitance	C_{SO_HIZ}	–	–	25	pF	Tri-state 1)	P_11.3.15

1) Not subject to production test, specified by design.

2) Maximum SPI clock frequency in the application may be less depending on the load at the SO pin and the microcontroller SPI peripheral timing requirements.

12 SPI Registers

12.1 Description of Protocol

For each command received at the SI pin of the SPI interface, a serial data stream is returned at the same time on the SO pin. The content of the SO dat

a frame is dependent on the command which was received on the SI pin during the previous frame. A READ command (R/W = 0) returns the contents of the addressed register one SPI frame later. The data bits in the READ command are ignored. A WRITE command (R/W = 1) will write the databits in the SPI word to the addressed register. The actual contents of that register will be returned to the SPI master (microcontroller) during the next SPI frame. The response is not an echo of the data received from the SI pin, it is the actual contents of the register addressed in the previous SPI frame.

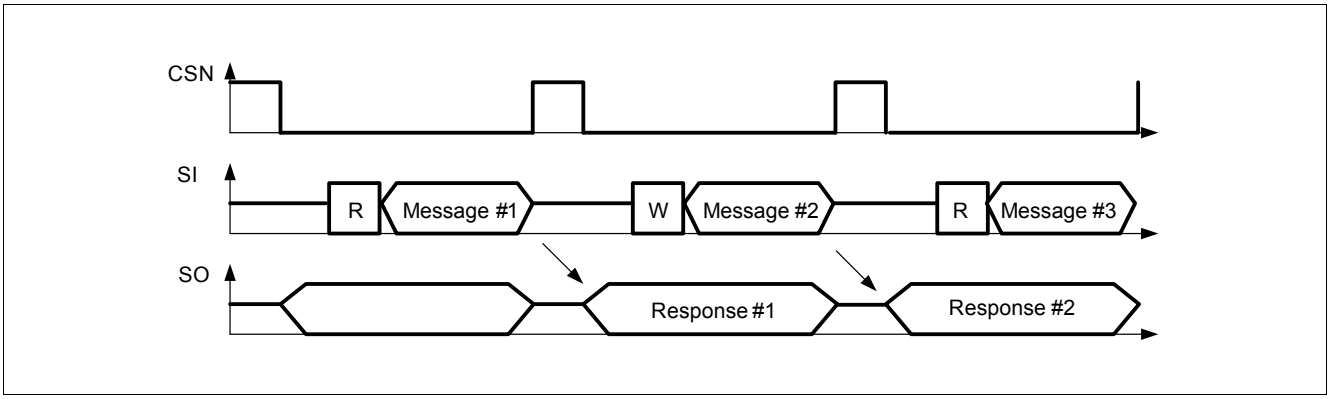

Figure 36 SPI Protocol

Each SPI message for the TLE82453-3SA has a length of 32 bit. The message from the microcontroller must be sent MSB first. The data from the SO pin is sent MSB first.

The response to an invalid SPI message is the IC Version and Manufacturer ID register (ICVID).

The SO data in the frame immediately following a reset condition is the IC Version and Manufacturer ID (ICVID) register.

12.2 ICVID REGISTER

ICVID

IC Version and Manufacturer ID **Reset Value: 00C1 xx00$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	0	0	0	0	0	0	0	Manufacturer ID							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Version								not used							WDS

Field	Bits	Type	Description
R/W	31	rw	**Read / Write bit** 0 = Read 1 = Read (cannot write to this register) When reading this register, the R/W bit is 0
Manuf ID	23:16	r	**IC Manufacturer ID** 1100 0001 = Infineon
Version	15:8	r	**IC Version** C11 step = 0000 0110
WDS	1	r	**CLK Watchdog Status** 0 = CLK signal OK or watchdog disabled (Reset value) 1 = Watchdog timeout fault (cleared only by reset)

12.3 CONFIGURATION REGISTER

CONFIG
Configuration Register **Reset Value: 0100 000x$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	0	0	0	0	0	0	1	not used							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDIAG2	IDIAG1	IDIAG0	SR2		SR1		SR0		FME	FM2	FM1	FM0	HL2	HL1	HL0

Field	Bits	Type	Description
R/W	31	rw	**Read / Write bit** 0 = Read 1 = Write When reading this register, the R/W bit is 0
IDIAG0-2	15:13	rw	**Set Off State Diagnostic current** 0 = High-Side current source is active (Reset value) 1 = Low-Side current source is active
SR0-2	12:7	rw	**Set slew rate setting of channel** 00 = Set the channel slew rate to SR0 (Reset value) 01 = Set the channel slew rate to SR1 10 = Set the channel slew rate to SR2 11 = Ignored (previous setting is used)
FME	6	rw	**Set Fault Mask for EN pin** 0 = EN pin state does not influence the FAULTN pin (Reset value) 1 = FAULTN pin is driven low if the EN pin is low.
FM0-2	5:3	rw	**Set Fault Mask for channel** 0 = Channel faults do not influence the FAULTN pin (Reset value) 1 = FAULTN pin is driven low when a fault is detected on the channel
HL0-2	2:0	r	**HSLS2, HSLS1, and HSLS0 pin status** (Reset value = state of HSLS pins) 0 = Highside configuration 1 = Lowside configuration

12.4 DIAGNOSIS REGISTER

DIAG
Diagnosis Register **Reset Value: 0250 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	0	0	0	0	0	1	0	CRC	RST	CPUV	CPW	OVB	not used	RE2	RE1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RE0	UV2	UV1	UV0	OT2	OT1	OT0	OL OFF2	OL OFF1	OL OFF0	OLSB 2	OLSB 1	OLSB 0	OVC2	OVC1	OVC0

Field	Bits	Type	Description
R/W	31	rw	**Read / Write bit** 0 = Read 1 = Read (cannot write to this register) When reading this register, the R/W bit is 0
CRC	23	r	**EEPROM CRC fault bit** 0 = no fault detected (Reset value) 1 = fault detected
RST	22	r	**Reset bit** 0 = no reset detected 1 = reset detected (cleared after register is read)
CPUV	21	r	**Charge Pump undervoltage shutdown** 0 = no fault detected (Reset value) 1 = fault detected
CPW	20	r	**Charge Pump undervoltage warning** 0 = no fault detected 1 = fault detected (Reset value)
OVB	19	r	**Overvoltage on VBAT pin** 0 = no fault detected (Reset value) 1 = fault detected
RE0-2	17:15	r	**Regulator Error** 0 = no fault detected (Reset value) 1 = fault detected REx bit is set if the commanded current is not reached after 8 PWM periods
UV0-2	12:14	r	**Undervoltage on Load Supply pin** 0 = no fault detected (Reset value) 1 = fault detected
OT0-2	11:9	r	**Overtemperature fault bits** 0 = no fault detected (Reset value) 1 = fault detected

Field	Bits	Type	Description
OL OFF0-2	8:6	r	**Open Load Fault when channel is off** 0 = no fault detected (Reset value) 1 = fault detected
OLSB0-2	5:3	r	**Open Load / Switch-Bypass fault bit** 0 = no fault detected (Reset value) 1 = fault detected
OVC0-2	2:0	r	**Overcurrent fault bit** 0 = no fault detected (Reset value) 1 = fault detected

12.5 CLK-DIVIDER REGISTER

CLK-DVD
Clock Divider Register **Reset Value: 0300 0818$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	0	0	0	0	0	1	1	not used							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
not used			WDEN	M						N				Fsys div	

Field	Bits	Type	Description
R/W	31	rw	**Read / Write bit** 0 = Read 1 = Write When reading the register, the R/W bit is 0
WDEN	12	rw	**Enable CLK pin watchdog** 0 = Disable Watchdog (Reset value) 1 = Enable Watchdog The output stages are disabled until the WDEN bit is set. To operate the device without the watchdog function, the WDEN bit must be set to 1 and then cleared to 0.
M	11:6	rw	**Set mantissa of pre-divider** (Reset value = 32 decimal) Fdither = Fsys / ((M+1) * 2^N)
N	5:2	rw	**Set exponent of pre-divider** (Reset value = 6) Fdither = Fsys / ((M+1) * 2^N)
Fsys div	1:0	rw	**Set F_{CLK} / F_{SYS} divider** 00 - divide by 8 (Reset value) 01 - divide by 6 10 - divide by 4 11 - divide by 2 Note: Autozero should be initiated after changing the divider, first write to this register after powerup automatically starts the autozero process

Note: Following a reset or power-up event, the outputs are disabled until this register has been written to.

12.6 CALIBRATION REGISTER

CAL
Calibration Register **Reset Value: 0500 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	0	0	0	0	1	0	1	CM	not used						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
not used										CAL2		CAL1		CAL0	

Field	Bits	Type	Description
R/W	31	rw	**Read / Write bit** 0 = Read 1 = Write When reading this register, the R/W bit is 0
CM	23	rw	**Enable Calibration Mode** 0 = Disable Calibration Mode (Reset value) 1 = Enable Calibration Mode
CAL2	5:4	rw	**Set LOAD2 output stage state in calibration mode** 00 = HS and LS FETs off (Reset value) 01 = HS FET off, LS FET on 10 = HS FET on, LS FET off 11 = HS and LS FETs off
CAL1	3:2	rw	**Set LOAD1 output stage state in calibration mode** 00 = HS and LS FETs off (Reset value) 01 = HS FET off, LS FET on 10 = HS FET on, LS FET off 11 = HS and LS FETs off
CAL0	1:0	rw	**Set LOAD0 output stage state in calibration mode** 00 = HS and LS FETs off (Reset value) 01 = HS FET off, LS FET on 10 = HS FET on, LS FET off 11 = HS and LS FETs off

12.7 SETPOINT REGISTER

SETPOINT
Setpoint register **Reset Value: 1x40 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	0	0	1	0	not used	Channel #		EN	AL	not used					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
not used					Setpoint										

Field	Bits	Type	Description
R/W	31	rw	**Read / Write bit** 0 = Read 1 = Write When reading this register, the R/W bit is 0
Channel	25:24	rw	**Channel Number** 00 = LOAD0 01 = LOAD1 10 = LOAD2
EN	23	rw	**Enable channel** 1 = enable the addressed channel 0 = disable the addressed channel EN cannot be set=1 until the Diag register is read
Auto Limit	22	rw	**Enable integrator autolimit for the addressed channel** 1 = enable autolimit (Reset value) limit=20d and -20d 0 = disable autolimit
Setpoint	10:0	rw	**Set average current setpoint of addressed channe**l (Reset value=0) lsb = (1500/2047) mA

12.8 DITHER REGISTER

DITHER
Dither Register **Reset Value: 1x00 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	0	0	1	1	not used	Channel #		EN	SYNC	CFB MODE	not used				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Number of dither steps						not used				Dither step size					

Field	Bits	Type	Description
R/W	31	rw	**Read / Write bit** 0 = Read 1 = Write When reading this register, the R/W bit is 0
Channel	25:24	rw	**Channel Number** 00 = LOAD0 01 = LOAD1 10 = LOAD2
EN	23	rw	**Enable dither for the addressed channel** 1 = enable dither 0 = disable dither (reset value)
SYNC	22	rw	**Enable Synchronization of Dither to PWM frequency** 1 = enable synchronization - start of dither synched to start of PWM cycle 0 = disable synchronization - free running dither (Reset value)
CFB MODE	21	rw	**Mode for Current Feedback** 1 = Min / Max / PWM periods per dither period 0 = Average current and switching period
Steps	15:10	rw	**Set the dither steps of the addressed channel** (Reset value = 0) number of steps in a quarter dither cycle. Step duration = 1/Fdith
Step Size	5:0	rw	**Set the dither stepsize of addressed channel** (Reset value = 0) lsb = (1500/2047) mA. Note: the product of the Steps and Step Size values must not exceed 1023, otherwise the dither waveform will be incorrect.

12.9 INTEGRATOR LIMIT REGISTER

INT LIMIT
Integrator Register **Reset Value: 2xFF FFFF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	0	1	0	0	not used	Channel #		High Limit							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
High Limit (cont)				Low Limit											

Field	Bits	Type	Description
R/W	31	rw	**Read / Write bit** 0 = Read 1 = Write When reading this register, the R/W bit is 0
Channel	25:24	rw	**Channel Number** 00 = LOAD0 01 = LOAD1 10 = LOAD2
High Limit	23:12	rw	**Set high limit of integrator (Reset value = 07FFH)** effective value is 32 * High Limit value
Low Limit	11:0	rw	**Set low limit of integrator (Reset value= 07FFH)** effective value is -32 * Low Limit value

12.10 PWM PERIOD REGISTER

PWM PERIOD
PWM period register **Reset Value: 2x20 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	0	1	0	1	not used	Channel #		not used	KI_index			not used			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
not used				PWM Period											

Field	Bits	Type	Description
R/W	31	rw	**Read / Write bit** 0 = Read 1 = Write When reading this register, the R/W bit is 0
Channel	25:24	rw	**Channel Number** 00 = LOAD0 01 = LOAD1 10 = LOAD2
KI_index	22:20	rw	**Set the KI gain for the PWM period controller** KI = 2^-KI_index. Maximum value = 6. Writing 7 to this field will result in KI_index=6 KI_index reset value = 010_B KI reset value = 1/4
PWM Period	11:0	rw	**Set the PWM period** lsb = 16 / F_{SYS}

12.11 INTEGRATOR THRESHOLD &OPEN ON REGISTER

Integrator Threshold & Open On Register

Reset Value: 3x00 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	**0**	**1**	**1**	**0**	**not used**	**Channel #**		**not used**		**Integrator Threshold**					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Integrator Threshold (cont)										**Open Load on Limit**					

Field	Bits	Type	Description
R/W	31	rw	**Read / Write bit** 0 = Read 1 = Write When reading this register, the R/W bit is 0
Channel	25:24	rw	**Channel Number** 00 = LOAD0 01 = LOAD1 10 = LOAD2
Integrator Threshold	21:6	r	**Integrator Threshold - Read Only** threshold at which the output stage is turned off. Controlled by PWM period controller. Reset value = 0
Open Load on Limit	5:0	rw	**Set the open load while on current threshold** lsb = (1500/255) mA Reset value = 0 Must be written with a non-zero value to enable open load while on fault detection

12.12 AUTOZERO REGISTER

AUTOZERO
Autozero Register **Reset Value: 3x80 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	0	1	1	1	not used	Channel #		AZ Start							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
not used			AZ Value												

Field	Bits	Type	Description
R/W	31	rw	**Read / Write bit** 0 = Read 1 = Write When reading this register, the R/W bit is 0
Channel	25:24	rw	**Channel Number** 00 = LOAD0 01 = LOAD1 10 = LOAD2
AZ Start	23	rw	**Initiate Auto Zero** 1 = start autozero sequence (Reset value) 0 = no effect The EN bit in the SETPOINT register must be set to 0 in order to perform the autozero function.
AZ Value	12:0	r	**Read the offset of addressed channel (Reset value = 0)** After the autozero sequence is completed, the AZ Value field will contain the measured offset.

12.13 FEEDBACK REGISTER

FEEDBACK
Feedback Register **Reset Value: 4x00 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	1	0	0	0	not used	Channel #		CAL MODE - Current Feedback							
								CFB=0 - Current Feedback							
								CFB=1 - Max Current							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAL MODE - Current Feedback (cont)								not used							
CFB=0 Current FB (cont)				CFB=0 Period Feedback											
CFB=1 - MIN Current								CFB = 1 - # switching periods in dither cycle							

Field	Bits	Type	Description
R/W	31	rw	**Read / Write bit** 0 = Read 1 = Read (cannot write to this register) When reading this register, the R/W bit is 0
Channel	25:24	r	**Channel Number** 00 = LOAD0 01 = LOAD1 10 = LOAD2
CAL MODE Current FB	23:8	r	**CAL Mode = 1 Current Feedback** lsb = (1500/65535) mA
Current FB	23:12	r	**CAL Mode = 0 & CFB Mode = 0 Current Feedback** Average Load Current = 1.5 * Current FB / Period FB Average current measured over the last switching cycle Field value = 0 if channel is not operating Value set to 00 after read
Period FB	11:0	r	**CAL Mode = 0 & CFB Mode = 0 Switching Period Feedback** 1 lsb = 16 / F_{SYS} Period of last switching cycle Field value = 0 if channel is not operating
MAX Current	23:16	r	**CAL Mode = 0 & CFB Mode = 1 MAX Current Feedback** lsb = (1500/127) mA Maximum current measured over last dither cycle (dither enabled) Maximum current measured since last read of this register (dither off) Field value = 0 if channel is not operating Value set to 00 after read

Field	Bits	Type	Description
MIN Current	15:8	r	**CAL Mode = 0 & CFB Mode = 1 MIN Current Feedback** lsb = (1500/127) mA Minimum current measured over last dither cycle (dither enabled) Minimum current measured since last read of this register (dither off) Field value = 0 if channel is not operating Value set to FF after read
Switching cycles per dither cycle	7:0	r	**CAL Mode = 0 & CFB Mode = 1 Switching cycles per dither cycle** 1 lsb = 1 switching cycle Field value = 0 if channel is not operating or dither is disabled Value set to 00 after read

Attention: Max. current, Min. current and Switching cycles per dither are set as indicated in the SPI description

13 Application Information

This is the description how the IC is used in its environment…

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

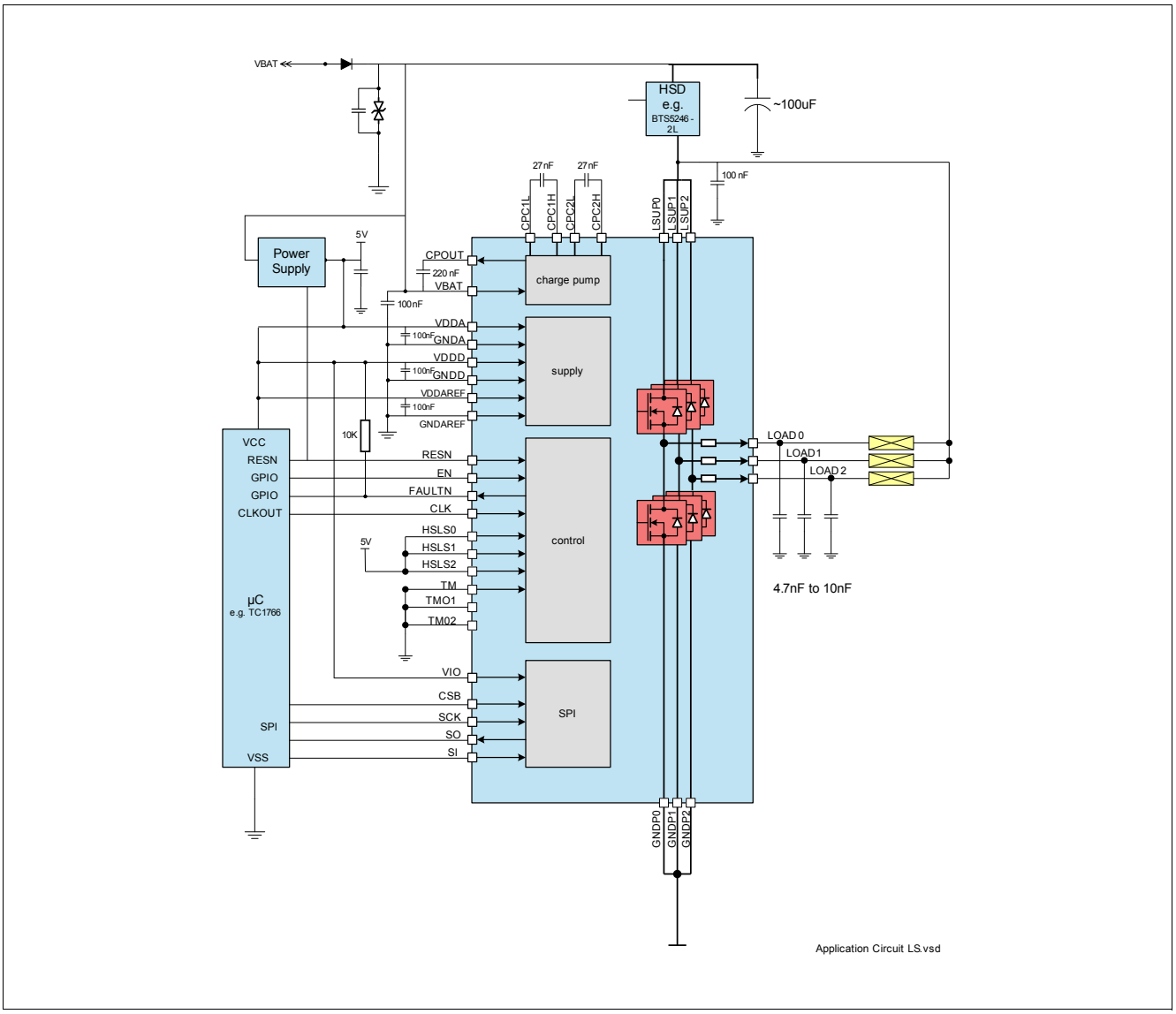

Figure 37 Application Diagram - Low-Side Configuration

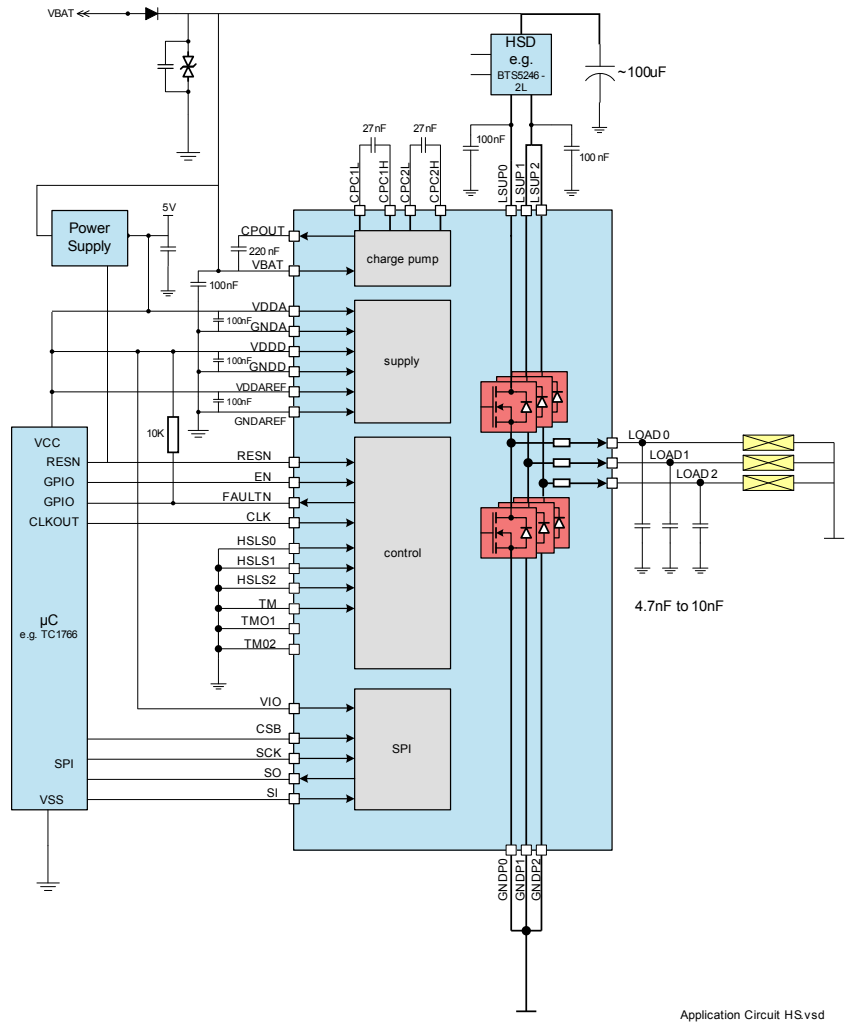

Figure 38 Application Diagram - High-Side Configuration

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

13.1 Further Application Information

- Please contact us for information regarding the pin FMEA
- For further information you may contact **http://www.infineon.com/**

14 Package Outlines

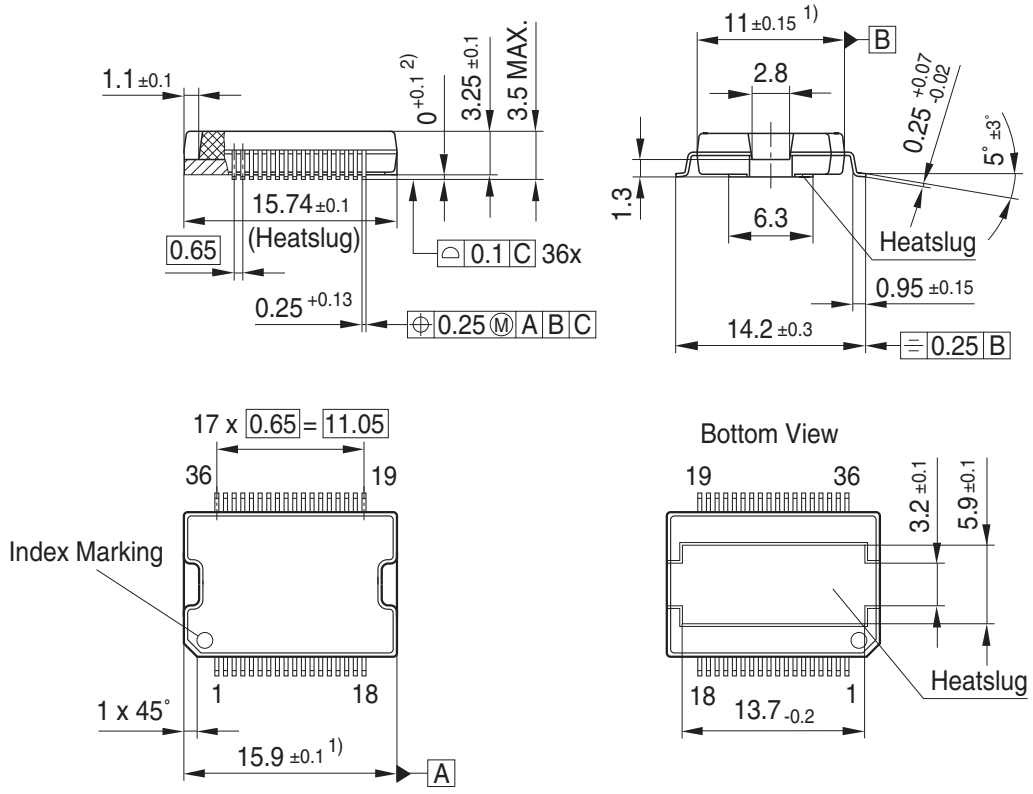

Figure 39 PG-DSO-36

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

15 Revision History

Revision	Date	Changes
1.0	2015-03-17	Initial Data Sheet

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