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NTE4528B & NTE4528BT
Integrated Circuit
CMOS, Dual Retriggerable/Resettable
Monostable Multivibrator

Description:

The NTE4528B (16–Lead DIP) and NTE4528BT (SOIC–16) are dual, retriggerable, resettable monostable multivibrators that may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components, C_X and R_X.

Features:

- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3Vcd to 18Vdc
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- These devices should only be used in circuits where he pulse width is < 10μs. For circuits requiring a pulse width > 10μs, please see NTE4538B, which is pin–for–pin compatible.

Absolute Maximum Ratings: (Voltages Referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out} . . . . . –0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in} . . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{out} . . . . . ±10mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . –7.0mW/°C
Ambient Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L . . . . . +260°C

Note 1. Stresses exceeding Absolute Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

These devices contain protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage "0" Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current	I_{OH}									
(V_{OH} = 2.5Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	mAdc
(V_{OH} = 4.6Vdc)			−0.64	–	−0.51	−0.88	–	−0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	mAdc
(V_{OL} = 0.4Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	µAdc
		15	–	15	–	0.015	15	–	600	µAdc
Total Supply Current at an External Load Capacitance (C_L) and at External Timing Capacitance (C_X), use the formula. (Note 3)	I_T	–	$I_T(C_L, C_X) = [(C_L + 0.36C_X)\ V_{DD} f + 21 \times 10^{-8}$ $R_X C_X (V_{DD}^{-2}) 2f] \times 10^{-3}$ where: I_T in µA (per circuit), C_L and C_X in pF, R_X in MΩ, V_{DD} in Vdc, f in kHz is input frequency.							µAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}							
t_{TLH}, t_{THL} = (1.5ns/pf) C_L + 25ns		–	–	5.0	–	100	200	ns
t_{TLH}, t_{THL} = (0.75ns/pf) C_L + 12.5ns		–	–	10	–	50	100	ns
t_{TLH}, t_{THL} = (0.55ns/pf) C_L + 0.5ns		–	–	15	–	40	80	ns

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. If C_X > 15µF, use a discharge protection diode.

Note 5. R_X is in Ω, C_X is in farads, V_{DD} and V_{SS} in volts, Pw_{out} in seconds.

Switching Characteristics (Cont'd): (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Min	Typ	Max	Unit
Turn−Off, Turn−On Delay Time A or B to Q or $\overline{Q}$	t_{PHL}, t_{PHL}							
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 240ns		15	5.0	5.0	–	325	650	ns
t_{PLH}, t_{PHL} = (0.75ns/pf) C_L + 37.5ns				10	–	120	240	ns
t_{PLH}, t_{PHL} = (0.55ns/pf) C_L + 37.5ns				15	–	90	180	ns
Turn−Off, Turn−On Delay Time A or B to Q or $\overline{Q}$	t_{PHL}, t_{PHL}							
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 620ns		1000	10	5.0	–	705	–	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 255ns				10	–	290	–	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 185ns				15	–	210	–	ns
Input Pulse Width A or B	t_{WH}	15	5.0	5.0	150	70	–	ns
				10	75	30	–	ns
				15	55	30	–	ns
	t_{WL}	1000	10	5.0	–	70	–	ns
				10	–	30	–	ns
				15	–	30	–	ns
Output Pulse Width Q or $\overline{Q}$	t_W	15	5.0	5.0	–	550	–	ns
				10	–	350	–	ns
				15	–	300	–	ns
Output Pulse Width Q or $\overline{Q}$ (For C_X > 0.01μF use formula: t_W = 0.2 R_X C_X L_n [V_{DD} − V_{SS}]) Note 4	t_W	10,000	10	5.0	15	30	45	μs
				10	10	50	90	μs
				15	15	55	90	μs
Pulse Width match between Circuits in the same package	11−12	10,000	10	5.0	–	6.0	25	%
				10	–	8.0	35	%
				15	–	8.0	35	%
Reset Propagation Delay $\overline{Reset}$ to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0	5.0	–	325	600	ns
				10	–	90	225	ns
				15	–	60	170	ns
		1000	10	5.0	–	1000	–	ns
				10	–	300	–	ns
				15	–	250	–	ns
Retrigger Time	t_{rr}	15	5.0	5.0	0	–	–	ns
				10	0	–	–	ns
				15	0	–	–	ns
		1000	10	5.0	0	–	–	ns
				10	0	–	–	ns
				15	0	–	–	ns
External Timing Resistance	R_X	–	–	–	5.0	–	1000	kΩ
External Timing Capacitance	C_X	–	–	–	No Limits (Note 5)			μF

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

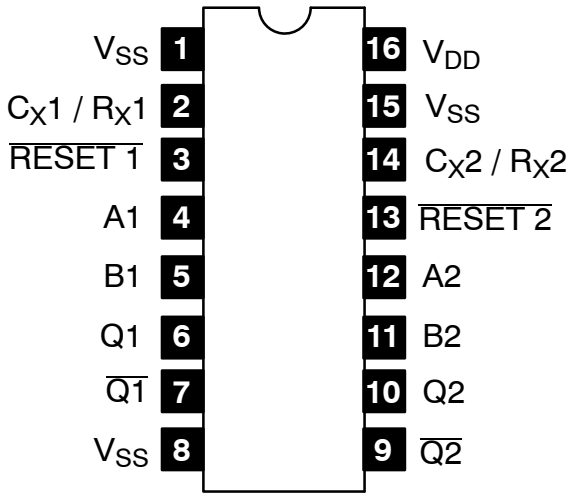
Note 4. If C_X > 15μF, use a discharge protection diode.

Note 5. R_X is in Ω, C_X is in farads, V_{DD} and V_{SS} in volts, Pw_{out} in seconds.

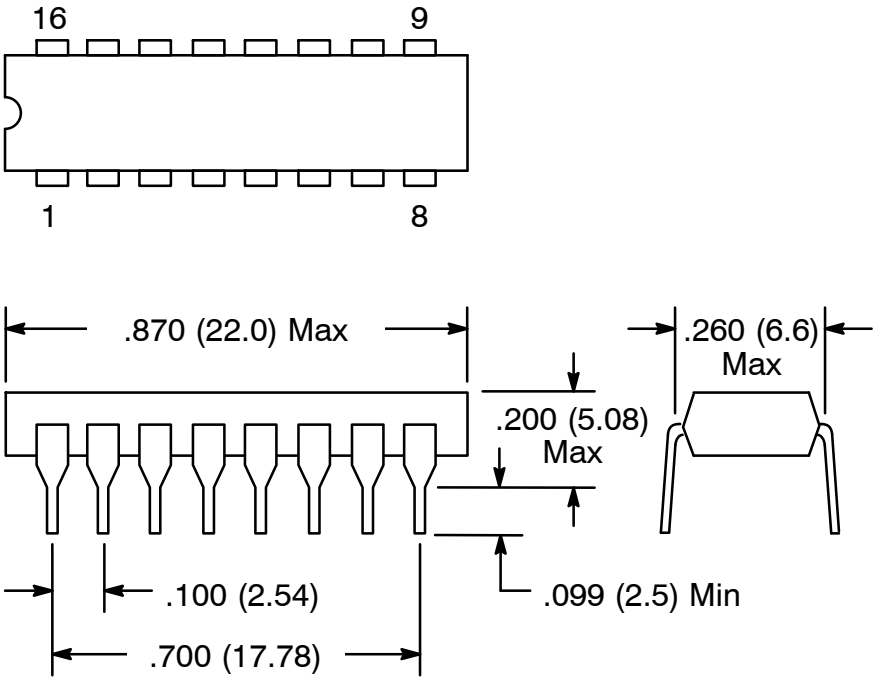
Function Table:

Inputs			Outputs	
Reset	**A**	**B**	**Q**	**$\overline{Q}$**
H	↑	H	⊓	⊔
H	L	↓	⊓	⊔
H	↑ ↓	L	Not Triggered	
H	H	↑ ↓	Not Triggered	
H	L, H, ↓	H	Not Triggered	
H	L	L, H, ↑	Not Triggered	
L	X	X	L	H
↓ ↑	X	X	Not Triggered	

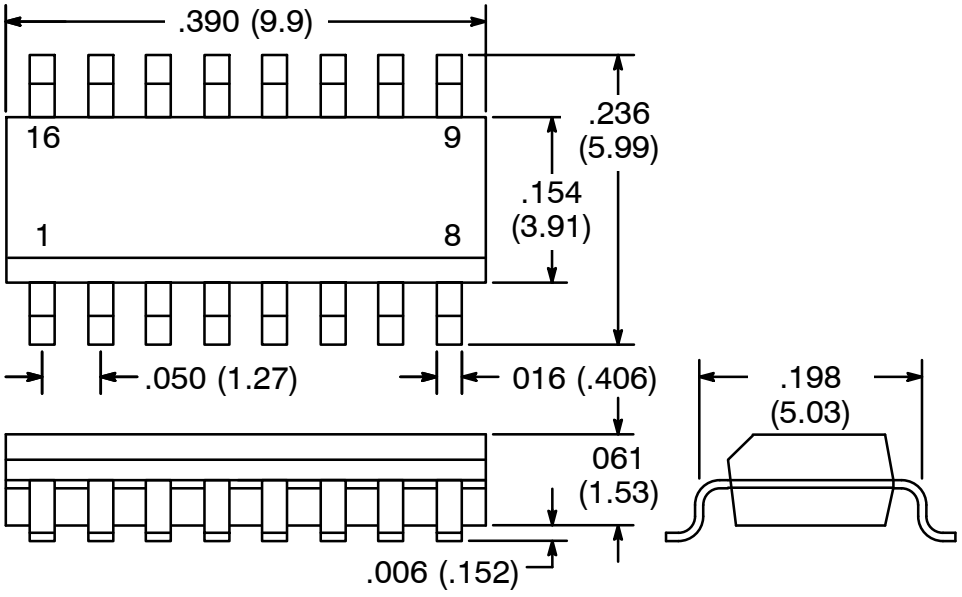
Pin Connection Diagram



NTE4528B



NTE4528BT



NOTE: Pin1 on Beveled Edge