TPS65022 Power Management IC for Li-Ion Powered Systems

1 Features

- 1.2-A, 97% Efficient Step-Down Converter for System Voltage (VDCDC1)
- 1-A, Up to 95% Efficient Step-Down Converter for Memory Voltage (VDCDC2)
- 900-mA, 90% Efficient Step-Down Converter for Processor Core (VDCDC3)
- 30-mA LDO and Switch for Real-Time Clock (VRTC)
- 2 × 200 mA General-Purpose LDO
- Dynamic Voltage Management for Processor Core
- Preselectable LDO Voltage Using Two Digital Input Pins
- Externally Adjustable Reset Delay Time
- Battery Backup Functionality
- Separate Enable Pins for Inductive Converters
- I²C Compatible Serial Interface
- 85-µA Quiescent Current
- Low Ripple PFM Mode
- Thermal Shutdown Protection

2 Applications

- PDA
- Cellular and Smart Phones
- Internet Audio Players
- Digital Still Cameras
- Digital Radio Players
- Split Supply TMS320™ DSP Family and µP Solutions:
  OMAP™1610, OMAP1710, OMAP330, XScale Bulverde, Samsung ARM-Based Processors, and so forth
- Intel® PXA270, and so forth

3 Description

The TPS65022 is an integrated Power Management IC for applications powered by one Li-Ion or Li-Polymer cell, and which require multiple power rails. The TPS65022 provides three highly efficient, step-down converters targeted at providing the core voltage, peripheral, I/O and memory rails in a processor based system.

All three step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents. The TPS65022 also integrates two general-purpose 200-mA LDO voltage regulators, which are enabled with an external input pin. Each LDO operates with an input voltage range between 1.5 V and 6.5 V, allowing them to be supplied from one of the step-down converters or directly from the battery.

The default output voltage of the LDOs can be digitally set to 4 different voltage combinations using the DEFLDO1 and DEFLDO2 pins.

The serial interface can be used for dynamic voltage scaling, masking interrupts, or for disabling, enabling, and setting the LDO output voltages. The interface is compatible with the Fast/Standard mode I²C specification, allowing transfers at up to 400 kHz. The TPS65022 is available in a 40-pin (RHA) VQFN package, and operates over a free-air temperature of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65022	VQFN (40)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

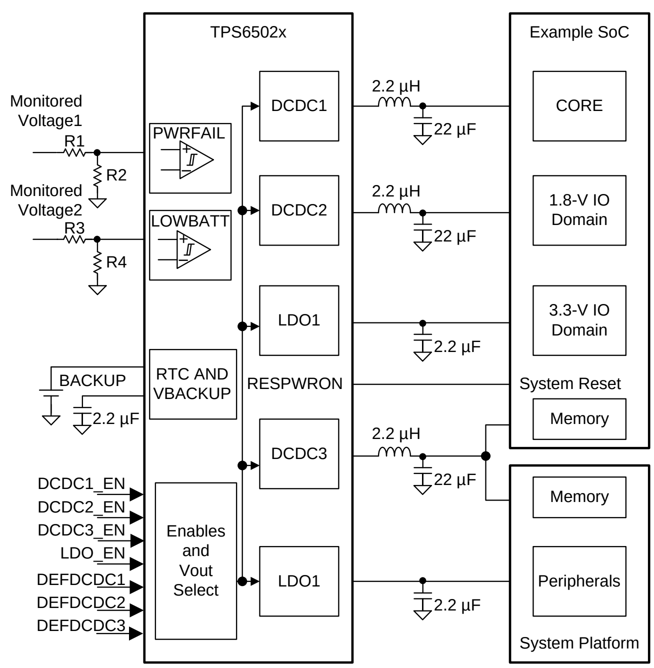


Table of Contents

4 Revision History

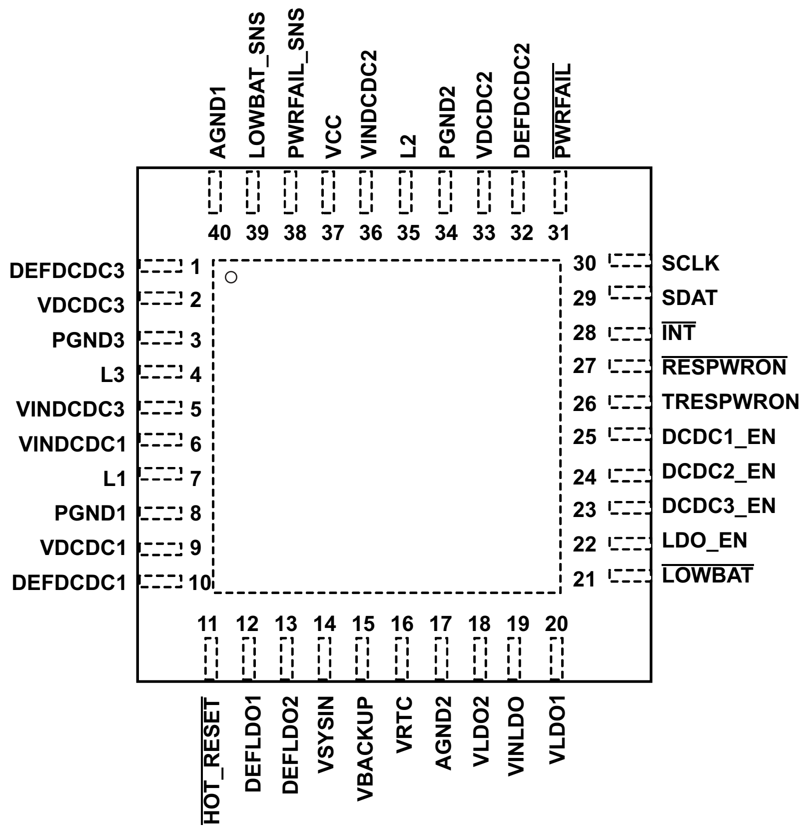
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2006) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

5 Pin Configuration and Functions

RHA Package
40-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SWITCHING REGULATOR SECTION			
AGND1	40	—	Analog ground connection. All analog ground pins are connected internally on the chip.
AGND2	17	—	Analog ground connection. All analog ground pins are connected internally on the chip.
DCDC1_EN	25	I	VDCDC1 enable pin. A logic high enables the regulator, a logic low disables the regulator.
DCDC2_EN	24	I	VDCDC2 enable pin. A logic high enables the regulator, a logic low disables the regulator.
DCDC3_EN	23	I	VDCDC3 enable pin. A logic high enables the regulator, a logic low disables the regulator.
DEFDCDC1	10	I	Input signal indicating default VDCDC1 voltage, 0 = 3 V, 1 = 3.3 V. This pin can also be connected to a resistor divider between VDCDC1 and GND. If the output voltage of the DCDC1 converter is set in a range from 0.6 V to VINDCDC1 V.
DEFDCDC2	32	I	Input signal indicating default VDCDC2 voltage, 0 = 1.8 V, 1 = 2.5 V. This pin can also be connected to a resistor divider between VDCDC2 and GND. If the output voltage of the DCDC2 converter is set in a range from 0.6 V to VINDCDC2 V.
DEFDCDC3	1	I	Input signal indicating default VDCDC3 voltage, 0 = 1.3 V, 1 = 1.55 V. This pin can also be connected to a resistor divider between VDCDC3 and GND. If the output voltage of the DCDC3 converter is set in a range from 0.6 V to VINDCDC3 V.
L1	7	—	Switch pin of VDCDC1 converter. The VDCDC1 inductor is connected here.
L2	35	—	Switch pin of VDCDC2 converter. The VDCDC2 inductor is connected here.
L3	4	—	Switch pin of VDCDC3 converter. The VDCDC3 inductor is connected here.
PGND1	8	—	Power ground for VDCDC1 converter

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PGND2	34	—	Power ground for VDCDC2 converter
PGND3	3	—	Power ground for VDCDC3 converter
PowerPAD™	—	—	Connect the power pad to analog ground.
VCC	37	I	Power supply for digital and analog circuitry of VDCDC1, VDCDC2, and VDCDC3 DC-DC converters. This must be connected to the same voltage supply as VINDCDC3, VINDCDC1, and VINDCDC2. Also supplies serial interface block
VDCDC1	9	I	VDCDC1 feedback voltage sense input, connect directly to VDCDC1
VDCDC2	33	I	VDCDC2 feedback voltage sense input, connect directly to VDCDC2
VDCDC3	2	I	VDCDC3 feedback voltage sense input, connect directly to VDCDC3
VINDCDC1	6	I	Input voltage for VDCDC1 step-down converter. This must be connected to the same voltage supply as VINDCDC2, VINDCDC3, and VCC.
VINDCDC2	36	I	Input voltage for VDCDC2 step-down converter. This must be connected to the same voltage supply as VINDCDC1, VINDCDC3, and VCC.
VINDCDC3	5	I	Input voltage for VDCDC3 step-down converter. This must be connected to the same voltage supply as VINDCDC1, VINDCDC2, and VCC.
LDO REGULATOR SECTION			
DEFLD01	12	I	Digital input, used to set default output voltage of LDO1 and LDO2
DEFLD02	13	I	Digital input, used to set default output voltage of LDO1 and LDO2
LDO_EN	22	I	Enable input for LDO1 and LDO2. Logic high enables the LDOs, logic low disables the LDOs
VBACKUP	15	I	Connect the backup battery to this input pin.
VINLDO	19	I	I Input voltage for LDO1 and LDO2
VLDO1	20	O	Output voltage of LDO1
VLDO2	18	O	Output voltage of LDO2
VRTC	16	O	Output voltage of the LDO/switch for the real time clock
VSYSIN	14	I	Input of system voltage for VRTC switch
CONTROL AND I^2C SECTION			
HOT_RESET	11	I	Push button input used to reboot or wake-up processor through RESPWRON output pin
INT	28	O	Open-drain output
LOW_BAT	21	O	Open-drain output of LOW_BAT comparator
LOWBAT_SNS	39	I	Input for the comparator driving the LOW_BAT output.
PWRFAIL	31	O	Open-drain output. Active low when PWRFAIL comparator indicates low VBAT condition.
PWRFAIL_SNS	38	I	Input for the comparator driving the PWRFAIL output.
RESPWRON	27	O	Open-drain System reset output
SCLK	30	I	Serial interface clock line
SDAT	29	I/O	Serial interface data/address
TRESPWRON	26	I	Connect the timing capacitor to this pin to set the reset delay time: 1 nF → 100 ms

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage range on all pins except AGND and PGND pins with respect to AGND	–0.3	7	V
	Current at VINDCDC1, L1, PGND1, VINDCDC2, L2, PGND2, VINDCDC3, L3, PGND3		2000	mA
	Peak current at all other pins		1000	mA
T_A	Operating free-air temperature	–40	85	°C
T_J	Maxiumum junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Input voltage range step-down convertors (VINDCDC1, VINDCDC2, VINDCDC3); pins need to be tied to the same voltage rail	2.5		6	V
V_O	Output voltage range for VDCDC1 step-down convertor (1)	0.6		VINDCDC1	V
	Output voltage range for VDCDC2 (mem) step-down convertor (1)	0.6		VINDCDC2	
	Output voltage range for VDCDC3 (core) step-down convertor (1)	0.6		VINDCDC3	
V_I	Input voltage range for LDOs (VINLDO1, VINLDO2)	1.5		6.5	V
V_O	Output voltage range for LDOs (VLDO1, VLDO2)	1		VINLDO1-2	V
$I_{O(DCDC2)}$	Output current at L1			1200	mA
	Inductor at L1 (2)	2.2	3.3		µH
$C_{I(DCDC1)}$	Input capacitor at VINDCDC1 (2)	10			µF
$C_{O(DCDC1)}$	Output capacitor at VDCDC1 (2)	10	22		µF
$I_{O(DCDC2)}$	Output current at L2			1000	mA
	Inductor at L2 (2)	2.2	3.3		µH
$C_{I(DCDC2)}$	Input capacitor at VINDCDC2 (2)	10			µF
$C_{O(DCDC2)}$	Output capacitor at VDCDC2 (2)	10	22		µF
$I_{O(DCDC3)}$	Output current at L3			900	mA
	Inductor at L3 (2)	2.2	3.3		µH
$C_{I(DCDC3)}$	Input capacitor at VINDCDC3 (2)	10			µF
$C_{O(DCDC3)}$	Output capacitor at VDCDC3 (2)	10	22		µF
$C_{I(VCC)}$	Input capacitor at VCC (2)	1			µF
$C_{i(VINLDO)}$	Input capacitor at VINLDO (2)	1			µF
$C_{O(VLDO1-2)}$	Output capacitor at VLDO1, VLDO2 (2)	2.2			µF
$I_{O(VLDO1-2)}$	Output current at VLDO1, VLDO2			200	mA
$C_{O(VRTC)}$	Output capacitor at VRTC (2)	4.7			µF

(1) When using an external resistor divider at DEFDCDC3, DEFDCDC2, DEFDCDC1
(2) See *Application and Implementation* for more information.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C
	Resistor from VINDCDC3, VINDCDC2, VINDCDC1 to VCC used for filtering [3]		1	10	Ω

(3) Up to 3 mA can flow into V_{CC} when all 3 converters are running in PWM. This resistor causes the UVLO threshold to be shifted accordingly.

6.4 Thermal Information

THERMAL METRIC [1]		TPS65022	UNIT
		RHA (VQFN)	
		40 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL SIGNALS : SCLK, SDAT (input), DCDC1_EN, DCDC2_EN, DCDC3_EN, LDO_EN, DEFLDO1, DEFLDO2						
V_{IH}	High level input voltage	Rpullup at SCLK and SDAT = 4.7 kΩ, pulled to VRTC	1.3		VCC	V
V_{IL}	Low level input voltage	Rpullup at SCLK and SDAT = 4.7 kΩ, pulled to VRTC	0		0.4	V
I_H	Input bias current			0.01	0.1	μA
CONTROL SIGNALS : $\overline{\text{HOT\_RESET}}$						
V_{IH}	High level input voltage		1.3		VCC	V
V_{IL}	Low level input voltage		0		0.4	V
I_{IB}	Input bias current			0.01	0.1	μA
$t_{deglitch}$	Deglitch time at $\overline{\text{HOT\_RESET}}$		25	30	35	ms
CONTROL SIGNALS : $\overline{\text{LOWBAT}}$, $\overline{\text{PWRFAIL}}$, $\overline{\text{RESPWRON}}$, $\overline{\text{INT}}$, SDAT (output)						
V_{OH}	High level output voltage				6	V
V_{OL}	Low level output voltage	I_{IL} = 5 mA	0		0.3	V
	Duration of low pulse at $\overline{\text{RESPWRON}}$	External capacitor 1 nF		100		ms
ICONST	internal charge and discharge current on pin TRESPWRON	used for generating $\overline{\text{RESPWRON}}$ delay	1.7	2	2.3	μA
TRESPWR ON_LOWTH	internal lower comparator threshold on pin TRESPWRON	used for generating $\overline{\text{RESPWRON}}$ delay	0.225	0.25	0.275	V
TRESPWR ON_UPTH	internal upper comparator threshold on pin TRESPWRON	used for generating $\overline{\text{RESPWRON}}$ delay	0.97	1	1.103	V
	Resetpwron threshold	VRTC falling	–3%	2.4	3%	V
	Resetpwron threshold	VRTC rising	–3%	2.52	3%	V
I_{LK}	leakage current	output inactive high			0.1	μA

Electrical Characteristics (continued)

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY PINS: VCC, VINDCDC1, VINDCDC2, VINDCDC3							
$I_{(q)}$	Operating quiescent current, PFM	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)}$ = 0 V	All 3 DCDC converters enabled, zero load and no switching, LDOs enabled		85	100	µA
			All 3 DCDC converters enabled, zero load and no switching, LDOs off		78	90	
			DCDC1 and DCDC2 converters enabled, zero load and no switching, LDOs off		57	70	
			DCDC1 converter enabled, zero load and no switching, LDOs off		43	55	
I_I	Current into VCC; PWM	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)}$ = 0 V	All 3 DCDC converters enabled and running in PWM, LDOs off		2	3	mA
			DCDC1 and DCDC2 converters enabled and running in PWM, LDOs off		1.5	2.5	
			DCDC1 converter enabled and running in PWM, LDOs off		0.85	2	
$I_{(q)}$	Quiescent current	All converters disabled, LDOs off, $V_{(VSYSIN)}$ = 0 V	VCC = 3.6 V, VBACKUP = 3 V		23	33	µA
			VCC = 2.6 V, VBACKUP = 3 V		3.5	5	
			VCC = 3.6 V, VBACKUP = 0 V			43	
SUPPLY PINS: VBACKUP, VSYSIN, VRTC							
$I_{(q)}$	Operating quiescent current	VBACKUP = 3 V, VSYSIN = 0 V; VCC = 2.6 V, current into VBACKUP			20	33	µA
$I_{(SD)}$	Operating quiescent current	VBACKUP < V_VBACKUP, current into VBACKUP			2	3	µA
	VRTC LDO output voltage	VSYSIN = VBACKUP = 0 V, I_O = 0 mA			3		V
I_O	Output current for VRTC	VSYSIN < 2.57 V and VBACKUP < 2.57 V				30	mA
	VRTC short-circuit current limit	VRTC = GND; VSYSIN = VBACKUP = 0 V				100	mA
	Maximum output current at VRTC for $\overline{RESPWRON}$ = 1	VRTC > 2.6 V, V_{CC} = 3 V; VSYSIN = VBACKUP = 0 V		30			mA
V_O	Output voltage accuracy for VRTC	VSYSIN = VBACKUP = 0 V; I_O = 0 mA		–1%		1%	
	Line regulation for VRTC	VCC = VRTC + 0.5 V to 6.5 V, I_O = 5 mA		–1%		1%	
	Load regulation VRTC	I_O = 1 mA to 30 mA; VSYSIN = VBACKUP = 0 V		–3%		1%	
	Regulation time for VRTC	Load change from 10% to 90%			10		µs
I_{lkg}	Input leakage current at VSYSIN	VSYSIN < V_VSYSIN				2	µA
	$r_{DS(on)}$ of VSYSIN switch					12.5	Ω
	$r_{DS(on)}$ of VBACKUP switch					12.5	Ω
	Input voltage range at VBACKUP(1)			2.73		3.75	V
	Input voltage range at VSYSIN(1)			2.73		3.75	V
	VSYSIN threshold	VSYSIN falling		–3%	2.55	3%	V
	VSYSIN threshold	VSYSIN rising		–3%	2.65	3%	V
	VBACKUP threshold	VBACKUP falling		–3%	2.55	3%	V
	VBACKUP threshold	VBACKUP falling		–3%	2.65	3%	V
SUPPLY PIN: VINLDO							
$I_{(q)}$	Operating quiescent current	Current per LDO into VINLDO			16	30	µA
$I_{(SD)}$	Shutdown current	Total current for both LDOs into VINLDO, VLDO = 0 V			0.1	1	µA
VDCDC1 STEP-DOWN CONVERTER							
V_I	Input voltage range, VINDCDC1			2.5		6	V
I_O	Maximum output current			1200			mA
$I_{(SD)}$	Shutdown supply current in VINDCDC1	DCDC1_EN = GND			0.1	1	µA
$r_{DS(on)}$	P-channel MOSFET on-resistance	VINDCDC1 = $V_{(GS)}$ = 3.6 V			125	261	mΩ
I_{lkg}	P-channel leakage current	VINDCDC1 = 6 V				2	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance	VINDCDC1 = $V_{(GS)}$ = 3.6 V			130	260	mΩ
I_{lkg}	N-channel leakage current	$V_{(DS)}$ = 6 V			7	10	µA

(1) Based on the requirements for the Intel PXA270 processor.

Electrical Characteristics (continued)

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless noted otherwise)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Forward current limit (P- and N-channel)		2.5 V < $V_{I(MAIN)}$ < 6 V	1.55	1.75	1.95	A
f_S	Oscillator frequency			1.3	1.5	1.7	MHz
	Fixed output voltage FPWMDCDC1 = 0	3 V	VINDCDC1 = 3.3 V to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–2%		2%	
		3.3 V	VINDCDC1 = 3.6 V to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–2%		2%	
	Fixed output voltage FPWMDCDC1 = 1	3 V	VINDCDC1 = 3.3 V to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–1%		1%	
		3.3 V	VINDCDC1 = 3.6 V to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–1%		1%	
	Adjustable output voltage with resistor divider at DEFDCDC1; FPWMDCDC1 = 0		VINDCDC1 = VDCDC1 + 0.3 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC1; FPWMDCDC1 = 1		VINDCDC1 = VDCDC1 + 0.3 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–1%		1%	
	Line Regulation		VINDCDC1 = VDCDC1 + 0.3 V (min 2.5 V) to 6 V; I_O = 10 mA		0		%/V
	Load Regulation		I_O = 10 mA to 1200 mA		0.25		%/A
	Soft start ramp time		VDCDC1 ramping from 5% to 95% of target value		750		µs
	Internal resistance from L1 to GND				1		MΩ
	VDCDC1 discharge resistance		DCDC1 discharge = 1		300		Ω
VDCDC2 STEP-DOWN CONVERTER							
V_I	Input voltage range, VINDCDC2			2.5		6	V
I_O	Maximum output current			1000			mA
$I_{(SD)}$	Shutdown supply current in VINDCDC2		DCDC2_EN = GND		0.1	1	µA
$r_{DS(on)}$	P-channel MOSFET on-resistance		VINDCDC2 = $V_{(GS)}$ = 3.6 V		140	300	mΩ
I_{lkg}	P-channel leakage current		VINDCDC2 = 6 V			2	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance		VINDCDC2 = $V_{(GS)}$ = 3.6 V		150	297	mΩ
I_{lkg}	N-channel leakage current		$V_{(DS)}$ = 6 V		7	10	µA
I_{LIMF}	Forward current limit (P- and N-channel)		2.5 V < VINDCDC2 < 6 V	1.4	1.55	1.7	A
f_S	Oscillator frequency			1.3	1.5	1.7	MHz
	Fixed output voltage FPWMDCDC2 = 0	1.8 V	VINDCDC2 = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 1 A	–2%		2%	
		2.5 V	VINDCDC2 = 2.8 V to 6 V; 0 mA ≤ I_O ≤ 1 A	–2%		2%	
	Fixed output voltage FPWMDCDC2 = 1	1.8 V	VINDCDC2 = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 1 A	–2%		2%	
		2.5 V	VINDCDC2 = 2.8 V to 6 V; 0 mA ≤ I_O ≤ 1 A	–1%		1%	
	Adjustable output voltage with resistor divider at DEFDCDC2 FPWMDCDC2 = 0		VINDCDC2 = VDCDC2 + 0.3 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1 A	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC2; FPWMDCDC2 = 1		VINDCDC2 = VDCDC2 + 0.3 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1 A	–1%		1%	
	Line Regulation		VINDCDC2 = VDCDC2 + 0.3 V (min 2.5 V) to 6 V; I_O = 10 mA		0		%/V
	Load Regulation		I_O = 10 mA to 1 mA		0.25		%/A
	Soft start ramp time		VDCDC2 ramping from 5% to 95% of target value		750		µs
	Internal resistance from L2 to GND				1		MΩ
	VDCDC2 discharge resistance		DCDC2 discharge =1		300		Ω
VDCDC3 STEP-DOWN CONVERTER							
V_I	Input voltage range, VINDCDC3			2.5		6	V
I_O	Maximum output current			900			mA
$I_{(SD)}$	Shutdown supply current in VINDCDC3		DCDC3_EN = GND		0.1	1	µA
$r_{DS(on)}$	P-channel MOSFET on-resistance		VINDCDC3 = $V_{(GS)}$ = 3.6 V		310	698	mΩ
I_{lkg}	P-channel leakage current		VINDCDC3 = 6 V		0.1	2	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance		VINDCDC3 = $V_{(GS)}$ = 3.6 V		220	503	mΩ
I_{lkg}	N-channel leakage current		$V_{(DS)}$ = 6 V		7	10	µA
	Forward current limit (P- and N-channel)		2.5 V < VINDCDC3 < 6 V	1.15	1.34	1.52	A
f_S	Oscillator frequency			1.3	1.5	1.7	MHz

Electrical Characteristics (continued)

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Fixed output voltage FPWMDCDC3 = 0	All VDCDC3	VINDCDC3 = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 800 mA	–2%		2%	
	Fixed output voltage FPWMDCDC3 = 1	All VDCDC3	VINDCDC3 = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 800 mA	–1%		1%	
	Adjustable output voltage with resistor divider at DEFDCDC3 FPWMDCDC3 = 0		VINDCDC3 = VDCDC3 + 0.5 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 800 mA	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC3; FPWMDCDC3 = 1		VINDCDC3 = VDCDC3 + 0.5 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 800 mA	–1%		1%	
	Line Regulation		VINDCDC3 = VDCDC3 + 0.3 V (min 2.5 V) to 6 V; I_O = 10 mA		0		%/V
	Load Regulation		I_O = 10 mA to 400 mA		0.25		%/A
	Soft start ramp time		VDCDC3 ramping from 5% to 95% of target value		750		μs
	Internal resistance from L3 to GND				1		MΩ
	VDCDC3 discharge resistance		DCDC3 discharge =1		300		Ω
VLDO1 and VLDO2 LOW DROPOUT REGULATORS							
V_I	Input voltage range for LDO1, 2			1.5		6.5	V
V_O	LDO1 output voltage range			1		3.3	V
V_O	LDO2 output voltage range			1		3.3	V
I_O	Maximum output current for LDO1, LDO2		V_I = 1.8 V, V_O = 1.3 V	200			mA
			V_I = 1.5 V, V_O = 1.3 V		120		
$I_{(SC)}$	LDO1 and LDO2 short circuit current limit		$V_{(LDO1)}$ = GND, $V_{(LDO2)}$ = GND			400	mA
	Minimum voltage drop at LDO1, LDO2		I_O = 50 mA, VINLDO = 1.8 V			120	mV
			I_O = 50 mA, VINLDO = 1.5 V		65	150	
			I_O = 200 mA, VINLDO = 1.8 V			300	
	Output voltage accuracy for LDO1, LDO2		I_O = 10 mA	–2%		1%	
	Line regulation for LDO1, LDO2		VINLDO1,2 = VLDO1,2 + 0.5 V (min 2.5 V) to 6.5 V, I_O = 10 mA	–1%		1%	
	Load regulation for LDO1, LDO2		I_O = 0 mA to 50 mA	–1%		1%	
	Regulation time for LDO1, LDO2		Load change from 10% to 90%		10		μs
ANALOGIC SIGNALS DEFDCDC1, DEFDCDC2, DEFDCDC3							
V_{IH}	High level input voltage			1.3		VCC	V
V_{IL}	Low level input voltage			0		0.1	V
	Input bias current				0.001	0.05	μA
THERMAL SHUTDOWN							
$T_{(SD)}$	Thermal shutdown		Increasing junction temperature		160		°C
	Thermal shutdown hysteresis		Decreasing junction temperature		20		°C
INTERNAL UNDERVOLTAGE LOCK OUT							
UVLO	Internal UVLO		VCC falling	–2%	2.35	2%	V
$V_{(UVLO\_HYST)}$	Internal UVLO comparator hysteresis				120		mV
VOLTAGE DETECTOR COMPARATORS							
	Comparator threshold (PWRFAIL_SNS, LOWBAT_SNS)		Falling threshold	–1%	1	1%	V
	Hysteresis			40	50	60	mV
	Propagation delay		25 mV overdrive			10	μs
POWER GOOD							
$V_{(PGOODF)}$			VDCDC1, VDCDC2, VDCDC3, VLDO1, VLDO2, decreasing	–12%	–10%	–8%	
$V_{(PGOODR)}$			VDCDC1, VDCDC2, VDCDC3, VLDO1, VLDO2, increasing	–7%	–5%	–3%	

6.6 Timing Requirements

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 2.5 V to 5.5 V, VBACKUP = 3 V, T_A = –40°C to 85°C.

		MIN	MAX	UNIT
f_{MAX}	Clock frequency		400	kHz
$t_{wH(HIGH)}$	Clock high time	600		ns
$t_{wL(LOW)}$	Clock low time	1300		ns
t_R	DATA and CLK rise time		300	ns
t_F	DATA and CLK fall time		300	ns
$t_{h(STA)}$	Hold time (repeated) START condition (after this period the first clock pulse is generated)	600		ns
$t_{h(DATA)}$	Setup time for repeated START condition	600		ns
$t_{h(DATA)}$	Data input hold time	0		ns
$t_{su(DATA)}$	Data input setup time	100		ns
$t_{su(STO)}$	STOP condition setup time	600		ns
$t_{(BUF)}$	Bus free time	1300		ns

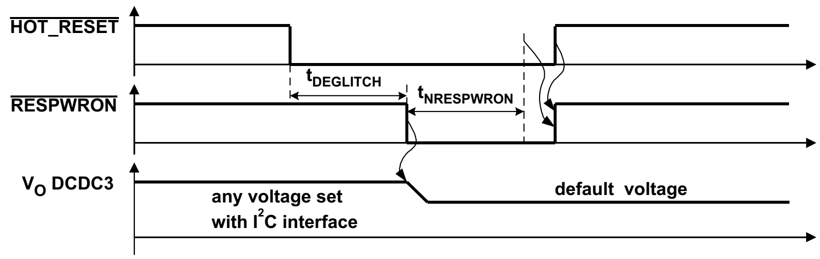


Figure 1. HOT_RESET Timing

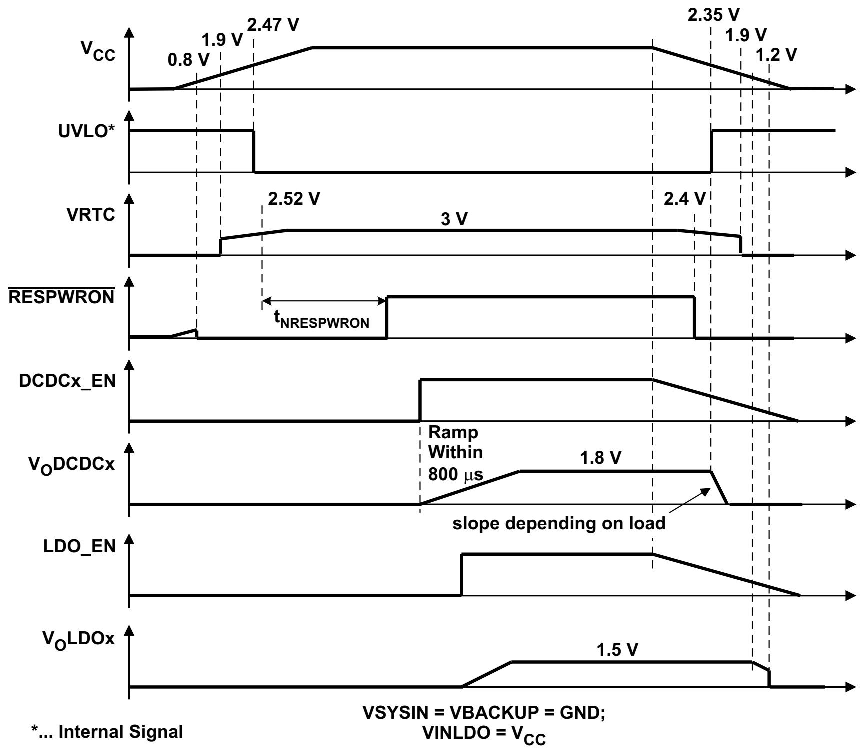


Figure 2. Power-Up and Power-Down Timing

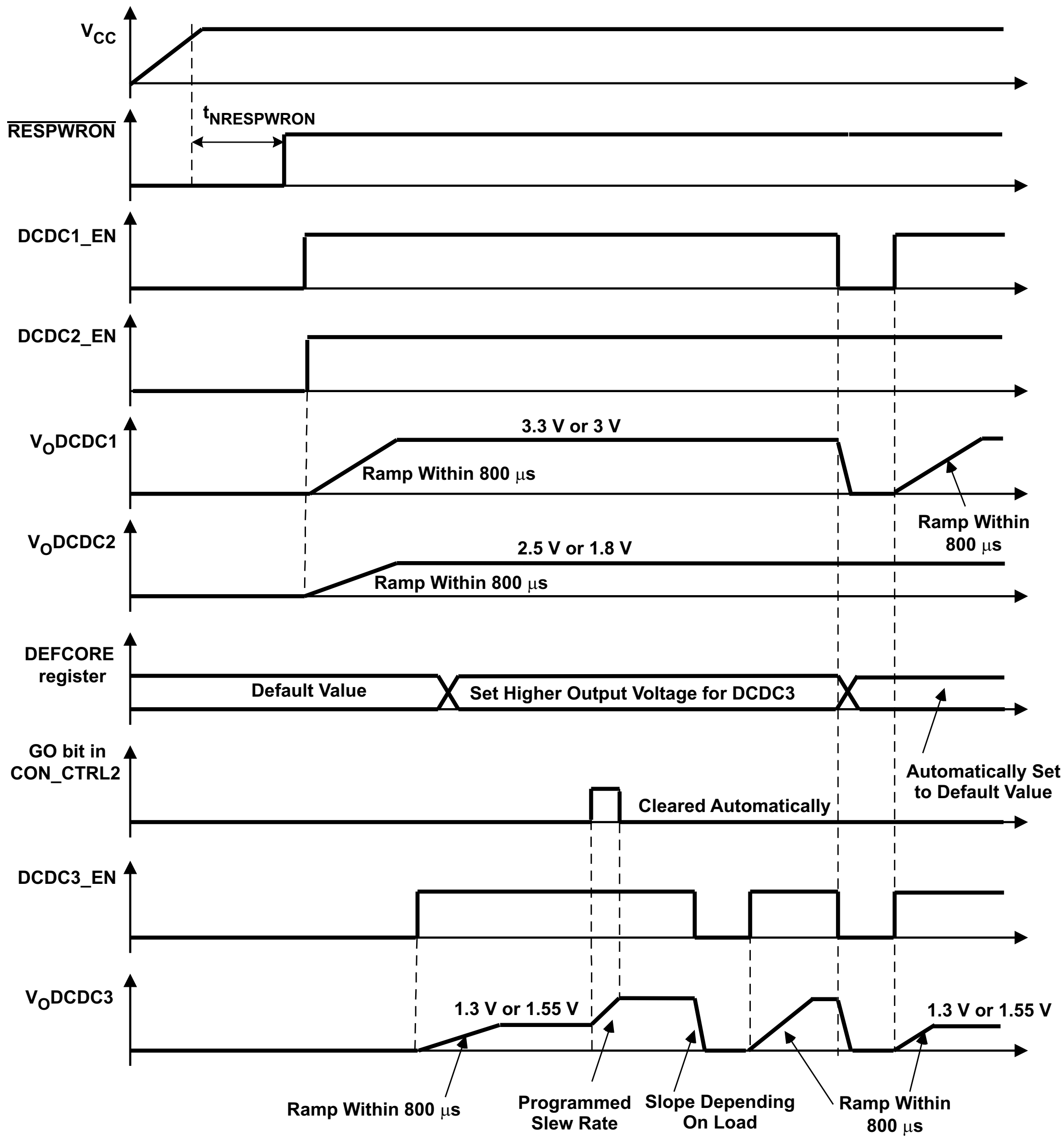


Figure 3. DVS Timing

6.7 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
Efficiency	vs Output current	Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, Figure 9, Figure 10
Line transient response		Figure 11, Figure 12, Figure 13
Load transient response		Figure 14, Figure 15, Figure 16
Output voltage ripple		Figure 17, Figure 18, Figure 19
Startup		Figure 20, Figure 21
Line transient response		Figure 22, Figure 23, Figure 24
Load transient response		Figure 25, Figure 26, Figure 27

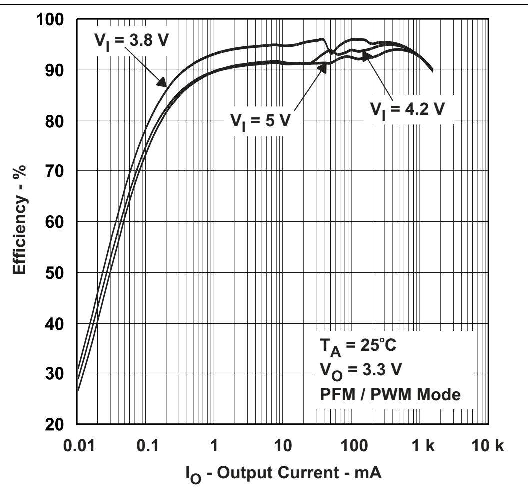


Figure 4. DCDC1: Efficiency vs Output Current

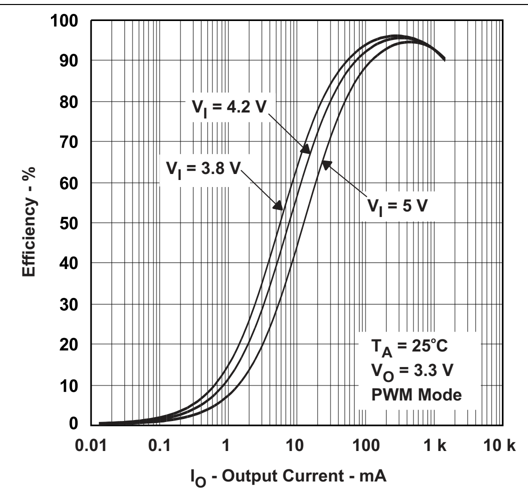


Figure 5. DCDC1: Efficiency vs Output Current

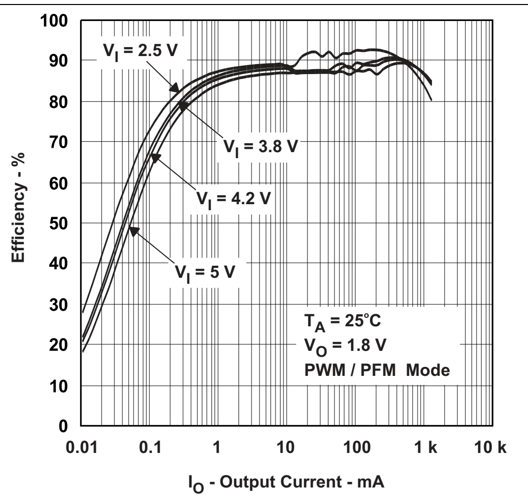


Figure 6. DCDC2: Efficiency vs Output Current

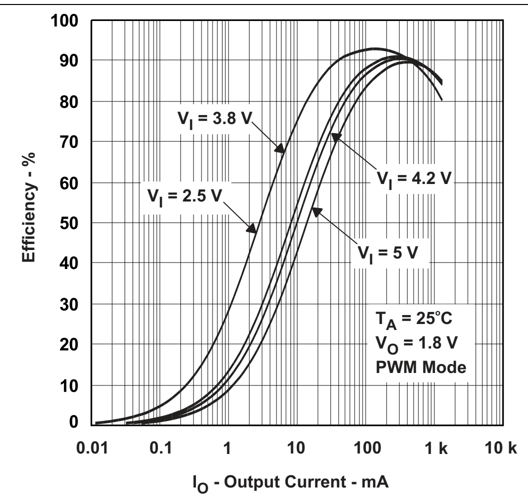


Figure 7. DCDC2: Efficiency vs Output Current

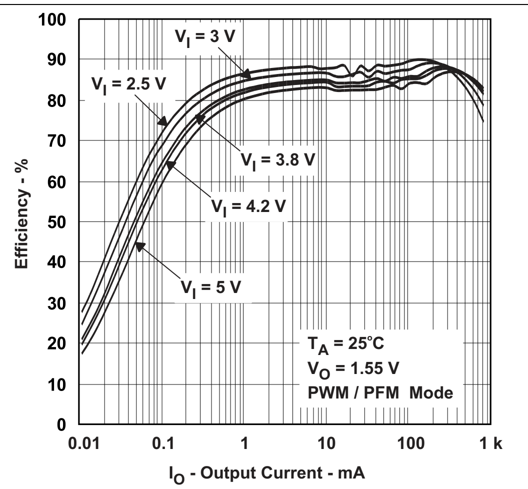


Figure 8. DCDC3: Efficiency vs Output Current

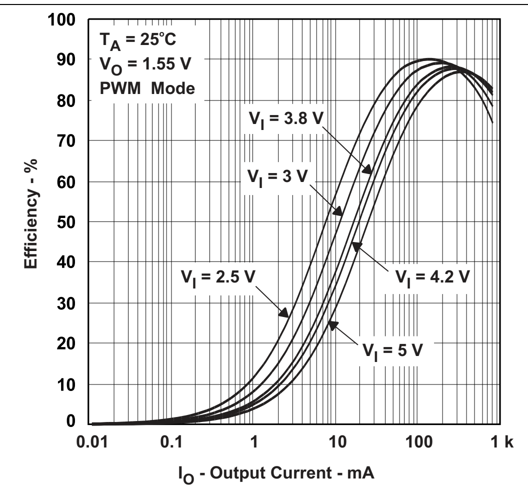


Figure 9. DCDC3: Efficiency vs Output Current

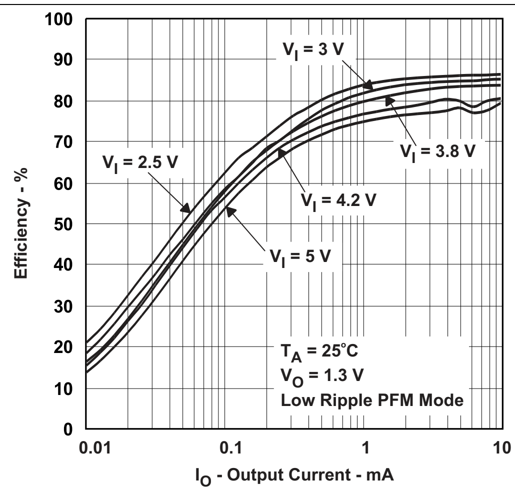


Figure 10. DCDC3: Efficiency vs Output Current

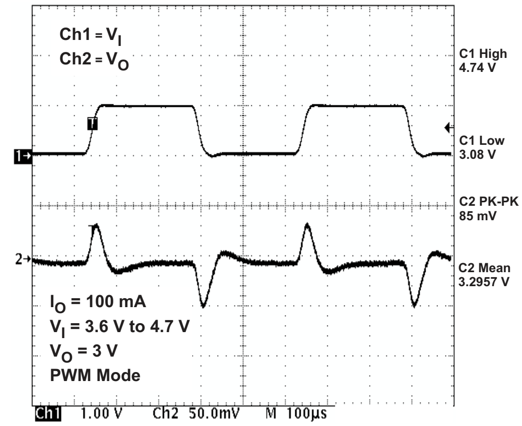


Figure 11. VDCDC1 Line Transient Response

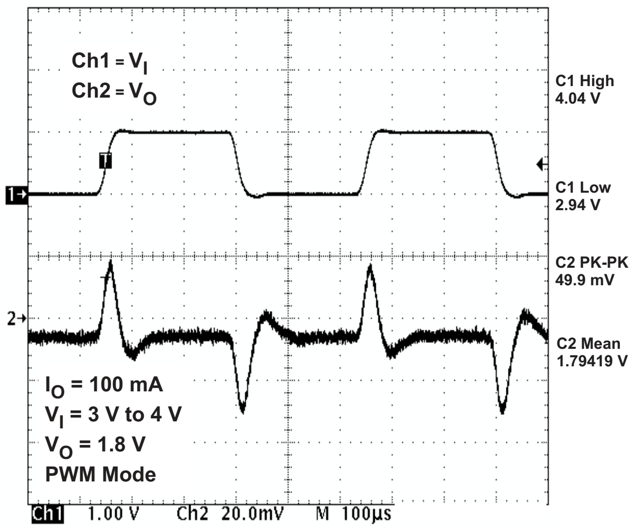


Figure 12. VDCDC2 Line Transient Response

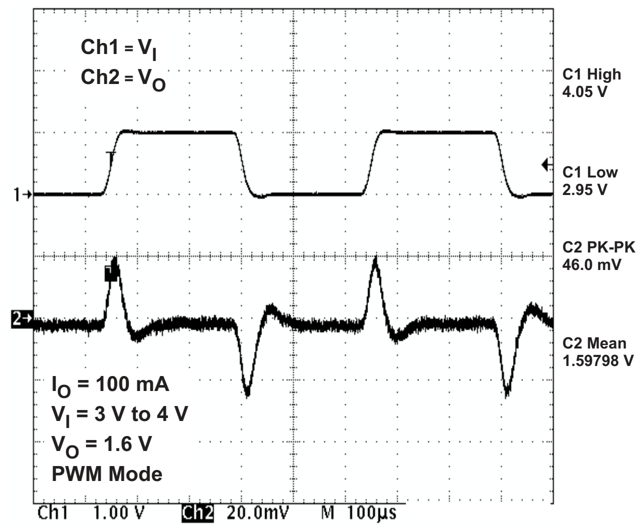


Figure 13. VDCDC3 Line Transient Response

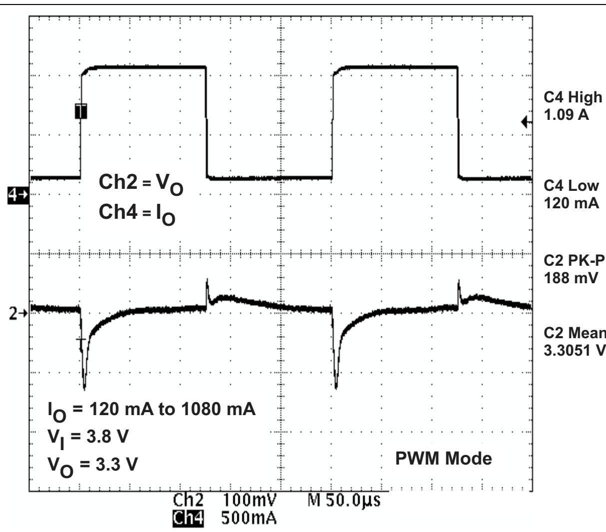


Figure 14. VDCDC1 Load Transient Response

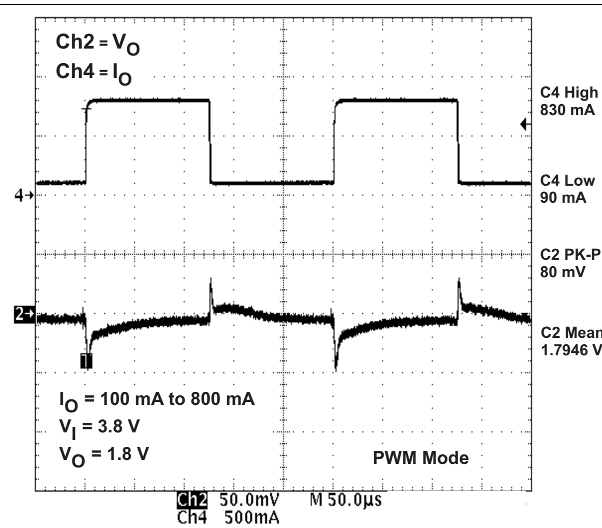


Figure 15. VDCDC2 Load Transient Response

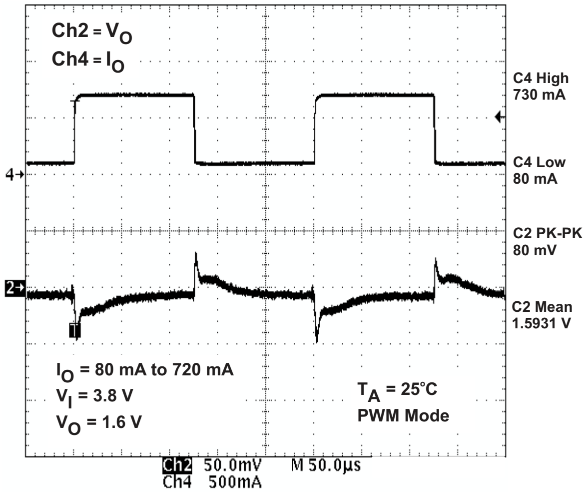


Figure 16. VDCDC3 Load Transient Response

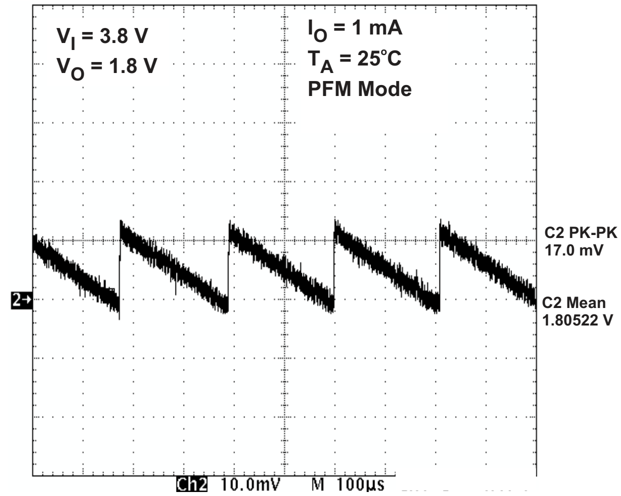


Figure 17. VDCDC2 Output Voltage Ripple

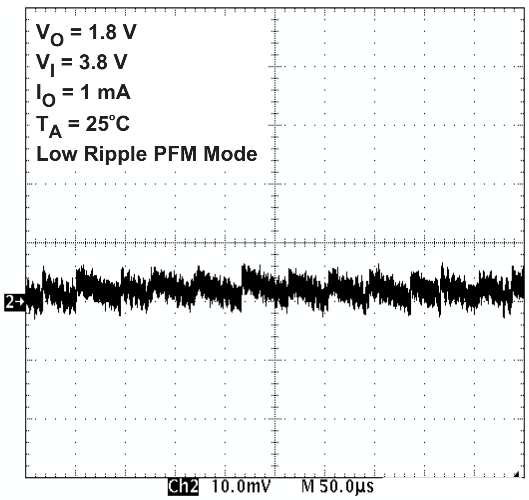


Figure 18. VDCDC2 Output Voltage Ripple

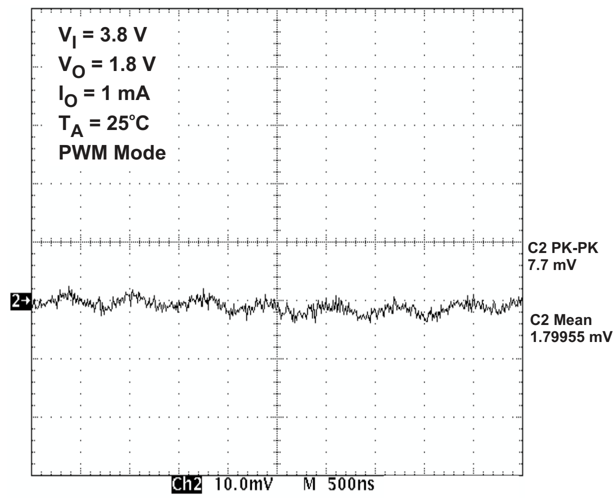


Figure 19. VDCDC2 Output Voltage Ripple

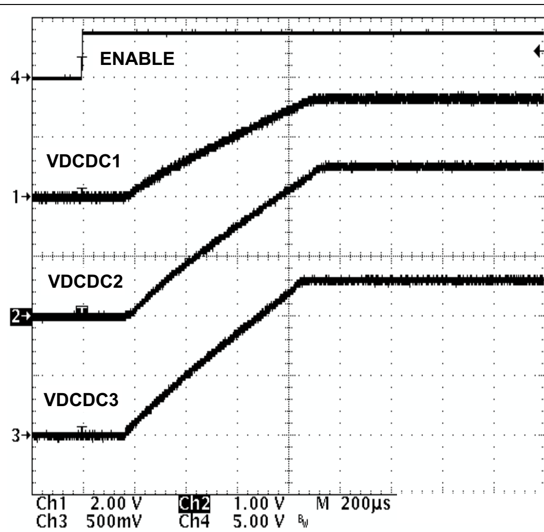


Figure 20. Startup VDCDC1, VDCDC2, and VDCDC3

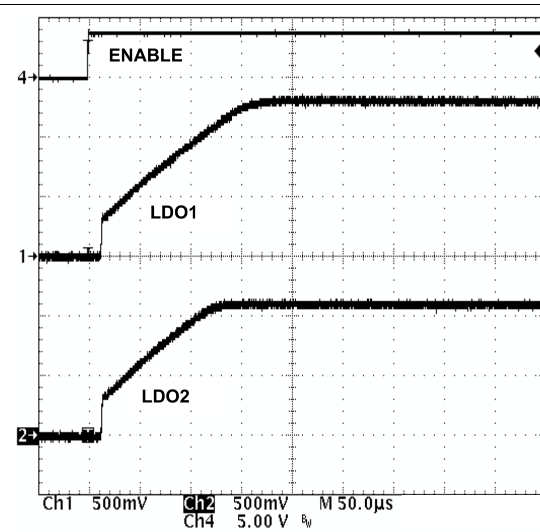


Figure 21. Startup LDO1 and LDO2

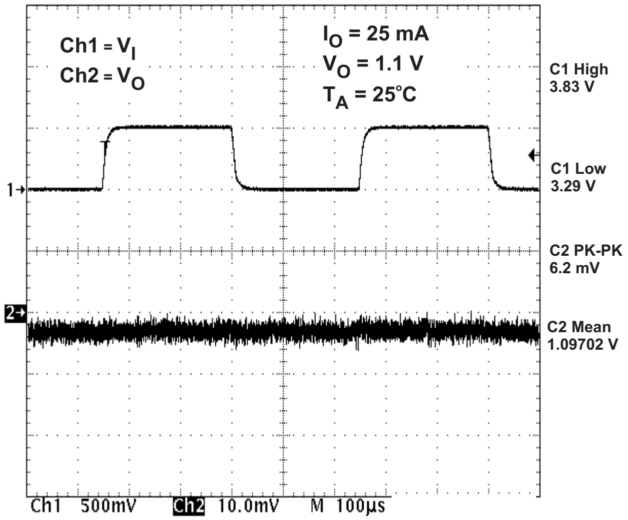


Figure 22. LDO1 Line Transient Response

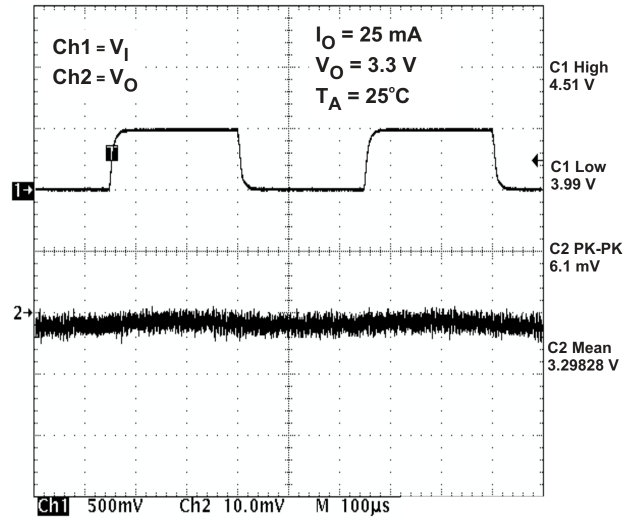


Figure 23. LDO2 Line Transient Response

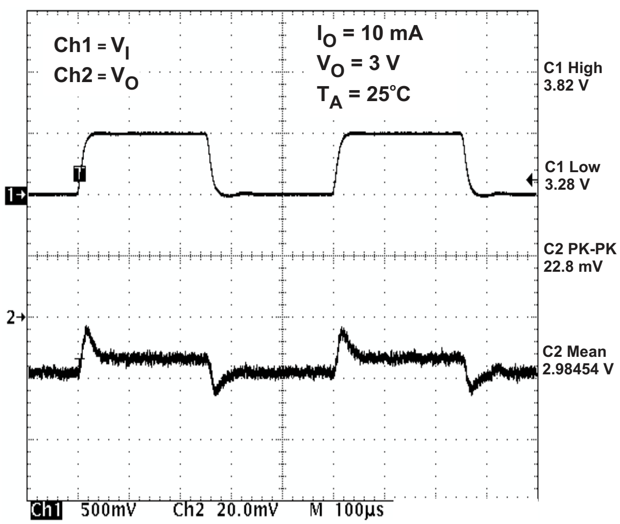


Figure 24. VRTC Line Transient Response

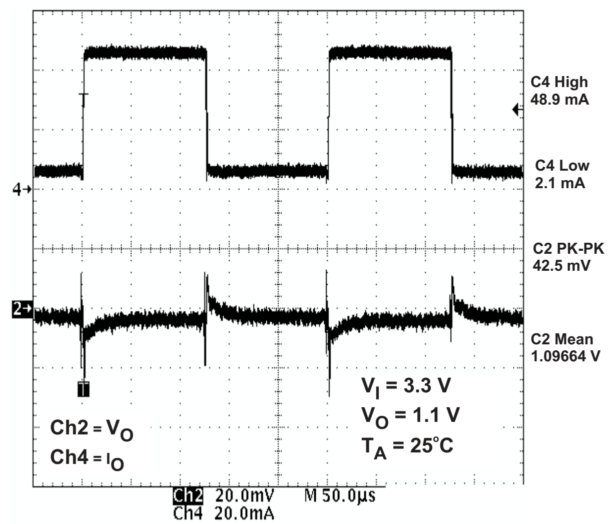


Figure 25. LDO1 Load Transient Response

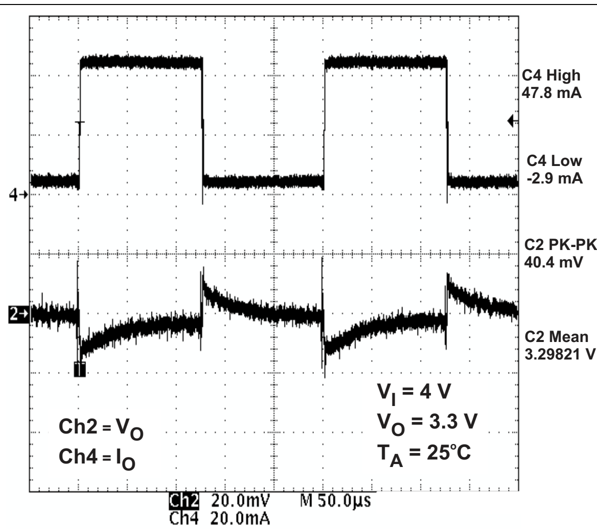


Figure 26. LDO2 Load Transient Response

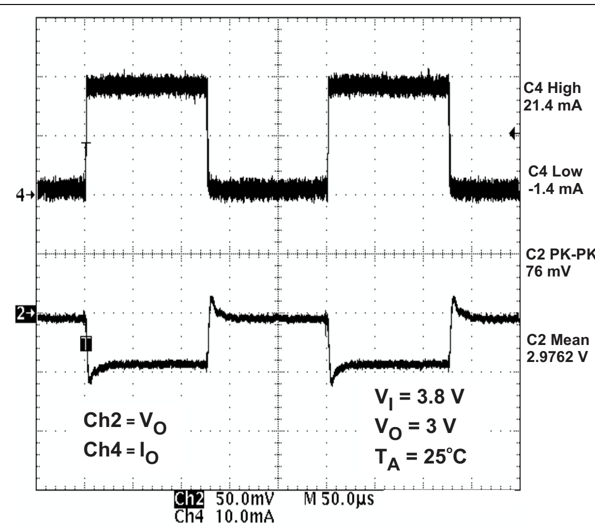


Figure 27. VRTC Load Transient Response

7 Detailed Description

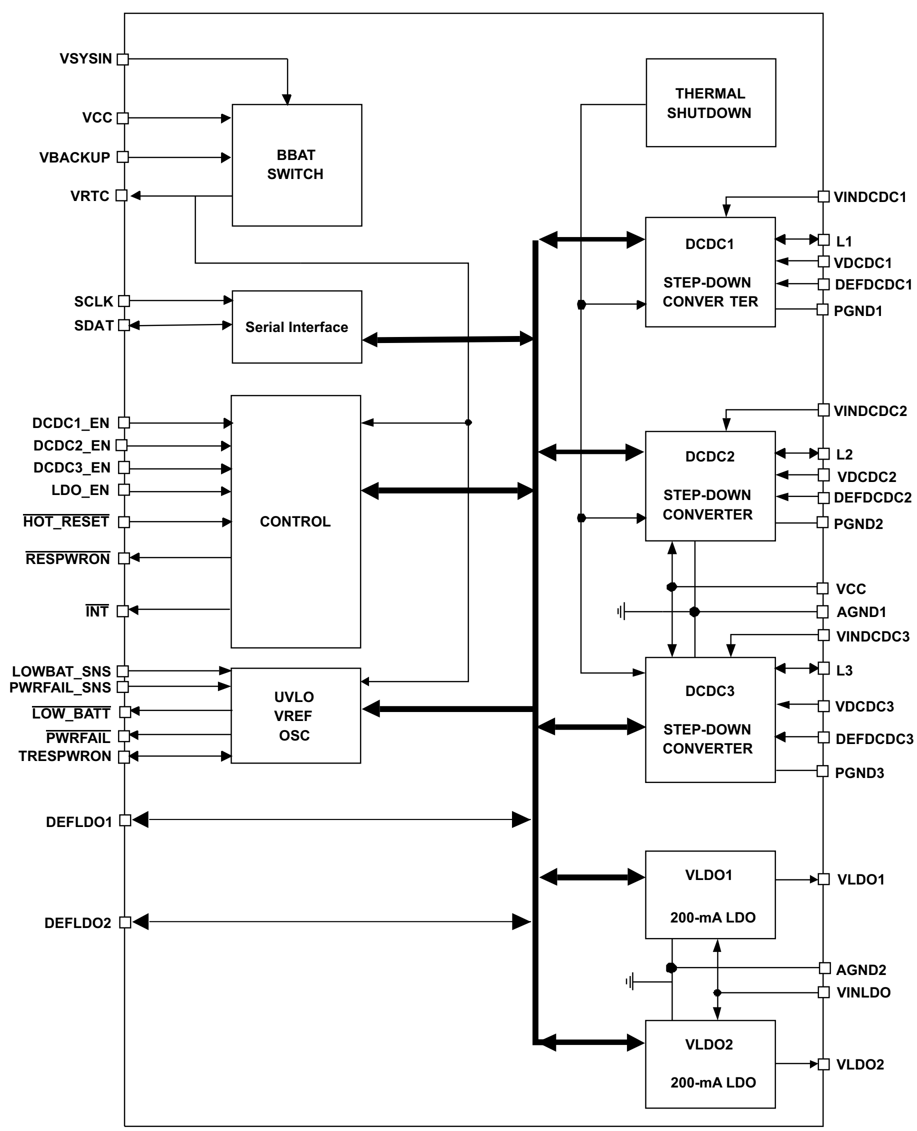
7.1 Overview

TPS65022 has 5 regulator channels, 3 DCDCs and 2 LDOs. DCDC3 has dynamic voltage scaling feature, DVS, that allows for power reduction to CORE supplies during idle operation or over voltage during heavy duty operation. With DVS and 2 more DCDCs plus 2 LDOs, the TPS65022 is ideal for CORE, Memory, IO, and peripheral power for the entire system of a wide range of suitable applications.

The device incorporates enables for the DCDCs and LDOs, I2C for device control, pushbutton and a reset interface that complete the system and allow for the TPS65022 to be adapted for different kinds of processors or FPGAs.

For noise sensitive circuits, the DCDCs can be synchronized out of phase from one another, reducing the peak noise at the switching frequency. Each converter can be forced to operate in PWM mode to ensure constant switching frequency across the entire load range. However, for low load efficiency performance the DCDCs automatically enter PSM mode, which reduces the switching frequency when the load current is low, saving power at idle operation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VRTC Output and Operation With or Without Backup Battery

The VRTC pin is an always-on output, intended to supply up to 30 mA to a permanently required rail. This is the VCC_BATT rail of the Intel® PXA270 Bulverde processor for example.

In applications using a backup battery, the backup voltage can be either directly connected to the TPS65022 VBACKUP pin if a Li-Ion cell is used, or through a boost converter (TPS61070) if a single NiMH battery is used. The voltage applied to the VBACKUP pin is fed through a PMOS switch to the VRTC pin. The TPS65022 asserts the RESPWRON signal if VRTC drops below 2.4 V. This, together with 375 mV at 30 mA drop out for the PMOS switch means that the voltage applied at VBACKUP must be greater than 2.775 V for normal system operation.

When the voltage at the VSYSIN pin exceeds 2.65 V, the path from VBACKUP to VRTC is cut, and VRTC is supplied by a similar PMOS switch from the voltage source connected to the VSYSIN input. Typically this is the VDCDC1 converter but can be any voltage source within the appropriate range.

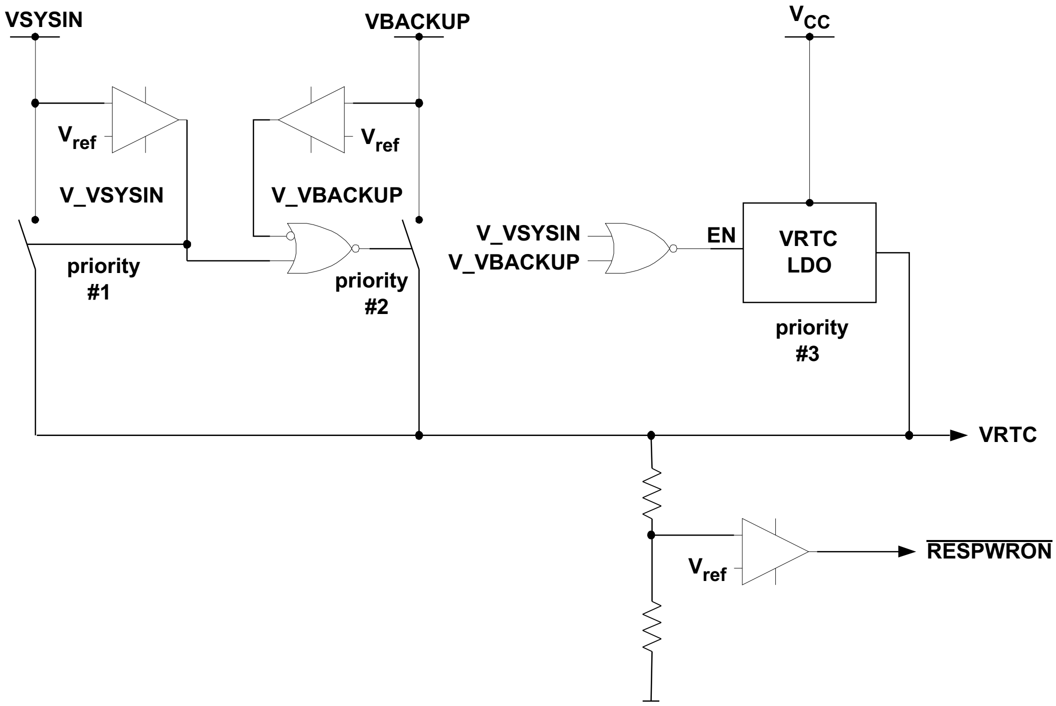
In systems where no backup battery is used, the VBACKUP pin is connected to GND. In this case, a low power LDO is enabled, supplied from VCC and capable of delivering 30 mA to the 3-V output. This LDO is disabled if the voltage at the VSYSIN input exceeds 2.65 V. VRTC is then supplied from the external source connected to this pin as previously described.

Inside TPS65022 there is a switch (Vmax switch) that selects the higher voltage between VCC and VBACKUP. This is used as the supply voltage for some basic functions. The functions powered from the output of the Vmax switch are:

- INT output
- RESPWRON output
- HOT_RESET input
- LOW_BATT output
- PWRFAIL output
- Enable pins for DC-DC converters, LDO1 and LDO2
- Undervoltage lockout comparator (UVLO)
- Reference system with low frequency timing oscillators
- LOW_BATT and PWRFAIL comparators

The main 1.5-MHz oscillator, and the I^2C interface are only powered from V_{CC}.

Feature Description (continued)



V_VSYSIN, V_VBACKUP thresholds: falling = 2.55 V, rising = 2.65 V ±3%
$\overline{\text{RESPWRON}}$ thresholds: falling = 2.4 V, rising = 2.52 V ±3%

Figure 28. RTC and nRESPWRON

7.3.2 Step-Down Converters, VDCDC1, VDCDC2, and VDCDC3

The TPS65022 incorporates three synchronous step-down converters operating typically at 1.5-MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converters automatically enter the power save mode (PSM), and operate with pulse frequency modulation (PFM). The VDCDC1 converter is capable of delivering 1.2-A output current, the VDCDC2 converter is capable of delivering 1 A and the VDCDC3 converter is capable of delivering up to 900 mA.

The converter output voltages can be programmed by the DEFDCDC1, DEFDCDC2 and DEFDCDC3 pins. The pins can either be connected to GND, VCC, or to a resistor divider between the output voltage and GND. The VDCDC1 converter defaults to 3 V or 3.3 V depending on the DEFDCDC1 configuration pin. If DEFDCDC1 is tied to ground, the default is 3 V. If it is tied to VCC, the default is 3.3 V. When the DEFDCDC1 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC1 V. See the application information section for more details.

The VDCDC2 converter defaults to 1.8 V or 2.5 V depending on the DEFDCDC2 configuration pin. If DEFDCDC2 is tied to ground, the default is 1.8 V. If it is tied to VCC, the default is 2.5 V. When the DEFDCDC2 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC2 V.

The VDCDC3 converter defaults to 1.3 V or 1.55 V depending on the DEFDCDC3 configuration pin. If DEFDCDC3 is tied to ground the default is 1.3 V. If it is tied to VCC, the default is 1.55 V. When the DEFDCDC3 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC3 V. The core voltage can be reprogrammed through the serial interface in the range of 0.8 V to 1.6 V with a programmable slew rate. The converter is forced into PWM operation whilst any programmed voltage change is underway, whether the voltage is being increased or decreased. The DEFCORE and DEFSLEW registers are used to program the output voltage and slew rate during voltage transitions.

The step-down converter outputs (when enabled) are monitored by power good (PG) comparators, the outputs of which are available through the serial interface. The outputs of the DC-DC converters can be optionally discharged through on-chip 300-Ω resistors when the DC-DC converters are disabled.

Feature Description (continued)

During PWM operation, the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on. The inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch if the current limit of the P-channel switch is exceeded. After the adaptive dead time used to prevent shoot through current, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal, again turning off the N-channel rectifier and turning on the P-channel switch.

The three DC-DC converters operate synchronized to each other with the VDCDC1 converter as the master. A 180° phase shift between the VDCDC1 switch turn on and the VDCDC2 and a further 90° shift to the VDCDC3 switch turn on decreases the input RMS current and smaller input capacitors can be used. This is optimized for a typical application where the VDCDC1 converter regulates a Li-Ion battery voltage of 3.7 V to 3.3 V, the VDCDC2 converter from 3.7 V to 2.5 V, and the VDCDC3 converter from 3.7 V to 1.5 V. The phase of the three converters can be changed using the CON_CTRL register.

7.3.3 Power Save Mode Operation

As the load current decreases, the converters enter the power save mode operation. During PSM, the converters operate in a burst mode (PFM mode) with a frequency between 750 kHz and 1.5 MHz, nominal for one burst cycle. However, the frequency between different burst cycles depends on the actual load current and is typically far less than the switching frequency with a minimum quiescent current to maintain high efficiency.

In order to optimize the converter efficiency at light load, the average current is monitored and if in PWM mode the inductor current remains below a certain threshold, then PSM is entered. The typical threshold to enter PSM is calculated as follows:

$$I_{PFMDCDC1\ enter} = \frac{VINDCDC1}{24\ \Omega}$$

$$I_{PFMDCDC2\ enter} = \frac{VINDCDC2}{26\ \Omega}$$

$$I_{PFMDCDC3\ enter} = \frac{VINDCDC3}{39\ \Omega} \quad (1)$$

During the PSM the output voltage is monitored with a comparator, and by maximum skip burst width. As the output voltage falls below the threshold, set to the nominal V_O, the P-channel switch turns on and the converter effectively delivers a constant current defined as follows.

$$I_{PFMDCDC1\ leave} = \frac{VINDCDC1}{18\ \Omega}$$

$$I_{PFMDCDC2\ leave} = \frac{VINDCDC2}{20\ \Omega}$$

$$I_{PFMDCDC3\ leave} = \frac{VINDCDC3}{29\ \Omega} \quad (2)$$

If the load is below the delivered current then the output voltage rises until the same threshold is crossed in the other direction. All switching activity ceases, reducing the quiescent current to a minimum until the output voltage has again dropped below the threshold. The power save mode is exited, and the converter returns to PWM mode if either of the following conditions are met:

1. the output voltage drops 2% below the nominal V_O due to increasing load current
2. the PFM burst time exceeds 16 × 1/fs (10.67 μs typical).

Feature Description (continued)

These control methods reduce the quiescent current to typically 14 µA per converter, and the switching activity to a minimum, thus achieving the highest converter efficiency. Setting the comparator thresholds at the nominal output voltage at light load current results in a low output voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor. Increasing capacitor values makes the output ripple tend to zero. The PSM is disabled through the I^2C interface to force the individual converters to stay in fixed frequency PWM mode.

7.3.4 Low Ripple Mode

Setting Bit 3 in register CON-CTRL to 1 enables the low ripple mode for all of the DC-DC converters if operated in PFM mode. For an output current less than approximately 10 mA, the output voltage ripple in PFM mode is reduced, depending on the actual load current. The lower the actual output current on the converter, the lower the output ripple voltage. For an output current above 10 mA, there is only a minor difference in output voltage ripple between PFM mode and low ripple PFM mode. As this feature also increases switching frequency, it is used to keep the switching frequency above the audible range in PFM mode down to a low output current.

7.3.5 Soft-Start

Each of the three converters has an internal soft-start circuit that limits the inrush current during start-up. The soft start is realized by using a very low current to initially charge the internal compensation capacitor. The soft start time is typically 750 µs if the output voltage ramps from 5% to 95% of the final target value. If the output is already pre-charged to some voltage when the converter is enabled, then this time is reduced proportionally. There is a short delay of typically 170 µs between the converter being enabled and switching activity actually starting. This is to allow the converter to bias itself properly, to recognize if the output is pre-charged, and if so to prevent discharging of the output while the internal soft start ramp catches up with the output voltage.

7.3.6 100% Duty Cycle Low Dropout Operation

The TPS65022 converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage required to maintain DC regulation depends on the load current and output voltage. It is calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT(max)} \times (r_{DS(on)}max + R_L)$$

where

- $I_{OUT(max)}$ = maximum load current (Note: ripple current in the inductor is zero under these conditions)
- $r_{DS(on)}max$ = maximum P-channel switch $r_{DS(on)}$
- R_L = DC resistance of the inductor
- $V_{OUT(min)}$ = nominal output voltage minus 2% tolerance limit (3)

7.3.7 Active Discharge When Disabled

When the VDCDC1, VDCDC2, and VDCDC3 converters are disabled, due to an UVLO, DCDC_EN or OVERTEMP condition, it is possible to actively pull down the outputs. This feature is disabled per default and is individually enabled through the CON_CTRL2 register in the serial interface. When this feature is enabled, the VDCDC1, VDCDC2, and VDCDC3 outputs are discharged by a 300 Ω (typical) load which is active as long as the converters are disabled.

7.3.8 Power Good Monitoring

All three step-down converters and both the LDO1 and LDO2 linear regulators have power good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below its target value with 5% hysteresis. The outputs of these comparators are available in the PGOODZ register through the serial interface. An interrupt is generated when any voltage rail drops below the 10% threshold. The comparators are disabled when the converters are disabled and the relevant PGOODZ register bits indicate that power is good.

Feature Description (continued)

7.3.9 Low Dropout Voltage Regulators

The low dropout voltage regulators are designed to operate well with low value ceramic input and output capacitors, with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 300 mV at rated output current. Each LDO supports a current limit feature. Both LDOs are enabled by the LDO_EN pin, both LDOs can be disabled or programmed through the serial interface using the REG_CTRL and LDO_CTRL registers. The LDOs also have reverse conduction prevention. This allows the possibility to connect external regulators in parallel in systems with a backup battery. The TPS65022 step-down and LDO voltage regulators automatically power down when the V_{CC} voltage drops below the UVLO threshold or when the junction temperature rises above 160°C.

7.3.10 Undervoltage Lockout

The undervoltage lockout circuit for the five regulators on the TPS65022 prevents the device from malfunctioning at low-input voltages and from excessive discharge of the battery. It disables the converters and LDOs. The UVLO circuit monitors the VCC pin, the threshold is set internally to 2.35 V with 5% (120 mV) hysteresis. Note that when any of the DC-DC converters are running, there is an input current at the VCC pin, which is up to 3 mA when all three converters are running in PWM mode. This current must be taken into consideration if an external RC filter is used at the VCC pin to remove switching noise from the TPS65022 internal analog circuitry supply.

7.3.11 Power-Up Sequencing

The TPS65022 power-up sequencing is designed to be entirely flexible and customer driven. This is achieved by providing separate enable pins for each switch-mode converter, and a common enable signal for the LDOs. The relevant control pins are described in Table 2.

Table 2. Control Pins and Status Outputs for DC-DC Converters

PIN NAME	INPUT OUTPUT	FUNCTION
DEFDCDC3	I	Defines the default voltage of the VDCDC3 switching converter. DEFDCDC3 = 0 defaults VDCDC3 to 1.3 V, DEFDCDC3 = VCC defaults VDCDC3 to 1.55 V.
DEFDCDC2	I	Defines the default voltage of the VDCDC2 switching converter. DEFDCDC2 = 0 defaults VDCDC2 to 1.8 V, DEFDCDC2 = VCC defaults VDCDC2 to 2.5 V.
DEFDCDC1	I	Defines the default voltage of the VDCDC1 switching converter. DEFDCDC1 = 0 defaults VDCDC1 to 3 V, DEFDCDC1 = VCC defaults VDCDC1 to 3.3 V.
DCDC3_EN	I	Set DCDC3_EN = 0 to disable and DCDC3_EN = 1 to enable the VDCDC3 converter
DCDC2_EN	I	Set DCDC2_EN = 0 to disable and DCDC2_EN = 1 to enable the VDCDC2 converter
DCDC1_EN	I	Set DCDC1_EN = 0 to disable and DCDC1_EN = 1 to enable the VDCDC1 converter
HOT_RESET	I	The HOT_RESET pin generates a reset (RESPWRON) for the processor.HOT_RESET does not alter any TPS65022 settings except the output voltage of VDCDC3. Activating HOT_RESET sets the voltage of VDCDC3 to its default value defined with the DEFDCDC3 pin. HOT_RESET is internally de-bounced by the TPS65022.
RESPWRON	O	RESPWRON is held low when power is initially applied to the TPS65022. The VRTC voltage is monitored: RESWPRON is low when VRTC < 2.4 V and remains low for a time defined by the external capacitor at the TRESPWRON pin. RESPWRON can also be forced low by activation of the HOT_RESET pin.
TRESPWRON	I	Connect a capacitor here to define the RESET time at the RESPWRON pin. 1 nF typically gives 100 ms.

7.3.12 System Reset + Control Signals

The RESPWRON signal can be used as a global reset for the application. It is an open-drain output. The RESPWRON signal is generated according to the power good comparator of VRTC, and remains low for $t_{nrespwron}$ seconds after VRTC has risen above 2.52 V (falling threshold is 2.4 V, 5% hysteresis). $t_{nrespwron}$ is set by an external capacitor at the TRESPWRON pin. 1 nF gives typically 100 ms. RESPWRON is also triggered by the HOT_RESET input. This input is internally debounced, with a filter time of typically 30 ms.

The PWRFAIL and LOW_BAT signals are generated by two voltage detectors using the PWRFAIL_SNS and LOWBAT_SNS input signals. Each input signal is compared to a 1 V threshold (falling edge) with 5% (50 mV) hysteresis.

The DCDC3 converter is reset to its default output voltage defined by the DEFDCDC3 input, when $\overline{\text{HOT\_RESET}}$ is asserted. Other I^{2}C registers are not affected. Generally, the DCDC3 converter is set to its default voltage with one of these conditions: $\overline{\text{HOT\_RESET}}$ active, VRTC lower than its threshold voltage, undervoltage lockout (UVLO) condition, $\overline{\text{RESPWRON}}$ active, both DCDC3-converter AND DCDC1-converter disabled. In addition, the voltage of VDCDC3 changes to 1xxx0, if the VDCDC1 converter is disabled. Where xxx is the state before VDCDC1 was disabled.

7.3.12.1 DEFLDO1 and DEFLDO2

These two pins are used to set the default output voltage of the two 200 mA LDOs. The digital value applied to the pins is latched during power up and determines the initial output voltage according to Table 3. The voltage of both LDOs can be changed during operation with the I^{2}C interface as described in the interface description.

Table 3. LDO1 and LDO2 Default Voltage Options

DEFLDO2	DEFLDO1	VLDO1	VLDO2
0	0	1.1 V	1.3 V
0	1	1.5 V	1.3 V
1	0	2.6 V	2.8 V
1	1	3.15 V	3.3 V

7.3.12.2 Interrupt Management and the $\overline{\text{INT}}$ Pin

The $\overline{\text{INT}}$ pin combines the outputs of the PGOOD comparators from each DC-DC converter and LDOs. The $\overline{\text{INT}}$ pin is used as a POWER_OK pin indicating when all enabled supplies are in regulation. If the PGOODZ register is read through the serial interface, any active bits are then blocked from the $\overline{\text{INT}}$ output pin.

Interrupts can be masked using the MASK register; default operation is not to mask any DCDC or LDO interrupts since this provides the POWER_OK function.

7.4 Device Functional Modes

The TPS650231 device is in the ON or the OFF mode. The OFF mode is entered when the voltage on VCC is below the UVLO threshold, 2.35 V (typically). Once the voltage at V CC has increased above UVLO, the device enters ON mode. In the ON mode, the DCDCs and LDOs are available for use.

7.5 Programming

7.5.1 Serial Interface

The serial interface is compatible with the standard and fast mode I^{2}C specifications, allowing transfers up to 400 kHz. The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements and charger status to be monitored. Register contents remain intact as long as VCC remains above 2 V. The TPS65022 has a 7-bit address: 1001000, other addresses are available upon contact with the factory. Attempting to read data from the register addresses not listed in this section results in FFh being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS65022 device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS65022 device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge–related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS65022 device must leave the data line high to enable the master to generate the stop condition.

Programming (continued)

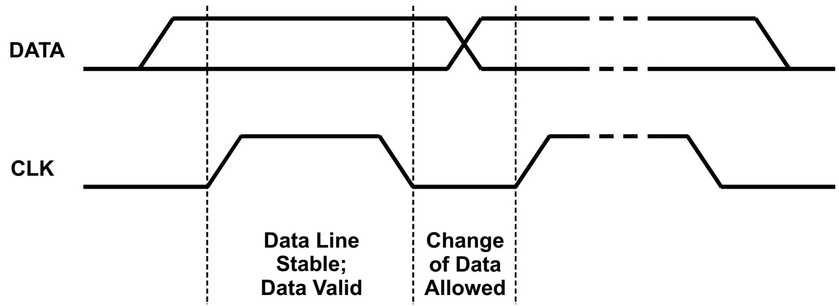


Figure 29. Bit Transfer on the Serial Interface

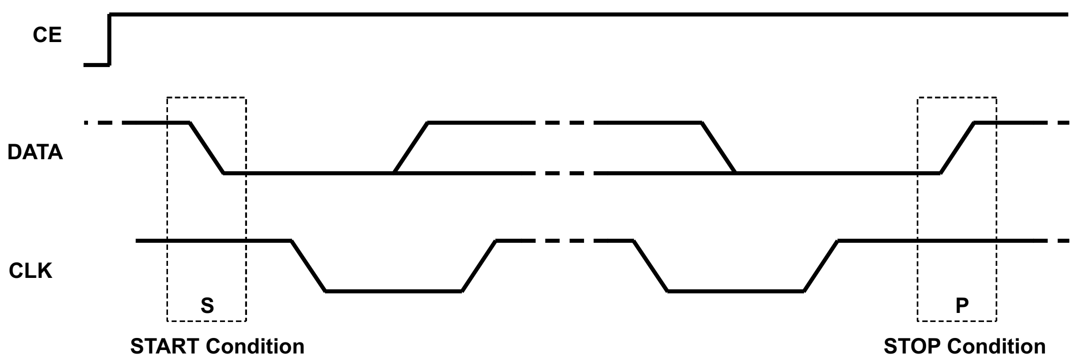


Figure 30. START and STOP Conditions

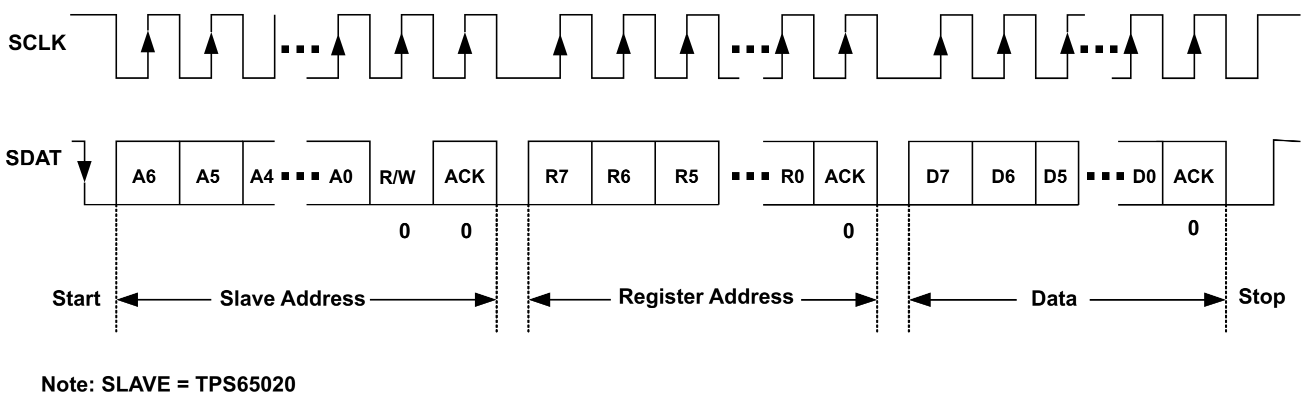


Figure 31. Serial Interface WRITE to TPS65022 Device

Programming (continued)

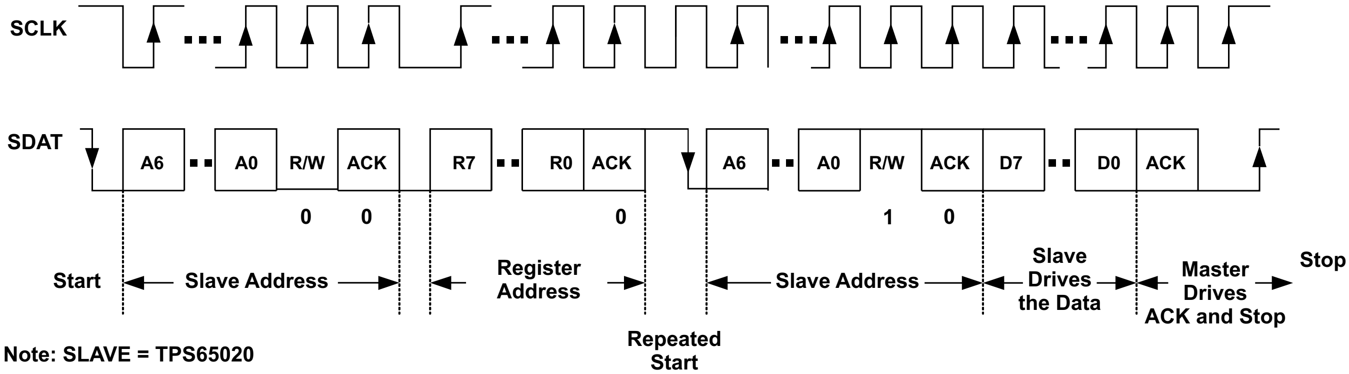


Figure 32. Serial Interface READ from TPS65022: Protocol A

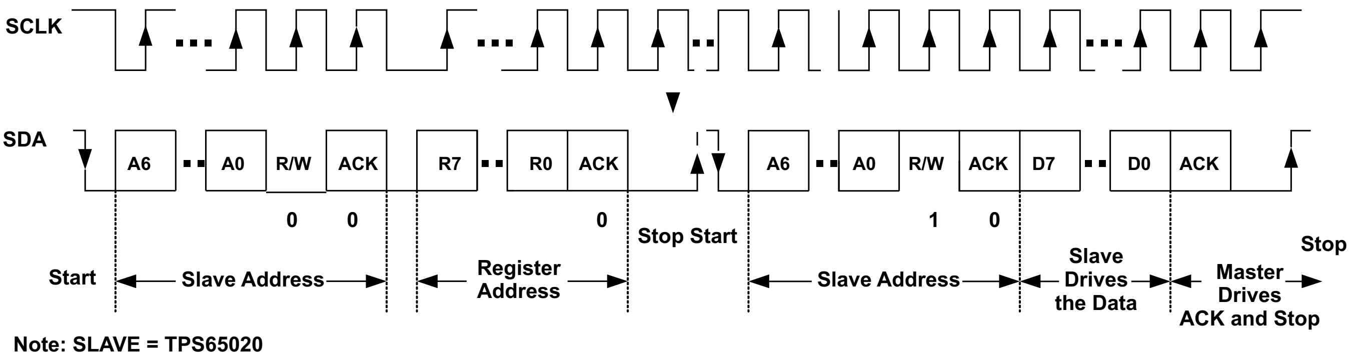


Figure 33. Serial Interface READ from TPS65022: Protocol B

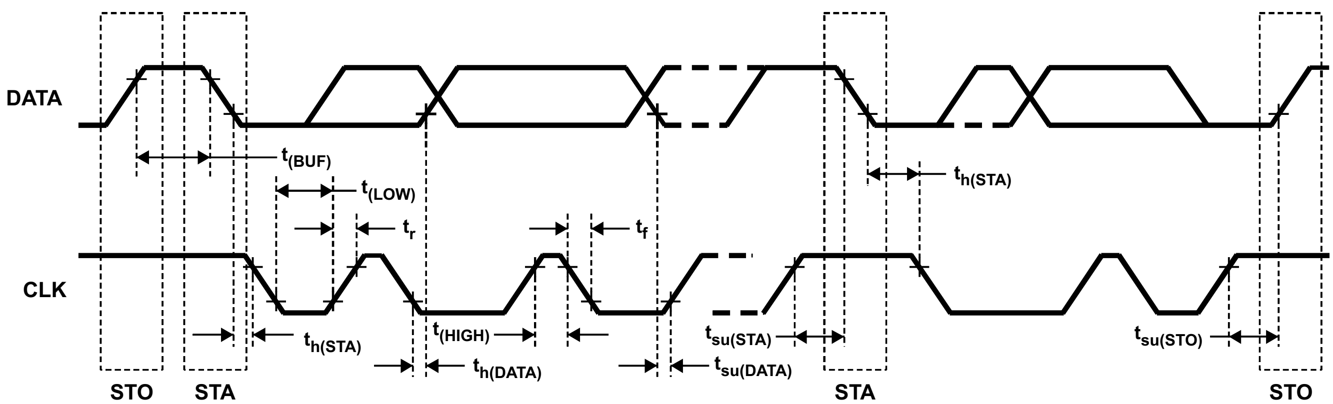


Figure 34. Serial Interface Timing Diagram

7.6 Register Maps

7.6.1 VERSION Register Address: 00h (read only)

Table 4. VERSION Register

VERSION	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	0	0	1	0	0	0	1	0
Read/Write	R	R	R	R	R	R	R	R

7.6.2 PGOODZ Register Address: 01h (read only)

Table 5. PGOODZ Register

PGOODZ	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	PWRFAILZ	LOWBATTZ	PGOODZ VDCDC1	PGOODZ VDCDC2	PGOODZ VDCDC3	PGOODZ LDO2	PGOODZ LDO1	
Set by signal	PWRFAIL	LOWBATT	PGOODZ VDCDC1	PGOODZ VDCDC2	PGOODZ VDCDC3	PGOODZ LDO2	PGOODZ LDO1	
Default value loaded by:	PWRFAILZ	LOWBATTZ	PGOOD VDCDC1	PGOOD VDCDC2	PGOOD VDCDC3	PGOOD LDO2	PGOOD LDO1	
Read/Write	R	R	R	R	R	R	R	R

Bit 7 PWRFAILZ:

0 = indicates that the PWRFAIL_SNS input voltage is above the 1-V threshold

1 = indicates that the PWRFAIL_SNS input voltage is below the 1-V threshold

Bit 6 LOWBATTZ:

0 = indicates that the LOWBATT_SNS input voltage is above the 1-V threshold

1 = indicates that the LOWBATT_SNS input voltage is below the 1-V threshold

Bit 5 PGOODZ VDCDC1:

0 = indicates that the VDCDC1 converter output voltage is within its nominal range. This bit is zero if the VDCDC1 converter is disabled.

1 = indicates that the VDCDC1 converter output voltage is below its target regulation voltage

Bit 4 PGOODZ VDCDC2:

0 = indicates that the VDCDC2 converter output voltage is within its nominal range. This bit is zero if the VDCDC2 converter is disabled.

1 = indicates that the VDCDC2 converter output voltage is below its target regulation voltage

Bit 3 PGOODZ VDCDC3: .

0 = indicates that the VDCDC3 converter output voltage is within its nominal range. This bit is zero if the VDCDC3 converter is disabled and during a DVM controlled output voltage transition.

1 = indicates that the VDCDC3 converter output voltage is below its target regulation voltage

Bit 2 PGOODZ LDO2:

0 = indicates that the LDO2 output voltage is within its nominal range. This bit is zero if LDO2 is disabled.

1 = indicates that LDO2 output voltage is below its target regulation voltage

Bit 1 PGOODZ LDO1

0 = indicates that the LDO1 output voltage is within its nominal range. This bit is zero if LDO1 is disabled.

1 = indicates that the LDO1 output voltage is below its target regulation voltage

7.6.3 MASK Register Address: 02h (read/write) Default Value: C0h

Table 6. MASK Register

MASK	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	MASK PWRFAILZ	MASK LOWBATTZ	MASK VDCDC1	MASK VDCDC2	MASK VDCDC3	MASK LDO2	MASK LDO1	
Default	1	1	0	0	0	0	0	0
Default value loaded by:	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

The MASK register can be used to mask particular fault conditions from appearing at the $\overline{INT}$ pin. MASK<n> = 1 masks PGOODZ<n>.

7.6.4 REG_CTRL Register Address: 03h (read/write) Default Value: FFh

The REG_CTRL register is used to disable or enable the power supplies through the serial interface. The contents of the register are logically AND'ed with the enable pins to determine the state of the supplies. A UVLO condition resets the REG_CTRL to 0xFF, so the state of the supplies defaults to the state of the enable pin. The REG_CTRL bits are automatically reset to default when the corresponding enable pin is low.

Table 7. REG_CTRL Register

REG_CTRL	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function			VDCDC1 ENABLE	VDCDC2 ENABLE	VDCDC3 ENABLE	LDO2 ENABLE	LDO1 ENABLE	
Default	1	1	1	1	1	1	1	1
Set by signal			DCDC1_ENZ	DCDC2_ENZ	DCDC3_ENZ	LDO_ENZ	LDO_ENZ	
Default value loaded by:			UVLO	UVLO	UVLO	UVLO	UVLO	
Read/Write			R/W	R/W	R/W	R/W	R/W	

Bit 5 VDCDC1 ENABLE

DCDC1 Enable. This bit is logically AND'ed with the state of the DCDC1_EN pin to turn on the DCDC1 converter. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the pin DCDC1_EN is pulled to GND, allowing DCDC1 to turn on when DCDC1_EN returns high.

Bit 4 VDCDC2 ENABLE

DCDC2 Enable. This bit is logically AND'ed with the state of the DCDC2_EN pin to turn on the DCDC2 converter. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the pin DCDC2_EN is pulled to GND, allowing DCDC2 to turn on when DCDC2_EN returns high.

Bit 3 VDCDC3 ENABLE

DCDC3 Enable. This bit is logically AND'ed with the state of the DCDC3_EN pin to turn on the DCDC3 converter. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the pin DCDC3_EN is pulled to GND, allowing DCDC3 to turn on when DCDC3_EN returns high.

Bit 2 LDO2 ENABLE

LDO2 Enable. This bit is logically AND'ed with the state of the LDO2_EN pin to turn on LDO2. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the pin LDO_EN is pulled to GND, allowing LDO2 to turn on when LDO_EN returns high.

Bit 1 LDO1 ENABLE

LDO1 Enable. This bit is logically AND'ed with the state of the LDO1_EN pin to turn on LDO1. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the pin LDO_EN is pulled to GND, allowing LDO1 to turn on when LDO_EN returns high.

7.6.5 CON_CTRL Register Address: 04h (read/write) Default Value: B1h

Table 8. CON_CTRL Register

CON_CTRL	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	DCDC2 PHASE1	DCDC2 PHASE0	DCDC3 PHASE1	DCDC3 PHASE0	LOW RIPPLE	FPWM DCDC2	FPWM DCDC1	FPWM DCDC3
Default	1	0	1	1	0	0	0	1
Default value loaded by:	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The CON_CTRL register is used to force any or all of the converters into forced PWM operation, when low output voltage ripple is vital. It is also used to control the phase shift between the three converters in order to minimize the input rms current, hence reduce the required input blocking capacitance. The DCDC1 converter is taken as the reference and consequently has a fixed zero phase shift.

Table 9. DCDC2 and DCDC3 Phase Delay

CON_CTRL<7:6>	DCDC2 CONVERTER DELAYED BY		CON_CTRL<5:4>	DCDC3 CONVERTER DELAYED BY
00	zero		00	zero
01	1/4 cycle		01	1/4 cycle
10	**1/2 cycle**		10	1/2 cycle
11	3/4 cycle		**11**	**3/4 cycle**

Bit 3 LOW RIPPLE:

0 = PFM mode operation optimized for high efficiency for all converters

1 = PFM mode operation optimized for low output voltage ripple for all converters

Bit 2 FPWM DCDC2:

0 = DCDC2 converter operates in PWM / PFM mode

1 = DCDC2 converter is forced into fixed frequency PWM mode

Bit 1 FPWM DCDC1:

0 = DCDC1 converter operates in PWM / PFM mode

1 = DCDC1 converter is forced into fixed frequency PWM mode

Bit 0 FPWM DCDC3:

0 = DCDC3 converter operates in PWM / PFM mode

1 = DCDC3 converter is forced into fixed frequency PWM mode

7.6.6 CON_CTRL2 Register Address: 05h (read/write) Default Value: 40h

Table 10. CON_CTRL2 Register

CON_CTRL2	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	GO	Core adj allowed				DCDC2 discharge	DCDC1 discharge	DCDC3 discharge
Default	0	1	0	0	0	0	0	0
Default value loaded by:	UVLO + DONE	RESET(1)				UVLO	UVLO	UVLO
Read/Write	R/W	R/W				R/W	R/W	R/W

The CON_CTRL2 register can be used to take control the inductive converters.

RESET(1): CON_CTRL2[6] is reset to its default value by one of these events:
- undervoltage lockout (UVLO)
- DCDC1_EN and DCDC3_EN pulled low
- HOT_RESET pulled low
- RESPWRON active
- VRTC below threshold

Bit 7 GO:

0 = no change in the output voltage for the DCDC3 converter

1 = the output voltage of the DCDC3 converter is changed to the value defined in DEFCORE with the slew rate defined in DEFSLEW. This bit is automatically cleared when the DVM transition is complete. The transition is considered complete in this case when the desired output voltage code has been reached, not when the VDCDC3 output voltage is actually in regulation at the desired voltage.

Bit 6 CORE ADJ Allowed:

0 = the output voltage is set with the I^2C register

1 = DEFDCDC3 is either connected to GND or VCC or an external voltage divider. When connected to GND or VCC, VDCDC3 defaults to 1.3 V or 1.55 V respectively at start-up.

Bit 2– 0 0 = the output capacitor of the associated converter is not actively discharged when the converter is disabled

1 = the output capacitor of the associated converter is actively discharged when the converter is disabled. This decreases the fall time of the output voltage at light load.

7.6.7 DEFCORE Register Address: 06h (read/write) Default Value: 14h/1Eh

Table 11. DEFCORE Register

DEFCORE	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function				CORE4	CORE3	CORE2	CORE1	CORE0
Default	0	0	0	1	DEFDCDC3	1	DEFDCDC3	0
Default value loaded by:				RESET(2)	RESET(1)	RESET(1)	RESET(1)	RESET(2)
Read/Write				R/W	R/W	R/W	R/W	R/W

RESET(1): DEFCORE[3:1] are reset to the default value by one of these events:
- undervoltage lockout (UVLO)
- DCDC1_EN and DCDC3_EN pulled low
- HOT_RESET pulled low
- RESPWRON active
- VRTC below threshold

RESET(2): DEFCORE[4] and DEFCORE[0] are reset to the default value by one of these events:
- undervoltage lockout (UVLO)
- DCDC1_EN pulled low
- HOT_RESET pulled low
- RESPWRON active
- VRTC below threshold

Table 12. DCDC3 DVS Voltages

CORE4	CORE3	CORE2	CORE1	CORE0	VDCDC3		CORE4	CORE3	CORE2	CORE1	CORE0	VDCDC3
0	0	0	0	0	0.8 V		1	0	0	0	0	1.2 V
0	0	0	0	1	0.825 V		1	0	0	0	1	1.225 V
0	0	0	1	0	0.85 V		1	0	0	1	0	1.25 V
0	0	0	1	1	0.875 V		1	0	0	1	1	1.275 V
0	0	1	0	0	0.9 V		1	0	1	0	0	1.3 V
0	0	1	0	1	0.925 V		1	0	1	0	1	1.325 V
0	0	1	1	0	0.95 V		1	0	1	1	0	1.35 V
0	0	1	1	1	0.975 V		1	0	1	1	1	1.375 V
0	1	0	0	0	1 V		1	1	0	0	0	1.4 V
0	1	0	0	1	1.025 V		1	1	0	0	1	1.425 V
0	1	0	1	0	1.05 V		1	1	0	1	0	1.45 V
0	1	0	1	1	1.075 V		1	1	0	1	1	1.475 V
0	1	1	0	0	1.1 V		1	1	1	0	0	1.5 V
0	1	1	0	1	1.125 V		1	1	1	0	1	1.525 V
0	1	1	1	0	1.15 V		1	1	1	1	0	1.55 V
0	1	1	1	1	1.175 V		1	1	1	1	1	1.6 V

7.6.8 DEFSLEW Register Address: 07h (read/write) Default Value: 06h

Table 13. DEFSLEW Register

DEFSLEW	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function						SLEW2	SLEW1	SLEW0
Default						1	1	0
Default value loaded by:						UVLO	UVLO	UVLO
Read/Write						R/W	R/W	R/W

Table 14. DCDC3 DVS Slew Rate

SLEW2	SLEW1	SLEW0	VDCDC3 SLEW RATE
0	0	0	0.15 mV/μs
0	0	1	0.3 mV/μs
0	1	0	0.6 mV/μs
0	1	1	1.2 mV/μs
1	0	0	2.4 mV/μs
1	0	1	4.8 mV/μs
1	**1**	**0**	**9.6 mV/μs**
1	1	1	Immediate

7.6.9 LDO_CTRL Register Address: 08h (read/write) Default Value: set with DEFLDO1 and DEFLDO2

Table 15. LDO_CTRL Register

LDO_CTRL	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function		LDO2_2	LDO2_1	LDO2_0		LDO1_2	LDO1_1	LDO1_0
Default		DEFLDOx	DEFLDOx	DEFLDOx		DEFLDOx	DEFLDOx	DEFLDOx
Default value loaded by:		UVLO	UVLO	UVLO		UVLO	UVLO	UVLO
Read/Write		R/W	R/W	R/W		R/W	R/W	R/W

The LDO_CTRL registers can be used to set the output voltage of LDO1 and LDO2.

The default voltage is set with DEFLDO1 and DEFLDO2 pins as described in Table 3.

Table 16. LDO1 and LDO2 I^2C Voltage Options

LDO1_2	LDO1_1	LDO1_0	LDO1 OUTPUT VOLTAGE		LDO2_2	LDO2_1	LDO2_0	LDO2 OUTPUT VOLTAGE
0	0	0	1 V		0	0	0	1.05 V
0	0	1	1.1 V		0	0	1	1.2 V
0	1	0	1.35 V		0	1	0	1.3 V
0	1	1	1.5 V		0	1	1	1.8 V
1	0	0	2.2 V		1	0	0	2.5 V
1	0	1	2.6 V		1	0	1	2.8 V
1	1	0	2.85 V		1	1	0	3 V
1	1	1	3.15 V		1	1	1	3.3 V

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input Voltage Connection

The low power section of the control circuit for the step-down converters DCDC1, DCDC2 and DCDC3 is supplied by the V_{CC} pin while the circuitry with high power such as the power stage is powered from the VINDCDC1, VINDCDC2, and VINDCDC3 pins. For proper operation of the step-down converters, VINDCDC1, VINDCDC2, VNDCDC3, and Vcc need to be tied to the same voltage rail. Step-down converters that are planned to be not used, still need to be powered from their input pin on the same rails than the other step-down converters and V_{CC}.

LDO1 and LDO2 share a supply voltage pin which can be powered from the V_{CC} rails or from a voltage lower than V_{CC}, for example, the output of one of the step-down converters as long as it is operated within the input voltage range of the LDOs. If both LDOs are not used, the VINLDO pin can be tied to GND.

8.1.2 Unused Regulators

If a step-down converter is not used, the input supply voltage pin VINDCDCx must connect to the V_{CC} rail along with supply input of the other step-down converters. TI recommends closing the control loop such that an inductor and output capacitor is added in the same way when operated normally. If one of the LDOs is not used, its output capacitor should be added as well. If both LDOs are not used, the input supply pin and the output pins of the LDOs (VINLDO, VLDO1, VLDO2) should be tied to GND.

8.2 Typical Application

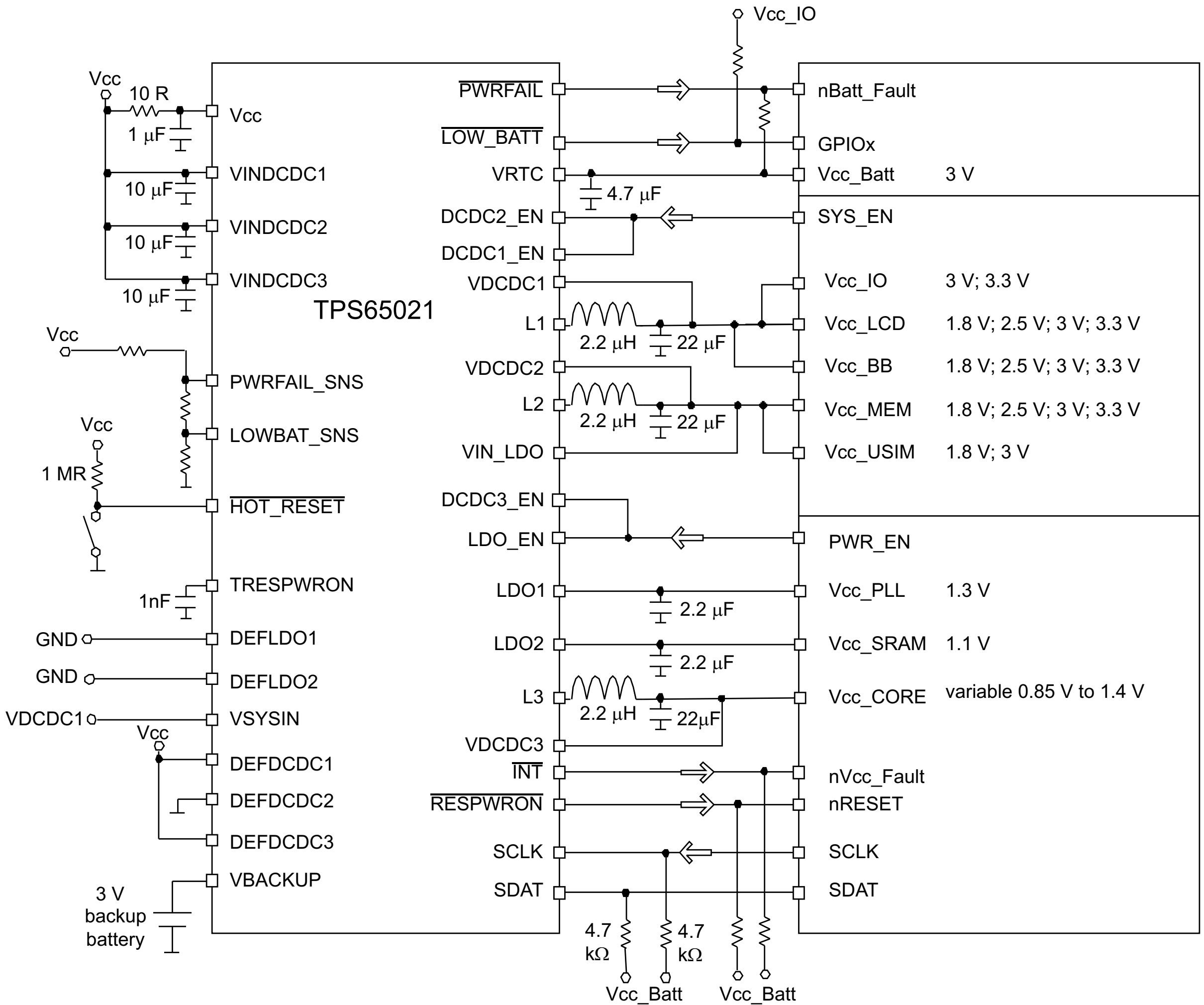


Figure 35. Typical Configuration for the Intel® PXA270 Bulverde Processor

8.2.1 Design Requirements

The TPS65022 device has only a few design requirements. Use the following parameters for the design example:

- 1-µF bypass capacitor on VCC, located as close as possible to the VCC pin to ground
- VCC, VINDCDC1, VINDCDC2, and VINDCDC3 must be connected to the same voltage supply with minimal voltage difference
- Input capacitors must be present on the VINDCDC1, VINDCDC2, VINDCDC3, and VIN_LDO supplies if used
- Output inductor and capacitors must be used on the outputs of the DCDC converters if used
- Output capacitors must be used on the outputs of the LDOs if used

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection for the DC-DC Converters

Each of the converters in the TPS65022 typically use a 3.3 µH output inductor. Larger or smaller inductor values are used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance should be selected for highest efficiency.

Typical Application (continued)

For a fast transient response, a 2.2-μH inductor in combination with a 22-μF output capacitor is recommended.

Equation 4 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 4. This is needed because during heavy load transient the inductor current rises above the value calculated under Equation 4.

$$\Delta I_L = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \right) \quad (4)$$

$$I_{L(max)} = I_{OUT(max)} + \left(\frac{\Delta I_L}{2} \right)$$

where

- f = Switching Frequency (1.5 MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- $I_{L(max)}$ = Maximum inductor current (5)

The highest inductor current occurs at maximum V_{IN}.

Open core inductors have a soft saturation characteristic, and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS65022 (2 A for the VDCDC1 and VDCDC2 converters, and 1.5 A for the VDCDC3 converter). The core material from inductor to inductor differs and has an impact on the efficiency especially at high switching frequencies.

See Table 17 and the typical applications for possible inductors.

Table 17. Tested Inductors

DEVICE	INDUCTOR VALUE	TYPE	COMPONENT SUPPLIER
DCDC3 converter	3.3 μH	CDRH2D14NP-3R3	Sumida
	3.3 μH	LPS3010-332	Coilcraft
	3.3 μH	VLF4012AT-3R3M1R3	TDK
	2.2 μH	VLF4012AT-2R2M1R5	TDK
DCDC2 converter	3.3 μH	CDRH2D18/HPNP-3R3	Sumida
	3.3 μH	VLF4012AT-3R3M1R3	TDK
	2.2 μH	VLCF4020-2R2	TDK
DCDC1 converter	3.3 μH	CDRH3D14/HPNP-3R2	Sumida
	3.3 μH	CDRH4D28C-3R2	Sumida
	3.3 μH	MSS5131-332	Coilcraft
	2.2 μH	VLCF4020-2R2	TDK

8.2.2.2 Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the inductive converters implemented in the TPS65022 allow the use of small ceramic capacitors with a typical value of 10 μF for each converter without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. See Table 18 for recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. The RMS ripple current is calculated as:

$$I_{RMSCout} = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{6}$$

At nominal load current, the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{out} = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \times \left(\frac{1}{8 \times C_{out} \times f} + ESR \right) \tag{7}$$

Where the highest output voltage ripple occurs at the highest input voltage V_{in}.

At light load currents, the converters operate in PSM and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

8.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Each DC-DC converter requires a 10-µF ceramic input capacitor on its input pin VINDCDCx. The input capacitor is increased without any limit for better input voltage filtering. The VCC pin is separated from the input for the DC-DC converters. A filter resistor of up to 10R and a 1-µF capacitor is used for decoupling the VCC pin from switching noise. Note that the filter resistor may affect the UVLO threshold since up to 3 mA can flow through this resistor into the VCC pin when all converters are running in PWM mode.

Table 18. Possible Capacitors

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
22 µF	1206	TDK C3216X5R0J226M	Ceramic
22 µF	1206	Taiyo Yuden JMK316BJ226ML	Ceramic
22 µF	0805	TDK C2012X5R0J226MT	Ceramic
22µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 µF	0805	TDK C2012X5R0J106M	Ceramic

8.2.2.4 Output Voltage Selection

The DEFDCDC1, DEFDCDC2, and DEFDCDC3 pins are used to set the output voltage for each step-down converter. See Table 19 for the default voltages if the pins are pulled to GND or to VCC. If a different voltage is needed, an external resistor divider can be added to the DEFDCDCx pin as shown in Figure 36.

The output voltage of VDCDC3 is set with the I^2C interface. If the voltage is changed from the default, using the DEFCORE register, the output voltage only depends on the register value. Any resistor divider at DEFDCDC3 does not change the voltage set with the register.

Table 19. DCDC1, DCDC2, and DCDC3 Default Voltage Levels

PIN	LEVEL	DEFAULT OUTPUT VOLTAGE
DEFDCDC1	VCC	3.3 V
	GND	3 V
DEFDCDC2	VCC	2.5 V
	GND	1.8 V
DEFDCDC3	VCC	1.55 V
	GND	1.3 V

Using an external resistor divider at DEFDCDCx:

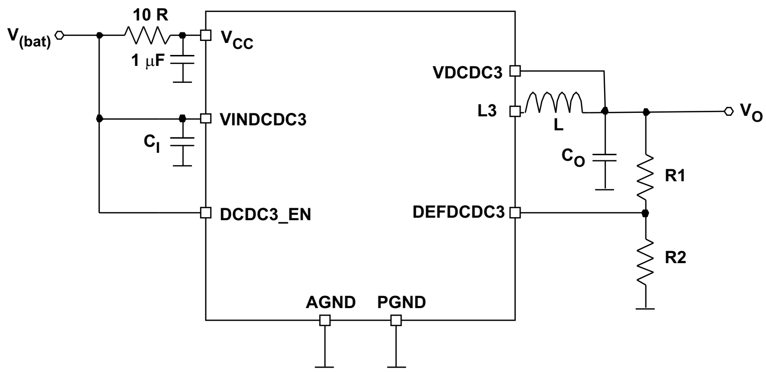


Figure 36. External Resistor Divider

When a resistor divider is connected to DEFDCDCx, the output voltage can be set from 0.6 V up to the input voltage $V_{(bat)}$. The total resistance (R1 + R2) of the voltage divider should be kept in the 1-MR range in order to maintain a high efficiency at light load.

$V_{(DEFDCDCx)}$ = 0.6 V

$$V_{OUT} = V_{DEFDCDCx} \times \frac{R1 + R2}{R2} \qquad R1 = R2 \times \left(\frac{V_{OUT}}{V_{DEFDCDCx}}\right) - R2 \tag{8}$$

8.2.2.5 VRTC Output

The VRTC output is typically connected to the Vcc_Batt pin of a Intel® PXA270 processor. During power-up of the processor, the TPS65022 internally switches from the LDO or the backup battery to the system voltage connected at the VSYSIN pin (see Figure 28).It is required that a 4.7-µF (minimum) capacitor be added to the VRTC pin even if the output is not used.

8.2.2.6 LDO1 and LDO2

The LDOs in the TPS65022 are general-purpose LDOs which are stable using ceramics capacitors. The minimum output capacitor required is 2.2 µF. The LDOs output voltage can be changed to different voltages between 1 V and 3.3 V using the I^2C interface. Therefore, they can also be used as general-purpose LDOs in applications powering processors different from PXA270. The supply voltage for the LDOs must connect to the VINLDO pin, giving the flexibility to connect the lowest voltage available in the system and provides the highest efficiency.

8.2.2.7 TRESPWRON

This is the input to a capacitor that defines the reset delay time after the voltage at VRTC rises above 2.52 V. The timing is generated by charging and discharging the capacitor with a current of 2 µA between a threshold of 0.25 V and 1 V for 128 cycles. A 1-nF capacitor gives a delay time of 100 ms.

While there is no real upper and lower limit for the capacitor connected to TRESPWRON, do not leave signal pins open.

$$t_{(reset)} = 2 \times 128 \times \left(\frac{(1\,V - 0.25\,V) \times C_{(reset)}}{2\,\mu A}\right) \tag{9}$$

where

- $t_{(reset)}$ is the reset delay time
- $C_{(reset)}$ is the capacitor connected to the TRESPWRON pin

The minimum and maximum values for the timing parameters called ICONST (2 µA), TRESPWRON_UPTH (1 V) and TRESPWRON_LOWTH (0.25 V) can be found under the electrical characteristics.

8.2.2.8 *V_{CC}-Filter*

An RC filter connected at the VCC input is used to keep noise from the internal supply for the bandgap and other analog circuitry. A typical value of 10 R and 1 µF is used to filter the switching spikes, generated by the DC-DC converters. A larger resistor than 10 R should not be used because the current into V_{CC} of up to 3 mA causes a voltage drop at the resistor causing the undervoltage lockout circuitry connected at V_{CC} internally to switch off too early.

8.2.3 Application Curves

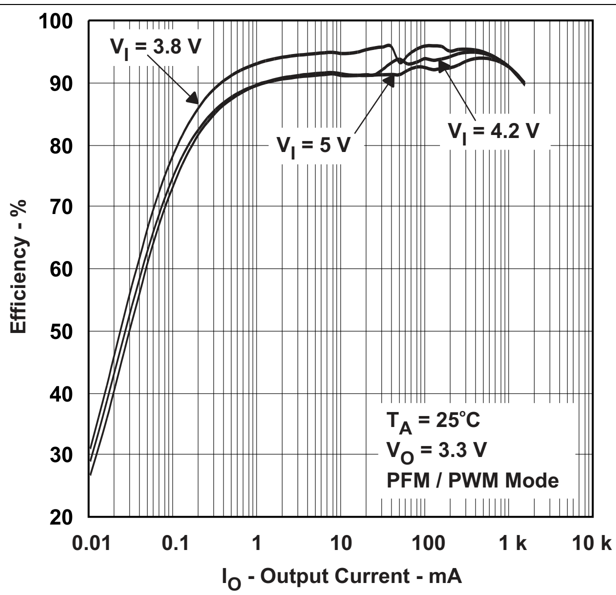


Figure 37. DCDC1 Efficiency

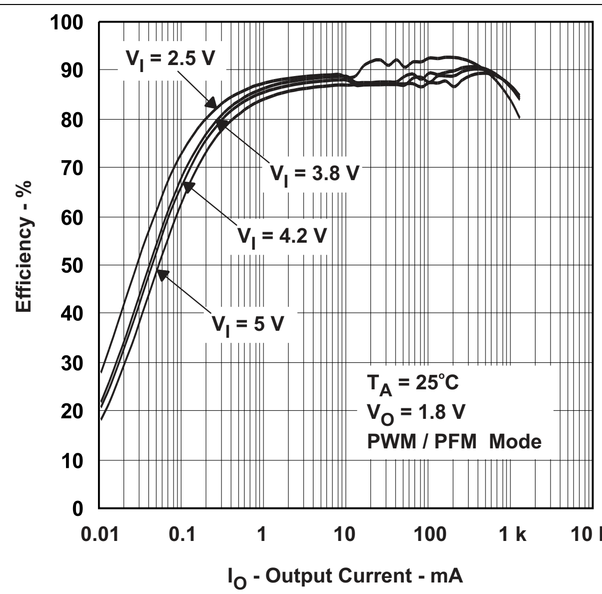


Figure 38. DCDC2 Efficiency

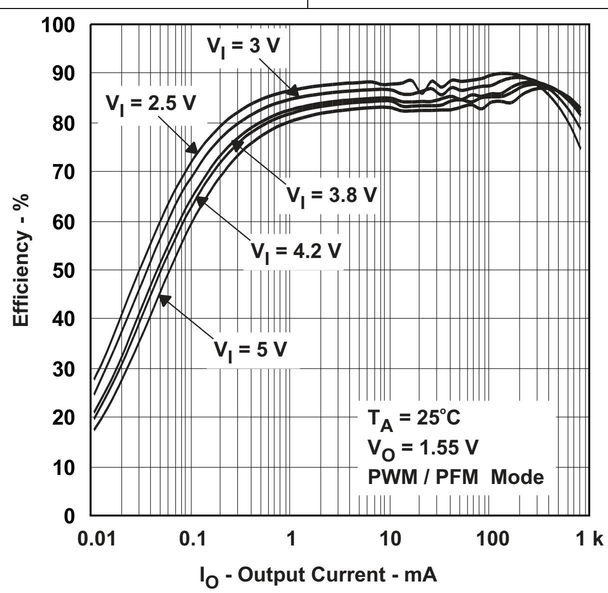


Figure 39. DCDC3 Efficiency

9 Power Supply Recommendations

For a supply voltage on pins V_{CC}, VINDCDC1, VINDCDC2 and VINDCDC3 below 3 V, TI recommends enabling the DCDC1, DCDC2 and DCDC3 converters in sequence. If all 3 step-down converters are enabled at the same time while the supply voltage is close to the internal reset detection threshold, a reset may be generated during power-up. Therefore TI recommends enabling the DC-DC converter in sequence. This can be done by driving one or two of the enable pins with a RC delay or by driving the enable pin by the output voltage of one of the other step-down converters. If a voltage above 3 V is applied on pin VBACKUP while V_{CC} and VINDCDCx is below 3 V, there is no restriction in the power-up sequencing as VBACKUP will be used to power the internal circuitry.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulators may show poor line and/or load regulation, and stability issues as well as EMI problems. It is critical to provide a low impedance ground path. Use wide and short traces for the main current paths. The input capacitors should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

For TPS65022, connect the PGND pins of the device to the PowerPAD™ land of the PCB and connect the analog ground connections (AGND) to the PGND at the PowerPAD. It is essential to provide a good thermal and electrical connection of all GND pins using multiple vias to the GND-plane. Keep the common path to the AGND pins, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. The VDCDCx line should be connected right to the output capacitor and routed away from noisy components and traces (for example, the L1, L2, and L3 traces).

10.2 Layout Example

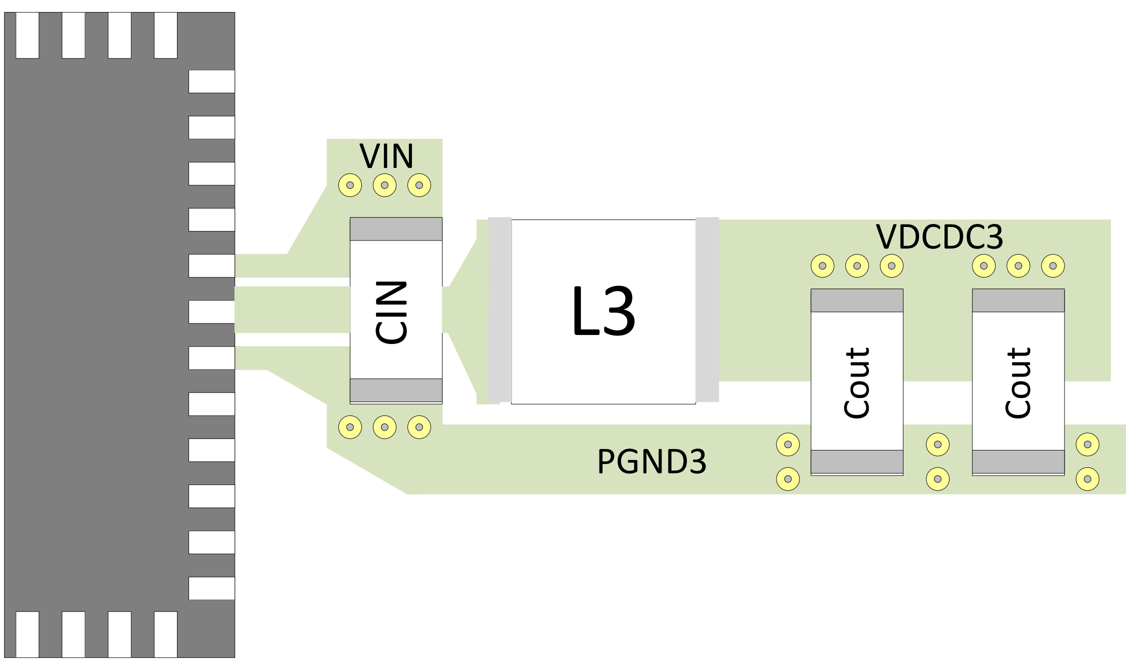


Figure 40. DC–DC Regulator Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

TMS320, OMAP, PowerPAD, E2E are trademarks of Texas Instruments.
Intel is a registered trademark of Intel Corporation.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65022RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65022	Samples
TPS65022RHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65022	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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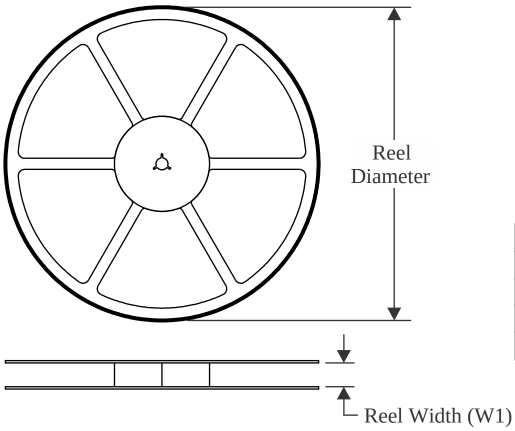
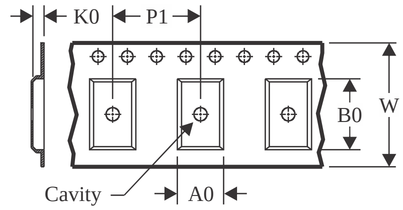
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

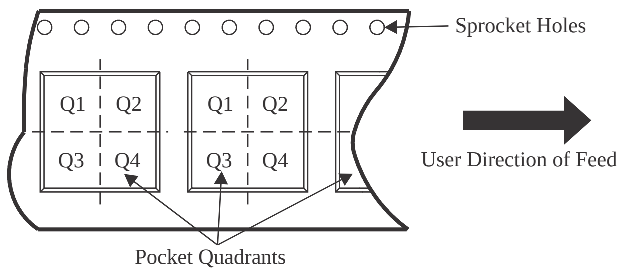


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

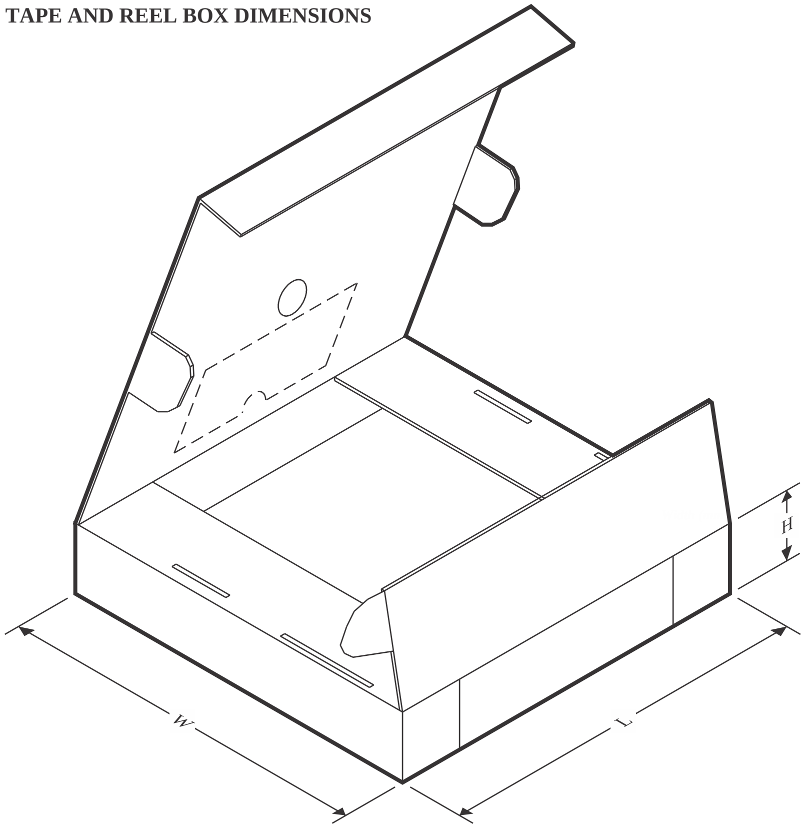
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65022RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65022RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

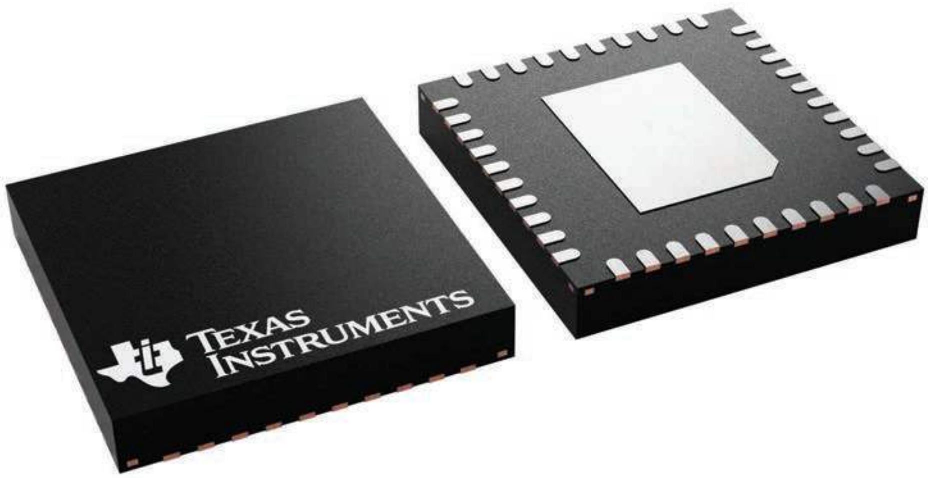
TAPE AND REEL BOX DIMENSIONS

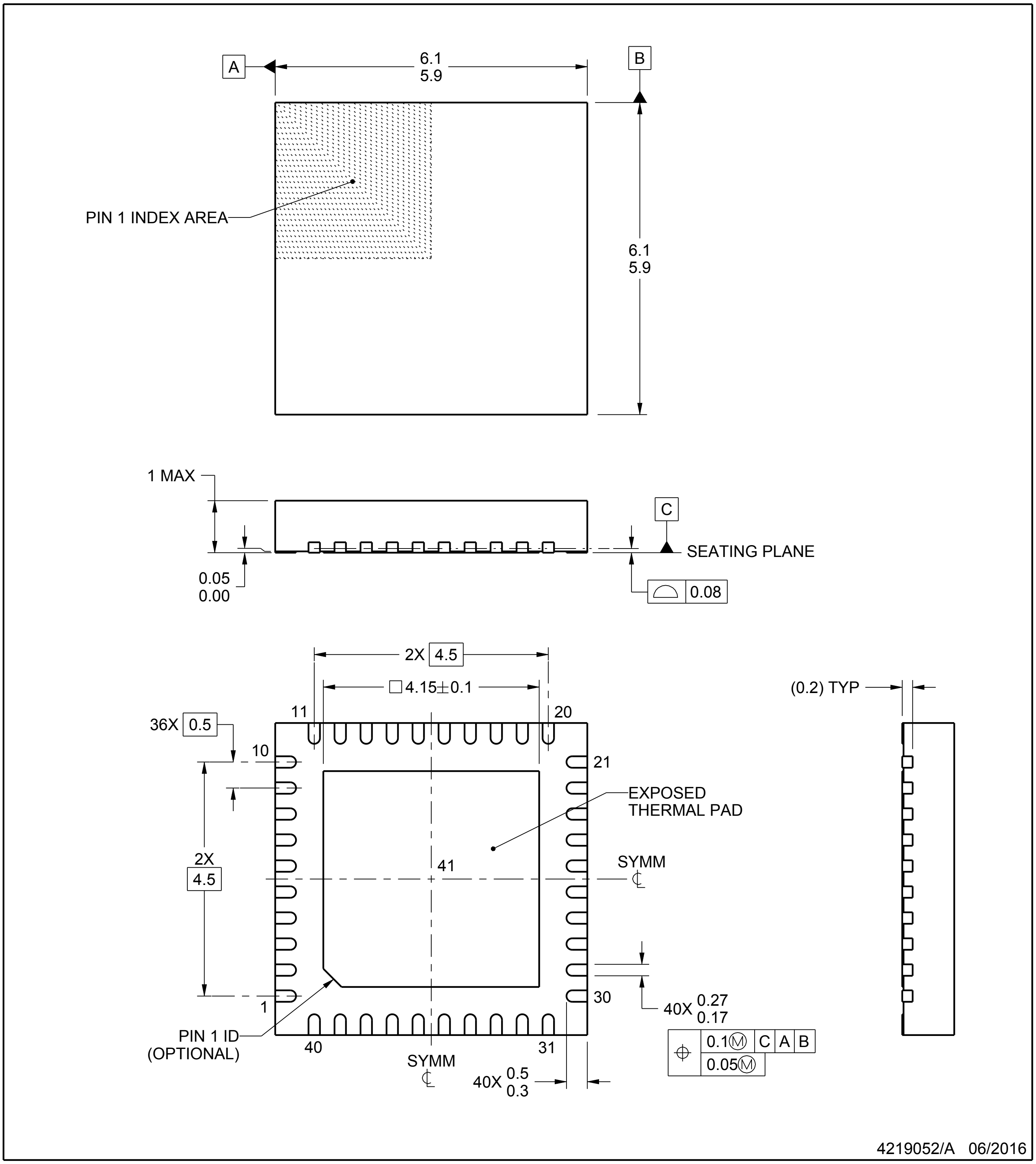


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65022RHAR	VQFN	RHA	40	2500	356.0	356.0	35.0
TPS65022RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

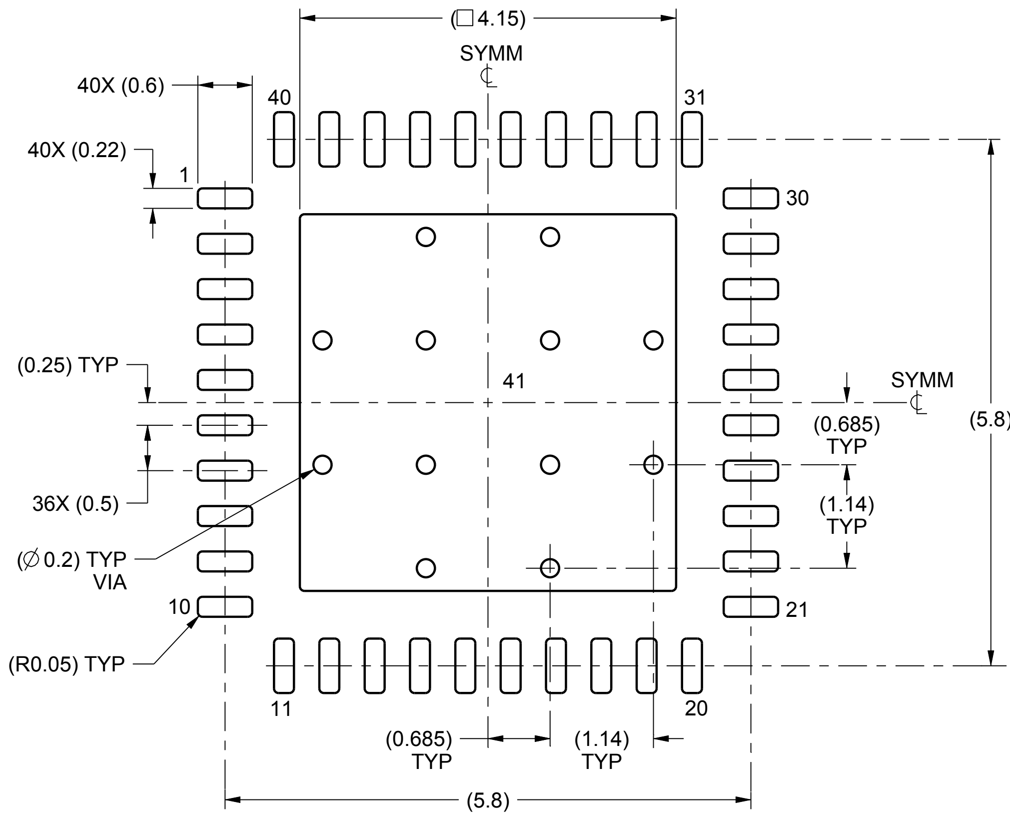
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



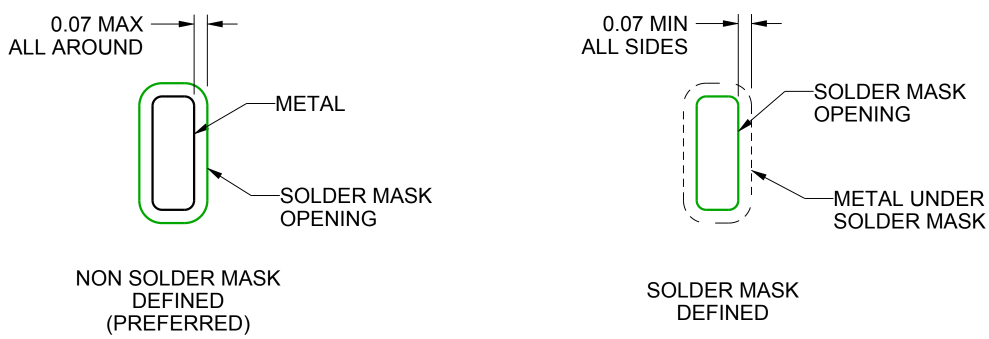


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

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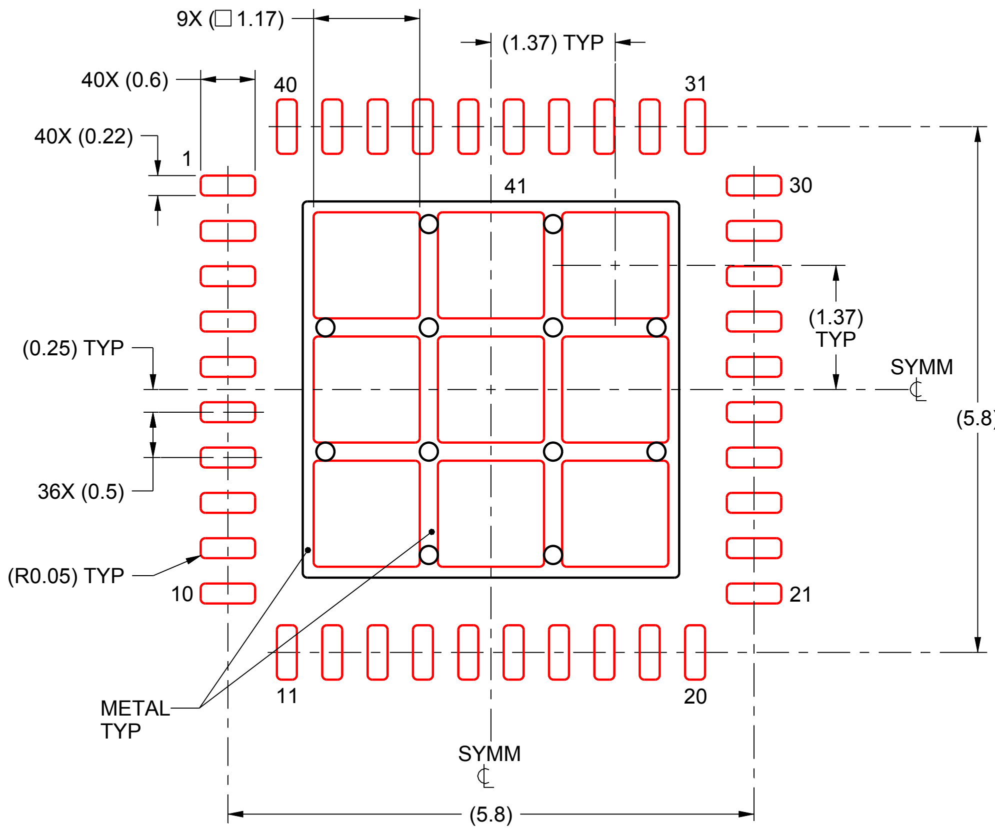
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.