LC^{2}MOS Complete Embedded Servo Front Ends for HDD

AD7773/AD7775*

FEATURES

- 10-Bit, 3 μs ADC
- Two DACs with Output Amplifiers
  - One 10-Bit, 4 μs Settling DAC
  - One 8-Bit, 3 μs Settling DAC
- Fully Integrated Burst Demodulator
- Power-Down Mode
- +5 V Only
- Fast Interface Port
- 28-Pin SOIC Package

APPLICATIONS

- Embedded Servo For HDD
- Combined Dedicated/Embedded Servo

GENERAL DESCRIPTION

The AD7773 and AD7775 provide all the functionality necessary to implement the servo demodulator and head positioning tasks in embedded servo systems. A power-down mode which turns all the linear circuitry OFF enhances the use of the AD7773 and AD7775 in portable systems.

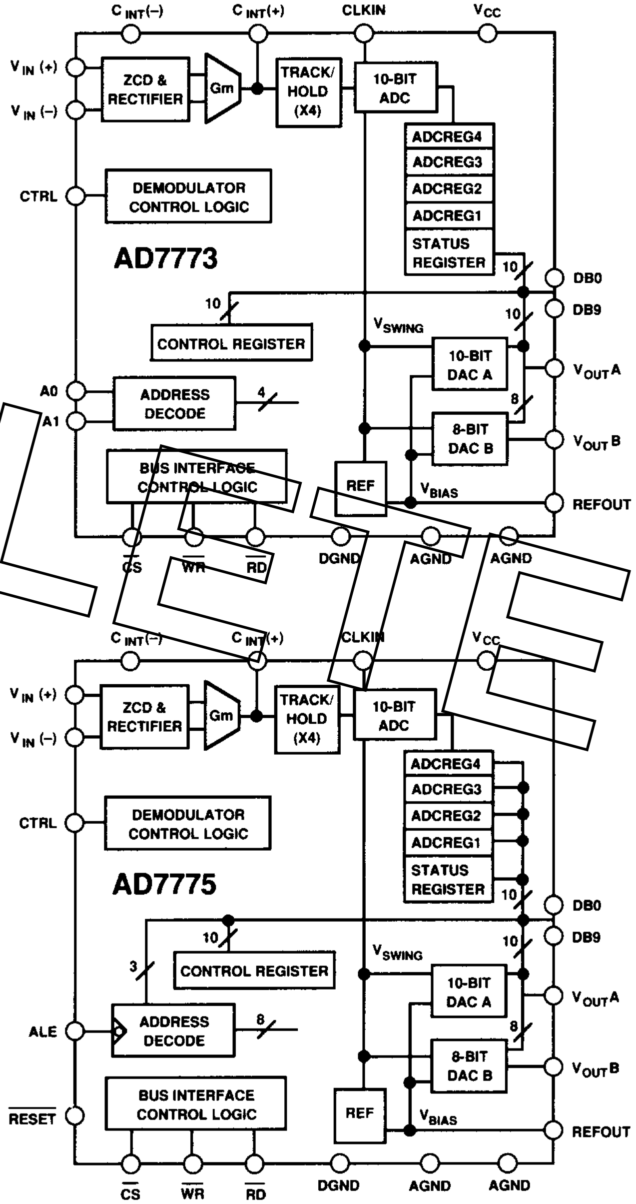
The demodulator channel can capture high speed servo data from a variety of embedded servo patterns. Up to four sequential servo burst signals can be synchronously demodulated, full-wave rectified and integrated. At the end of a burst period the integrated output voltage, representing the amplitude of a captured burst, is sampled and held on one of four internal track/hold amplifiers prior to conversion. After conversion the digitized burst signals from the ADC are fed to four 10-bit wide data registers.

The AD7773 and AD7775 also contain two independent voltage-output DACs: one with 10-bit resolution and one with 8-bit resolution. The two DACs produce output signals of the form $V_{BIAS} \pm V_{SWING}$ where V_{BIAS} and V_{SWING} are internally generated on-chip. The V_{BIAS} signal is available externally on the REFOUT pin.

The devices are easily interfaced to popular DSP processors and microcontrollers. The AD7773 has a 10-bit data port with separate address pins. The AD7775 has a 10-bit multiplexed address/data bus with an ALE input to latch the address.

The AD7773 and AD7775 are fabricated in linear compatible CMOS (LC^{2}CMOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The devices are available in 28-pin SOIC packages and 32-pin TSOPs.

FUNCTIONAL BLOCK DIAGRAMS



---

*Protected by U.S. Patent No. 4,990,916.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

AD7773/AD7775—SPECIFICATIONS

(V_{CC} = +5 V ± 5%; AGND = DGND = 0 V; CLKIN = 6.67 MHz; C_{INT} = 200 pF; Burst Frequency = 5 MHz; Cycles Integrated = 4. All specifications T_{MIN} to T_{MAX}, unless otherwise stated.)

Parameter	J Version[1]	Units	Conditions/Comments
DEMODULATOR CHANNEL			All AC Test Waveforms are Sinusoidal. Minimum Signal Frequency Is 2 MHz.
ADC Resolution	10	Bits	
Demodulator Channel Gain, G_{CH}	352	LSB/V p–p min	Channel Gain is (384 ± 32) LSB/V p–p
	416	LSB/V p–p max	
Intercept of Transfer Function on ADC Code Axis, ADC_{INTCPT}	−137/+35	LSB min/max	See Terminology & Figure 19
Differential Input Resistance	4/6.5	kΩ min/max	Typically 5 kΩ; Measured at DC; See Terminology
Differential Input Capacitance[2]	1/4	pF min/max	
Common-Mode Input Resistance	2/3.5	kΩ min/max	Typically 2.5 kΩ; Measured at DC; See Terminology
Common-Mode Input Capacitance[2]	5/15	pF min/max	
ZCD Differential Hysteresis, V_H	40/120	mV p–p min/max	Typically 55 mV; See Figure 20 under Design Information
Frequency Response to Pulse Harmonics			
2nd Harmonics	±10	% typ	See Terminology
3rd Harmonics	±20	% typ	
Common-Mode Rejection Ratio[2]	46	dB min	See Terminology
Power Supply Rejection Ratio[2]	40	dB min	See Terminology
Channel Noise Level[2]	49	dB min	See Terminology
Composite Noise Rejection[2]	38	dB min	Referenced to Half-Scale; See Terminology
V_{IN}, Differential Input Signal Range for Guaranteed Positive Slope	0.24/2.26	V p–p min/max	See Terminology
ADC Code for 0 mV p–p Differential Input Voltage, ADC_0	+35	LSB max	See Figure 19
ADC Code for 240 mV p–p Differential Input Voltage, ADC_{240}	ADC_{200} + 4	LSB min	ADC_{200} Is ADC Code for 200 mV p–p Differential Input Voltage
ADC Code for 417 mV p–p Differential Input Voltage, ADC_{417}	ADC_0 + 10	LSB min	
ADC Code for 2260 mV p–p Differential Input Voltage, ADC_{2260}	ADC_{2500} − 4	LSB min	ADC_{2500} Is ADC Code for 2500 mV p–p Differential Input Voltage
ADC Code for 2500 mV p–p Differential Input Voltage, ADC_{2500}	1022	LSB max	
Voltage Change Across C_{INT} for Full-Scale ADC Range	REFOUT/2	V typ	
Gm, Transconductance from V_{IN} to I_{OUT} at $C_{INT}(+)$	0.277/0.306	mS min/max	
Relative Accuracy	±4	LSB max	0.625 V to 1.875 V; See Terminology
	±8	LSB max	0.417 V to 2.083 V
Differential Nonlinearity	−1.3/+2	LSB max	Guaranteed Monotonic to 9 Bits; See Terminology
Channel Mismatch	10	LSB max	Measured at Half-Scale; See Terminology
Crosstalk Between Bursts	5	LSB max	See Terminology
ADC Conversion Time	14 T_{CLKIN}	µs max	Per Captured Burst; See Terminology
T_{CLKIN}	0.15/0.5	µs min/max	Period of Input Clock CLKIN
T_{CLKIN} High[2]	60	ns min	Minimum High Time for CLKIN
T_{CLKIN} Low[2]	60	ns min	Minimum Low Time for CLKIN
Output Coding	Unipolar Binary		
ANALOG OUTPUTS[3]			Applies to Both DACs
Output Voltage Range	$V_{BIAS} - V_{SWING}$	V min	
	$V_{BIAS} + V_{SWING}$	V max	
Digital-to-Analog Glitch Impulse[2]	15	nV sec typ	See Terminology
Digital Feedthrough[2]	1	nV sec typ	See Terminology
DC Output Impedance[2]	5	Ω max	Typically 0.5 Ω
Short-Circuit Current[2]	20	mA max	See Terminology
Power Supply Rejection Ratio[2]	20	dB min	See Terminology
Input Coding	Offset Binary/2s Complement		Programmable via Location CR6 of the Control Register

Parameter	J Version[1]	Units	Conditions/Comments
ANALOG OUTPUTS[3] (Continued)			
DAC A			
Resolution	10	Bits	
Output Voltage Settling Time[2]	4	µs max	Settling Time to Within ±1/2 LSB of Final Value; Typically 2.0 µs
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Bias Offset Error	±20	LSB max	
Plus or Minus Full-Scale Error	±16	LSB max	Referenced to REFOUT/2
DAC B			
Resolution	8	Bits	
Output Voltage Settling Time[2]	3	µs max	Settling Time to Within ±1/2 LSB of Final Value; Typically 2.0 µs
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Bias Offset Error	±6	LSB max	
Plus or Minus Full-Scale Error	±6	LSB max	Referenced to REFOUT/2.
LOGIC INPUTS			
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, CTRL, CLKIN, $\overline{RESET}$ & ALE (AD7775), A0 & A1 (AD7773)			
Input Low Voltage, V_{INL}	0.8	V max	
Input High Voltage, V_{INL}	2.4	V min	
Input Leakage Current	10	µA max	
Input Capacitance[2]	10	pF max	
LOGIC OUTPUTS			
DB0–DB9 (AD7773)			
AD0–DB9 (AD7775)			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 µA
Floating State Leakage Current	10	µA max	
Floating State Capacitance[2]	10	pF max	
POWER REQUIREMENTS			
V_{CC} Range	4.75/5.25	V min/V max	For Specified Performance
I_{CC}, Normal Mode[4]	30	mA max	Control Register Locations CR8 = CR9 = Logic High
I_{CC}, Power Down Mode[5]	1.5	mA max	Control Register Locations CR8 = Logic High, CR9 = Logic Low; All Linear Circuitry OFF
Power-Up Time to Operational Specifications[2]	500	µs max	From Power Down Mode
DAC REFERENCE INPUTS			
V_{BIAS} for both DACs	REFOUT	V	Internally Connected. Available Externally on REFOUT Pin
V_{SWING} for both DACs	REFOUT/2	V	Internally Connected
REFERENCE OUTPUT[6]			
REFOUT	2.1/2.2	V min/max	
Reference Load Change	±3	mV max	For Reference Load Current Change of 0 to ±500 µA
	±5	mV max	For Reference Load Current Change of 0 to ±2 mA
			Reference Load Should Not Change During Conversion

NOTES

[1] Temperature range as follows: J Version: 0°C to +70°C.

[2] Guaranteed by design, not production tested.

[3] Output load of 10k‖100 pF is referenced to REFOUT.

[4] Input signal levels are as follows: V_{INL} = 0.85 V, V_{INH} = 2.35 V; $\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = $\overline{RESET}$ (AD7775 only) = A0, A1 (AD7773 only) = V_{INH}; ALE (AD7775 Only) = CTRL = V_{INL}; CLKIN = 6.67 MHz at 50% Mark-Space ratio between V_{INL} & V_{INH}; no conversion in progress and data bus, DB0–DB9 (AD7773 Only), AD0–DB9 (AD7775 only), tied to 0 V.

[5] Input signal levels are as follows: V_{INL} = 0 V, V_{INH} = V_{CC}; $\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = $\overline{RESET}$ (AD7775 only) = A0, A1 (AD7773 Only) = V_{INH}; ALE (AD7775 only) = CTRL = CLKIN = V_{INL}; data bus, DB0–DB9 (AD7773 only), AD0–AD9 (AD7775 only) tied to 0 V.

[6] For capacitive loads greater than 100 pF a series resistor is required.

Specifications subject to change without notice.

INTERFACE TIMING CHARACTERISTICS—AD7773[1, 2] (V_{CC} = +5 V ± 5%; AGND = DGND = 0 V)

Parameter	Label	Limit at T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
INTERFACE TIMING				
Address Setup to $\overline{WR}$ or $\overline{RD}$ Falling Edge	t_1	4	ns min	
Address Hold after $\overline{WR}$ or $\overline{RD}$ Rising Edge	t_2	0	ns min	
Address Setup to $\overline{CS}$ Falling Edge	t_3	9	ns min	
$\overline{WR}$ or $\overline{RD}$ Rising Edge to $\overline{CS}$ Rising Edge	t_4	0	ns min	
$\overline{WR}$ or $\overline{RD}$ Pulse Width	t_5	53	ns min	
$\overline{CS}$ or $\overline{RD}$ Active to Valid Data[3]	t_6	**60**	ns max	Timed from Whichever Occurs Last
Bus Relinquish Time after $\overline{RD}$[4]	t_7	10	ns min	
		22	ns max	
Data Valid to $\overline{WR}$ Rising Edge	t_8	55	ns min	
Data Valid after $\overline{WR}$ Rising Edge	t_9	10	ns min	
Delay Time Between Stack Reads	t_{15}	100	ns min	See Figure 12b

NOTES

[1] See Figures 1 and 2.

[2] Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[3] t_6 is measured with the load circuit of Figure 3 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[4] t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 3. The measured time is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time t_7 quoted above is the true bus relinquish time of the device and, as such, is independent of the external bus loading capacitance.

Specifications subject to change without notice.

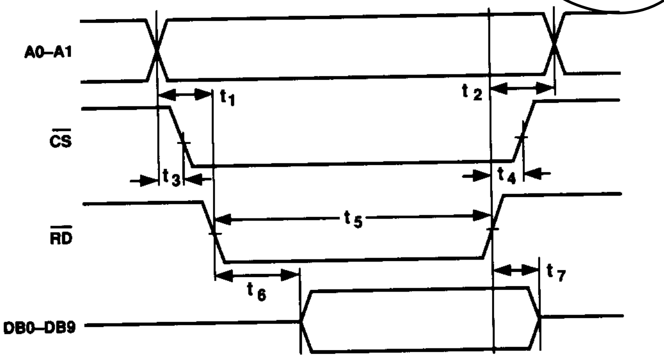


Figure 1. Read Cycle Timing for AD7773 Interface

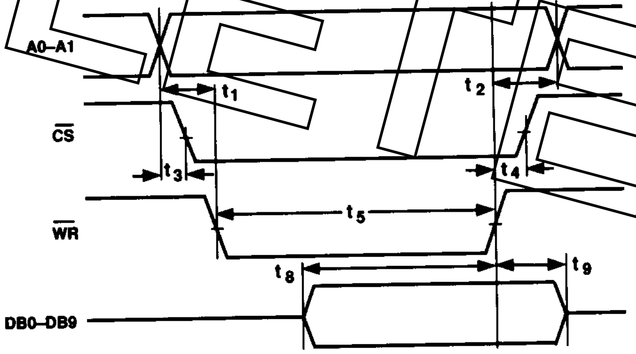


Figure 2. Write Cycle Timing for AD7773 Interface

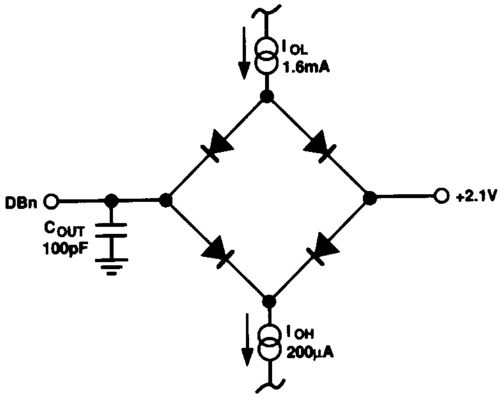


Figure 3. Load Circuit for Bus Timing Characteristics

INTERFACE TIMING CHARACTERISTICS—AD7775[1, 2] (V_{CC} = +5 V ± 5%; AGND = DGND = 0 V)

Parameter	Label	Limit at T_{MIN} to T_{MAX}	Units	Test Conditions/Comments
INTERFACE TIMING				
ALE Pulse Width	t_1	50	ns min	
$\overline{WR}$ or $\overline{RD}$ Rising Edge to ALE Rising Edge	t_2	50	ns min	
ALE Rising Edge to $\overline{CS}$ Falling Edge	t_3	22	ns min	
$\overline{CS}$ Falling Edge to $\overline{RD}$ Falling Edge	t_4	60	ns min	
$\overline{CS}$ Falling Edge to $\overline{WR}$ Falling Edge	t_5	30	ns min	
$\overline{WR}$ or $\overline{RD}$ Rising Edge to $\overline{CS}$ Rising Edge	t_6	0	ns min	
$\overline{WR}$ Pulse Width	t_7	53	ns min	
ALE Falling Edge to $\overline{WR}$ or $\overline{RD}$ Falling Edge	t_8	22	ns min	
Address Setup to ALE Falling Edge	t_9	47	ns min	
Address Hold after ALE Falling Edge	t_{10}	22	ns min	
$\overline{RD}$ Active to Valid Data[3]	t_{11}	75	ns max	Measured with t_4 = 60 ns
Bus Relinquish Time after $\overline{RD}$[4]	t_{12}	10	ns min	
		62	ns max	
Data Valid to $\overline{WR}$ Rising Edge	t_{13}	55	ns min	
Data Valid after $\overline{WR}$ Rising Edge	t_{14}	10	ns min	
Delay Time Between Stack Reads	t_{15}	100	ns min	See Figure 13b

---

NOTES

[1] See Figures 4 and 5.

[2] Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[3] Data access time depends directly on t_4, the $\overline{CS}$ to $\overline{RD}$ setup time, e.g., $t_{11} = 135 - t_4$. Time t_{11} is measured with the load circuit of Figure 3 and is defined as the time required for an output to cross 0.8 V or 2.4 V.

[4] t_{12} is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time t_{12} quoted above is the true bus relinquish time of the device and, as such, is independent of external bus loading capacitance.

Specifications subject to change without notice.

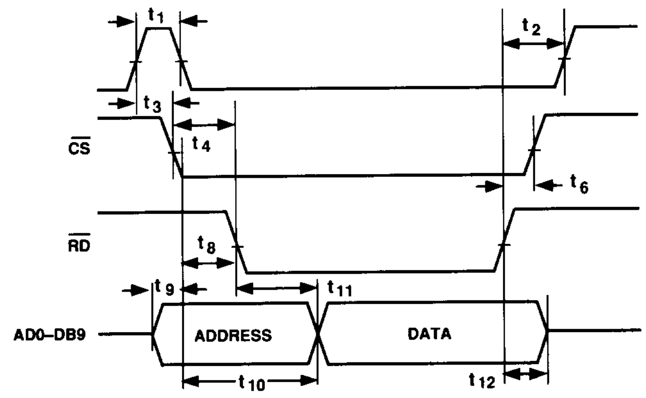


Figure 4. Read Cycle Timing for AD7775

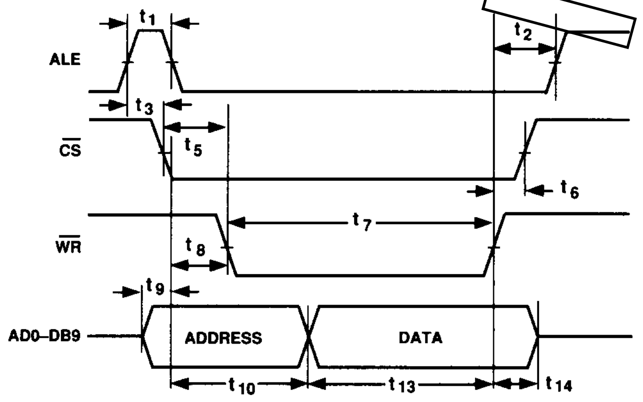


Figure 5. Write Cycle Timing for AD7775

DEMODULATOR TIMING CHARACTERISTICS[1] (V_{CC} = +5 V ± 5%; AGND = DGND = 0 V)

Parameter	Label	Limit at T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
$\overline{\text{RESET}}$ Rising Edge to CTRL Rising Edge[2]	–	100	ns min	For AD7775 Only
$\overline{\text{WR}}$ Rising Edge to CTRL Rising Edge[2]	–	200	ns min	Applies Only after a Write Instruction to the Control Register
$\overline{\text{RESET}}$ Pulse Width[2]	–	100	ns min	For AD7775 Only
SYNCHRONOUS DETECTOR MODE[3]				
CTRL High Time	t_{C1}	$(N + 3.5)\ t_{CYC}$	ns min	Minimum N for Guaranteed Performance Is 4, Maximum N Is 15. Programmable via Locations CR0–CR3 of the Control Register
CTRL Low Time[2]	t_{C2}	$1.5\ t_{CYC}$	ns min	
Input Signal Period	t_{CYC}	200 500	ns min ns max	Fundamental Input Frequency Must Lie Between 2 MHz and 5 MHz
GATED DETECTOR MODE[4]				
CTRL High Time	t_{C1}	800	ns min	
CTRL Low Time[2]	t_{C2}	$600 + 0.375\ t_C1$	ns min	
Input Signal Frequency	f_{IN}	5	MHz max	Corresponds to 200 ns Minimum Input Signal Period
CALIBRATION MODE[5]				
CTRL High Time	t_{C1}	800	ns min	Assumes Internal Calibration Voltage Has Settled; See Under Circuit Description for Calibration Mode
CTRL Low Time[2]	t_{C2}	300	ns min	

NOTES

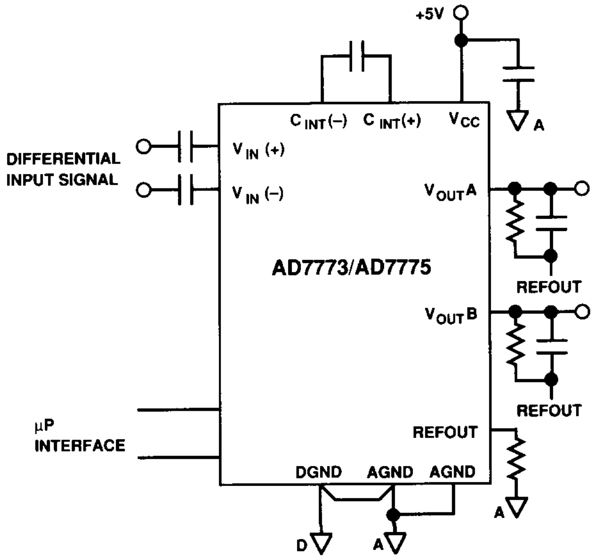
[1] All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2] Sample tested at +25°C to ensure compliance.

[3] See Figures 8a and 8b.

[4] See Figure 9.

[5] See Figure 10.



AC Test Circuit

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to AGND or DGND	−0.3 V, +7 V
AGND to DGND	−0.3 V, V_{CC} +0.3 V
Digital Inputs to DGND	−0.3 V, V_{CC} +0.3 V
Digital Outputs to DGND	−0.3 V, V_{CC} +0.3 V
Analog Inputs to AGND	−0.3 V, V_{CC} +0.3 V
Analog Outputs to AGND	−0.3 V, V_{CC} +0.3 V
Operating Temperature Range	
Commercial (J Version)	0°C to +70°C
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation, SOIC	1 W
θ_{JA} Thermal Impedance	75°C/W
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation, TSOP	750 mW
θ_{JA} Thermal Impedance	80°C/W
Lead Temperature (Soldering, 10 secs)	+235°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

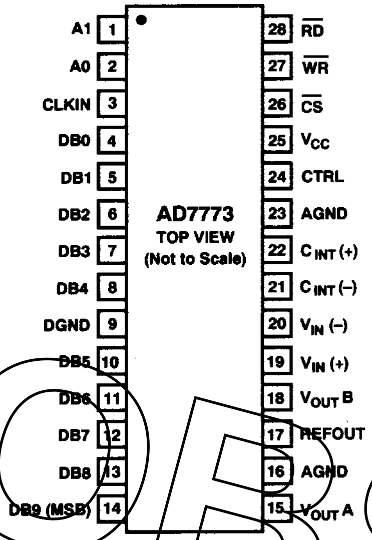
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

WARNING!

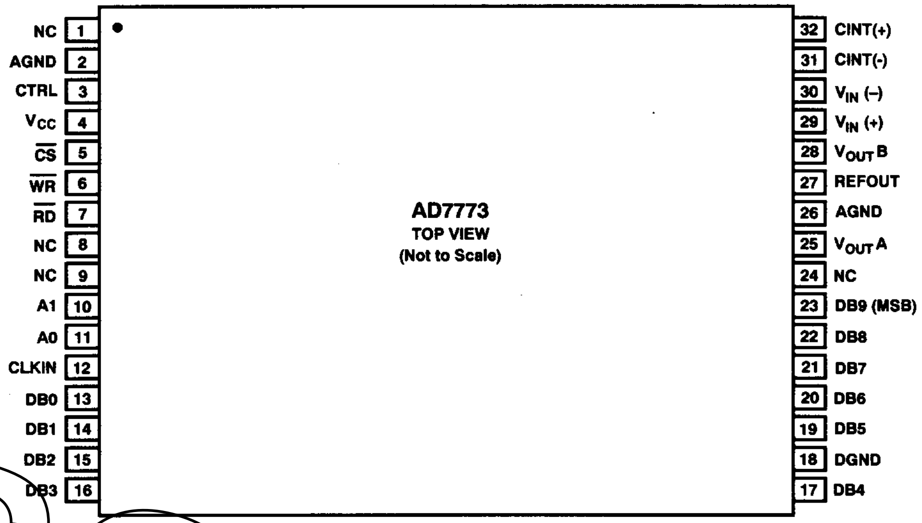
ESD SENSITIVE DEVICE

PIN CONFIGURATIONS

AD7773 SOIC

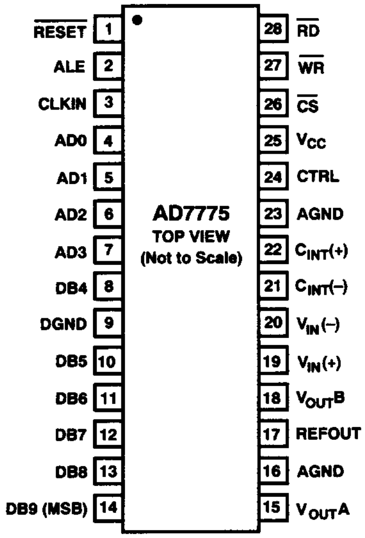


AD7773 TSOP

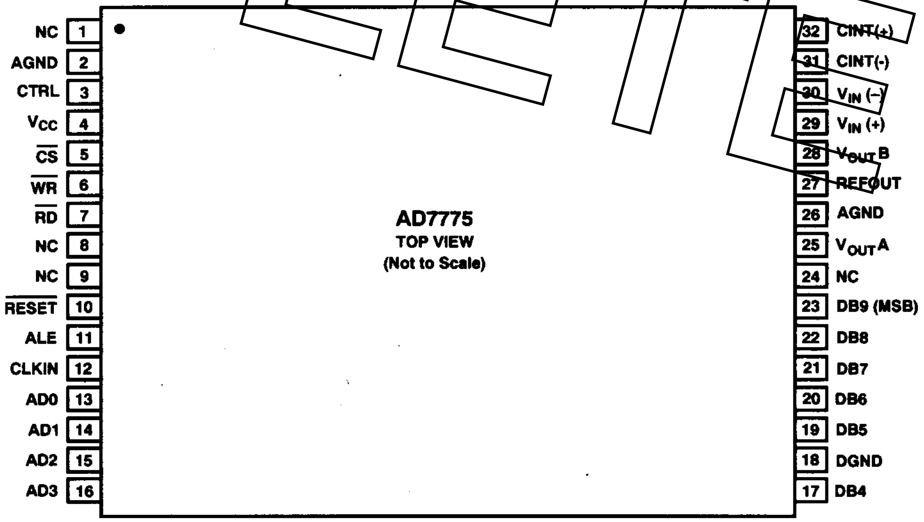


NC = NO CONNECT

AD7775 SOIC



AD7775 TSOP



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Package Option
AD7773JR	0°C to +70°C	R-28[1]
AD7773JU	0°C to +70°C	U-32[2]
AD7775JR	0°C to +70°C	R-28
AD7775JU	0°C to +70°C	U-32

NOTES

[1] R = Small Outline IC (SOIC).

[2] U = Thin Small Outline Package (TSOP).

SOIC PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
Power Supplies		
25	V_{CC}	+5 V Power Supply.
9	DGND	Digital Ground.
16 & 23	AGND	Analog Ground.
Microprocessor Interface		
28	$\overline{RD}$	Read Input (Active Low). When active it is used in conjunction with $\overline{CS}$ to read data over the Input/Output bus. See the truth tables for Microprocessor Interfacing.
27	$\overline{WR}$	Write Input (Active Low). When active it is used in conjunction with $\overline{CS}$ to write data over the Input/Output bus.
26	$\overline{CS}$	Chip Select Input (Active Low). The device is selected when this input is low.
Microprocessor Interface—AD7773 Only		
4–8 & 10–14	DB0–DB4 DB5–DB9	Input/Output Data Bus. A 10-bit wide bidirectional data port over which data is transferred into or out of the AD7773. DB0 is the Least Significant Bit.
2 1	A0 A1	Address Inputs A0 and A1 select one of four registers. See Table I for details.
Microprocessor Interface—AD7775 Only		
4–8 & 10–14	AD0–DB4 DB5–DB9	Multiplexed Address/Data Input/Output Bus. An ALE signal is used to demultiplex the bus. After the falling edge of ALE the address present on AD0–AD3 must be removed and $\overline{WR}$ or $\overline{RD}$ exercised to complete the instruction. The bus now transfers 10 bits of data into or out of the AD7775. AD0 is the Least Significant Bit.
2	ALE	Address Latch Enable Input used to demultiplex the address/data bus. On the falling edge of ALE address inputs AD1–AD3 are internally latched (AD0 is a don't care) and remain latched until ALE returns High. See Table II for details.
1	$\overline{RESET}$	Reset Input (Active Low). Used as a hardware reset for various functional blocks: Loads half-scale code into both DAC registers. Resets the internal ADC register stack Write Pointer to the bottom-most register. Loads Control Register with 364 (Hex). See Control Register Description. Loads Status Register with 3E0 (Hex). See Status Register Description.
Demodulator Channel		
19 20	$V_{IN}(+)$ $V_{IN}(-)$	Differential Inputs to the input amplifier. Analog input signals to these pins should be capacitively coupled.
22 21	$C_{INT}(+)$ $C_{INT}(-)$	The value of capacitor connected between these pins sets the integrator time constant. See under Design Information for choosing the C_{INT} capacitor.
24	CTRL	Control Input. All signal capture operations are controlled by this input. The number of CTRL pulses applied to the device must equal the number of bursts to be captured.
3	CLKIN	Clock input. A clock is required for the ADC. An external TTL-compatible clock must be applied to this input pin. See the T_{CLKIN} specifications for CLKIN information.
Analog Outputs		
		Each of the two DACs has the same output voltage range given by: $V_{OUT} = V_{BIAS} \pm V_{SWING} = REFOUT \pm V_{SWING}$ With midcode in either DAC register the respective DAC output is equal to REFOUT.
15	$V_{OUT}A$	Analog Output Voltage from DAC A. 1 LSB = 2 V_{SWING}/1024 = REFOUT/1024 =2.1 mV.
18	$V_{OUT}B$	Analog Output Voltage from DAC B. 1 LSB = 2 V_{SWING}/256 = REFOUT/256 = 8.6 mV.
17	REFOUT	Voltage Reference Output. Internally this is used as the reference for the ADC and as the bias level (V_{BIAS}) for the two DACs.

TSOP PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
Power Supplies		
4	V_{CC}	+5 V Power Supply.
18	DGND	Digital Ground.
2 & 26	AGND	Analog Ground.
Microprocessor Interface		
7	$\overline{RD}$	Read Input (Active Low). When active it is used in conjunction with $\overline{CS}$ to read data over the Input/Output bus. See the truth tables for Microprocessor Interfacing.
6	$\overline{WR}$	Write Input (Active Low). When active it is used in conjunction with $\overline{CS}$ to write data over the Input/Output bus.
5	$\overline{CS}$	Chip Select Input (Active Low). The device is selected when this input is low.
Microprocessor Interface—AD7773 Only		
13–17 & 19–23	DB0–DB4 DB5–DB9	Input/Output Data Bus. A 10-bit wide bidirectional data port over which data is transferred into or out of the AD7773. DB0 is the Least Significant Bit.
11 10	A0 A1	Address Inputs A0 and A1 select one of four registers. See Table I for details.
Microprocessor Interface—AD7775 Only		
13–17 & 19–23	AD0–DB4 DB5–DB9	Multiplexed Address/Data Input/Output Bus. An ALE signal is used to demultiplex the bus. After the falling edge of ALE the address present on AD0–AD3 must be removed and $\overline{WR}$ or $\overline{RD}$ exercised to complete the instruction. The bus now transfers 10 bits of data into or out of the AD7775. AD0 is the Least Significant Bit.
11	ALE	Address Latch Enable Input used to demultiplex the address/data bus. On the falling edge of ALE address inputs AD1–AD3 are internally latched (AD0 is a don't care) and remain latched until ALE returns High. See Table II for details.
10	$\overline{RESET}$	Reset Input (Active Low). Used as a hardware reset for various functional blocks: Loads half-scale code into both DAC registers. Resets the internal ADC register stack Write Pointer to the bottom-most register. Loads Control Register with 364 (Hex). See Control Register Description. Loads Status Register with 3E0 (Hex). See Status Register Description.
Demodulator Channel		
29	$V_{IN}(+)$	Differential Inputs to the input amplifier. Analog input signals to these pins should be capacitively coupled.
30	$V_{IN}(-)$	
32	$C_{INT}(+)$	The value of capacitor connected between these pins sets the integrator time constant. See under Design Information for choosing the C_{INT} capacitor.
31	$C_{INT}(-)$	
3	CTRL	Control Input. All signal capture operations are controlled by this input. The number of CTRL pulses applied to the device must equal the number of bursts to be captured.
12	CLKIN	Clock input. A clock is required for the ADC. An external TTL-compatible clock must be applied to this input pin. See the T_{CLKIN} specifications for CLKIN information.
Analog Outputs		
		Each of the two DACs has the same output voltage range given by: $V_{OUT} = V_{BIAS} \pm V_{SWING} = REFOUT \pm V_{SWING}$ With midcode in either DAC register the respective DAC output is equal to REFOUT.
25	$V_{OUT}A$	Analog Output Voltage from DAC A. 1 LSB = $2\ V_{SWING}/1024$ = REFOUT/1024 = 2.1 mV.
28	$V_{OUT}B$	Analog Output Voltage from DAC B. 1 LSB = $2\ V_{SWING}/256$ = REFOUT/256 = 8.6 mV.
27	REFOUT	Voltage Reference Output. Internally this is used as the reference for the ADC and as the bias level (V_{BIAS}) for the two DACs.
1, 8, 9, 24	NC	No Connects.

CONTROL REGISTER DESCRIPTION

The control register is 10-bits wide and can only be written to. Individual bit functions are described below. Normally the demodulator channel operates as a synchronous detector to capture complete cycles of a servo burst waveform. However, if CR0 to CR3 are loaded with all 0s, the demodulator channel performs as a simple gated detector stage, gated ON/OFF by the CTRL input. See under CIRCUIT DESCRIPTION—Gated Detector Mode.

CR0 to CR3 determine the number of complete cycles to be synchronously detected within a single burst:

CR3	CR2	CR1	CR0	Cycles
0	0	0	0	Gated Detector
0	0	0	1	NA
0	0	1	0	NA
0	0	1	1	NA
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

CR4 and CR5 determine the number of bursts which are to be captured.

CR5	CR4	Number of Bursts
0	0	1
0	1	2
1	0	3
1	1	4

CR6 determines whether DAC coding is offset binary or twos complement.

CR6	Coding
0	Offset Binary
1	Twos Complement

CR7, CR8 and CR9 are decoded to provide a number of different functions. CR7 determines whether a signal will be acquired via the synchronous detector's differential inputs or direct from the $C_{INT}(+)$ pin. $\overline{CR7}$ is ANDed with the internally generated integrate signal INT to make or break the signal path from the rectifier output to the $C_{INT}(+)$ pin. With CR7 low the rectifier output drives the external integrating capacitor on the C_{INT} pins and all input signals are acquired through the $V_{IN}(+)$ and $V_{IN}(-)$ differential input pins. With CR7 high the synchronous detector stage is bypassed and all input signals are now acquired through the single-ended $C_{INT}(+)$ pin.

CR9	CR8	CR7	Function
0	0	X*	Soft Reset
0	1	X	Power Down
1	0	0	Not Allowed
1	0	1	Calibration Mode
1	1	0	Normal Mode
1	1	1	Not Allowed

*X = don't care.

Soft Reset: Soft Reset performs the same functions that the $\overline{\text{RESET}}$ input performs. On receipt of a reset command (either via software or hardware) the control register is loaded with 364 (Hex) as shown below.

CR0	0
CR1	0
CR2	1
CR3	0
CR4	0
CR5	1
CR6	1
CR7	0
CR8	1
CR9	1

Also on receipt of a reset command the status register is loaded with 3E0 (Hex); i.e., locations SR0–SR4 are loaded with all 0s indicating four good burst captures and conversions complete.

Power Down: In the power down mode all linear circuitry is turned off. Both DAC outputs and the REFOUT output are pulled weakly (5 kΩ) to AGND.

Calibration Mode: The purpose of this mode is to allow any channel mismatch which may exist between the four internal track/hold amplifiers to be easily measured. See under CIRCUIT DESCRIPTION—Calibration Mode section.

Normal Mode: This is the normal operating mode and allows external differential input signals to be acquired and converted. The contents of locations CR0–CR3 determine whether the demodulator channel will be in the synchronous detector mode or gated detector mode.

STATUS REGISTER DESCRIPTION

The status register (SR) is the bottom-most register of the 5-deep register stack. It is 10 bits wide and can be written to or read from. Its function is to provide status information on device operation. Location SR0 acts as a BUSY signal for the demodulator channel. SR0 is set high on the rising edge of the first CTRL pulse in a new burst capture sequence and remains high throughout the complete signal acquisition cycle and the subsequent conversion cycle. When the programmed number of conversions are complete, location SR0 is set low. The number of conversions carried out equals the number of bursts captured. This number is programmable from 1 to 4 via locations CR4 and CR5 of the control register. Up to four bursts can be captured and each of these capture operations has an individual status flag, SR1–SR4, associated with it. A logic low or "good" flag in location SR1, for instance, indicates that burst #1 was captured correctly. Alternatively, a logic high or "bad" flag in location SR1 indicates that a problem occurred while capturing burst #1; i.e., for whatever reason, less than the programmed number of cycles in burst #1 were captured. Locations SR5–SR9 of the status register are reserved and must always be read as logic highs for correct operation of the AD7773 and AD7775.

Primarily intended as a read only location, the status register has very limited write functionality. A write to the status register automatically loads all 1s into locations SR0–SR4 regardless of data present on the data bus. These flag settings represent four bad burst captures and conversions incomplete.

As mentioned previously, locations SR5–SR9 are used for production test purposes and must be written high for correct operation of the AD7773 and AD7775. All write instructions to the status register must load the word $11111XXXXX_2$. Repeated write instructions to address 11_2 (AD7773) or $011X_2$ (AD7775) are all decoded to the status register.

CIRCUIT DESCRIPTION

The AD7773 and AD7775 are intended primarily for embedded servo head positioning applications in Winchester-type disk drives. The demodulator channel can capture high speed servo data from a variety of embedded servo patterns. Up to four sequential input signals can be captured, converted to digital form and stored in the four data registers ADCREG1–ADCREG4. The 10-bit DAC output can be used to control the head position via a voice coil motor (VCM). The 8-bit DAC output can be used for spindle speed control, gain control, filter control etc. There are two major modes of operation of the demodulator channel—synchronous detector mode and gated detector mode. In the synchronous detector mode the differential input signals are applied in bursts to the differential inputs $V_{IN}(+)$ and $V_{IN}(-)$. A zero crossing detector (ZCD) is used to synchronously detect full cycles of the input signal within a given burst which are then rectified and integrated. Both the number of cycles within an individual burst and also the number of bursts to be captured are programmable. In the gated detector mode the synchronous detector is bypassed and the differential input signals are simply rectified and integrated as long as CTRL remains high. Whether in the synchronous detector mode or in the gated detector mode, a third mode, a calibration or CAL mode, is possible where a reference voltage is connected to the $C_{INT}(+)$ pin to allow any mismatch which exists between the four track/hold (T/H) amplifiers to be easily measured. A simplified diagram of the demodulator channel is shown in Figure 6. With CR7 a logic Low the normal mode is selected and SW1 is closed when a valid integrate INT signal is provided by the demodulator control logic. Switches SW1 and SW3 are functional only in the normal mode. In the calibrate mode CR7 is set to a logic high and SW1 is open regardless of the INT signal. Switch SW2 is closed only in the calibrate mode. The sequence of events in each mode is explained in the following text.

Synchronous Detector Mode

The differential input circuitry is shown in Figure 7. The value of the input capacitors should be chosen so that the pole formed by the capacitor and the 2.5 kΩ equivalent input resistance is at least an order of magnitude below the lowest input signal frequency. These input resistors have a tolerance of ±40% with a typical temperature coefficient of −300 ppm/°C. The differential inputs are biased at approximately 1 V above AGND by means of a low output impedance voltage source.

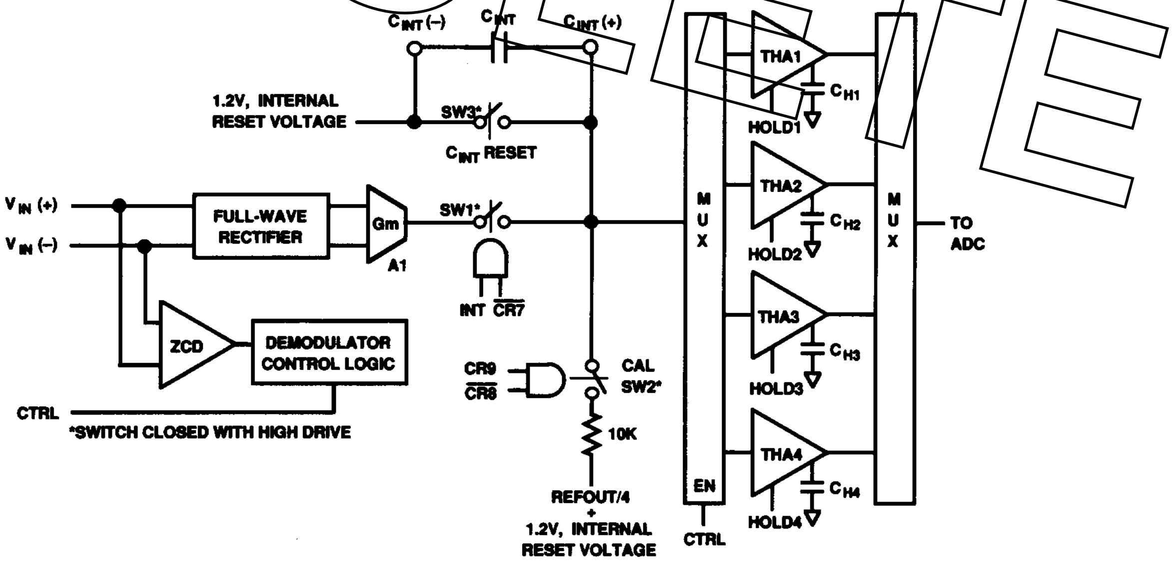


Figure 6. Simplified Block Diagram of Demodulator Channel

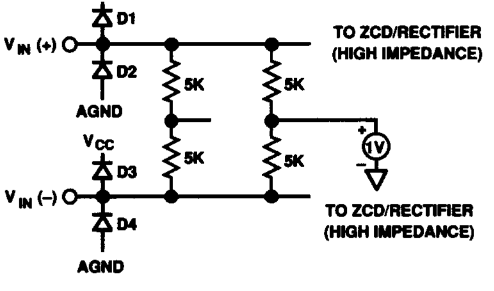


Figure 7. Simplified Input Circuitry of Demodulator Channel

From the input pins the signal passes to both a zero crossing detector (ZCD) and a full wave rectifier. The output of the rectifier drives a transconductance amplifier to convert the rectified input voltage into an output current suitable for charging the external integrating capacitor C_{INT}. Except during actual ADC conversions the ZCD is always enabled and produces a continuous pulse stream output reflecting the differential input signal transitions through 0 V. In fact, the input signal change must exceed the ZCD's input hysteresis, V_H, before its output changes. See Figure 20 in the DESIGN INFORMATION section. Since the ZCD output is usually completely asynchronous with the timing of the CTRL input, the main task of the demodulator control logic is to synchronize these two signals in order to integrate only full cycles of the input waveform. This is achieved by initializing the cycle counter logic on the first ZCD output falling edge recognized after CTRL goes high and releasing the counter on the following ZCD output falling edge. This produces the integrate (INT) signal to close switch SW1 to start integrating. Full cycles of the input waveform can now be counted from falling edge to falling edge of the ZCD output. The asynchronous nature of the two signals results in a random lock-in time before the integrator starts, which can vary from 1 cycle to 2 cycles of the input waveform. This is illustrated in Figures 8a and 8b. CTRL must be high for a minimum time of (N + 3.5) t_{CYC}; i.e., 7.5 cycles of the maximum burst frequency of 5 MHz when N = 4.

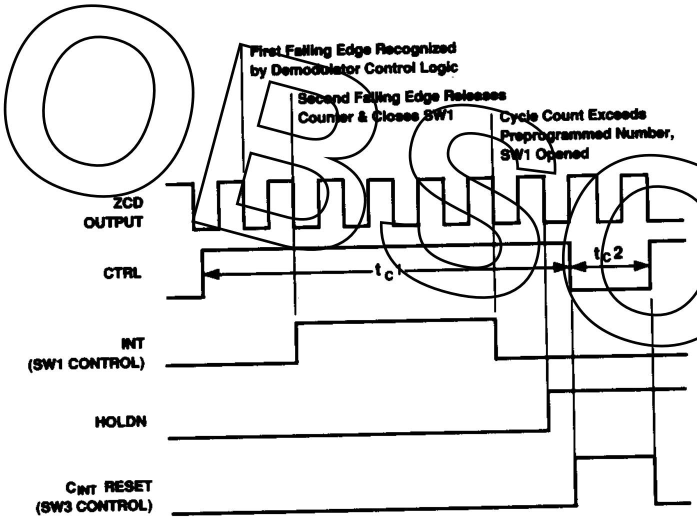


Figure 8a. Synchronous Detector Timing Waveforms with Lock-In Time of 2 Cycles & N = 4.

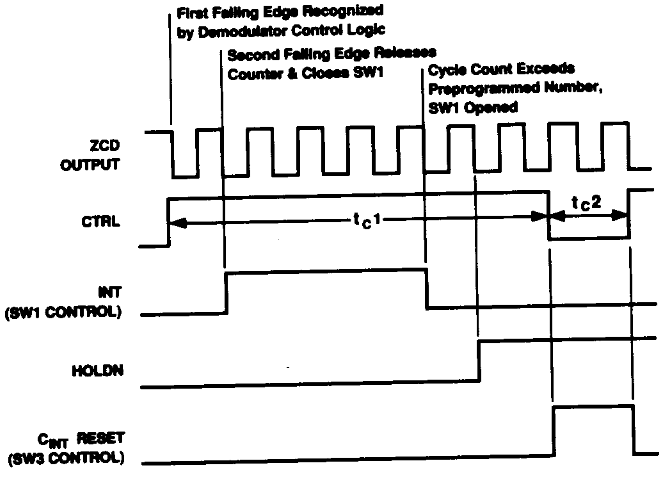


Figure 8b. Synchronous Detector Timing Waveforms with Lock-In Time of 1 Cycle & N = 4.

After the counter is released, the number of subsequent falling edges is counted and is compared with the number previously loaded into locations CR0–CR3 of the control register. When this count exceeds the preprogrammed number, the demodulator control logic brings INT Low, opening switch SW1 to halt the integrator. To ensure that the selected track/hold amplifier correctly acquires the integrated voltage on C_{INT}, a further one full cycle of the ZCD output (i.e., one full cycle of the input waveform) is counted before a hold signal, HOLD1–HOLD4, is generated.

When CTRL returns low, switch SW3 is closed to reset the voltage across the integrating capacitor to 0 V. The waveforms in Figure 8 are drawn for a correct burst capture and the status flag associated with this burst, SR1–SR4, is set "good"—a logic low—in the status register. However, there may be occasions when, for whatever reason, less than the programmed number of cycles occur in a burst, and in these circumstances the trailing edge of CTRL acts as a fail-safe hold signal for the T/H amplifier. For instance if, while capturing a burst, the signal amplitude drops below the minimum ZCD comparator threshold, then the ZCD will obviously cease providing zero-crossing pulses and invalidate the cycle counting logic. In situations like this, the trailing edge of CTRL terminates the integrator directly. If any individual burst capture is terminated by the falling edge of CTRL, then its associated status flag in the status register is set high indicating a "bad" capture. In the situation where an expected burst is so low in amplitude as not even to trigger the ZCD, switch SW1 remains open and no signal is integrated. Again, this is flagged as incorrect operation and its associated status flag is set high or "bad" on the falling edge of CTRL. In either of these cases operation of the channel proceeds normally with an A/D conversion being carried out on the incorrectly captured burst and the result stored in its respective data register.

As each differential input signal burst is captured, one of the four internal T/H amplifiers tracks the integrated signal on the C_{INT} pin. When a burst capture is complete, the tracking T/H amplifier is placed in the hold mode and the voltage on its hold capacitor remains held for subsequent A/D conversion. The selection of which T/H amplifier tracks the integrator output is determined by the contents of a write pointer. The write pointer logic ensures that the integrator output corresponding to the first burst captured is placed on C_{H1}, the integrator output corresponding to the second burst captured is placed on C_{H2} and so on. The write pointer is incremented after each CTRL pulse. Each individual burst capture operation requires its own separate CTRL pulse, i.e., if there are four bursts to be captured, four CTRL pulses are required. The number of bursts captured is compared with the number (1, 2, 3 or 4) previously loaded into locations CR4 and CR5 of the control register. When the number of bursts captured equals the preprogrammed number of bursts expected, the rectifier/integrator section is turned off, the ZCD is disabled and the voltages held on the internal hold capacitors C_{H1}–C_{H4} are sequentially applied to the ADC and are converted. As the ADC converts the held voltages, the results are loaded, again sequentially, into the data registers under the control of the write pointer. ADCREG1 is filled first, followed by ADCREG2, etc. When all held voltages have been converted, the T/H amplifiers are released back into their track mode and the write pointer is left pointing at T/H amplifier #1. At this time also, the ZCD is again enabled. Note, however, that the 4-channel T/H multiplexer is enabled on the rising edge of the first CTRL pulse in a new burst capture sequence and remains enabled only for the duration of the capture sequence.

Gated Detector Mode

In this mode the synchronous detector is bypassed and the demodulator channel behaves as a simple gated detector. To select the gated detector mode, locations CR0–CR3 of the control register are loaded with all 0s, location CR7 is loaded with a logic low and locations CR8 and CR9 are loaded with logic highs. A simplified timing diagram of the channel operating as a gated detector is shown in Figure 9. When CTRL goes high at the start of a signal capture operation, switch SW1 is closed and the integrator starts integrating the rectifier's output. It will continue to do so as long as CTRL remains high, eventually saturating if CTRL is held high for too long. A minimum CTRL high pulse width of 800 ns is required in this mode. When CTRL returns low, switch SW1 is opened and the integrator is halted. As the rectifier's output is being integrated across C_{INT}, it is also being tracked by one of the four T/H amplifiers. To provide additional time for this T/H amplifier to completely acquire the integrated voltage, the falling edge of CTRL triggers a one-shot which delays the hold signal, HOLD1–HOLD4, until it times out. This delay, t_C3, has a maximum time of 600 ns. When the hold signal is generated the tracking T/H amplifier is put in the hold mode and the voltage on its hold capacitor remains held for subsequent A/D conversion. The hold signal, in turn, triggers the C_{INT} reset signal, closing SW3 and resetting the voltage across C_{INT} to 0 V. Note that both plates of the C_{INT} capacitor are at the internal reset voltage level of 1.2 V, available on $C_{INT}(-)$, in readiness for the next signal capture operation. The minimum CTRL low time, t_C2, depends on the duration of the preceding CTRL high time. The longer the integration time, the longer must be the reset time, since the reset current is fixed. The minimum CTRL low time can be determined from the expression:

$$t_C2 = 0.6\ \mu s + 0.375\ t_C1$$

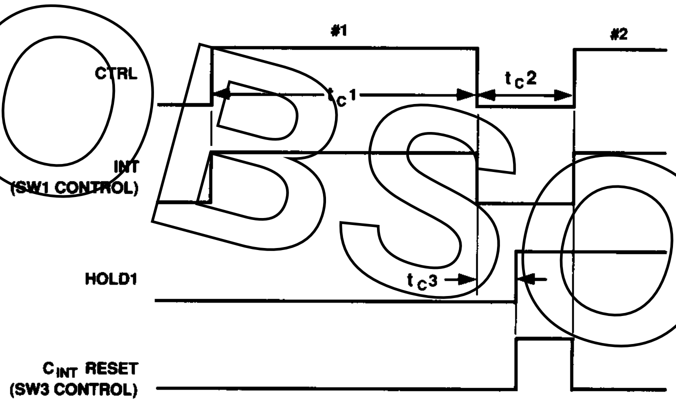


Figure 9. Channel Timing Waveforms for Gated Detector Mode

When the number of gated signals captured equals the preprogrammed number expected, the rectifier/integrator section is disabled and the held voltages are sequentially applied to the ADC and are converted. From here on, channel operation is identical to the synchronous detector mode as previously described. Note that locations SR1–SR4 of the status register now convey no meaningful information and should be ignored for gated detector operation.

Calibration Mode

The purpose of this mode is to allow any channel mismatch existing between the internal T/H amplifiers to be easily measured. The number of T/H amplifiers tested will equal the number stored in locations CR4 and CR5 of the control register. Additionally the number of CTRL pulses applied must also equal this number. The calibration (CAL) mode is selected by loading locations CR9 and CR8 of the control register with a logic high and a logic low, respectively. This condition is decoded to close switch SW2 and connect an internal dc reference, nominally REFOUT/4 above the $C_{INT}(-)$ pin, to the $C_{INT}(+)$ pin. Additionally, to avoid shorting the integrator output, switch SW1 must be opened by loading a logic high into location CR7. Unlike either the synchronous or gated detector modes, the voltage on C_{INT} is not discharged between successive CTRL pulses. In this mode the CTRL pulses simply generate the hold signals for the T/H amplifiers. The falling edge of the first CTRL pulse generates a hold signal, HOLD1, for T/H amplifier #1, the falling edge of the second CTRL pulse generates HOLD2 for T/H amplifier #2, and so on. A timing diagram of the channel in the CAL mode is shown in Figure 10.

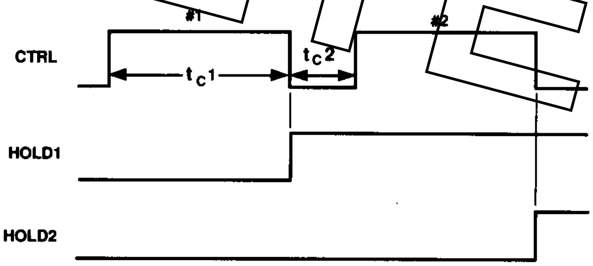


Figure 10. Channel Timing Waveforms for Calibration Mode

A minimum CTRL pulse width of 800 ns is required to allow sufficient acquisition time for the relevant T/H amplifier. Note that this pulse width assumes that the voltage on the $C_{INT}(+)$ pin has settled to the nominal REFOUT/2 level before the first CTRL pulse is applied. In order to use the minimum CTRL pulse widths the demodulator channel must be placed in the calibration mode some time prior to applying the first CTRL pulse. With C_{INT} = 200 pF, this setup time is no longer than 20 µs. Alternatively, this setup time can be avoided by making the first CTRL pulse sufficiently wide to ensure that the calibration voltage on the $C_{INT}(+)$ pin has settled. Subsequent CTRL pulses can obviously have minimum pulse widths.

Analog Outputs

The AD7773 and AD7775 contain two independent voltage-output DACs: DAC A with 10-bit resolution and DAC B with 8-bit resolution. The two DACs produce output voltages of the form $V_{BIAS} \pm V_{SWING}$. Both V_{BIAS} and V_{SWING} reference levels are generated internally with V_{BIAS} being available externally on the REFOUT pin. V_{SWING} is nominally equal to REFOUT/2. With half-scale code in a DAC register, the DAC output voltage is equal to V_{BIAS}; with a positive full-scale code the DAC output is $V_{BIAS} + V_{SWING} - 1$ LSB; with a negative full-scale code the DAC output is $V_{BIAS} - V_{SWING}$. Dependent upon the logic level stored in location CR6 of the control register, the DAC coding (for both DACs) will be either twos complement coding (CR6 = 1) or offset binary coding (CR6 = 0). Note that on receipt of a reset command (either via software or hardware), location CR6 is loaded with a logic high and the analog outputs of both DACs go to V_{BIAS}. Figures 11a and 11b show the DAC transfer functions for twos complement and offset binary coding, respectively.

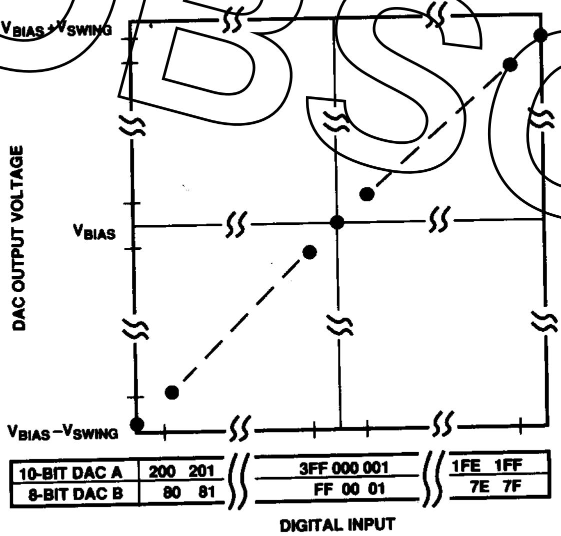


Figure 11a. DAC Output Voltages vs. DAC Input Codes in Hex—Twos Complement Coding

For twos complement coding the DAC output voltage can be expressed as:

$$V_{OUT}A/B = V_{BIAS} + V_{SWING}\,(2\,D_{A/B})$$

where subscripts A and B refer to DACs A and B.

For DAC A, $D_A = N_A/1024$

where N_A is the decimal equivalent of the twos complement input code; i.e.,

$$-512 \leq N_A \leq +511$$

For DAC B, $D_B = N_B/256$

where N_B is the decimal equivalent of the twos complement input code; i.e.,

$$-128 \leq N_B \leq +127$$

With offset binary coding selected via location CR6 of the control register, the DAC output voltage can be expressed as:

$$V_{OUT}A/B = V_{BIAS} + V_{SWING}\,(2\,D_{A/B} - 1)$$

where subscripts A and B again refer to DACs A and B.

For DAC A, $D_A = N_A/1024$

as before, where N_A is the input code in decimal; i.e.,

$$0 \leq N_A \leq +1023$$

For DAC B, $D_B = N_B/256$

as before, where N_B is the input code in decimal; i.e.,

$$0 \leq N_B \leq +255$$

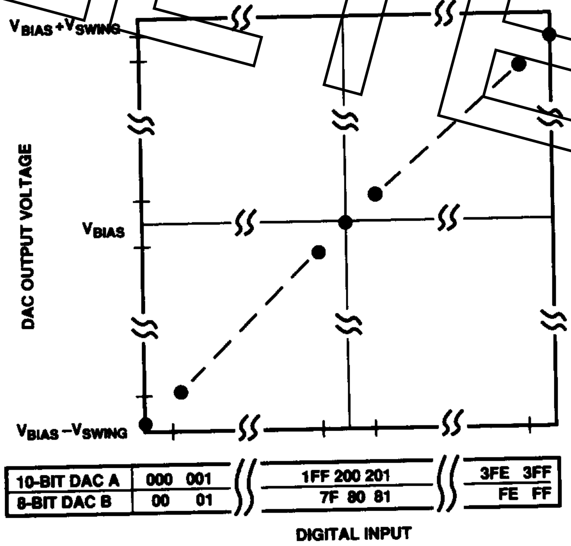


Figure 11b. DAC Output Voltages vs. DAC Input Codes in Hex—Offset Binary Coding

MICROPROCESSOR INTERFACING

Tables I and II show the truth tables for AD7773 and AD7775 microprocessor interfacing, respectively. The multiplexed address/data bus used by the AD7775 is demultiplexed internally by means of the ALE signal. On the falling edge of ALE address inputs AD1, AD2 and AD3 are latched and remain latched until ALE returns high again. Note that address input AD0 is a "don't care" input. This decoding scheme allows 2-byte word operations to even addresses only and simplifies the interface to the 80C196, for instance, where word operations to odd addresses are not guaranteed to operate in a consistent manner. DAC data is always transferred as right-justified data, i.e., the LSB should always appear on AD0 whether loading the 10-bit DAC A or 8-bit DAC B. Similarly for the AD7773, which has a dedicated 10-bit-wide data bus, DAC data is always transferred as right-justified data, i.e., the LSB should always appear on DB0 whether loading DAC A or DAC B.

Table I. AD7773 Truth Table for Microprocessor Interfacing

$\overline{\text{CS}}$	$\overline{\text{RD}}$	$\overline{\text{WR}}$	A1	A0	DB0–DB9	Functions/Comments
1	X*	X	X	X	High Z	Data Port High Impedance.
0	1	0	0	0	DAC Data	Load 10-Bit DAC A Data to DAC A Register.
0	0	1	0	0	Low Z	Reserved. Do Not Use.
0	1	0	0	1	DAC Data	Load 8-Bit DAC B Data to DAC B Register.
0	0	1	0	1	Low Z	Reserved. Do Not Use.
0	1	0	1	0	CR Data	Load Control Register (CR) Data to CR. See Control Register Description.
0	0	1	1	0	Low Z	Reserved. Do Not Use.
0	1	0	1	1	SR Data	Load Status Register (SR) Data to SR. See Status Register Description.
0	0	1	1	1	Stack Data	Contents of Stack Placed on Data Bus. See Stack Reading Description.

*X = don't care.

Table II. AD7775 Truth Table for Microprocessor Interfacing

$\overline{\text{CS}}$	$\overline{\text{RD}}$	$\overline{\text{WR}}$	AD3*	AD2*	AD1*	AD0	AD0-DB9	Function/Comments
1	X**	X	X	X	X	X	High Z	Data Port High Impedance.
0	1	0	X	0	0	X	DAC Data	Load 10-Bit DAC A Data to DAC A Register.
0	0	1	0	0	0	X	Low Z	Reserved. Do Not Use.
0	1	0	X	0	1	X	DAC Data	Load 8-Bit DAC B Data to DAC B Register.
0	0	1	0	0	1	X	Low Z	Reserved. Do Not Use.
0	1	0	X	1	0	X	CR Data	Load Control Register (CR) Data to CR. See Control Register Description.
0	0	1	0	1	0	X	Low Z	Reserved. Do Not Use.
0	1	0	X	1	1	X	SR Data	Load Status Register (SR) Data to SR. See Status Register Description.
0	0	1	0	1	1	X	Stack Data	Contents of Stack Placed on Data Bus. See Stack Reading Description.
0	0	1	1	0	0	X	ADC Data	Contents of ADCREG1 Placed on Data Bus.
0	0	1	1	0	1	X	ADC Data	Contents of ADCREG2 Placed on Data Bus.
0	0	1	1	1	0	X	ADC Data	Contents of ADCREG3 Placed on Data Bus.
0	0	1	1	1	1	X	ADC Data	Contents of ADCREG4 Placed on Data Bus.

*Latched internally on the falling edge of ALE.
**X = don't care.

Stack Reading

The register stack consists of a total of five registers: the status register and the four ADC data registers, ADCREG1–ADCREG4. The status register is the bottom-most register of the 5-deep register stack. Dependent upon the system architecture, the stack can be read in one of two ways. If the AD7773 and AD7775 are interfaced directly to a microprocessor bus then repeated read instructions to the stack address rotates the active stack locations through the data bus. One stack location is transferred per read instruction. This method of stack reading is shown in Figure 12a for the AD7773 (stack address = 11_2) and in Figure 13a for the AD7775 (stack address = $011X_2$). However, if the AD7773 or AD7775 is not directly interfaced to the microprocessor bus but comes through some peripheral controller (e.g., a proprietary gate array), then the stack can be rotated by keeping the $\overline{CS}$ input low and repeatedly pulsing the $\overline{RD}$ input. This method of stack reading is shown in Figures 12b and 13b for the AD7773 and AD7775, respectively.

For the AD7773, stack rotation is the only way in which data in the upper registers can be accessed. For the AD7775, however, the stack registers are individually addressable and the user can choose to access the data by rotating the stack, or by individually addressing the registers in any order preferred.

A read pointer ensures correct operation of the stack by setting equal the number of data registers which can be rotated and the number of bursts to be captured. The first read instruction to the register stack returns the contents of the status register. The read pointer is then incremented so that the next read operation from the stack—using the same address—returns the conversion data from ADCREG1 and so on. If n is the number of bursts to be captured (n = 1, 2, 3 or 4), then n + 1 read instructions are required to rotate the stack through all active stack registers. The stack is rotated only once with all additional read instructions repeatedly placing the contents of the status register on the data bus. Note that the stack will rotate only when the programmed number of conversions are complete; i.e., only when status register flag SR0 has returned low. When new data is loaded to the stack, for example, when a new burst sequence is captured, the read pointer is again enabled to rotate the stack registers through the data bus. Operation of the stack is summarized in Table III where all the read instructions are from stack addresses; 11_2 for the AD7773 and $011X_2$ for the AD7775.

Table III. Stack Read Operations

Read Instruction Sequence	Data Bus
1st Read	Status Register
2nd Read	ADCREG1
3rd Read	Status Register if CR (5, 4) = (0, 0); ADCREG2 otherwise
4th Read	Status Register if CR (5, 4) = (0, 0) or (0, 1); ADCREG3 otherwise
5th Read	Status Register if CR (5, 4) = (0, 0), (0, 1) or (1, 0); ADCREG4 otherwise
6th Read	Status Register. Succeeding Read instructions always call the Status Register

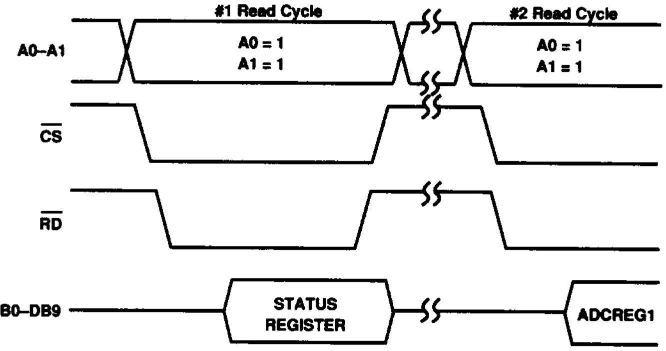


Figure 12a. AD7773 Stack Read Option 1

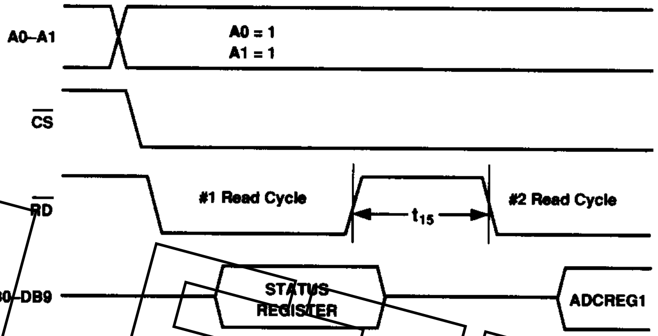


Figure 12b. AD7773 Stack Read Option 2

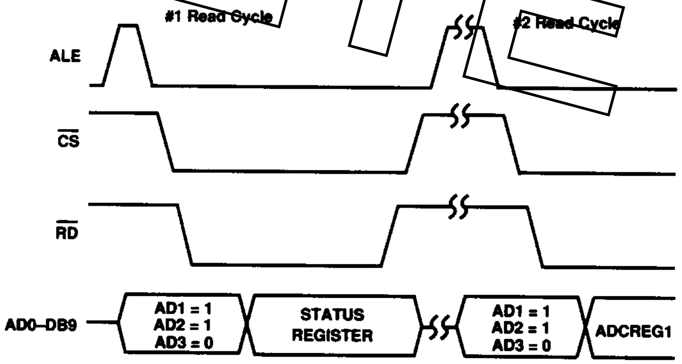


Figure 13a. AD7775 Stack Read Option 1

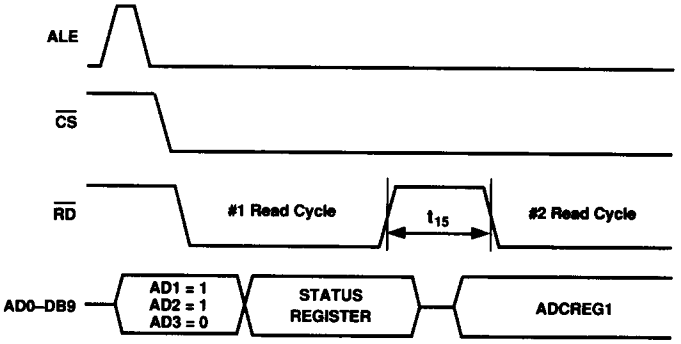


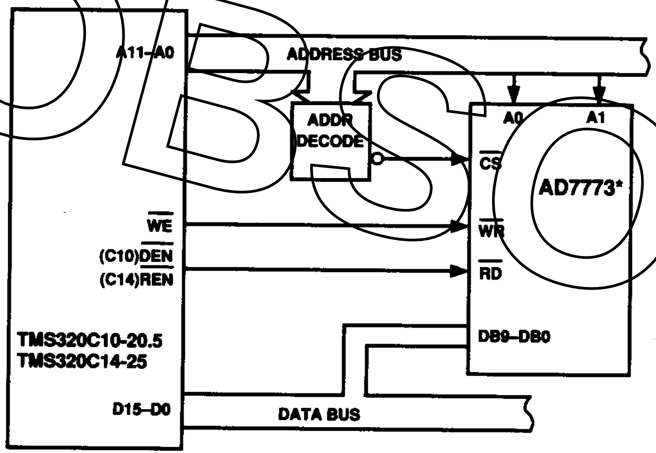
Figure 13b. AD7775 Stack Read Option 2

Microprocessor/Microcomputer Interfacing Circuits

With its separate data and address bus architecture the AD7773 is intended to interface to DSP machines such as the ADSP-2101, ADSP-2105 and the TMS320 family. The AD7775, with its multiplexed address/data bus, is suitable for microcontrollers such as the 80C196 family.

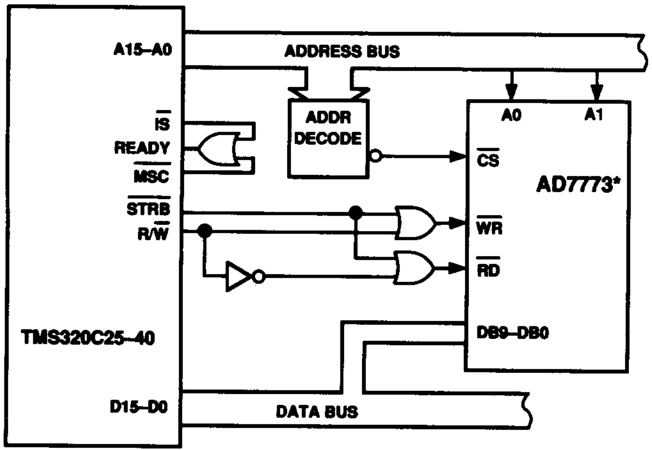
Figure 14 shows the AD7773 interfaced to the TMS320C10 @ 20.5 MHz and the TMS320C14 @ 25 MHz. Figure 15 shows the interface with the TMS320C25 @ 40 MHz. Note that one wait state is required with this interface. The ADSP-2101-50 and the ADSP-2105-40 interface is shown in Figure 16. One wait state is required with either of these machines.

Figure 17 shows the AD7775 interface to the 80C196KB @ 12 MHz and the 80C196KC @ 16 MHz. One wait state is required with the 16 MHz machine. The 80C196 is configured to operate with a 16-bit multiplexed address/data bus.



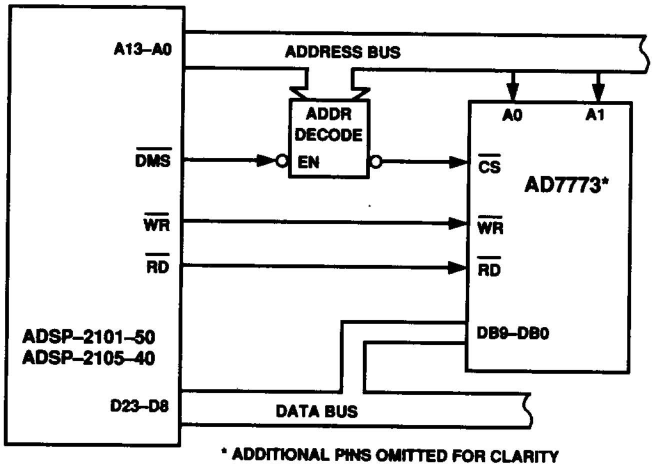
* ADDITIONAL PINS OMITTED FOR CLARITY

Figure 14. AD7773 to TMS320C10 & -C14 Interface



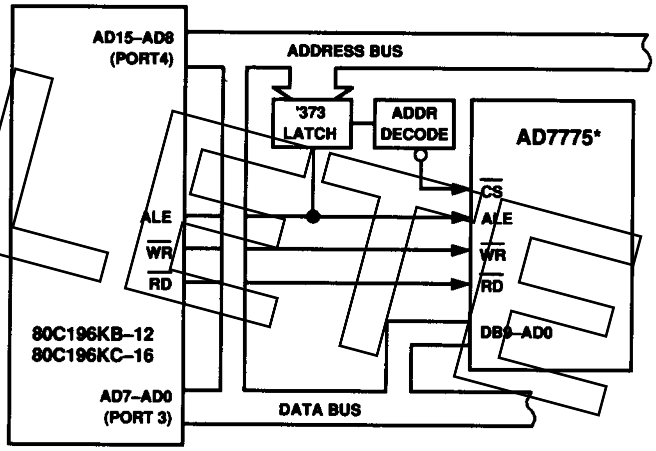
* ADDITIONAL PINS OMITTED FOR CLARITY

Figure 15. AD7773 to TMS320C25 Interface



* ADDITIONAL PINS OMITTED FOR CLARITY

Figure 16. AD7773 to ADSP-2101 & ADSP-2105 Interface



* ADDITIONAL PINS OMITTED FOR CLARITY

Figure 17. AD7775 to 80C196 Interface

DEMODULATOR CHANNEL

Relative Accuracy

The relative accuracy specification is similar to a least squares specification for a standard ADC. For the demodulator channel, however, the least squares line is fitted not between the voltage levels corresponding to the traditional first and last code transitions, but is fitted now between designated voltage limits on either side of the nominal half-scale input voltage, 1.25 V p–p differential. This scheme allows a tighter specification for signals around the half-scale point and a more relaxed specification for signals closer to zero-scale and full-scale. The AD7773/AD7775 specify linearity over the 1/4 FS to 3/4 FS signal range with a related linearity specification from 1/6 FS to 5/6 FS. For either range the ADC output codes which correspond to the designated input signal levels are found by applying a sequence of 5 MHz sinusoidal bursts to the demodulator channel and digitizing the signals. The 1/4 FS to 3/4 FS relative accuracy specification of the demodulator channel is the maximum deviation, in LSBs, of the ADC's actual code transition points from a least squares line fitted between the voltage limits of 0.625 V and 1.875 V inclusive. Note that this least squares line is of the form

$$Y = mX + c$$

where m is the gain of the channel, G_{CH}, in LSB/V p–p and c is the intercept of the transfer function on the ADC code axis, ADC_{INTCPT}, in LSBs. Values for m and c are computed after the least square line is fitted between 1/4 FS and 3/4 FS. The 1/6 FS to 5/6 FS relative accuracy specification is referred to the least squares line already fitted between 1/4 FS and 3/4 FS but which is now extended to range from 0.417 V to 2.083 V inclusive. A graphical representation of the two linearity ranges are shown in Figure 18 where ADC code transitions are plotted versus their corresponding input voltage levels; i.e., ADC_{417} represents the ADC output code for a differential input voltage of 417 mV p–p.

The LSB size is the inverse of the slope of the least squares line fitted, i.e., typically 1 LSB = 1/384 V = 2.60 mV. Note that due to both the zero-crossing detector threshold and the rectifier threshold, the least squares line shown in Figure 18 will not pass through the origin.

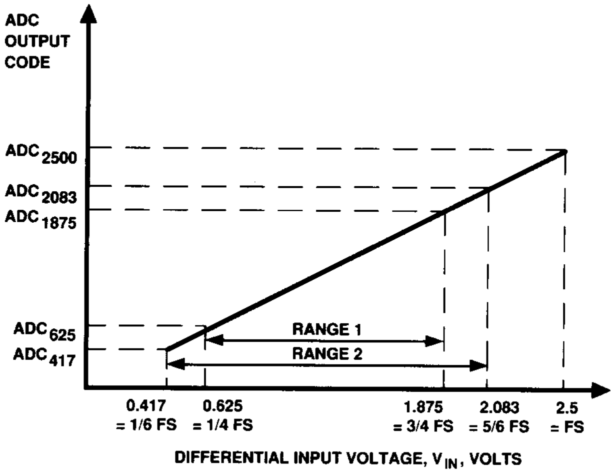


Figure 18. Guaranteed Linearity Ranges for the Demodulator Channel

Differential Input Resistance

This is the dc input resistance measured between $V_{IN}(+)$ and $V_{IN}(-)$.

Common-Mode Input Resistance

This is the dc input resistance measured between the shorted differential inputs, $V_{IN}(+)$ and $V_{IN}(-)$, and ground.

Intercept of Transfer Function on ADC Code Axis

When the least squares line fitted between 1/4 FS and 3/4 FS is extended backwards towards the origin, it will intercept the ADC code axis at some value. This value, which is called the intercept of the transfer function on the ADC code axis, is equal to the value c computed from the equation

$$Y = mX + c$$

which the least squares line adheres to. Figure 19 shows the typical demodulator performance for low level input signals. The minimum differential input signal is determined by the rectifier threshold.

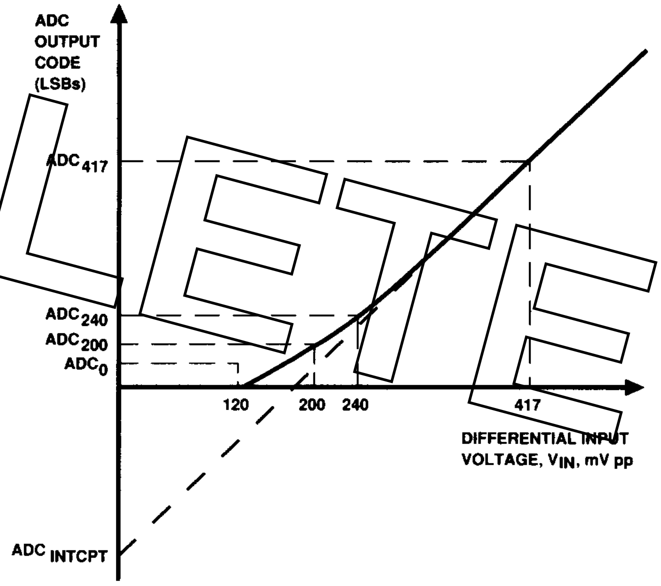


Figure 19. Demodulator Response for Low Level Input Signals

Frequency Response to Pulse Harmonics

This specification tests for gain peaking in the channel frequency response. Relative measurements, taken at three harmonically related frequencies, are compared and must be within specification. To maintain a constant integral at each frequency, the number of cycles are correspondingly increased as the signal period is decreased.

- Set up 5 MHz bursts at 0.7 V p–p and digitize. CR0–CR3 set for 4 cycles. Determine average ADC code, call it Code 1.
- Set up 10 MHz bursts at 0.7 V p–p and digitize. CR0–CR3 set for 8 cycles. Determine average ADC code, call it Code 2.
- Set up 16.25 MHz bursts at 0.7 V p–p and digitize. CR0–CR3 set for 13 cycles. Determine average ADC code, call it Code 3.
- Compare (Code 1–Code 2) and (Code 1–Code 3) to the limits specified.

Due to the demodulation technique used in the AD7773 and AD7775, the frequency spectrum of the input signal can have an impact on the demodulator channel performance. To meet the specifications the following limits are placed on the harmonic content of the input signal (quoted in dB relative to a fundamental at 5 MHz and 1.25 V p–p):

2nd Harmonic:	−50 dB
3rd Harmonic:	−12 dB
4th Harmonic:	−50 dB
5th Harmonic:	−24 dB
Higher Harmonics:	−40 dB total

Common-Mode Rejection Ratio

Common-mode rejection ratio (CMRR) is a measure of the change in digital output code when both inputs are changed by equal amounts. Repeated bursts of half-scale amplitude, differential 1.25 V p–p at 5 MHz, are applied to the demodulator channel and digitized. These bursts sit on a common-mode signal of 50 mV p–p magnitude and varying in frequency from 60 Hz to 30 kHz. The standard deviation of the resultant distribution of ADC codes is checked to be less than 3.1 LSBs, a result which includes the channel noise level. When corrected for the channel noise level by rms subtraction, e.g., $\{(3.1)^2 - (1.8)^2\}^{1/2}$, the standard deviation is found to be less than 2.5 LSBs, which is equivalent to a CMRR of 46 dB. This specification holds over the allowable V_{CC} range of 4.75 V to 5.25 V.

Power Supply Rejection Ratio

For the demodulator channel, power supply rejection ratio (PSRR) is a measure of the change in digital output code due to a change in the power supply voltage. Repeated bursts of half-scale amplitude, differential 1.25 V p–p at 5 MHz, are applied to the input and digitized. An ac signal, 50 mV p–p amplitude and varying in frequency from 60 Hz to 30 kHz, is summed with the +5 V power supply V_{CC}. The standard deviation of the resultant distribution of ADC codes is checked to be less than 5.4 LSBs, a result which includes the channel noise level. When corrected for the channel noise level by rms subtraction, e.g., $\{(5.4)^2 - (1.8)^2\}^{1/2}$, the standard deviation is found to be less than 5.1 LSBs, which is equivalent to a PSRR of 40 dB. This specification holds over the allowable V_{CC} range of 4.75 V to 5.25 V.

Channel Noise Level

Channel noise level is a measure of the intrinsic noise level of the modulator channel in the absence of common-mode signals and power supply interference. Repeated bursts of half-scale amplitude, differential 1.25 V p–p at 5 MHz, are applied to the input and digitized. The standard deviation of the resultant distribution of ADC codes is checked to be less than 1.8 LSBs. This is equivalent to a channel noise level of 49 dB. Note that the duration of the burst capture sequence must be less than or equal to 1 ms.

Composite Noise Rejection

Intended as an overall channel performance indicator, the composite noise rejection figure is an rms summation of the PSRR, CMRR, the channel noise level as defined above plus an INL error of 2.68 LSBs, representing the standard deviation, under identical test conditions, of the ADC codes from device to device. It is referenced to half-scale.

Channel Mismatch

Channel mismatch is a measure of the differences which may exist between the four internal track/hold (T/H) amplifiers. To measure mismatch the AD7773/AD7775 must be put in the calibration (CAL) mode by loading control register locations CR9 and CR8 with a logic high and a logic low, respectively. Additionally, CR7 must be loaded with a logic high. These conditions disconnect the output of the integrator from the integrating capacitor C_{INT} and connect an internal dc reference (Nominally REFOUT/4 above the voltage on the $C_{INT}(-)$ pin) to the $C_{INT}(+)$ pin. The remainder of the demodulator channel operates normally: under the control of the CTRL input, the four T/H amplifiers are connected in turn to track-and-hold this reference voltage. Subsequently the held voltages are converted. Check the ADC output code for each channel to ensure results are within 10 LSBs of each other. See under CIRCUIT DESCRIPTION for Calibration Mode section.

Crosstalk Between Bursts

Between successive bursts the integrating capacitor C_{INT} is discharged to 0 V. This occurs during time t_C2 of Figures 8a, 8b and 9. Note that both plates of the C_{INT} capacitor are at the internal reset voltage level of 1.2 V, available on $C_{INT}(-)$. Any residual signal voltage on this capacitor will be added to the integrated signal of the succeeding burst causing an apparent increase in the amplitude of that burst. The crosstalk specification defines by how much the amplitude of a burst is influenced by a preceding burst. By this definition the first burst suffers no crosstalk, the second burst suffers from the first burst, etc. To measure crosstalk a special burst sequence is applied to the demodulator input which keeps the amplitude of the burst under test constant at half-scale (differential 1.25 V p–p at 5 MHz) and alternates the amplitude of the preceding burst between 0 V and full scale. The average error due to crosstalk should be less than 5 LSB. Only two successive bursts are exercised in any one sequence.

ADC Conversion Time

Each conversion takes 14 CLKIN cycles. However, due to the asynchronous relationship between CLKIN and the burst detector operation, it is possible to get a delay of up to 2.5 CLKIN cycles before the first conversion actually starts. This means that the first conversion may not be finished for up to 14 + 2.5 CLKIN cycles after the final burst has been detected. Subsequent conversions will always take 14 CLKIN cycles. See under DESIGN INFORMATION—ADC Corruption for additional applications information.

ANALOG OUTPUTS

Relative Accuracy

For the DACs, relative accuracy or end-point nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the end points of the DAC transfer function. A graphical representation of the transfer curves for both twos complement and offset binary coding are shown in Figures 11a and 11b, respectively.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Bias Offset Error

If the DACs are ideal, the output voltage of any DAC with mid-scale code loaded will be equal to V_{BIAS} (i.e., REFOUT). The DAC bias offset error is the difference between the actual output voltage and V_{BIAS}, expressed in LSBs.

Plus and Minus Full-Scale Error

The DACs in the AD7773/AD7775 can be considered to provide bipolar output voltage ranges which are referred to V_{BIAS} instead of AGND. Plus full-scale error for any DAC is the difference, expressed in LSBs, between the actual output voltage with plus full-scale code loaded into the DAC register and the ideal output voltage ($V_{BIAS} + V_{SWING} - 1$ LSB). Minus full-scale error is similarly defined but the DACs are now loaded with their minus full-scale codes and the ideal output voltage is now $V_{BIAS} - V_{SWING}$. Note that plus and minus full-scale errors for the DAC outputs are referenced to REFOUT/2 and are measured after the bias offset errors have been adjusted out.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the digital inputs change state with the DAC selected. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed by 1 LSB at the major carry transition. Regardless of whether offset binary or 2s complement coding is used, the major carry transition occurs at the analog output voltage change of V_{BIAS} to $V_{BIAS} - 1$ LSB or vice versa.

Digital Feedthrough

Digital feedthrough is also a measure of the impulse injected into the analog output from the digital inputs but is measured when the DAC is not selected. It is essentially feedthrough across the die and package. It is important in the AD7773/AD7775 since it is a measure of the glitch impulse transferred to the analog output when data is transferred over the data bus (either in or out). It is specified in nV secs and is measured with a full-scale code change on the data bus, from all 0s to all 1s and vice versa.

Power Supply Rejection Ratio

For the analog outputs, power supply rejection ratio (PSRR) is a measure of the change in the analog output of either DAC due to a change in the power supply voltage V_{CC}. For the test both DACs are loaded with their half-scale codes and an ac signal of 200 mV p–p amplitude and varying in frequency from 60 Hz to 30 kHz is summed with the +5 V power supply. The maximum output signal level on either DAC will be 22 mV. Thus, the response will be at least 20 dB below the excitation level. This specification holds over the allowable V_{CC} range of 4.75 V to 5.25 V.

Short Circuit Current

This is defined as the maximum current which will be supplied by the DAC output pin, V_{OUT} A/B, if the pin is shorted to any potential between 0 V and V_{CC}. This condition can be allowed for up to 10 seconds provided that the power dissipation of the package is not exceeded.

DESIGN INFORMATION

Zero Crossing Detector

The zero crossing detector (ZCD) has a certain amount of hysteresis to prevent noise from getting through the input stage. The ZCD differential hysteresis, V_H, is typically 55 mV p–p and is specified to lie between 40 and 120 mV p–p. Only signals which exceed this level can change the ZCD's output. A 55 mV hysteresis represents approximately 5% of a typical 1.1 V differential input signal level to the demodulator channel. Figure 20 gives a graphical representation of the ZCD sensitivity and hysteresis.

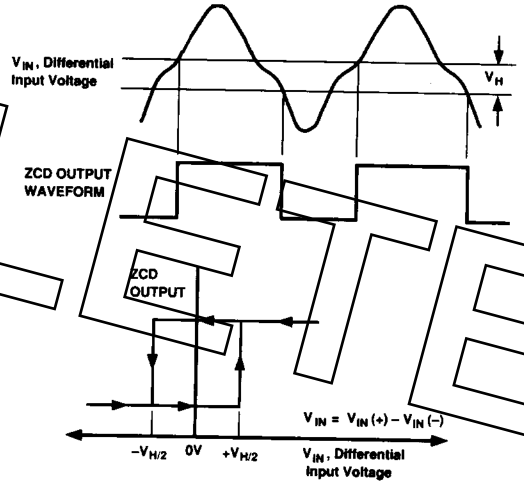


Figure 20. Zero Crossing Detector (ZCD) Sensitivity

Layout Hints

Ensure that the layout for the printed circuit board has the digital and analog grounds separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog inputs with AGND.

Establish a single-point analog ground separate from the logic system ground and as close as possible to the AD7773 or AD7775. Both AGND pins on the AD7773/AD7775 and all other signal grounds should be connected to this single-point analog ground. In turn, this star ground should be connected to the digital ground at one point only—preferably at the low impedance power supply itself.

Low impedance analog and digital power supply common returns are important for correct operation of the devices, so make the foil width for these tracks as wide as possible.

In order to ensure a low impedance +5 V power supply at the actual V_{CC} pin, it will be necessary to employ bypass capacitors from the pin itself to DGND. A 4.7 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor is sufficient.

ADC Corruption

Executing a read instruction to the AD7773/AD7775 while conversions are in progress can result in the conversion-in-progress being corrupted. This is due to transient currents which flow when the output data drivers turn on. The possibility of ADC corruption is avoided if read instructions to the AD7773/AD7775 are avoided for some time after the final CTRL pulse goes Low. The duration of this wait period should be:

$$T_{CLKIN}\ (NBursts.14 + 2.5 + 1)$$

made up from the following factors;

- N is the programmed number of bursts, 1 to 4, to be captured.
- Although each conversion takes only 14 CLKIN cycles, it can take up to 2.5 CLKIN cycles to synchronize the external clock with CTRL before any conversions start.
- A further CLKIN cycle should be allowed for location SR0 of the status register to be updated.

Synchronous Detector Timing Relationships

The relative timing between an input burst signal and its respective CTRL pulse determines which of the cycles within an individual burst are integrated. Two different timing examples which result in different cycles of the input waveform being integrated are shown in Figure 21. This is drawn for a two-burst pattern with N, the programmed number of cycles to be captured, set to 4.

In Example 1, the CTRL input goes high just after the rising edge of the ZCD output which itself occurs in the middle of the second cycle of burst 1. Approximately 3/2 cycles after this, the integrate (INT) signal goes high to start the integrator and remains high for four cycles of the input waveform. The CTRL input is maintained high for a further 2 cycles of the input waveform. With this timing relationship, cycles 4, 5, 6 and 7 of burst 1 are integrated. Since CTRL is kept low for the minimum time of 3/2 cycles of the captured input waveform, the same timing relationship between CTRL and the input signal is maintained for burst 2 and, again, cycles 4, 5, 6 and 7 are integrated.

In Example 2, the CTRL input goes high just after the falling edge of the ZCD output at the start of the first cycle of burst 1. Approximately 2 cycles later the integrate signal, INT, goes high and remains high for four cycles. CTRL is maintained high for a further 3/2 cycles before being brought low. With this timing, cycles 3, 4, 5 and 6 are integrated. The same timing relationship between CTRL and the input signal is maintained for burst 2 and, again, cycles 3, 4, 5 and 6 are integrated.

Late positioning of the CTRL input can have a similar result. For instance, in Example 1, if CTRL goes high one-half cycle later than shown, then there will be almost two full cycles delay from CTRL to INT going high. This would result in cycles 5, 6, 7 and 8 being integrated. In situations where a degree of synchronization is possible between CTRL and V_{IN}, making the rising edge of CTRL coincident with $V_{IN} = 0$ V and going positive is the optimum situation.

Changing Modes of Operation

The AD7773 and AD7775 have two normal operating modes—synchronous detector and gated detector modes – and one calibration mode. Changing between any of these modes simply requires changing the appropriate contents of the control register as already described under the individual descriptions of these modes. However, there are a number of considerations which should be followed when changing between modes. The first is that no mode change be attempted before the burst capture and conversion sequence is complete (i.e., not until location SR0 of the Status Register returns low). This will avoid any inadvertent corruption of a conversion in progress. The second consideration involves the delay between writing to the control register and starting a new burst capture sequence. This time is defined under the Demodulator Timing Characteristics as the $\overline{WR}$ rising edge to CTRL rising edge and is specified as 200 ns minimum. It is required to ensure that the correct conditions have been set up internal to the device.

A final consideration involves allowing sufficient time for the integrating capacitor, C_{INT}, to discharge when changing from the calibration mode to one of the other operating modes. This is necessary since, in this mode, C_{INT} is not discharged by the internal discharge switch, SW3, either between successive CTRL pulses or even on completion of the burst capture sequence. A discharge time of 300 ns—equivalent to $t_{c}2$, the CTRL low time in the calibration mode—is adequate after transferring out of the calibration mode. This discharge time and the previous set up time of 200 ns must be added together to arrive at a final overall delay.

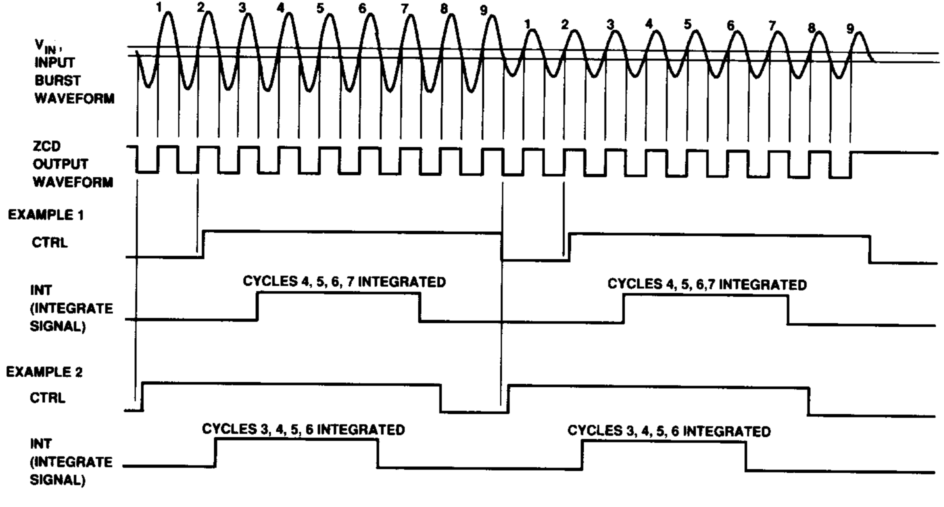


Figure 21. Two Examples of Movement of the Integration Window as a Result of Relative Timing Between CTRL and the Input Burst Signal

Choosing the C_{INT} Capacitor

In both the synchronous detector and gated detector modes the differential input signal is rectified and integrated across the integrating capacitor C_{INT}. The correct value of integrating capacitor must be used in order to optimize the channel performance for any particular integration period. If too high a value is chosen then the integrated signal voltage developed across C_{INT} will be lower than optimum, and hence, ADC resolution will be lost due to this effective compression of the signal. Similarly too low a value for C_{INT} can lead to signal voltages being developed across C_{INT} which are beyond the dynamic range of the ADC. This effective signal expansion results in loss of ADC resolution for full-scale input signals. The ideal value of C_{INT} is found from the expression:

$$C_{INT} = I \,.\, T/V_{C_{INT}} \qquad (1)$$

where I is the average rectifier output current, T is the integrate time and V_{CINT} is the integrated voltage across C_{INT}. Ideally the average rectifier current is a function only of Gm and V_{IN}, but due to the curvature of the transfer function at low input voltages (see Figure 19) an offset term must be subtracted from the peak-peak input voltage to correct for this curvature. Thus the average rectifier output current is expressed as:

$$\begin{aligned} I &= Gm \cdot V_{IN}\ (average) \qquad (2) \\ &= Gm\ [(V_{IN}\ p\text{–}p - V_{OFFSET})/2]\ (Crest\ Factor) \end{aligned}$$

For sinusoidal burst signals the crest factor is equal to $2/\pi$.

In the synchronous detector mode the integrate time can be expressed as:

$$\begin{aligned} T &= t_{INTEGRATE} \qquad (3) \\ &= N \cdot t_{CYC} \\ &= N/f_{IN} \end{aligned}$$

where N is the number programmed into locations CR0–CR3 of the control register. N can range from 4 to 15. Frequency f_{IN} is the frequency of the input signal. The AD7773 and AD7775 are guaranteed to operate with N = 4 and f_{IN} = 5 MHz maximum. In the gated detector mode the integrate time is simply the period of CTRL high or t_{C1} in Figure 9. V_{CINT} is the voltage change across C_{INT} which results in a full-scale change in the ADC output. V_{CINT} is typically equal to REFOUT/2 or 1.075 V. Tables IV and V give recommended values of C_{INT} versus input signal frequency and number of cycles. These computed values of capacitors are a combination of the actual value of capacitor used, C_{INT} (Cap), plus any stray capacitance on the C_{INT} (pin) to ground and $C_{INT}(-)$. The tolerance of C_{INT} (Cap) must also be allowed for using the tables. The most significant difference between the tables is that the values in Table IV are computed on the basis that a differential input signal of 2.5 V p–p will always result in an ADC output of 1022 LSBs or less. This in fact is how the AD7773/AD7775 is specified. Table V values are computed on the basis that a 2.5 V p–p differential signal will nominally result in an ADC output of 1022 LSBs.

Table IV. Recommended Values for C_{INT} in pF vs. Signal Frequency and Cycles for Minimum FS of 2.5 V p–p

Cycles	Input Signal Frequency, MHz 1	2	3	4	5
4	1000	500	333	250	200
5	1250	625	417	313	250
6	1500	750	500	375	300
7	1750	875	583	438	350
8	2000	1000	667	500	400
9	2250	1125	750	563	450
10	2500	1250	833	625	500
11	2750	1375	917	688	550
12	3000	1500	1000	750	600
13	3250	1625	1083	813	650
14	3500	1750	1167	875	700
15	3750	1875	1250	938	750

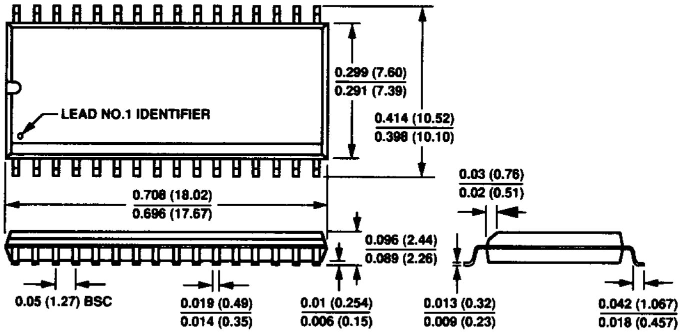
Table V. Recommended Values for C_{INT} in pF vs. Signal Frequency and Cycles for Nominal FS of 2.5 V p–p

Cycles	Input Signal Frequency, MHz 1	2	3	4	5
4	830	416	277	208	166
5	1040	520	347	260	208
6	1250	625	417	313	250
7	1455	728	485	364	291
8	1655	833	555	416	333
9	1870	935	623	468	374
10	2080	1040	693	520	416
11	2290	1145	763	573	458
12	2495	1248	832	624	499
13	2705	1353	902	676	541
14	2910	1455	970	728	582
15	3120	1560	1040	780	624

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

SOIC (R-28)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

TSOP (U-32)