QN9080-001-M17

Ultra Low-Power Bluetooth Smart 5.0 SIP

Rev. 1.0 — 5 December 2018 Objective data sheet

1. General description

The QN9080-001-M17 is a fully certified device supporting BLE and NFC. It has ultra-low power consumption, highly integrated with rich feature sets, fully FCC/CE/IC/MIC certified. The QN9080-001-M17 supports Bluetooth 5, and it is intended for ultra-small, portable connected wireless applications.

This ultra-small device is based on QN9080 die and NT3H2211 die. QN9080 is powered by an Arm® Cortex®-M4F, and has a dedicated fusion sensor co-processor (FSP) to further reduce power consumption by off-loading complex math computations to the hardware. 512 KB of on-board flash and 128 KB SRAM provide enough room and flexibility for complex applications. NT3H2211 is NFC Forum Type 2 Tag compliant IC with I2C interface, which supplies the fastest, least expensive way to add tap-and-go connectivity to just about any electronic applications.

The QN9080-001-M17 also integrates 32 MHz and 32.768 kHz crystals, a 2.4 GHz optimized antenna, and necessary components for QN9080 system to run. It offers a complete solution for applications requiring BLE wireless connectivity and fast pairing with NTAG as an option. Its low external component count reduces overall system size, complexity and shortens development time.

2. Features and benefits

- Key features:
  - Bluetooth 5.0 certified
  - Integrated antenna
  - Integrated 32 MHz and 32.768 kHz crystals
  - 32-bit Arm Cortex-M4F core at 32 MHz
  - 512 KB flash
  - 128 KB RAM
  - TX power: up to +2 dBm
  - RX sensitivity: -92.7 dBm in 1 Mbps mode and -89 dBm in 2 Mbps mode
- True single-chip Bluetooth Low Energy (v5.0) SoC solution:
  - Integrated Bluetooth LE radio, protocol stack and application profiles
  - Support central and peripherals roles
  - Support master/slave concurrency
  - Support 16 simultaneous links
  - Support secure connections
  - Support data packet length extension
  - 48-bit unique BD address
  - -92.7 dBm in 1 Mbps mode and -89 dBm in 2 Mbps mode

- TX output power from -20 dBm to +2 dBm
- Very low power consumption:
  - Single 1.67 V ~3.6 V power supply
  - 1 μA power-down mode, to wake up by GPIO
  - 2 μA power-down mode, to wake up by 32 kHz sleep timer, RTC and GPIO
  - 4 mA RX current at 3 V supply in 1 Mbps
  - Ultra Low power Bluetooth Low Energy 5.0 module
  - 3.5 mA TX current at 0 dBm TX power at 3 V supply in 1 Mbps mode
- Interface:
  - 32 General-Purpose Input/Output (GPIO) pins, with configurable pull-up/pull-down resistors
  - 8 external ADC inputs (shared with GPIO pins)
  - 2 Analog Comparator input pins (share with GPIO pins)
- Single power supply 1.67 V to 3.6 V
- Operating temperature range -40 °C to +85 °C
- 6 x9.7x1.17 mm LFLGA package

2.1 Feature of QN9080

- True single-chip Bluetooth Low Energy (v5.0) SoC solution
  - Integrated Bluetooth LE radio, protocol stack and application profiles
  - Supports central and peripherals roles
  - Supports master/slave concurrency
  - Supports 16 simultaneous links
  - Supports secure connections
  - Supports data packet length extension
  - Wifi/Bluetooth LE coexistence interface
  - 48-bit unique bluetooth device address
- RF
  - Fast and reliable RSSI in 1 dB step
  - TX output power from –20 dBm to 2 dBm
  - Single-ended RF port with integrated balun
  - Generic FSK modulation with programmed data rate from 250 Kbps to 2 Mbps
  - Compatible with worldwide radio frequency regulations
- Very low power consumption
  - Single 1.67 V to 3.6 V power supply
  - Integrated DC-to-DC buck converter and LDO
  - 1.0 μA power-down 1 mode, to wake up by GPIO
  - 2.5 μA power-down 0 mode, to wake up by 32 kHz sleep timer, RTC and GPIO
  - 3.5 mA RX current with DC-to-DC convertor enabled at 3 V supply in 1Mbps mode
  - 4 mA TX current at 0 dBm TX power with DC-to-DC converter enabled at 3 V supply in 1 Mbps mode
- Arm Cortex-M4 core (version r0p1)
  - Arm Cortex-M4 processor, running at a frequency of up to 32 MHz
  - Floating Point Unit (FPU) and Memory Protection Unit (MPU)

- Arm Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC)
- Serial Wire Debug (SWD) with six instruction breakpoints, two literal comparators, and four watch points, including serial wire output for enhanced debug capabilities
- System tick timer

- On-chip memory
  - 512 KB on-chip flash program memory and 2 KB page erase and write
  - 128 KB SRAM
  - 256 KB ROM
- ROM API support
  - Flash In-System Programming (ISP)
- Serial interfaces
  - Four Flexcomm serial peripherals
  - USART protocol supported by Flexcomm0, USART and I^2C by Flexcomm1, SPI and I2C by Flexcomm2, and SPI by Flexcomm3
  - Each Flexcomm includes a FIFO
  - I^2C-bus interfaces support fast mode and with multiple address recognition and monitor mode
  - USB 2.0 (full speed) device interface
  - Two quadrature decoders
  - SPI Flash Interface (SPIFI) uses a SPI bus superset with four data lines to access off-chip quad SPI flash memory at a much higher rate than is possible using standard SPI or SSP interfaces
  - Supports SPI memories with 1 or 4 data lines
- Digital peripherals
  - DMA controller with 20 channels, able to access memories and DMA capable peripherals
  - Up to 35 General Purpose Input Output (GPIO) pins, with configurable pull-up or pull-down resistors
  - GPIO registers are located on the AHB for fast access
  - 32 GPIOs can be selected as Pin INTerrupts (PINT), triggered by rising, or falling input edges
  - AES-128 security coprocessor
  - Random Number Generator (RNG)
  - CRC engine
  - Fusion Signal Processor (FSP) for data fusion and machine learning algorithms resulting in low power consumption compared to software processing

- Analog peripherals
  - 16-bit ADC with 8 external input channels, with sample rates of up to 32k sample per second, and with multiple internal and external trigger inputs
  - Integrated temperature sensor, connected to one internal dedicated ADC channel
  - Integrated battery monitor connected to one internal dedicated ADC channel
  - General-purpose 8-bit 1M sample per second DAC
  - Integrated capacitive sense up to 8 channels, able to wake up the MCU from low power states.
  - Two ultra low-power analog comparators, able to wake up the MCU from low power states.
- Timers
  - Four 32-bit general-purpose timers or counters, support capture inputs and compare outputs, PWM mode, and external count input
  - Sleep timer, which can work in power-down mode and wake up MCU
  - 32-bit Real Time Clock (RTC) with 1 second resolution running in the always-on power domain; can be used for wake-up from all low power modes including power-down
  - Watchdog Timer.
  - SC Timer or PWM.
- Clock generation
  - 32 MHz internal RC oscillator, which can be used as a system clock
  - 16 MHz or 32 MHz crystal oscillator, which can be used as a system and RF reference
  - 32 kHz on-chip RC oscillator
  - 32.768 kHz crystal oscillator
- Power control
  - Programmable Power Management Unit (PMU) to minimize power consumption
  - Reduced power modes: sleep, and power-down
  - Power-On Reset (POR)
  - Brown-Out Detection (BOD) with separate thresholds for interrupt and forced reset
- Single power supply 1.67 V to 3.6 V
- Operating temperature range −40 °C to +85 °C

See **QN908x data sheet** for more details.

2.2 Features of NTAG

- Interoperability
  - ISO/IEC 14443 Part 2 and 3 compliant
  - NTAG I2C plus development board is certified as NFC Forum Type 2 Tag (Certification ID: 58514)
  - Unique 7-byte UID
  - GET_VERSION command for easy identification of chip type and supported features
  - Input capacitance of 50 pF
- Host interface
  - I^2C slave

- Configurable event detection pin to signal NFC or pass-through data events
- Memory
  - 1912 bytes of EEPROM-based user memory
  - 64 bytes SRAM buffer for transfer of data between NFC and I^2C interfaces with memory mirror or pass-through mode
  - Clear arbitration between NFC and I^2C memory access
- Data transfer
  - Pass-through mode with 64-byte SRAM buffer
  - FAST_WRITE and FAST_READ NFC commands for higher data throughput
- Security and memory-access management
  - Full, read-only, or no memory access from NFC interface, based on 32-bit password
  - Full, read-only, or no memory access from I^2C interface
  - NFC silence feature to disable the NFC interface
  - Originality signature based on Elliptic Curve Cryptography (ECC) for simple, genuine authentication
- Power Management
  - Configurable field-detection output signal for data-transfer synchronization and device wake-up
  - Energy harvesting from NFC field, so as to power external devices (e.g. connected microcontroller)

See **NT3H2111_2211 Product Data Sheet** for more details.

2.3 Features of integrated 2.4 GHz antenna

- Monolithic SMD with small, low-profile and light-weight type.
- Wide bandwidth
- RoHS compliant

Note: When NFC function is required, the NFC tag antenna need to be connected externally.

3. Applications

- Health and medical devices
- Sports and fitness trackers
- Building and home automation
- Retail and advertising beacons

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
QN9080-001-M17	LFLGA54	SIP module in LGA package; body 6 × 9.7 × 1.17 mm	SOT1910 AA1

Table 2. Ordering options

Type number	Package number	Flash (KB)	Total SRAM (KB)	Cortex-M4 with FPU	FSP	USB FS	GPIO
QN9080-001-M17	3322 960 18570	512	128	1	1	1	32

5. Marking

Fig 1. QN9080-001-M17 package marking

Table 3. Marking codes

Line number	Content	Descriptions
1	NXP	Logo
2	QN9080-1-M17	Product identifier
3	XXXXX	STR number request. It will be removed on production
4	XXXXXXXXXXXX	QN batch number
5	E	TSMC
	t	ASE-K
	D	RoHS indicator (Dark green)
	YY	year; last two digits of year code of assembly
	WW	week code of assembly
	X	mask version
	X	for SIP before CQS; it will be removed after

QN9080-001-M17 has the following top-side marking:

Table 4. Device revision table

Revision identifier (R)	Revision description
001	Initial SIP module revision

QN9080-001-M17 device has received FCC "Modular Approval", in compliance with CFR 47 FCC part 15 regulations and in accordance to FCC public notice DA00-1407. The modular approvals notice and test reports are available on request.

Remark: FCC, IC & Japan ID are not mentioned on the package due to the small device size.

6. Block diagram

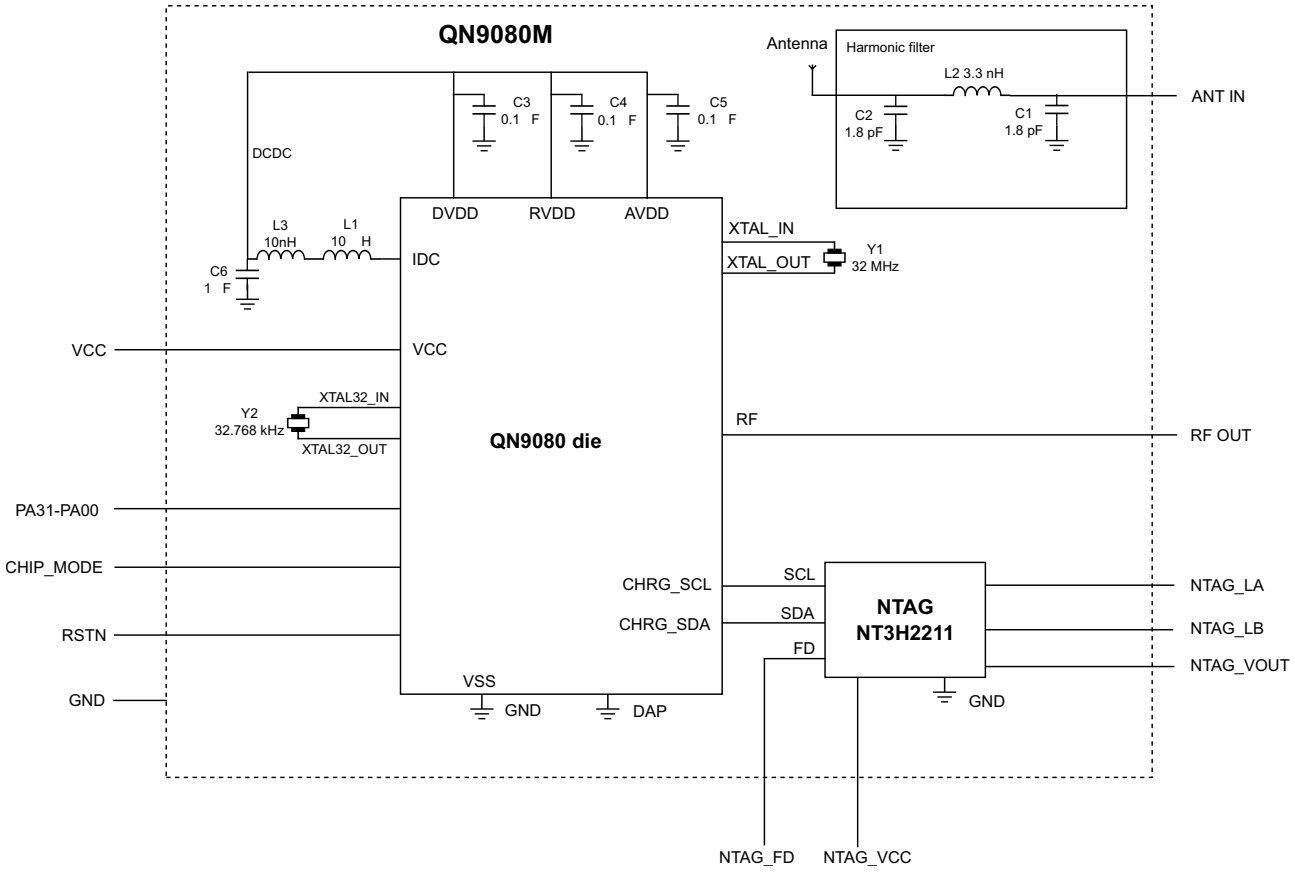


Fig 2. QN9080-001-M17 – high level HW block diagram

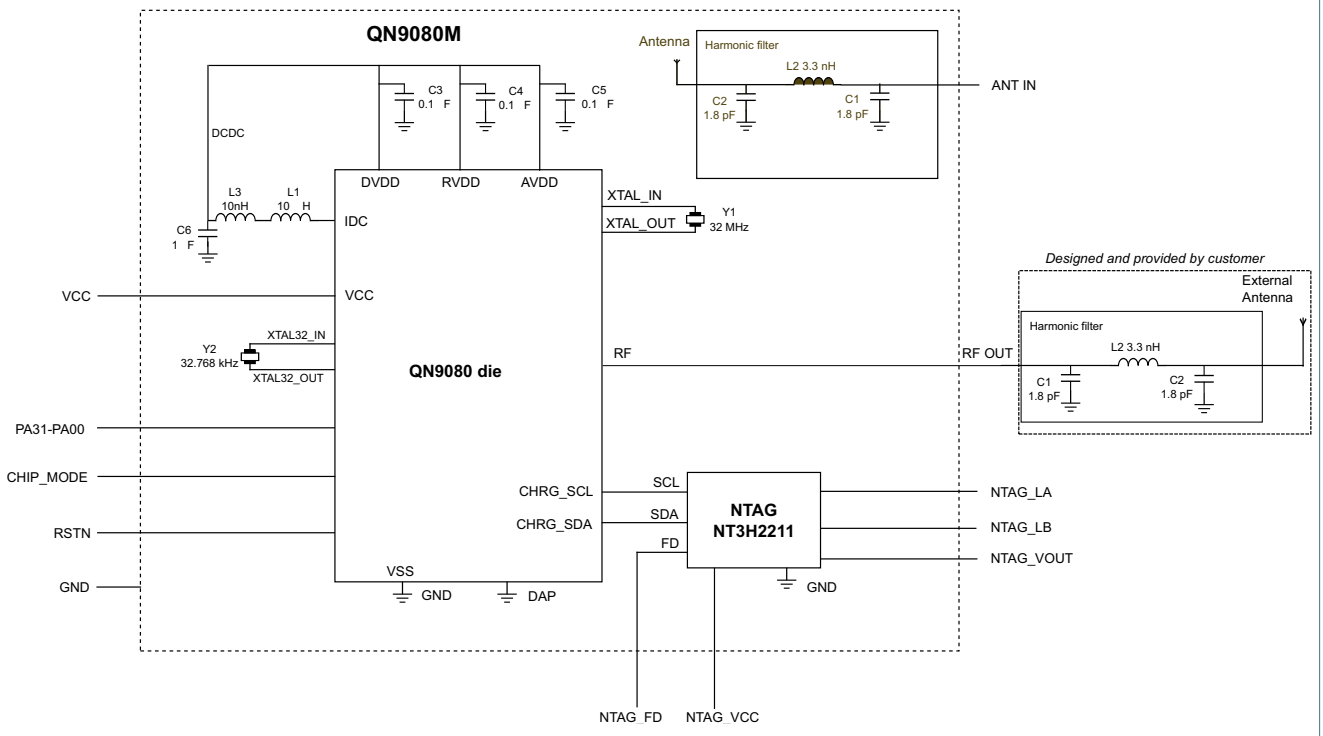


Fig 3. QN9080-001-M17 block diagram using external antenna

Remark: (1) QN9080-001-M17 is not certified with external antenna but only with its internal antenna. Customer using external antenna has to do new certification. (2) Harmonic filter is in adequacy with board.

7. Pinning information

7.1 Pinning

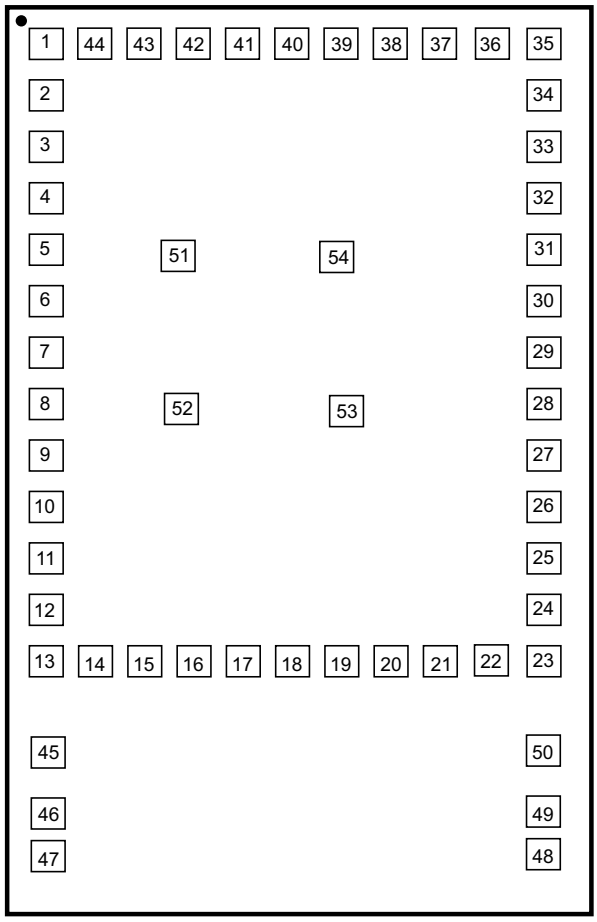


Fig 4. QN9080-001-M17 pinout diagram

7.2 Pin description

Table 5. Pin description

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA30	1	PU	GPIOA30	I/O	general-purpose digital input output pin
			ACMP1P	AI	analog comparator 1 positive input
			ETM_TRACEDAT3	O	ETM trace data output bit 3
			CTIMER3_MAT1	O	timer 3 match output 1
			FC2_SCK	I/O	flexcomm 2: SPI clock
			FC3_MOSI	I/O	flexcomm 3: SPI MOSI
			SPIFI_IO3	I/O	data bit 3 for the SPI flash interface

Table 5. Pin description *...continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA29	2	PU	GPIOA29	I/O	general-purpose digital input output pin
			ACMP1N	AI	analog comparator 1 negative input
			ETM_TRACEDAT2	O	ETM trace data output bit 2
			CTIMER3_MAT0	O	timer 3 match output 0
			FC2_SCK	I/O	flexcomm 2: SPI clock
			FC3_MISO	I/O	flexcomm 3: SPI MISO
			SPIFI_IO2	I/O	data bit 2 for the SPI flash interface
PA28	3	PU	GPIOA28	I/O	general-purpose digital input output pin
			CLK_AHB	O	AHB clock output
			ETM_TRACECLK	O	ETM trace clock output
			RTC_CAP	I	RTC capture input
			FC1_SCK	I/O	flexcomm 1: USART clock
			SD_DAC	O	sigma-delta modulator DAC output
			SPIFI_CSN	O	active low chip select output for the SPI flash interface
PA27	4	PU	GPIOA27	I/O	general-purpose digital input output pin
			USB_DM	I/O	USB0 bidirectional D- line
			SCT0_IN1	I	SCTimer input 1
			CTIMER1_MAT2	O	32-bit CTimer 1 match output 2
			FC2_SCL_MISO	I/O	flexcomm 2: I2C SCL, SPI MISO
			QDEC0_B	I	quadrature decoder 0 input channel B
			BLE_IN_PROC	O	BLE event in process indicator for coexistence
PA26	5	PU	GPIOA26	I/O	general-purpose digital input output pin
			USB_DP	I/O	USB0 bidirectional D+ line
			SCT0_IN0	I	SCTimer input 0
			CTIMER1_MAT0	O	32-bit CTimer 1 match output 0
			FC2_SDA_MOSI	I/O	flexcomm 2: I2C SDA, SPI MOSI
			QDEC0_A	I	quadrature decoder 0 input channel A
			BLE_SYNC	O	BLE sync pulse
LB	6	—	—	RF	NTAG antenna/coil terminal B
LA	7	—	—	RF	NTAG antenna/coil terminal A
PA25	8	PU	GPIOA25	I/O	general-purpose digital input output pin
			ACMP0P/CS7	AI	analog comparator 0 positive input, or capacitive touch sense button input 7
			ETM_TRACEDAT1	O	ETM trace data output bit 1
			CTIMER3_CAP1	I	timer 3 input capture 1
			RFE_TX_EN	O	TX enable for external RF front-end
			FC3_SSEL0	I/O	flexcomm 3: SPI SSEL0
			SPIFI_IO1	I/O	data bit 1 for the SPI flash interface

Table 5. Pin description *…continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA24	9	PU	GPIOA24	I/O	general-purpose digital input output pin
			ACMP0N/CS6	AI	analog comparator 0 negative input, or capacitive touch sense button input 6
			ETM_TRACEDAT0	O	ETM trace data output bit 0
			CTIMER3_CAP0	I	timer 3 input capture 0
			RFE_RX_EN	O	RX enable for external RF front-end
			FC3_SSEL1	I/O	flexcomm 3: SPI SSEL1
			SPIFI_IO0	I/O	data bit 0 for the SPI flash interface
SWDIO/ PA23	10	PU	SWDIO	I/O	serial wire debug I/O; it is the default function after booting
			GPIOA23	I/O	general-purpose digital input output pin
			SCT0_IN3	I	SCTimer input 3
			CTIMER3_MAT1	O	32-bit CTimer 3 match output 1
			FC2_SCL_SSEL1	I/O	flexcomm 2: I2C SCL, SPI SSEL1
			FC3_SSEL2	I/O	flexcomm 3: SPI SSEL2
			QDEC1_B	I	quadrature decoder 1 input channel B
SWCLK /PA22	11	PU	SWCLK	I/O	serial wire clock; it is the default function after reset
			GPIOA22	I/O	general-purpose digital input output pin
			SCT0_IN2	I	SCTimer input 2
			CTIMER3_MAT0	O	32-bit CTimer 3 match output 0
			FC2_SDA_SSEL0	I/O	flexcomm 2: I2C SDA, SPI SSEL0
			FC3_SSEL3	I/O	flexcomm 3: SPI SSEL3
			QDEC1_A	I	quadrature decoder 1 input channel A
PA21	12	PU	GPIOA21	I/O	general-purpose digital input output pin
			QDEC1_B	I	quadrature decoder 1 input channel B
			SCT0_OUT0	O	SCTimer output 0, PWM output 0
			CTIMER2_MAT1	O	32-bit CTimer 2 match output 1
			FC2_SSEL3	I/O	flexcomm 2: SPI SSEL3
			FC1_CTS_SDA	I/O	flexcomm 1: USART CTS, I2C SDA
			SPIFI_CSN	O	active low chip select output for the SPI flash interface
PA20	13	PU	GPIOA20	I/O	general-purpose digital input output pin
			QDEC1_A	I	quadrature decoder 1 input channel A
			SCT0_OUT1	O	SCTimer output 1, PWM output 1
			CTIMER2_MAT0	O	32-bit CTimer 2 match output 0
			SWO	I/O	serial wire trace output
			FC1_RTS_SCL	I/O	flexcomm 1: USART RTS, I2C SCL
			SPIFI_CLK	O	clock output for the SPI flash interface

Table 5. Pin description *…continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA19	14	PU	GPIOA19	I/O	general-purpose digital input output pin
			CS5	AI	capacitive touch sense button input 5
			SCT0_OUT2	O	SCTimer output 2, PWM output 2
			RFE_EN	O	enable for external RF front-end
			FC0_SCK	I/O	flexcomm 0: USART clock
			FC3_SSEL3	I/O	flexcomm 3: SPI SSEL3
			BLE_IN_PROC	O	BLE event in process indicator for coexistence
PA18	15	PU	GPIOA18	I/O	general-purpose digital input output pin
			CS4	AI	capacitive touch sense button input 4
			SCT0_OUT3	O	SCTimer output 3, PWM output 3
			CTIMER2_MAT2	O	32-bit CTimer 2 match output 2
			FC0_SCK	I/O	flexcomm 0: USART clock
			FC3_SSEL2	I/O	flexcomm 3: SPI SSEL2
			BLE_SYNC	O	BLE sync pulse
PA17	16	PU	GPIOA17	I/O	general-purpose digital input output pin
			CS3	AI	capacitive touch sense button input 3
			SD_DAC	O	sigma-delta modulator DAC output
			CTIMER2_MAT1	O	32-bit CTimer 2 match output 1
			FC0_RXD	I/O	flexcomm 0: USART RXD
			FC3_MISO	I/O	flexcomm 3: SPI MISO
			QDEC0_B	I	quadrature decoder 0 input channel B
PA16	17	PU	GPIOA16	I/O	general-purpose digital input output pin
			CS2	AI	capacitive touch sense button input 2
			SCT0_OUT1	O	SCTimer output 1, PWM output 1
			CTIMER2_MAT0	O	32-bit CTimer 2 match output 0
			FC0_TXD	I/O	flexcomm 0: USART TXD
			FC3_MOSI	I/O	flexcomm 3: SPI MOSI
			QDEC0_A	I	quadrature decoder 0 input channel A
PA15	18	PU	GPIOA15	I/O	general-purpose digital input output pin
			CS1	AI	capacitive touch sense button input 1
			SCT0_OUT0	O	SCTimer output 0, PWM output 0
			CTIMER2_CAP1	I	timer 2 input capture 1
			FC0_CTS	I/O	flexcomm 0: USART CTS
			FC3_SCK	I/O	flexcomm 3: SPI clock
			QDEC1_B	I	quadrature decoder 1 input channel B

Table 5. Pin description *…continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA14	19	PU	GPIOA14	I/O	general-purpose digital input output pin
			CS0	AI	capacitive touch sense button input 0
			ANT_SW	O	external antenna switch for diversity
			CTIMER2_CAP0	I	timer 2 input capture 0
			FC0_RTS	I/O	flexcomm 0: USART RTS
			FC3_SSEL0	I/O	flexcomm 3: SPI SSEL0
			QDEC1_A	I	quadrature decoder 1 input channel A
PA13	20	PU	GPIOA13	I/O	general-purpose digital input output pin
			R	I/O	reserved
			SCT0_OUT4	O	SCTimer output 4
			ACMP1_OUT	O	analog comparator 1 output
			FC1_RXD_SDA	I/O	flexcomm 1: USART RXD, I2C SDA
			FC3_SSEL1	I/O	flexcomm 3: SPI SSEL1
			RFE_EN	O	enable for external RF front-end
CHIP_MODE/PB02	21	PU	CHIP_MODE	I	boot selection with pull-up by default; it should be pulled low to go through the normal ISP process for firmware programming, otherwise the ISP process is escaped to jump to flash
			GPIOB02	I/O	general-purpose digital input output pin
			ANT_SW	O	external antenna switch for diversity
RSTN	22	PU	—	I	active low reset input
ANT_IN	23	—	—	RF	Internal antenna
RF_OUT	24	—	—	RF	RF input output port with Tx or Rx switch integrated on chip
GND	25	—	—		ground
PA12	26	PU	GPIOA12	I/O	general-purpose digital input output pin
			R	O	reserved
			SCT0_OUT5	O	SCTimer output 5
			ACMP0_OUT	O	analog comparator 0 output
			FC1_TXD_SCL	I/O	flexcomm 1: USART TXD, I2C SCL
			SD_DAC	O	sigma-delta modulator DAC output
			ANT_SW	O	external antenna switch for diversity
PA11	27	PU	GPIOA11	I/O	general-purpose digital input output pin
			ADC7	AI	ADC external input 7
			SCT0_IN3	I	SCTimer input 3
			CTIMER1_MAT2	O	32-bit CTimer 1 match output 2
			FC2_SSEL2	I/O	flexcomm 2: SPI SSEL2
			ACMP1_OUT	O	analog comparator 1 output
			BLE_RX	O	BLE reception indicator for coexistence

Table 5. Pin description *…continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA10	28	PU	GPIOA10	I/O	general-purpose digital input output pin
			ADC6	AI	ADC external input 6
			SCT0_IN2	I	SCTimer input 2
			CTIMER1_MAT1	O	32-bit CTimer 1 match output 1
			FC1_SCK	I/O	flexcomm 1: USART clock
			ACMP0_OUT	O	analog comparator 0 output
			BLE_TX	O	BLE transmit indicator for coexistence
PA09	29	PU	GPIOA9	I/O	general-purpose digital input output pin
			ADC5	AI	ADC external input 5
			SCT0_IN1	I	SCTimer input 1
			CTIMER1_MAT0	O	32-bit CTimer 1 match output 0
			FC1_RXD_SDA	I/O	flexcomm 1: USART RXD, I2C SDA
			BLE_PTI3	O	BLE packet traffic information bit 3
			SPIFI_IO3	I/O	data bit 3 for the SPI flash interface
PA08	30	PU	GPIOA8	I/O	general-purpose digital input output pin
			ADC4	AI	ADC external input 4
			SCT0_IN0	I	SCTimer input 0
			CTIMER1_CAP1	I	timer 1 input capture 1
			FC1_TXD_SCL	I/O	flexcomm 1: USART TXD, I2C SCL
			BLE_PTI2	O	BLE packet traffic information 2
			SPIFI_IO2	I/O	data bit 2 for the SPI flash interface
PA07	31	PU	GPIOA7	I/O	general-purpose digital input output pin
			ADC_VREFI	AI	ADC external reference voltage input
			SCT0_OUT2	O	SCTimer output 2
			CTIMER1_CAP0	I	timer 1 input capture 0
			FC1_CTS_SDA	I/O	flexcomm 1: USART CTS, I2C SDA
			BLE_PTI1	O	BLE packet traffic information 1
			SPIFI_CSN	O	active low chip select output for the SPI flash interface
PA06	32	PU	GPIOA6	I/O	general-purpose digital input output pin
			ADC_EX_CAP	A	connected with ADC external capacitor
			SCT0_OUT3	O	SCTimer output 3
			CTIMER0_MAT2	O	32-bit CTimer 0 match output 2
			FC1_RTS_SCL	I/O	flexcomm 1: USART RTS, I2C SCL
			BLE_PTI0	O	BLE packet traffic information bit 0
			SPIFI_CLK	O	clock output for the SPI flash interface

Table 5. Pin description *...continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA05	33	PU	GPIOA5	I/O	general-purpose digital input output pin
			ADC3	AI	ADC external input 3
			SCT0_OUT5	O	SCTimer output 5
			CTIMER0_MAT1	O	32-bit CTimer 0 match output 1
			FC0_RXD	I/O	flexcomm 0: USART RXD
			FC2_SCL_MISO	I/O	flexcomm 2: SCL, SPI MISO
			SPIF_IO1	I/O	data bit 1 for the SPI flash interface
PA04	34	PU	GPIOA4	I/O	general-purpose digital input output pin
			ADC2	AI	ADC external input 2
			SCT0_OUT4	O	SCTimer output 4
			CTIMER0_MAT0	O	32-bit CTimer 0 match output 0
			FC0_TXD	I/O	flexcomm 0: USART TXD
			FC2_SDA_MOSI	I/O	flexcomm 2: I2C SDA, SPI MOSI
			SPIF_IO0	I/O	data bit 0 for the SPI flash interface
PA03	35	PU	GPIOA3	I/O	general-purpose digital input output pin
			QDEC0_B	I	quadrature decoder 0 input channel B
			SCT0_OUT3	O	SCTimer output 3
			CTIMER0_MAT1	O	32-bit CTimer 0 match output 1
			R	O	reserved
			FC2_SDA_SSEL0	I/O	flexcomm 2: I2C SDA, SPI SSEL0
			RFE_TX_EN	O	TX enable for external RF front-end
PA02	36	PU	GPIOA2	I/O	general-purpose digital input output pin
			QDEC0_A	I	quadrature decoder 0 input channel A
			SCT0_OUT2	O	SCTimer output 2
			CTIMER0_MAT0	O	32-bit CTimer 0 match output 0
			R	I/O	reserved
			FC2_SCL_SSEL1	I/O	flexcomm 2: I2C SCL, SPI SSEL1
			RFE_RX_EN	O	RX enable for external RF front-end
NTAG_FD	37	—	—	O	field detection
VCC	38	—	—	—	power supply
NTAG_VCC	39	—	—	—	NTAG power supply
VOUT	40	—	—	—	output supply voltage(energy harvesting)
VSS1	41	—	—	—	ground

Table 5. Pin description *...continued*

Symbol	LFLGA54	Reset state[1]	Alternate function	Type	Description
PA01	42	PU	GPIOA1	I/O	general-purpose digital input output pin
			ADC1	AI	ADC external input 1
			SCT0_OUT1	O	SCTimer output 1
			CTIMER0_CAP1	I	32-bit CTimer 0 capture input 1
			FC0_CTS	I/O	flexcomm 0: USART CTS
			FC2_SSEL2	I/O	flexcomm 2: SPI SSEL2
			WLAN_RX	I	WLAN active high RX active indicator for coexistence
PA00	43	PU	GPIOA0	I/O	general-purpose digital input output pin
			ADC0	AI	ADC external input 0
			SCT0_OUT0	O	SCTimer output 0
			CTIMER0_CAP0	I	32-bit CTimer 0 capture input 0
			FC0_RTS	I/O	flexcomm 0: USART RTS
			FC2_SSEL3	I/O	flexcomm 2: SPI SSEL3
			WLAN_TX	I	WLAN active high TX active indicator for coexistence
PA31	44	PU	GPIOA31	I/O	general-purpose digital input output pin
			DAC	AO	DAC analog output
			RTC_CAP	I	RTC capture input
			CTIMER3_MAT2	O	Timer 3 match output 2
			SWO	I/O	serial wire trace output
			FC3_SCK	I/O	flexcomm 3: SPI clock
			SPIFI_CLK	O	clock output for the SPI flash interface
GND	45	—	—	—	ground
GND	46	—	—	—	ground
GND	47	—	—	—	ground
ANT_Pin3	48	—	—	—	Internal antenna ground
ANT_Pin2	49	—	—	—	Internal antenna ground
ANT_Pin1	50	—	—	—	Internal antenna ground
GND	51	—	—	—	ground
GND	52	—	—	—	ground
GND	53	—	—	—	ground
GND	54	—	—	—	ground

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{CC}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, AO = analog output, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation.

7.2.1 Termination of unused pins

Table 6 shows how to terminate pins that are not used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 6. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
RSTN	I; PU	the RSTN pin can be left unconnected if the application does not use it.
all PAnm	I; PU	can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software
CHIP_MODE	I; PU	can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up enabled.

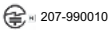
7.2.2 Pin states in different power modes

Table 7. Pin states in different power modes

Pin	Active - Sleep - Power Down modes
all PAnm	As configured in the SYSCON[1]. Default: internal pull-up enabled.
RSTN	Reset function enabled. Default: input, internal pull-up enabled

[1] Default and programmed pin states are retained in sleep, and power-down mode.

8. Compliance statements and documentation

- The FCC ID number of the QN9080-001-M17 is XXMQN9080M17
- The IC ID number of the QN9080-001-M17 is 8764A-QN9080M17
- The Japan ID number of the QN9080-001-M17 is 

8.1 FCC Statements and documentation

This section contains the Federal Communication Commission (FCC) statements and documents.

8.1.1 FCC interference Statements

- This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

- OEM integrators instructions
  - The OEM integrators are responsible for ensuring that the end-user has no manual instructions to remove or install SIP
  - The SIP is limited to installation in mobile or fixed applications, according to CFR 47 Part 2.1091(b)
  - Separate approval is required for all other operating configurations, including portable configurations with respect to CFR 47 Part 2.1093 and different antenna configurations
- User guide mandatory statements

  User's instructions of the host device must contain the following statements in addition to operation instructions:

  * "This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

  (1) This device may not cause harmful interference, and

  (2) This device must accept any interference received, including interference that may cause undesired operation"

  * "Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment"
- FCC RF Exposure requirements

  User's instructions of the host device must contain the following instructions in addition to operation instructions:

  Avoid direct contact to the antenna, or keep it to a 20cm minimum distance while using this equipment. This device must not be collocated or operating in conjunction with another antenna or transmitter.

This SIP has been designed to operate etheir with internal antenna or with external antennas having a maximum gain of 2 dBi. Antennas having a gain greater than 2 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms

8.1.2 FCC end product labelling

The final 'end product' should be labelled in a visible area with the following:
"Contains TX FCC ID: XXMQN9080M17 to reflect the SIP being used inside the product.

8.2 Industry Canada Statement

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device. This device complies with Industry Canada RF radiation exposure limits set forth for general population (uncontrolled exposure). This device must be installed to provide a separation distance of at least 20 cm from all persons and must not be collocated or operating in conjunction with any other antenna or transmitter.	Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) il ne doit pas produire de brouillage, et (2) l'utilisateur du dispositif doit être prêt à accepter tout brouillage radioélectrique re?u, même si ce brouillage est susceptible de compromettre le fonctionnement du dispositif. Le présent appareil est conforme aux niveaux limites d'exigences d'exposition RF aux personnes définies par Industrie Canada. Cet appareil doit être installé afin d'offrir une distance de séparation d'au moins 20 cm avec l'utilisateur, et ne doit pas être installé à proximité ou être utilisé en conjonction avec une autre antenne ou un autre émetteur.

To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropic radiated power (e.i.r.p.) is not more than that permitted for successful communication.

The Gain of SIP with internal antenna is -3dBi.

If customer wants, he can also use the SIP with external antenna with maximum gain of 2dbi. This feature is not certified by NXP and need to be done by the customer. Antennas having a gain greater than 2 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.

As long as the above condition is met, further transmitter testing will not be required.

However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this SIP installed (for example, digital device emissions, PC peripheral requirements, etc.).

8.2.1 Industry of Canada end product labelling

For Industry Canada purposes the following should be used:
"Contains Industry Canada ID IC: 8764A-QN9080M17

8.3 Japanese Radio Certification Statement

This equipment has been tested and found to comply with the Japanese Radio Certification Rules

8.3.1 Radio Certification end product labelling

For Japanese Radio Certification purposes, the following should be used:

"Contains Japanese Radio certificate product: Japan ID number is 207-990010

9. Static characteristics

9.1 General operating conditions

Table 8. General operating conditions

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{clk}	Clock frequency	—	—	—	32	MHz
V_{CC}	Supply voltage	—	1.67	3	3.6	V
V_{ESD}	Electrostatic discharge voltage	Human body model[2]; all pins	—	—	2	kV
		Charged device model; all pins	—	—	300	V
$T_{J(max)}$	Maximum junction temperature	—	—	—	85	°C

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9.2 Power consumption

Power measurements in active, sleep, power down modes were performed under the following conditions:

- All peripherals disabled
- Analog peripherals (ADC/DAC/ACMP/Capacitive Sense) powered down
- RF off
- Internal 32 MHz HFRCO powered down

Table 9. Static characteristics: Power consumption in active modes

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
32 MHz HFXO; DC-DC converter enabled, V_{CC} = 3.0 V							
I_{CC}	Supply current	CoreMark code executed from flash					
		CLK_AHB = 16 MHz	[2]	—	920	—	µA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples.

Table 10. Static characteristics: Bluetooth LE power consumption in active modes

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
32 MHz crystal oscillator, CLK_AHB = 16 MHz, transmitter mode: f_c = 2440 MHz, 1 Mbps mode							
I_{CC}	supply current	DC-to-DC converter enabled, V_{cc} = 3 V					
		Tx power = 0 dBm		—	3.5	—	mA
32 MHz crystal oscillator, CLK_AHB = 16 MHz, transmitter mode: f_c = 2440 MHz, 1 Mbps mode							
I_{CC}	supply current	DC-to-DC converter enabled, V_{cc} = 3 V					
		-92.7 dBm RX sensitivity		—	4	—	mA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples, with 50 Ω loading on RF port.

[3] Guaranteed by characterization, not tested in production.

Table 11. Static characteristics: Power consumption in sleep, and power-down modes

T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1][2]	Max[3]	Unit
I_{CC}	Supply current	Sleep mode: all SRAM on. Flash in standby mode. DC-to-DC converter enabled, V_{cc} = 3 V.				
		32 MHz crystal oscillator				
		CLK_AHB = 16 MHz	—	470	—	µA
		Power down mode; all clocks off. Flash is powered down. DC-DC disabled, V_{cc} = 3 V. T_{amb} = 25 °C.				
		8 KB SRAM powered	—	1.0	—	µA
		Power down mode; 32.768 kHz LFXO on. Flash is powered down. DC-DC disabled, V_{cc} = 3 V. T_{amb} = 25 °C.				
		8 KB SRAM powered	—	2.5	—	µA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples.

[3] Guaranteed by characterization, not tested in production.

9.3 Clock source

Table 12. 32 MHz clock source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{nom}	Nominal frequency	—	—	32	—	MHz
	Frequency tolerance	at +25°C	-10	—	+10	ppm
C_L	Load capacitance	—	—	10	—	pF
R_r	Equivalent resistance	—	—	—	60	Ω

Table 13. 32.768 kHz clock source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{nom}	Nominal frequency	—	—	32.768	—	kHz
	Frequency tolerance	at +25±3°C, Not include aging	-20	—	+20	ppm
C_L	Load capacitance	—	—	12.5	—	pF
R_r	Equivalent resistance	—	—	—	120	kΩ

10. RF characteristics

10.1 Receiver

Table 14. Receiver characteristics

T_{amb} = 25 °C; based on characterization; not tested in production. V_{CC} = 3 V; f_c = 2440 MHz; BER < 0.1 %, 1 Mbps mod

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S_{RX}	RX sensitivity	low power mode with DC-to-DC converter	—	–92.7	—	dBm
$P_{i(max)}$	maximum input power		—	0	—	dBm
C/I[1]	carrier-to-interference ratio	co-channel	—	6	—	dB
		adjacent channel at ±1 MHz	—	–4	—	dB
		alternate channel at ±2 MHz	—	–41	—	dB
α_{image}[1]	image rejection		—	–41	—	dB
$\alpha_{sup(oob)}$[1]	out-of-band suppression	30 MHz to 2000 MHz	–1	—	—	dBm
		2003 MHz to 2399 MHz	–10	—	—	dBm
		2484 MHz to 2997 MHz	–10	—	—	dBm
		3 GHz to 12.75 GHz	–10	—	—	dBm

[1] The values of these parameters are from QN9080 data sheet

10.2 Transmitter

Table 15. Transmitter characteristics

T_{amb} = 25 °C; based on QN9080 characterization; not tested in production.V_{CC} = 3 V; f_c = 2440 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{o(RF)}$	RF output frequency	—	2400	—	2483.5	MHz
α_{CS}	channel separation	—	—	2	—	MHz
P_o	output power	TX power	–20	—	+2	dBm
$P_{o(RF)step}$	RF output power step	—	—	1	—	dB
$P_{o(acc)}$	TX power accuracy	—	–2	—	+2	dB

Remark: The QN9080-001-M17 is a fully certified device supporting Bluetooth 5.0. There is a marginality (5% drift compare to the Min value of 185 kHz) on frequency deviation df2 99.9% at -40°C.

11. Internal antenna characteristic

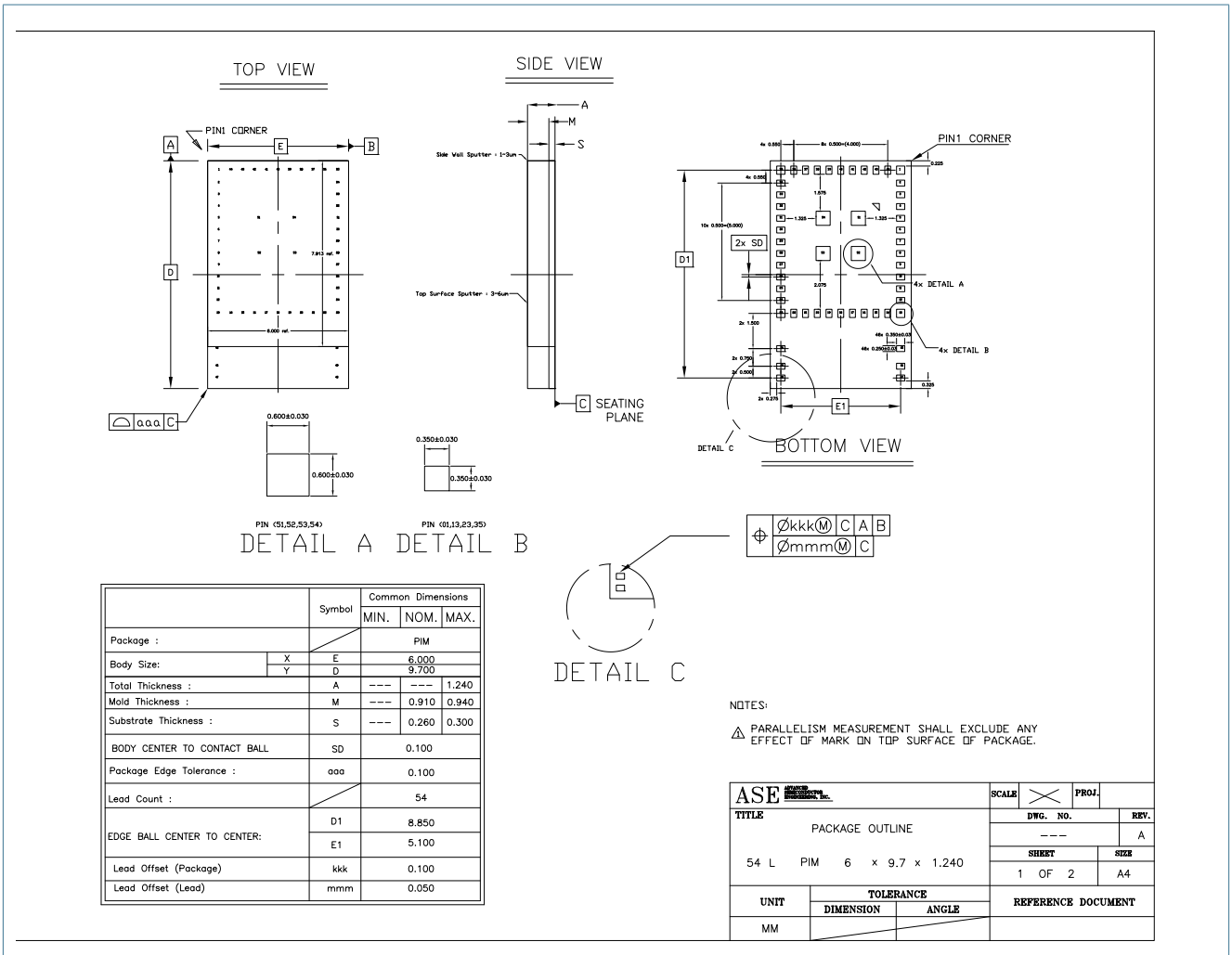
Table 16. BOD static characteristics

T_{amb} = 25 °C; based on characterization; not tested in production.

Parameter	Min	Typ	Max	Unit
Frequency range	2400	—	2480	MHz
Impedance	—	50	—	Ω
Peak gain	—	0.5	—	dBi

12. Layout guideline

12.1 Footprint information for reflow soldering



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			PIM		
Body Size:	X	E		6.000	
	Y	D		9.700	
Total Thickness :		A	---	---	1.240
Mold Thickness :		M	---	0.910	0.940
Substrate Thickness :		S	---	0.260	0.300
BODY CENTER TO CONTACT BALL		SD		0.100	
Package Edge Tolerance :		aaa		0.100	
Lead Count :				54	
EDGE BALL CENTER TO CENTER:		D1		8.850	
		E1		5.100	
Lead Offset (Package)		kkk		0.100	
Lead Offset (Lead)		mmm		0.050	

ASE		SCALE	PROJ.
TITLE: PACKAGE OUTLINE		DWG. NO.	REV.
54 L PIM 6 x 9.7 x 1.240		---	A
		SHEET 1 OF 2	SIZE A4
UNIT	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT	
MM			

Fig 5. Footprint information for reflow soldering of SIPs

12.2 Layout recommendation for ground plane implementation and clearance area for QN9080-001-M17 with integrated 2.4 GHz antenna

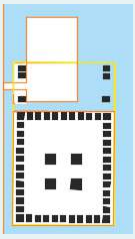
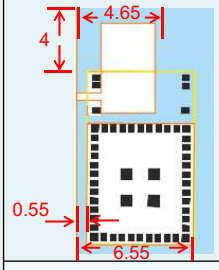
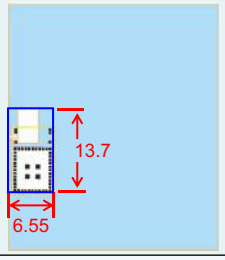
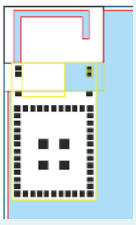
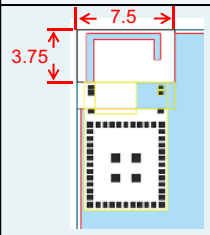
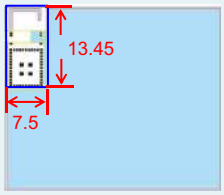
	Physical View	Antenna Clearance On EVB(mm)	Module + Antenna Clearance(mm)
Scenario #A (Center Edge)			
		4 x 4.65 mm	13.7x 6.55 mm
Scenario #B (Corner)			
		7.5 x 3.75 mm	13.45 x 7.5 mm

Fig 6. QN9080-001-M17 chip with integrated 2.4 GHz antenna / SIP clearance size (top view)

12.2.1 Center edge PCB ground plane design

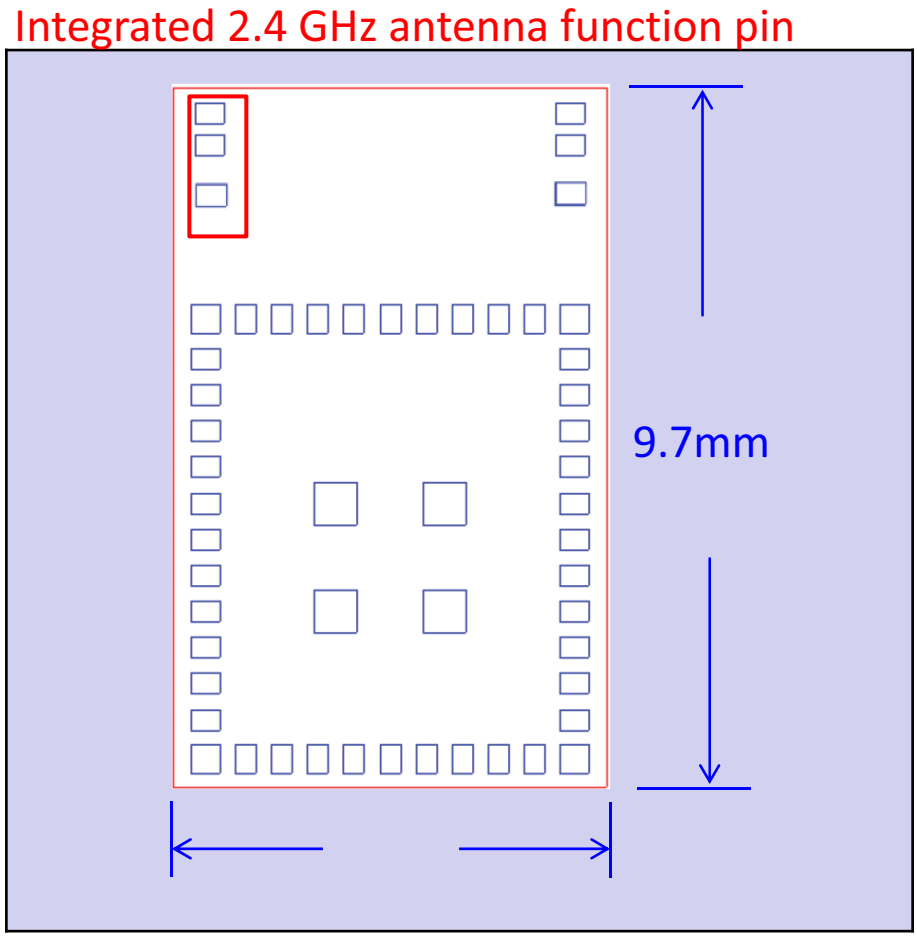


Fig 7. QN9080-001-M17 module on 36 mm x 31 mm PCB layout guide- center edge

- Do not route signal trace across antenna clearance area
- Connect pin 49 to Upper GND, pin 50 to lower GND

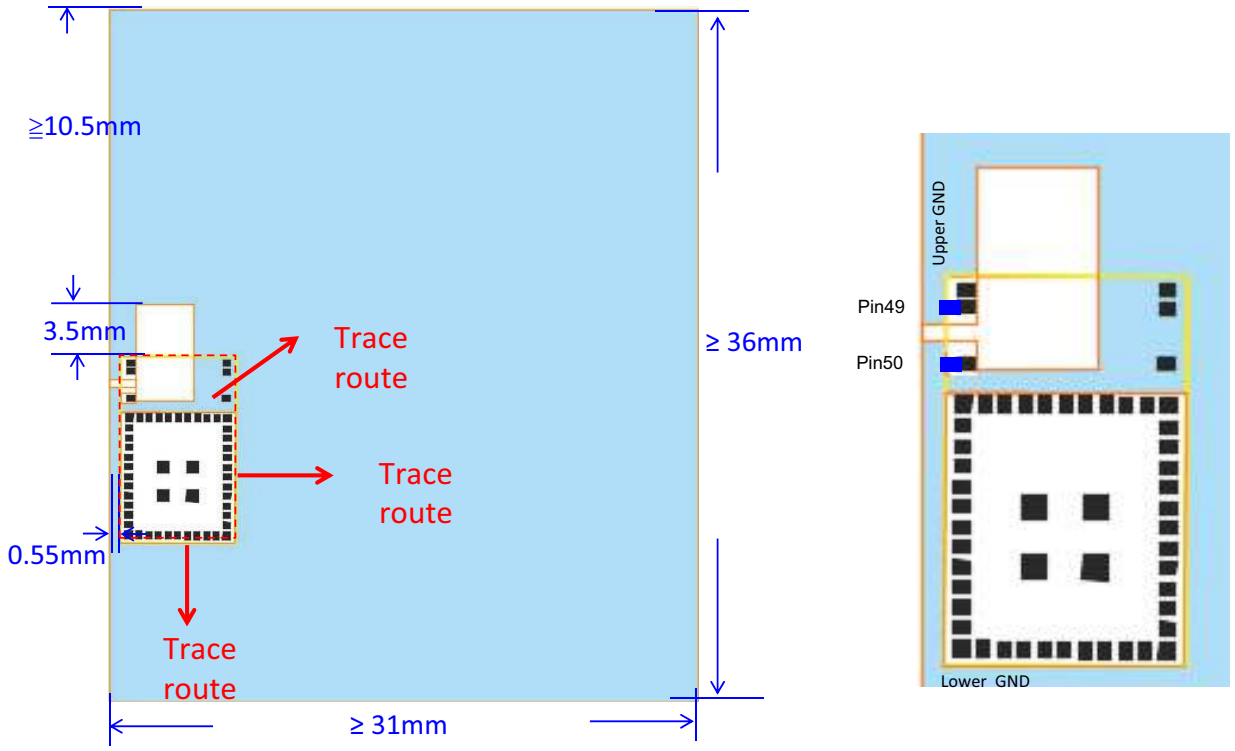
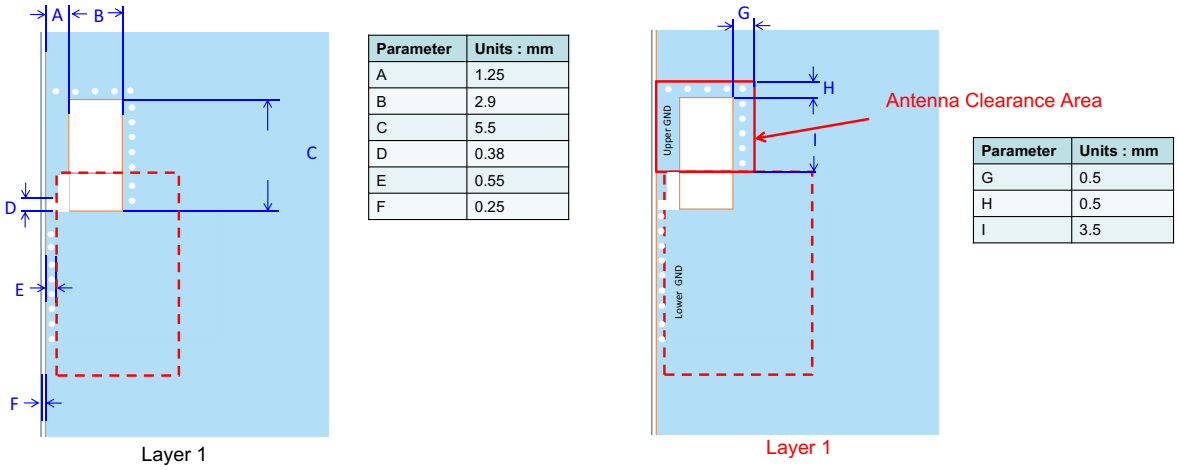


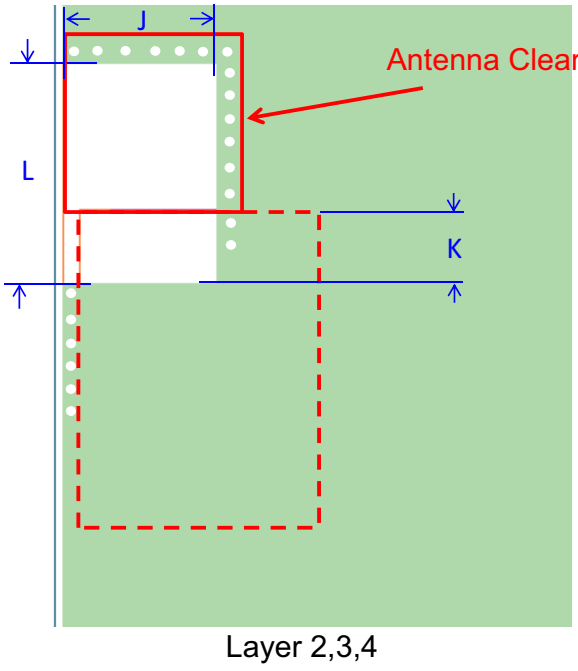
Fig 8. QN9080-001-M17 module on 36 mm x 31 mm GND PCB layout guide - center edge - clearance area



Parameter	Units : mm
A	1.25
B	2.9
C	5.5
D	0.38
E	0.55
F	0.25

Parameter	Units : mm
G	0.5
H	0.5
I	3.5

Fig 9. QN9080-001-M17 module on 36 mm x 31 mm GND PCB layout guide - center edge - clearance area layer 1 dimensions



Parameter	Units : mm
J	4.15
K	2
L	5.5

Fig 10. QN9080-001-M17 module on 36 mm x 31 mm GND PCB layout guide - center edge - clearance area layers 2, 3, 4 dimensions

12.2.2 Corner EVB ground plane design

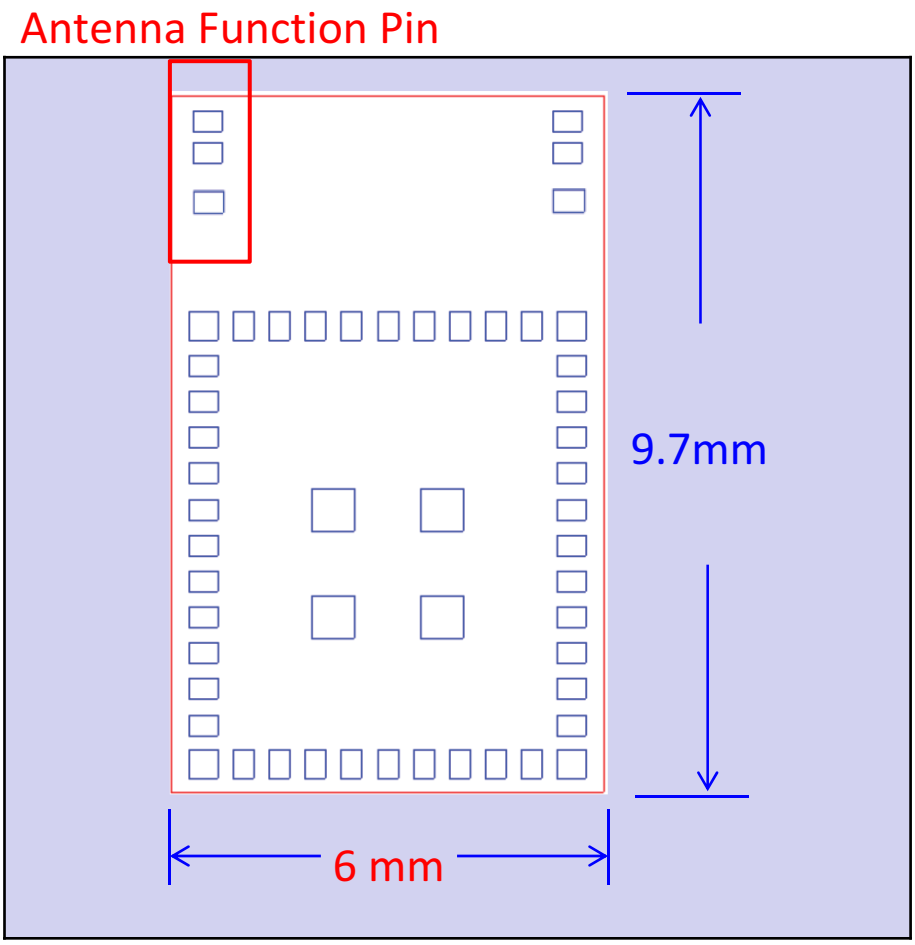


Fig 11. QN9080-001-M17 module on 36 mm x 31 mm PCB layout guide - corner

- Do not route signal trace across antenna clearance area
- Connect pin 48 to antenna trace

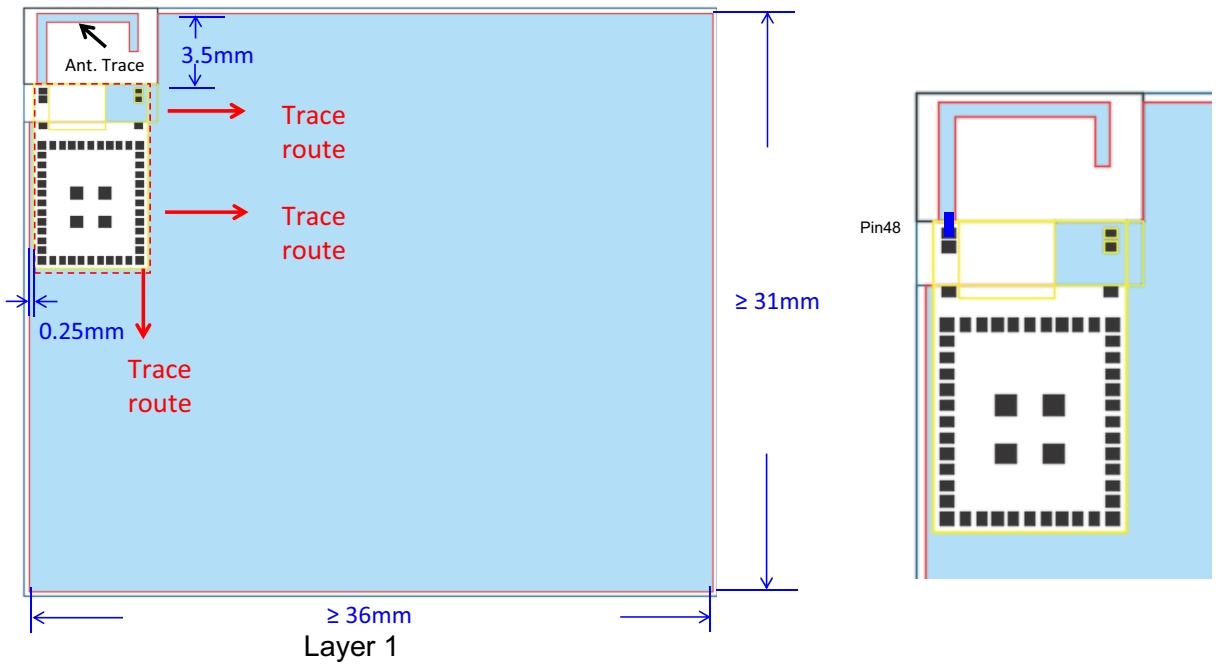
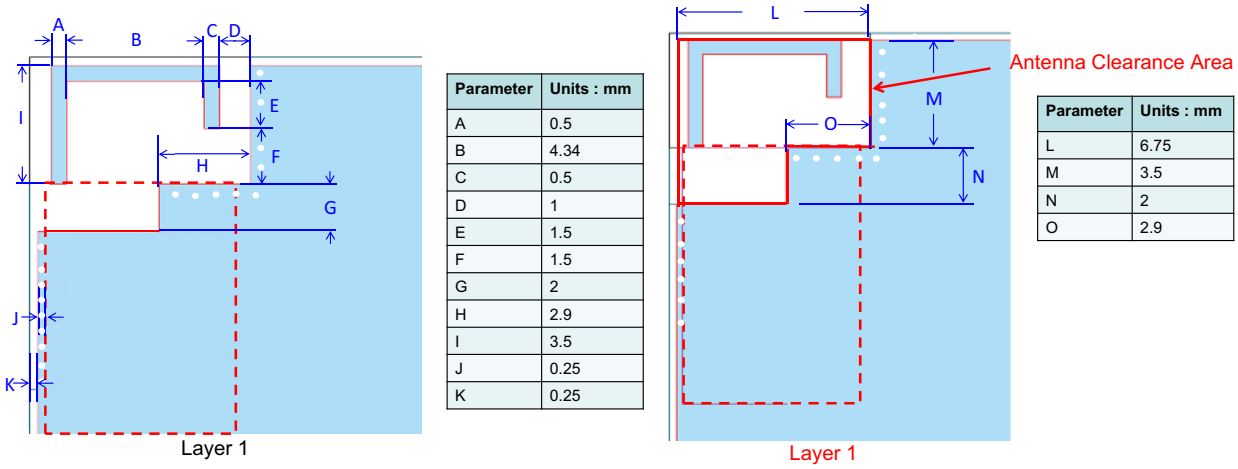


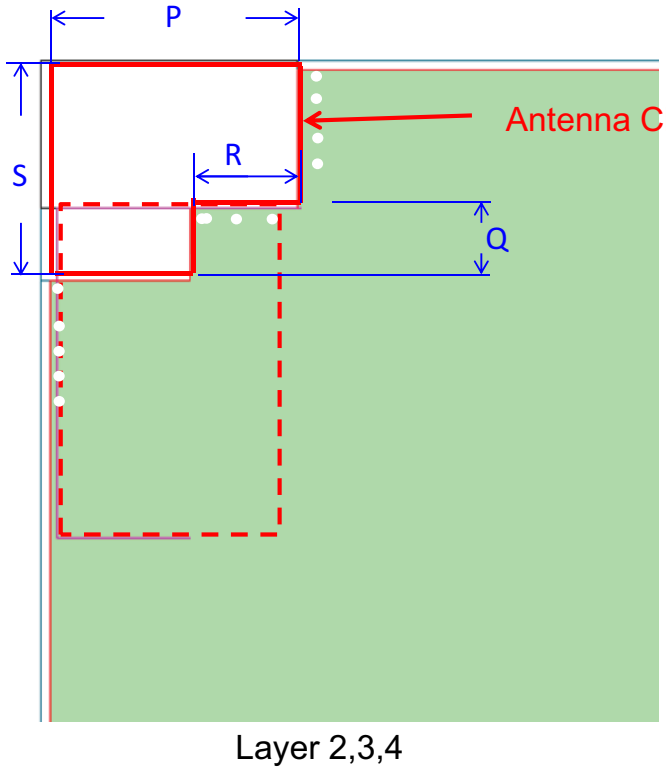
Fig 12. QN9080-001-M17 module on 36 mm x 31 mm GND PCB layout guide - corner - clearance area



Parameter	Units : mm
A	0.5
B	4.34
C	0.5
D	1
E	1.5
F	1.5
G	2
H	2.9
I	3.5
J	0.25
K	0.25

Parameter	Units : mm
L	6.75
M	3.5
N	2
O	2.9

Fig 13. QN9080-001-M17 module on 36 mm x 31 mm GND PCB layout guide - corner - clearance area layer 1 dimensions



Parameter	Units : mm
P	6.75
Q	2
R	2.9
S	5.5

Fig 14. QN9080-001-M17 module on 36 mm x 31 mm GND PCB layout guide - corner - clearance area layers 2, 3, 4 dimensions

12.3 Reflow profile

QN9080-001-M17 is an MSL3 and PSL R5G product. PSL has been defined based on the standard J-STD-075. For reflow soldering, it is requested to follow the reflow profile and the paste manufacturer's guidelines on peak flow temperature, soak times, time above liquid and ramp rates.

Table 17. Recommended solder reflow profile

Temperature range	Time
Peak temperature: 255 °C	10 s Max.
Heating: 230 °C or higher	30 s Max.
Preheating: 150 °C to 180 °C	60-120 s

12.4 Soldering paste and cleaning

NXP does not recommend to use a solder paste that requires the module and PCB assembly to be cleaned (rinsed in water) for the following reasons:

- Solder flux residues and water can be trapped by the PCB, can or components and result in short circuits

NXP recommends to use a 'no clean' solder paste for all its module products.

13. Package outline

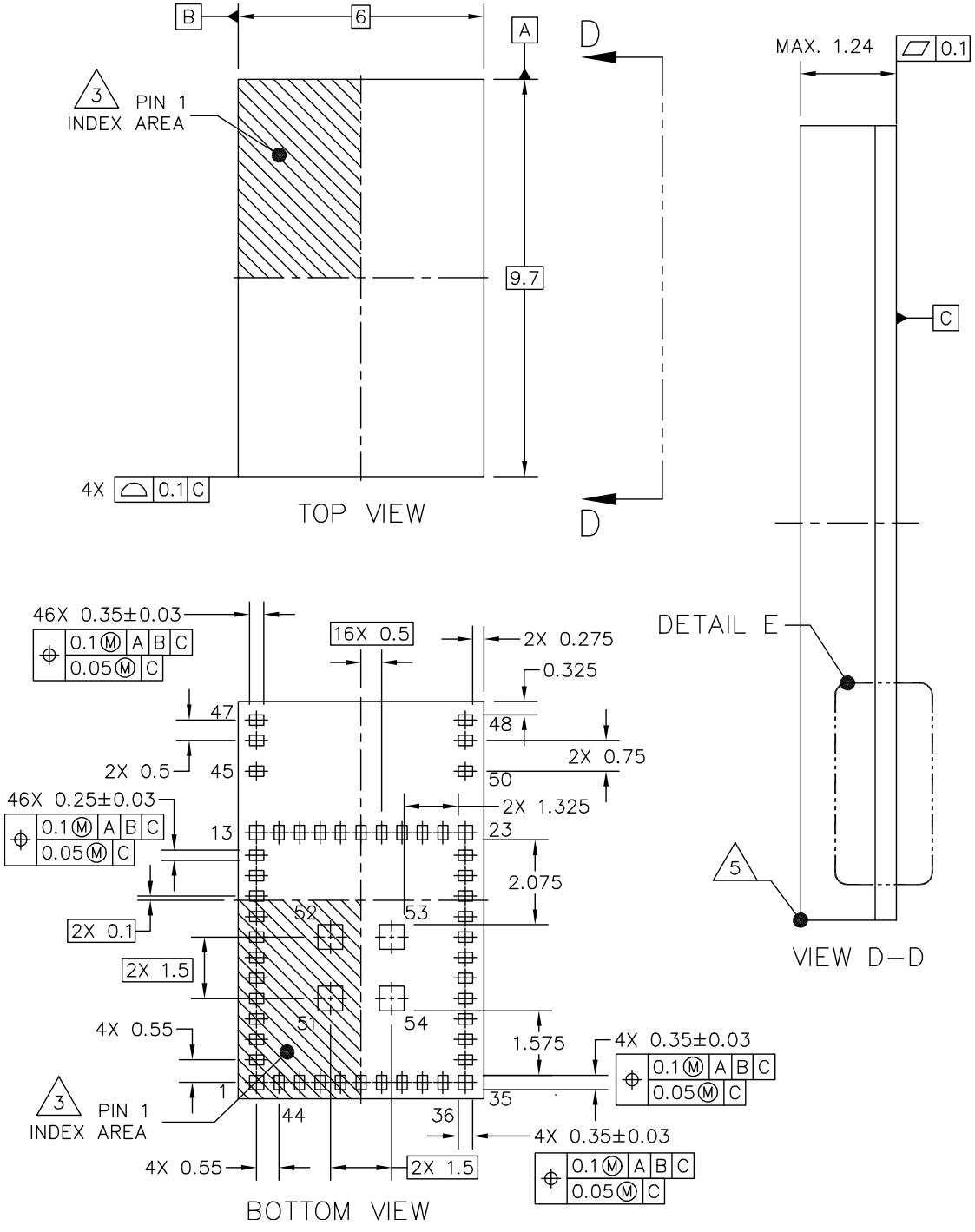


Fig 15. Package outline LFLGA54 (SOT1910-1)

14. Abbreviations

Table 18. Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
API	Application Program Interface
CLK	CLocK
CRC	Cyclic redundancy Check
CTS	Clear-To-Send
DC	Direct current
DIO	Digital Input Output
DMA	Direct memory Access
EEPROM	Electrically-Erasable Programmable Read Only Memory
FIFO	First In First Out
GPIO	General Purpose Input Output
ID	IDentification
IF	Intermediate frequency
IO	Input Output
MSL	Moisture sensitivity level
NVIC	Nested Vector Interrupt Controller
PCB	Printed-Circuit Board
PHY	PHYsical
POR	Power-On Reset
PWM	Pulse Width Modulation
RAM	Random Access Memory
RC	Remote Control
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RSSI	Receive Signal Strength Indication
RTS	Request-To-Send
RX	Received
SCL	Serial CLock
SDA	Serial DatA
SMDs	Surface Mount Devices
SPI-bus	Serial Peripheral Interface -bus
SysTick	System Tick timer
TX	Transmit

15. References

[1] **IEEE Std 802.15.4-2011 IEEE Standard for Information Technology Part 15.4 —** Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs).

[2] **Wireless Connectivity —** http://www.nxp.com/products/wireless-connectivity:WIRELESS-CONNECTIVITY

16. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
QN9080-001-M17 v1.0	20181205	Objective data sheet	Public release	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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19. Tables

20. Figures

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