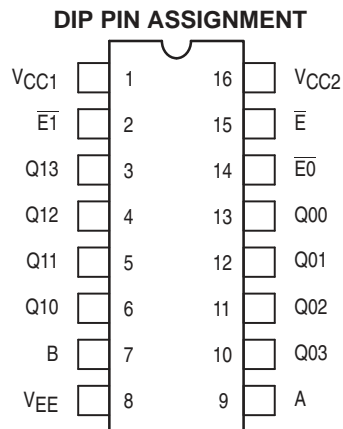
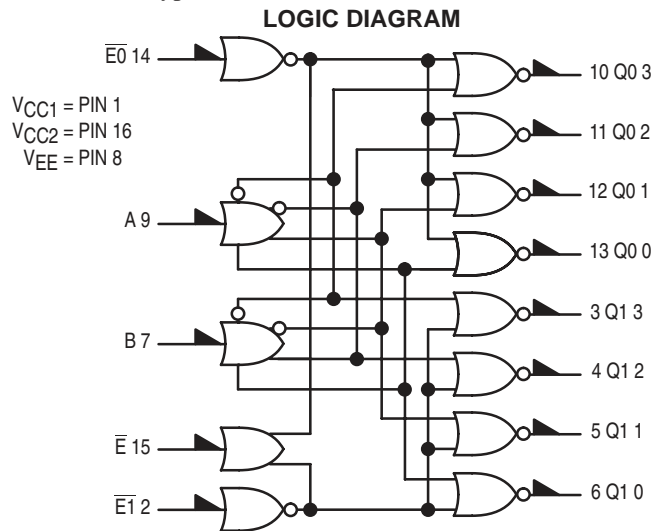


# MC10172

## Dual Binary to 1-4 Decoder (High)

The MC10172 is a binary-coded 2 line to dual 4 line decoder with selected outputs high. With either  $\overline{E0}$  or  $\overline{E1}$  low, the corresponding selected 4 outputs are low. The common enable  $\overline{E}$ , when high, forces all outputs low.

- $P_D = 325$  mW typ/pkg (No Load)
- $t_{pd} = 4.0$  ns typ
- $t_r, t_f = 2.0$  ns typ (20%–80%)



Pin assignment is for Dual-in-Line Package.  
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

### TRUTH TABLE

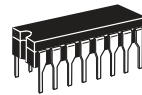
$\overline{E}$	$\overline{E1}$	$\overline{E0}$	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
H	X	X	X	X	L	L	L	L	L	L	L	L



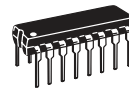
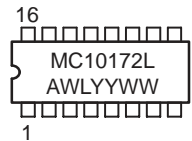
ON Semiconductor

<http://onsemi.com>

### MARKING DIAGRAMS



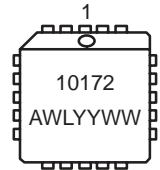
CDIP-16  
L SUFFIX  
CASE 620



PDIP-16  
P SUFFIX  
CASE 648



PLCC-20  
FN SUFFIX  
CASE 775



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC10172L	CDIP-16	25 Units / Rail
MC10172P	PDIP-16	25 Units / Rail
MC10172FN	PLCC-20	46 Units / Rail

# MC10172

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits						Unit		
			-30°C		+25°C			+85°C			
			Min	Max	Min	Typ	Max	Min		Max	
Power Supply Drain Current	$I_E$	8		85		65	77		85	mAdc	
Input Current	$I_{inH}$	14		350			220		220	$\mu$ Adc	
	$I_{inL}$	14	0.5		0.5			0.3		$\mu$ Adc	
Output Voltage Logic 1	$V_{OH}$	6	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	
		13	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		
Output Voltage Logic 0	$V_{OL}$	13	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	
Threshold Voltage Logic 1	$V_{OHA}$	6	-1.080		-0.980			-0.910		Vdc	
		13	-1.080		-0.980			-0.910			
Threshold Voltage Logic 0	$V_{OLA}$	6		-1.655			-1.630		-1.595	Vdc	
		13		-1.655			-1.630		-1.595		
Switching Times (50 $\Omega$ Load)										ns	
Propagation Delay		$t_{7+6-}$	6	1.5	6.2	1.5	4.0	6.0	1.5	6.4	
		$t_{7-6+}$	6	1.5	6.2	1.5	4.0	6.0	1.5	6.4	
		$t_{7+13-}$	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	
		$t_{7-13+}$	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	
Rise Time (20 to 80%)		$t_{6+}$	6	1.0	3.3	1.1	2.0	3.3	1.1	3.4	
		$t_{13+}$	13	1.0	3.3	1.1	2.0	3.3	1.1	3.4	
Fall Time (20 to 80%)		$t_{6-}$	6	1.0	3.3	1.1	2.0	3.3	1.1	3.4	
		$t_{13-}$	13	1.0	3.3	1.1	2.0	3.3	1.1	3.4	

# MC10172

## ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)					
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	
@ Test Temperature								
-30°C			-0.890	-1.890	-1.205	-1.500	-5.2	
+25°C			-0.810	-1.850	-1.105	-1.475	-5.2	
+85°C			-0.700	-1.825	-1.035	-1.440	-5.2	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V <sub>CC</sub> ) Gnd
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	
Power Supply Drain Current	I <sub>E</sub>	8					8	1, 16
Input Current	I <sub>inH</sub>	14	14				8	1, 16
	I <sub>inL</sub>	14		14			8	1, 16
Output Voltage Logic 1	V <sub>OH</sub>	6	2				8	1, 16
		13	14				8	1, 16
Output Voltage Logic 0	V <sub>OL</sub>	13	15	2,7,9,14			8	1, 16
Threshold Voltage Logic 1	V <sub>OHA</sub>	6			2		8	1, 16
		13			14		8	1, 16
Threshold Voltage Logic 0	V <sub>OLA</sub>	6		2,9,14		7	8	1, 16
		13		2,7,14		9	8	1, 16
Switching Times (50Ω Load)			<b>+1.11V</b>	<b>+0.31V</b>	<b>Pulse In</b>	<b>Pulse Out</b>	<b>-3.2 V</b>	<b>+2.0 V</b>
Propagation Delay	t <sub>7+6-</sub>	6	2	9, 14	7	6	8	1, 16
	t <sub>7-6+</sub>	6	2	9, 14	7	6	8	1, 16
	t <sub>7+13-</sub>	13	14	2, 9	7	13	8	1, 16
	t <sub>7-13+</sub>	13	14	2, 9	7	13	8	1, 16
Rise Time (20 to 80%)	t <sub>6+</sub>	6	2	9, 14	7	6	8	1, 16
	t <sub>13+</sub>	13	14	2, 9	7	13	8	1, 16
Fall Time (20 to 80%)	t <sub>6-</sub>	6	2	9, 14	7	6	8	1, 16
	t <sub>13-</sub>	13	14	2, 9	7	13	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.