LOW SKEW, DUAL, 1-TO-5 DIFFERENTIAL-TO-LVDS FANOUT BUFFER

ICS854210

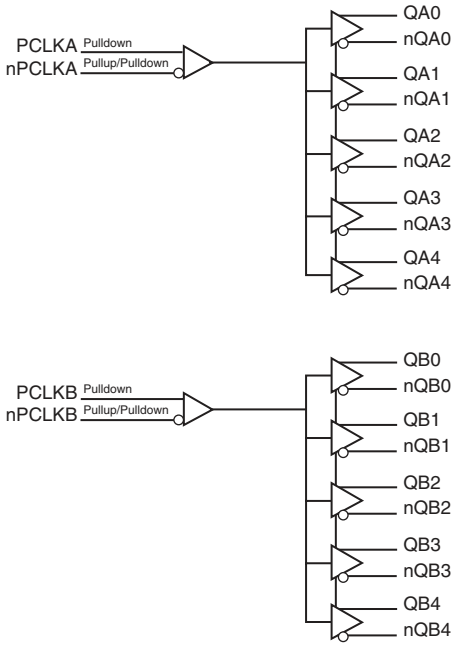
General Description

The ICS854210 is a low skew, high performance dual 1-to-5 Differential-to-LVDS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS854210 is characterized to operate from a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS854210 ideal for those clock distribution applications demanding well defined performance and repeatability.

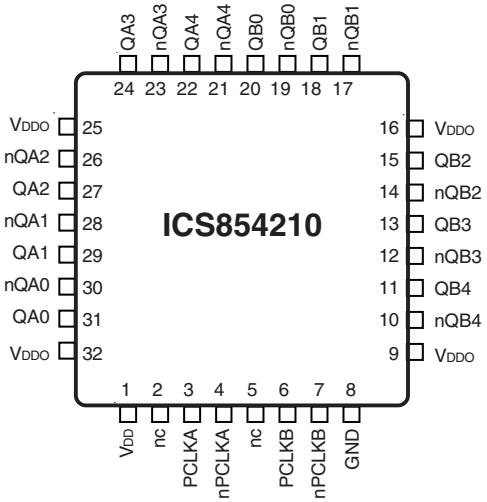
Features

- Two differential LVDS bank outputs
- Two differential LVPECL clock input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: 2GHz
- Translates any single ended input signal to LVDS levels with resistor bias on nPCLKx input
- Output skew: TBD
- Part-to-part skew: TBD
- Propagation delay: 280ps (typical)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DD}	Power		Power supply pin.
2, 5	nc	Unused		No connect.
3	PCLKA	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPCLKA	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{DD}/2 default when left floating.
6	PCLKB	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLKB	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{DD}/2 default when left floating.
8	GND	Power		Power supply ground.
9, 16, 25, 32	V_{DDO}	Power		Output supply pins.
10, 11	nQB4, QB4	Output		Differential output pair. LVDS interface levels.
12, 13	nQB3, QB3	Output		Differential output pair. LVDS interface levels.
14, 15	nQB2, QB2	Output		Differential output pair. LVDS interface levels.
17, 18	nQB1, QB1	Output		Differential output pair. LVDS interface levels.
19, 20	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
21, 22	nQA4, QA4	Output		Differential output pair. LVDS interface levels.
23, 24	nQA3, QA3	Output		Differential output pair. LVDS interface levels.
26, 27	nQA2, QA2	Output		Differential output pair. LVDS interface levels.
28, 29	nQA1, QA1	Output		Differential output pair. LVDS interface levels.
30, 31	nQA0, QA0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ
$R_{VDD/2}$	Pullup/Pulldown Resistors			50		kΩ

TABLE 3. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
PCLKA or PCLKB	nPCLKA or nPCLKB	QA0:QA4, QB0:QB4	nQA0:nQA4, nQB0:nQB4		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information, "Wiring the Differential Input to Accept Single Ended Levels".

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Negative Supply Voltage, V_{EE}	-4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	47.9°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDO}	Output Supply Current			TBD		mA

Table 4B. LVPECL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLKA, PCLKB	$V_{DD} = V_{IN} = 3.465V$			150	µA
		nPCLKA, nPCLKB	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	PCLKA, PCLKB	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
		nPCLKA, nPCLKB	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-10			µA
V_{TH}	Differential Input High Threshold Voltage					100	mV
V_{TL}	Differential Input Low Threshold Voltage			-100			mV
V_{PP}	Peak-to-Peak Input Voltage				0.15		V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.2			V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLKA, nPCLKA and PCLKB, nPCLKB is V_{DD} + 0.3V.

TABLE 4C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OD}	Differential Output Voltage					350					mV
ΔV_{OD}	V_{OD} Magnitude Change						50				mV
V_{OS}	Offset Voltage					1.25					V
ΔV_{OS}	V_{OS} Magnitude Change						50				mV

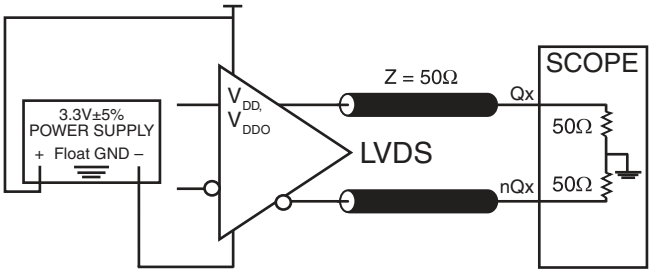
NOTE 1: Refer to Parameter Measurement Information, "3.3V Output Load Test Circuit" diagram.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

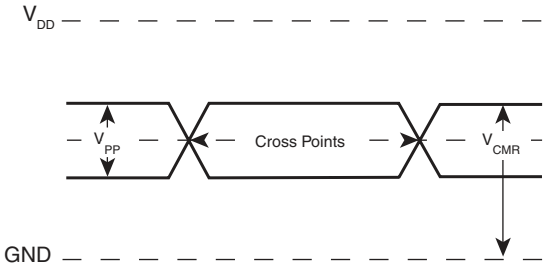
Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency			2			2			2		GHz
t_{PD}	Propagation Delay; NOTE 1			260			280			305		ps
*t*sk(o)	Output Skew; NOTE 2, 4			TBD			TBD			TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD			TBD			TBD		ps
t_R/t_F	Output Rise/Fall Time	20% to 80%		175			180			190		ps

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

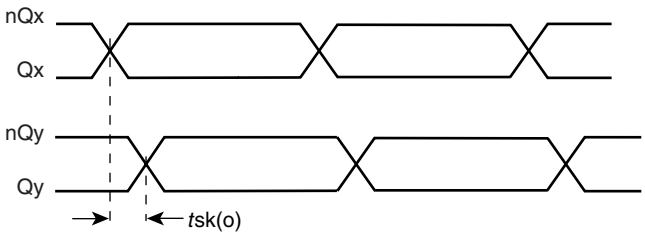
PARAMETER MEASUREMENT INFORMATION



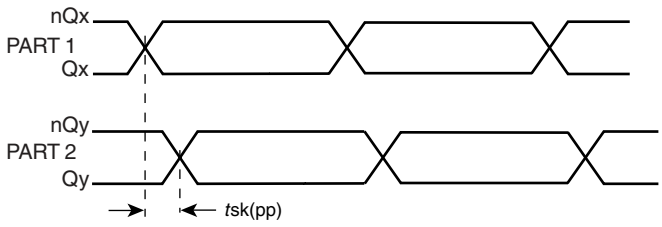
3.3V OUTPUT LOAD AC TEST CIRCUIT



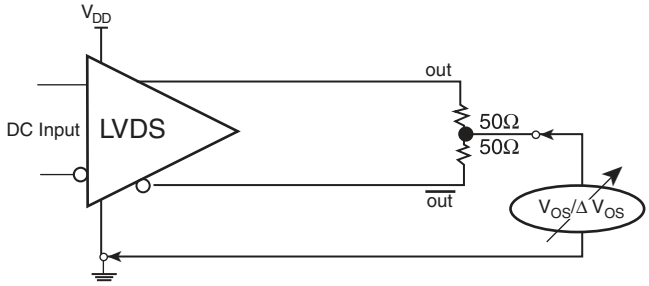
DIFFERENTIAL INPUT LEVEL



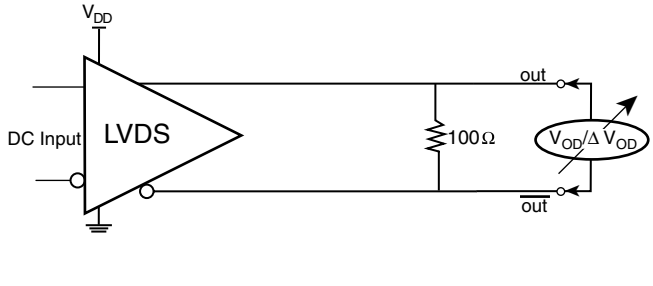
OUTPUT SKEW



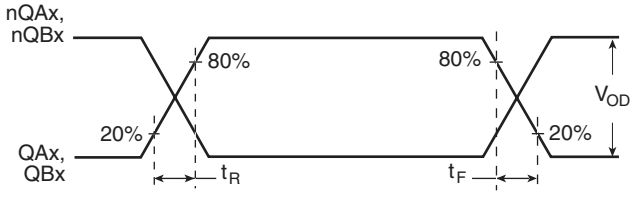
PART-TO-PART SKEW



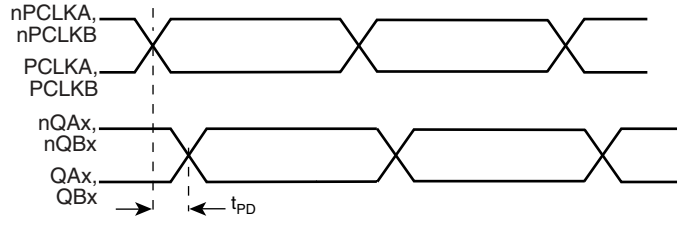
V_{OS} SETUP



V_{OD} SETUP



OUTPUT RISE/FALL TIME



PROPAGATION DELAY

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD}= 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

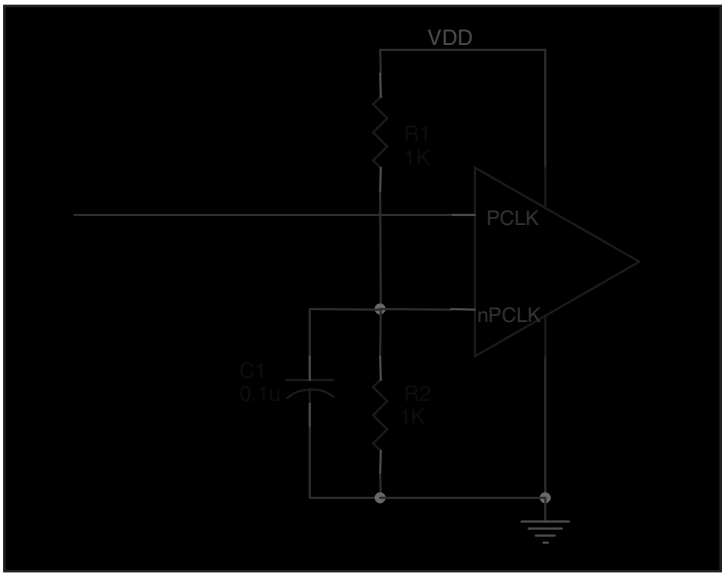


Figure 1. Single Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK InputS

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:

LVDS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

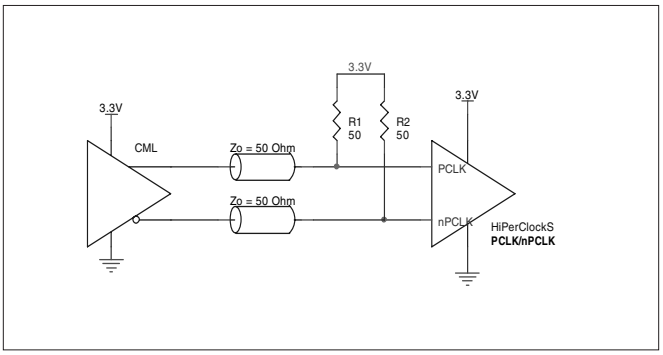


Figure 2A. HiPerClockS PCLK/nPCLK Input Driven by an Open Collector CML Driver

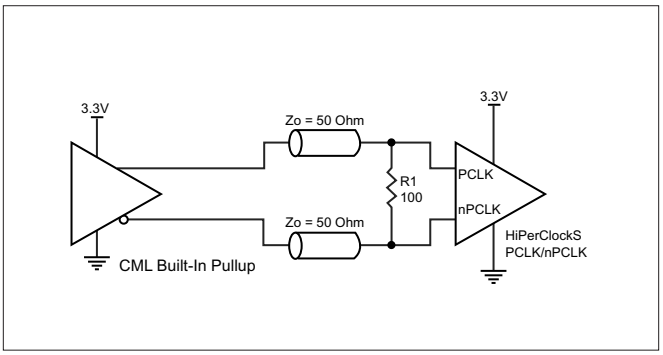


Figure 2B. HiPerClockS PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

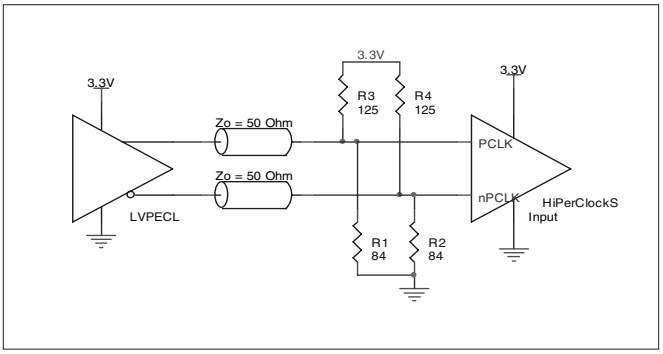


Figure 4C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

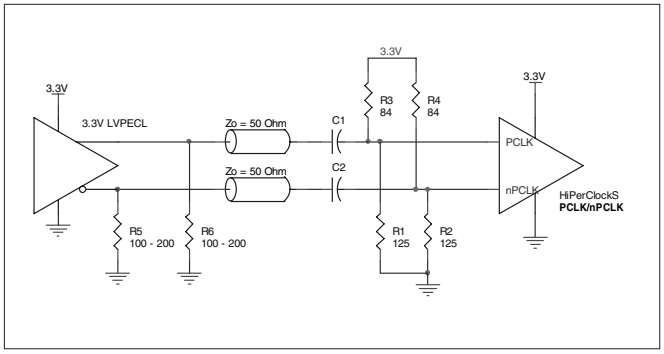


Figure 2D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

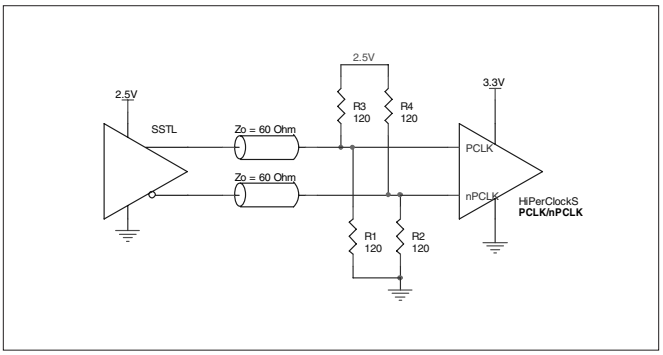


Figure 2E. HiPerClockS PCLK/nPCLK Input Driven by an SSTL Driver

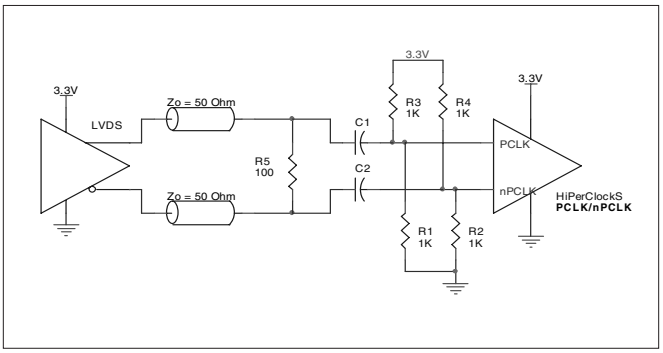


Figure 2F. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

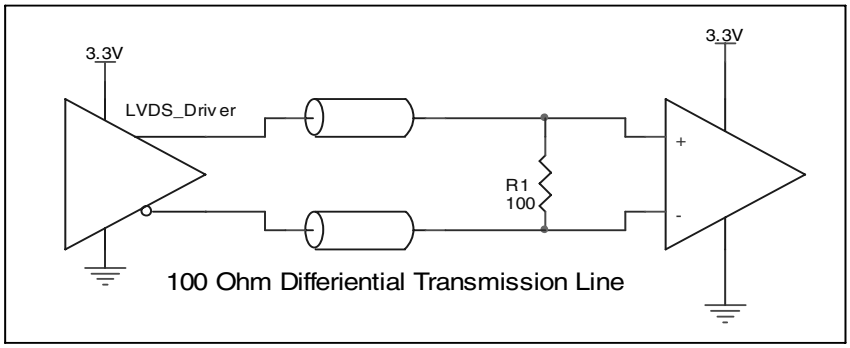


Figure 3. Typical LVDS Driver Termination

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 32L LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS854210 is: 394

Package Outline - Y Suffix for 32L LQFP

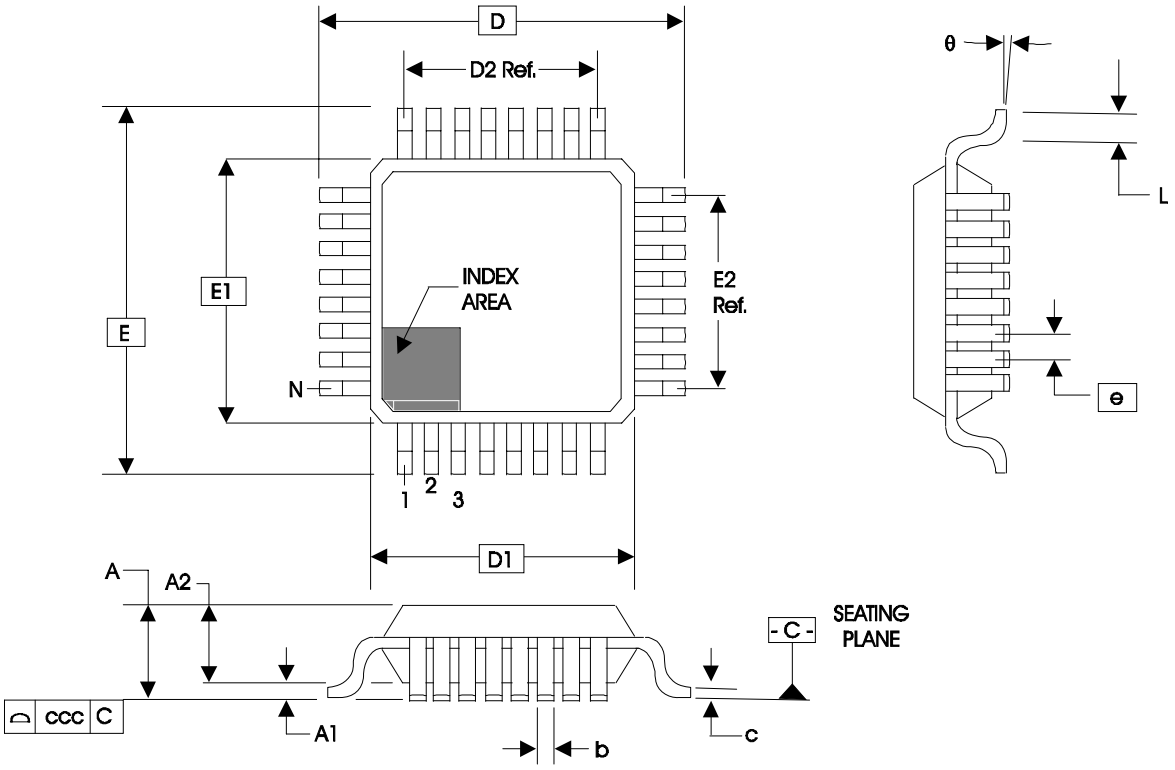


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS854210CY	ICS854210CY	32 lead LQFP	tray	-40°C to 85°C
ICS854210CYT	ICS854210CY	32 lead LQFP	1000 tape & reel	-40°C to 85°C
ICS854210CYLF	ICS854210CYL	32 Lead "Lead-Free" LQFP	tray	-40°C to 85°C
ICS854210CYLFT	ICS854210CYL	32 Lead "Lead-Free" LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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