# Ultrathin Quad µModule Regulator with Configurable 3A Output Array

## FEATURES

- Quad Output Step-Down µModule® Regulator with 3A per Output
- Wide Input Voltage Range: 4V to 20V
  - 2.375V to 20V with External Bias
- 0.6V to 3.3V Output Voltage
- 3A DC Output Current Each Channel
- ±1.5% Total Output Voltage Regulation
- Current Mode Control, Fast Transient Response
- Parallelable for Higher Output Current
- Output Voltage Tracking
- Internal Temperature Sensing Diode Output
- External Frequency Synchronization
- Overvoltage, Current and Temperature Protection
- 9mm × 15mm × 1.82mm LGA and 9mm × 15mm × 2.42mm BGA Packages

## APPLICATIONS

- FPGAs, GPUs and ASICs Applications
- PCIe and Backside PCB Mounting

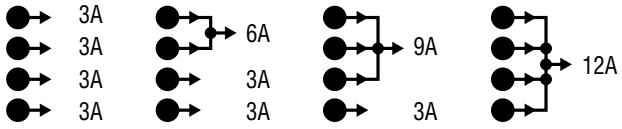


## DESCRIPTION

The LTM®4643 is a quad DC/DC step-down µModule (power module) regulator with 3A per output. Outputs can be paralleled in an array for up to 12A capability. Included in the package are the switching controllers, power FETs, inductors and support components. Operating over an input voltage range of 4V to 20V or 2.375V to 20V with an external bias supply, the LTM4643 supports an output voltage range of 0.6V to 3.3V each set by a single external resistor. Its high efficiency design delivers 3A continuous output current per channel. Only bulk input and output capacitors are needed.

Fault protection features include overvoltage, overcurrent and overtemperature protection. The LTM4643 is offered in a 9mm ×15mm × 1.82mm LGA and 9mm × 15mm × 2.42mm BGA packages with SnPb (BGA) or RoHS compliant terminal finish.

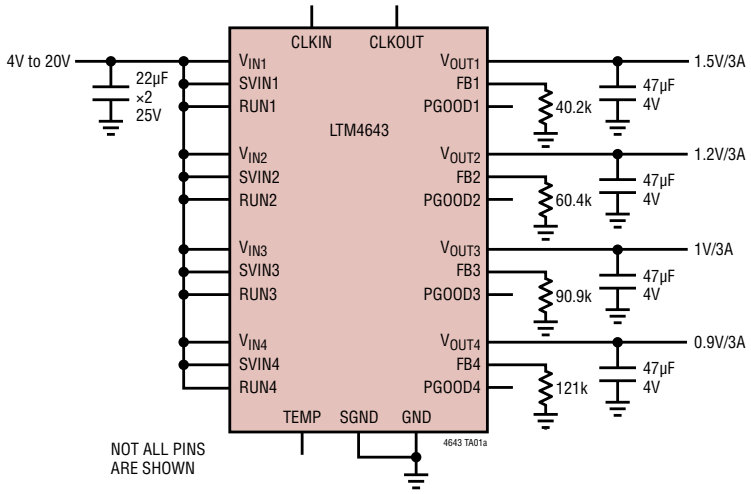
**Configurable Output Array***



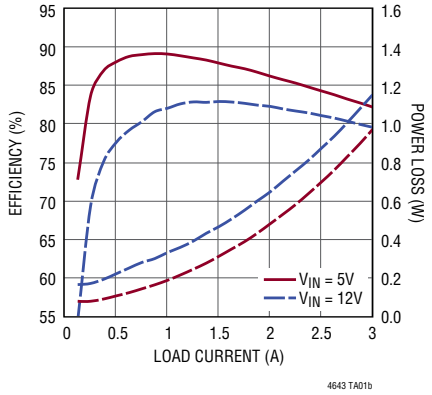

* Note 4

## TYPICAL APPLICATION

**4V to 20V Input, Quad 0.9V, 1V, 1.2V and 1.5V Output DC/DC µModule Regulator**




**1.5V Output Efficiency and Power Loss (Each Channel)**



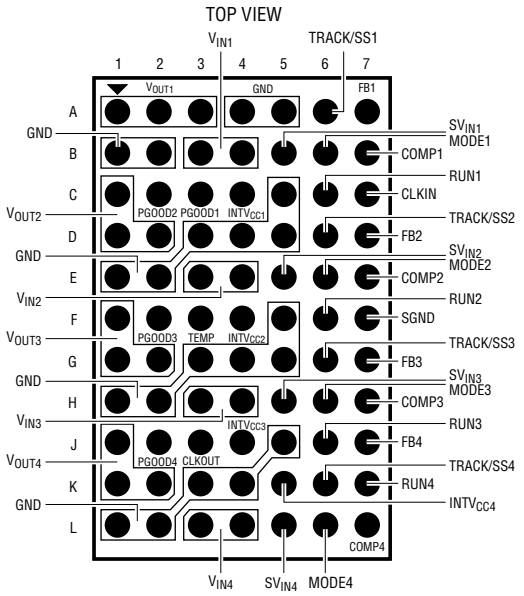

Rev D

## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$, $SV_{IN}$ (Per Channel)..... –0.3V to 22V
$V_{OUT}$ (Per Channel) (Note 3) .....–0.3V to $SV_{IN}$ or 6V
RUN (Per Channel)..... –0.3V to 22V
$INTV_{CC}$ (Per Channel) ..... –0.3V to 3.6V
PGOOD, MODE, TRACK/SS,
FB (Per Channel).....–0.3V to $INTV_{CC}$
CLKOUT (Note 3), CLKIN.....–0.3V to $INTV_{CC}$
Internal Operating Temperature Range
(Notes 2, 5).....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C
Peak Solder Reflow Body Temperature.....260°C

## PIN CONFIGURATION




LGA PACKAGE (WEIGHT = 0.70g)
77-LEAD (9mm × 15mm × 1.82mm)

BGA PACKAGE (WEIGHT = 0.83g)
77-LEAD (9mm × 15mm × 2.42mm)

$T_{JMAX}$ = 125°C, $\theta_{JCtop}$ = 17°C/W, $\theta_{JCbottom}$ = 2.75°C/W,
$\theta_{JB} + \theta_{BA}$ = 11°C/W, $\theta_{JA}$ = 10°C/W
θ VALUES PER JESD 51-12

## ORDER INFORMATION

| PART NUMBER | PAD OR BALL FINISH | PART MARKING* | | PACKAGE TYPE | MSL RATING | TEMPERATURE RANGE (SEE NOTE 2) |
|---|---|---|---|---|---|---|
| | | DEVICE | FINISH CODE | | | |
| LTM4643EV#PBF | Au (RoHS) | LTM4643V | e4 | LGA | 3 | –40°C to 125°C |
| LTM4643IV#PBF | Au (RoHS) | LTM4643V | e4 | LGA | 3 | –40°C to 125°C |
| LTM4643MPV#PBF | Au (RoHS) | LTM4643V | e4 | LGA | 3 | –55°C to 125°C |
| LTM4643EY#PBF | SAC305 (RoHS) | LTM4643Y | e1 | BGA | 3 | –40°C to 125°C |
| LTM4643IY#PBF | SAC305 (RoHS) | LTM4643Y | e1 | BGA | 3 | –40°C to 125°C |
| LTM4643MPY#PBF | SAC305 (RoHS) | LTM4643Y | e1 | BGA | 3 | –55°C to 125°C |
| LTM4643IY | SnPb (63/37) | LTM4643Y | e0 | BGA | 3 | –40°C to 125°C |
| LTM4643MPY | SnPb (63/37) | LTM4643Y | e0 | BGA | 3 | –55°C to 125°C |

- Contact the factory for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified internal operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2). $V_{IN}$ = 12V, per the typical application.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Switching Regulator Section: per Channel** | | | | | | | |
| $V_{IN}$, $SV_{IN}$ | Input DC Voltage | $SV_{IN}$ = $V_{IN}$ | ● | 4 | | 20 | V |
| $V_{OUT(RANGE)}$ | Output Voltage Range | | ● | 0.6 | | 3.3 | V |
| $V_{OUT(DC)}$ | Output Voltage, Total Variation with Line and Load | $C_{IN}$ = 22µF, $C_{OUT}$ = 100µF Ceramic, $R_{FB}$ = 40.2k, MODE = $INTV_{CC}$, $V_{IN}$ = 4V to 20V, $I_{OUT}$ = 0A to 3A (Note 4) | ● | 1.477 | 1.50 | 1.523 | V |
| $V_{RUN}$ | RUN Pin On Threshold | $V_{RUN}$ Rising | | 1.1 | 1.2 | 1.3 | V |
| $I_{Q(SVIN)}$ | Input Supply Bias Current | $V_{IN}$ = 12V, $V_{OUT}$ = 1.5V, MODE = $INTV_{CC}$<br>$V_{IN}$ = 12V, $V_{OUT}$ = 1.5V, MODE = GND<br>Shutdown, RUN = 0, $V_{IN}$ = 12V | | | 6<br>2<br>11 | | mA<br>mA<br>µA |
| $I_{S(VIN)}$ | Input Supply Current | $V_{IN}$ = 12V, $V_{OUT}$ = 1.5V, $I_{OUT}$ = 3A | | | 0.45 | | A |
| $I_{OUT(DC)}$ | Output Continuous Current Range | $V_{IN}$ = 12V, $V_{OUT}$ = 1.5V (Note 4) | | 0 | | 3 | A |
| $\Delta V_{OUT}$ (Line)/$V_{OUT}$ | Line Regulation Accuracy | $V_{OUT}$ = 1.5V, $V_{IN}$ = 4V to 20V, $I_{OUT}$ = 0A | ● | | 0.01 | 0.05 | %/V |
| $\Delta V_{OUT}$ (Load)/$V_{OUT}$ | Load Regulation Accuracy | $V_{OUT}$ = 1.5V, $I_{OUT}$ = 0A to 3A | ● | | 0.5 | 1.0 | % |
| $V_{OUT(AC)}$ | Output Ripple Voltage | $I_{OUT}$ = 0A, $C_{OUT}$ = 100µF Ceramic, $V_{IN}$ = 12V, $V_{OUT}$ = 1.5V | | | 5 | | mV |
| $\Delta V_{OUT(START)}$ | Turn-On Overshoot | $I_{OUT}$ = 0A, $C_{OUT}$ = 100µF Ceramic, $V_{IN}$ = 12V, $V_{OUT}$ = 1.5V | | | 30 | | mV |
| $t_{START}$ | Turn-On Time | $C_{OUT}$ = 100µF Ceramic, No Load, TRACK/SS = 0.01µF, $V_{IN}$ = 12V, $V_{OUT}$ = 1.5V | | | 2.5 | | ms |
| $\Delta V_{OUTLS}$ | Peak Deviation for Dynamic Load | Load: 0% to 50% to 0% of Full Load, $C_{OUT}$ = 47µF Ceramic, $V_{IN}$ = 12V, $V_{OUT}$ = 1.5V | | | 160 | | mV |
| $t_{SETTLE}$ | Settling Time for Dynamic Load Step | Load: 0% to 50% to 0% of Full Load, $C_{OUT}$ = 47µF Ceramic, $V_{IN}$ = 12V, $V_{OUT}$ = 1.5V | | | 40 | | µs |
| $I_{OUTPK}$ | Output Current Limit | $V_{IN}$ = 12V, $V_{OUT}$ = 1.5V | | 3.5 | 5 | | A |
| $V_{FB}$ | Voltage at FB Pin | $I_{OUT}$ = 0A, $V_{OUT}$ = 1.5V, –40°C to 125°C | ● | 0.593 | 0.60 | 0.607 | V |
| $I_{FB}$ | Current at FB Pin | (Note 3) | | | | ±30 | nA |
| $R_{FBHI}$ | Resistor Between $V_{OUT}$ and FB Pins | | | 60.05 | 60.40 | 60.75 | kΩ |
| $I_{TRACK/SS}$ | Track Pin Soft-Start Pull-Up Current | TRACK/SS = 0V | | | 2.5 | 4 | µA |
| $V_{IN(UVLO)}$ | $V_{IN}$ Undervoltage Lockout | $V_{IN}$ Falling<br>$V_{IN}$ Hysteresis | | 2.4 | 2.6<br>350 | 2.8 | V<br>mV |
| $t_{ON(MIN)}$ | Minimum On-Time | (Note 3) | | | 40 | | ns |
| $t_{OFF(MIN)}$ | Minimum Off-Time | (Note 3) | | | 70 | | ns |
| $V_{PGOOD}$ | PGOOD Trip Level | $V_{FB}$ With Respect to Set Output<br>$V_{FB}$ Ramping Negative<br>$V_{FB}$ Ramping Positive | | <br>–13<br>7 | <br>–10<br>10 | <br>–7<br>13 | <br>%<br>% |
| $I_{PGOOD}$ | PGOOD Leakage | | | | | 2 | µA |
| $V_{PGL}$ | PGOOD Voltage Low | $I_{PGOOD}$ = 1mA | | | 0.02 | 0.1 | V |
| $V_{INTVCC}$ | Internal $V_{CC}$ Voltage | $SV_{IN}$ = 4V to 20V | | 3.1 | 3.3 | 3.4 | V |
| $V_{INTVCC}$ Load Reg | $INTV_{CC}$ Load Regulation | $I_{CC}$ = 0mA to 20mA | | | 0.5 | | % |
| $f_{OSC}$ | Oscillator Frequency | | | | 1.2 | | MHz |
| CLKIN | CLKIN Threshold | | | | 0.7 | | V |

## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTM4643 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4643E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4643I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM4643MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

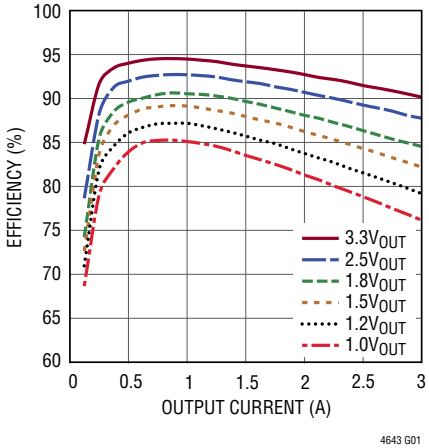
**Note 3:** 100% tested at wafer level.

**Note 4:** See output current derating curves for different $V_{IN}$, $V_{OUT}$ and $T_A$.

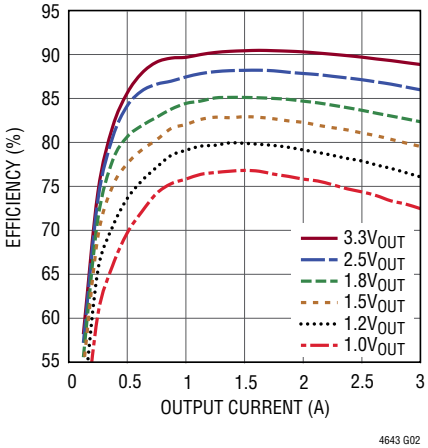
**Note 5:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

## TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

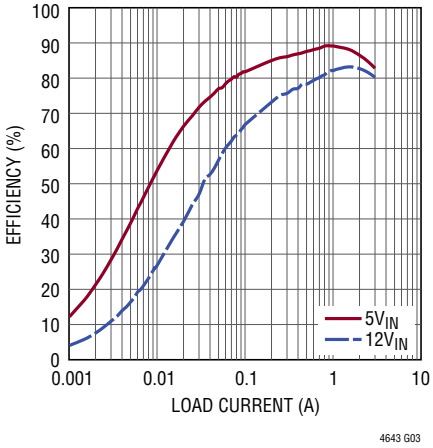
**Efficiency vs Load Current from $5V_{IN}$ (One Channel Operating)**



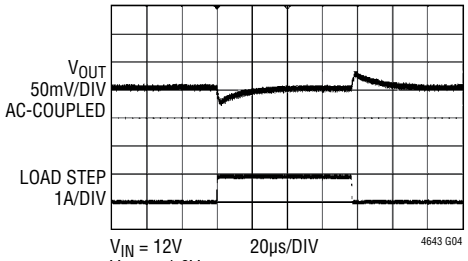

**Efficiency vs Load Current from $12V_{IN}$ (One Channel Operating)**




**DCM Mode Efficiency from $1.5V_{OUT}$**

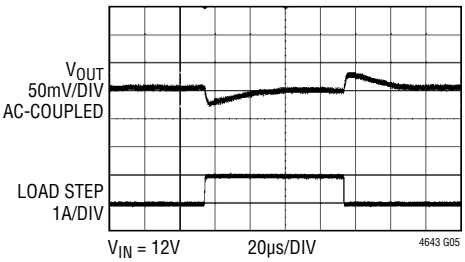



**1.0V Output Transient Response**



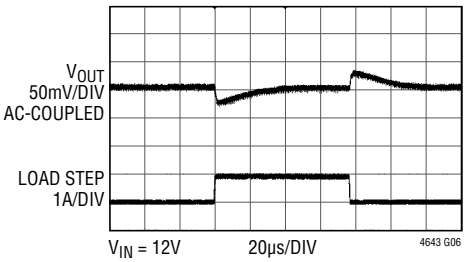

$V_{IN}$ = 12V 20µs/DIV
$V_{OUT}$ = 1.0V
OUTPUT CAPACITOR = 1 × 47µF CERAMIC CAP
LOAD STEP = 2A TO 3A WITH 1A/µS SLEW RATE
FEED FORWARD CAP = 100pF

**1.2V Output Transient Response**




$V_{IN}$ = 12V 20µs/DIV
$V_{OUT}$ = 1.2V
OUTPUT CAPACITOR = 1 × 47µF CERAMIC CAP
LOAD STEP = 2A TO 3A WITH 1A/µS SLEW RATE
FEED FORWARD CAP = 100pF

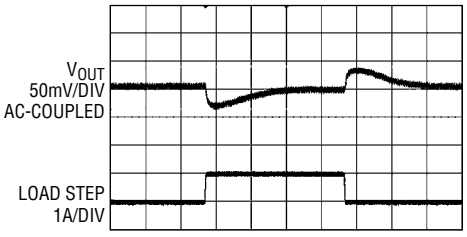
**1.5V Output Transient Response**




$V_{IN}$ = 12V 20µs/DIV
$V_{OUT}$ = 1.5V
OUTPUT CAPACITOR = 1 × 47µF CERAMIC CAP
LOAD STEP = 2A TO 3A WITH 1A/µS SLEW RATE
FEED FORWARD CAP = 100pF

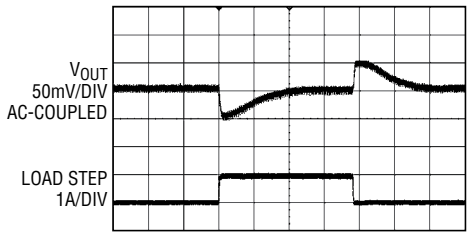
# TYPICAL PERFORMANCE CHARACTERISTICS

### 1.8V Output Transient Response



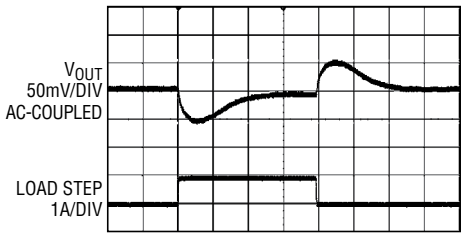

$V_{IN}$ = 12V 20µs/DIV
$V_{OUT}$ = 1.8V
OUTPUT CAPACITOR = 1 × 47µF CERAMIC CAP
LOAD STEP = 2A TO 3A WITH 1A/µS SLEW RATE
FEED FORWARD CAP = 100pF

### 2.5V Output Transient Response



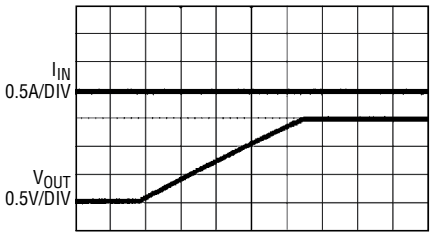

$V_{IN}$ = 12V 20µs/DIV
$V_{OUT}$ = 2.5V
OUTPUT CAPACITOR = 1 × 47µF CERAMIC CAP
LOAD STEP = 2A TO 3A WITH 1A/µS SLEW RATE
FEED FORWARD CAP = 100pF

### 3.3V Output Transient Response



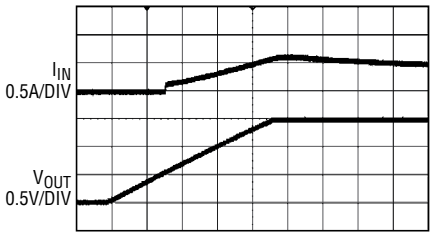

$V_{IN}$ = 12V 20µs/DIV
$V_{OUT}$ = 3.3V
OUTPUT CAPACITOR = 1 × 47µF CERAMIC CAP
LOAD STEP = 2A TO 3A WITH 1A/µS SLEW RATE
FEED FORWARD CAP = 100pF

### Start-Up with No Load Applied



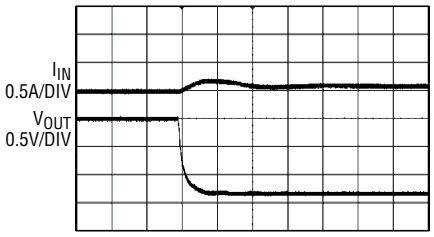

$V_{IN}$ = 12V 5ms/DIV
$V_{OUT}$ = 1.5V
INPUT CAPACITOR = 1 × 22µF CERAMIC CAP
OUTPUT CAPACITOR = 1 × 47µF CERAMIC CAP
SOFT START = 0.1µF

### Start-Up with 3A Load Applied



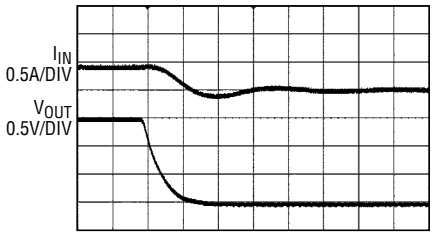

$V_{IN}$ = 12V 5ms/DIV
$V_{OUT}$ = 1.5V
INPUT CAPACITOR = 1 × 22µF CERAMIC CAP
OUTPUT CAPACITOR = 1 × 47µF CERAMIC CAP
SOFT START = 0.1µF

### Short-Circuit with No Load Applied



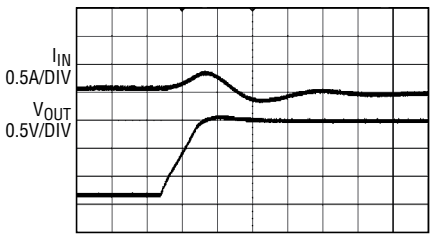

$V_{IN}$ = 12V 5ms/DIV
$V_{OUT}$ = 1.5V
INPUT CAPACITOR = 1 × 22µF CERAMIC CAP
OUTPUT CAPACITOR = 1 × 47µF CERAMIC CAP

### Short-Circuit with 3A Load Applied



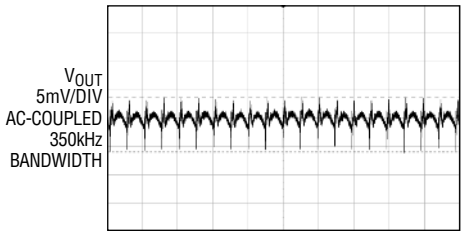

$V_{IN}$ = 12V 20µs/DIV
$V_{OUT}$ = 1.5V
INPUT CAPACITOR = 1 × 22µF CERAMIC CAP
OUTPUT CAPACITOR = 1 × 47µF CERAMIC CAP

### Short-Circuit with 3A Load Applied




$V_{IN}$ = 12V 20µs/DIV
$V_{OUT}$ = 1.5V
INPUT CAPACITOR = 1 × 22µF CERAMIC CAP
OUTPUT CAPACITOR = 1 × 47µF CERAMIC CAP

### Output Ripple




$V_{IN}$ = 12V 2µs/DIV
$V_{OUT}$ = 1.5V
OUTPUT CAPACITOR = 2 × 47µF CERAMIC CAP

## PIN FUNCTIONS

**PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.**

**$V_{OUT1}$ (A1, A2, A3), $V_{OUT2}$ (C1, D1, D2), $V_{OUT3}$ (F1, G1, G2), $V_{OUT4}$ (J1, K1, K2):** Power Output Pins of Each Switching Mode Regulator Channel. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See the Applications Information section for paralleling outputs.

**GND (A4-A5, B1-B2, C5, D3-D5, E1-E2, F5, G3-G5, H1-H2, J5, K3-K4, L1-L2):** Power Ground Pins for Both Input and Output Returns. Use large PCB copper areas to connect all GND together.

**$V_{IN1}$ (B3, B4), $V_{IN2}$ (E3, E4), $V_{IN3}$ (H3, H4), $V_{IN4}$ (L3, L4):** Power input pins connect to the drain of the internal top MOSFET for each switching mode regulator channel. Apply input voltages between these pins and GND pins. Recommend placing input decoupling capacitance directly between each of $V_{IN}$ pins and GND pins.

**PGOOD1, PGOOD2, PGOOD3, PGOOD4 (C3, C2, F2, J2):** Output Power Good with Open-Drain Logic of Each Switching Mode Regulator Channel. PGOOD is pulled to ground when the voltage on the FB pin is not within ±10% of the internal 0.6V reference.

**CLKOUT (J3):** Output Clock Signal for PolyPhase® Operation of the Module. The phase of CLKOUT with respect to CLKIN is set to 180°. CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND. See the Applications Information section for details. Strictly output; do not drive this pin. CLKOUT is only active when RUN4 is enabled.

**$INTV_{CC1}$, $INTV_{CC2}$, $INTV_{CC3}$, $INTV_{CC4}$ (C4, F4, J4, K5):** Internal 3.3V Regulator Output of Each Switching Mode Regulator Channel. The internal power drivers and control circuits are powered from this voltage. Each pin is internally decoupled to GND with 1µF low ESR ceramic capacitor already.

**$SV_{IN1}$, $SV_{IN2}$, $SV_{IN}$, $SV_{IN4}$ (B5, E5, H5, L5):** Signal $V_{IN}$. Filtered input voltage to the internal 3.3V regulator for the control circuitry of each Switching mode Regulator Channel. Tie this pin to the $V_{IN}$ pin respectively in most applications. Connect $SV_{IN}$ to an external voltage supply of at least 4V which must also be greater than $V_{OUT}$.

**TRACK/SS1, TRACK/SS2, TRACK/SS3, TRACK/SS4 (A6, D6, G6, K6):** Output Tracking and Soft-Start Pin of Each Switching Mode Regulator Channel. Allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to match the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 2.5µA pull-up current from $INTV_{CC}$ on this pin, so putting a capacitor here provides soft-start function.

**MODE1, MODE2, MODE3, MODE4 (B6, E6, H6, L6):** Operation Mode Select for Each Switching Mode Regulator Channel. Tie this pin to $INTV_{CC}$ to force continuous synchronous operation at all output loads. Tying it to SGND enables discontinuous current mode operation at light loads. Do not leave floating.

**RUN1, RUN2, RUN3, RUN4 (C6, F6, J6, K7):** Run Control Input of Each Switching Mode Regulator Channel. Enable regulator operation by tying the specific RUN pin above 1.2V. Pulling it below 1.1V shuts down the respective regulator channel. Do not leave floating.

**FB1, FB2, FB3, FB4 (A7, D7, G7, J7):** The Negative Input of the Error Amplifier for Each Switching Mode Regulator Channel. Internally, this pin is connected to $V_{OUT}$ of each channel with a 60.4kΩ precision resistor. Different output voltages can be programmed with an additional resistor between the FB and GND pins. In PolyPhase operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

## PIN FUNCTIONS

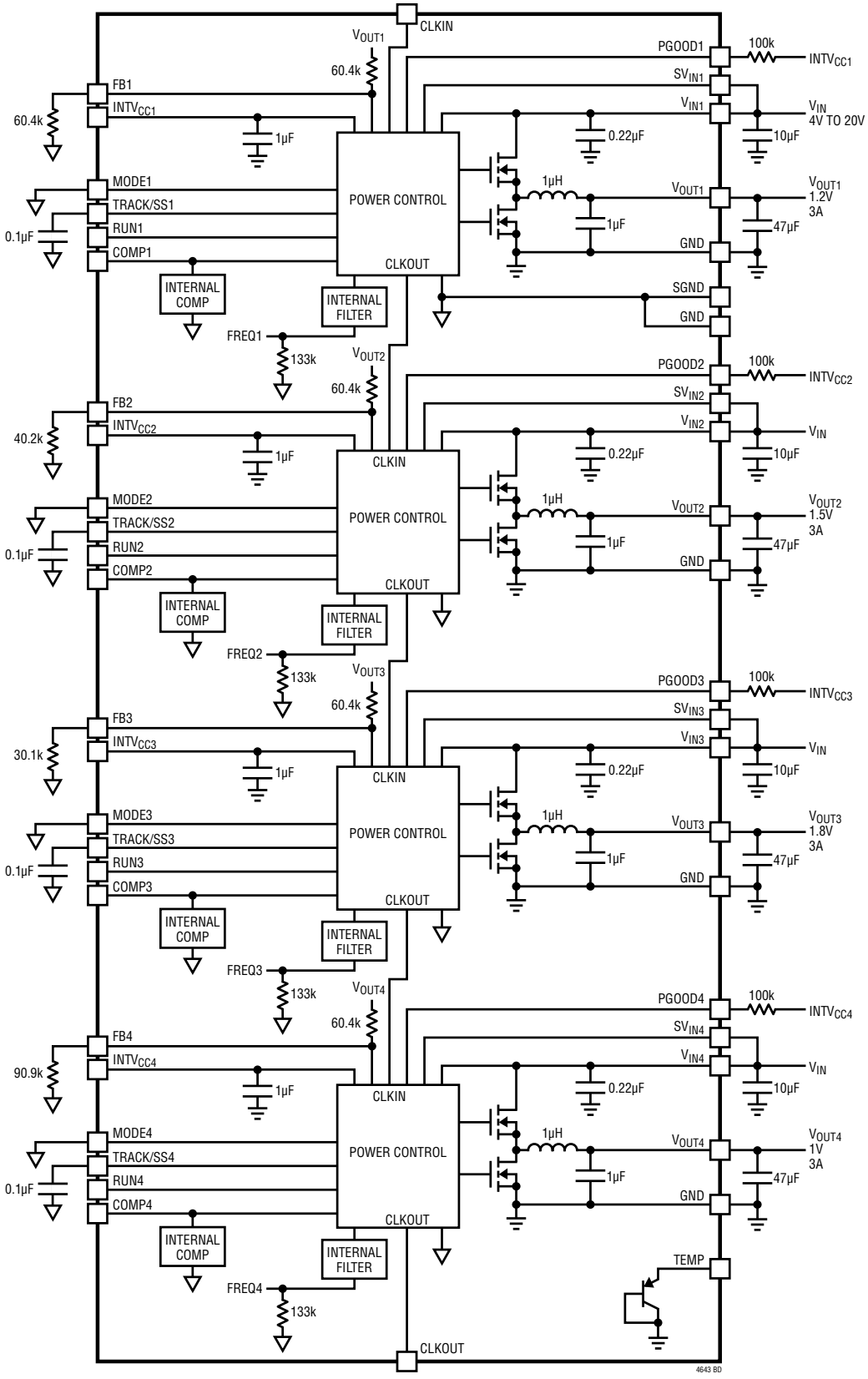
**COMP1, COMP2, COMP3, COMP4 (B7, E7, H7, L7):** Current Control Threshold and Error Amplifier Compensation Point of Each Switching Mode Regulator Channel. The internal current comparator threshold is proportional to this voltage. Tie the COMP pins together for parallel operation. The device is internally compensated.

**CLKIN (C7):** External Synchronization Input to Phase Detector of the Module. This pin is internally terminated to SGND with 20kΩ. The phase-locked loop will force the channel 1 turn-on signal to be synchronized with the rising edge of the CLKIN signal. Channel 2, channel 3 and channel 4 will also be synchronized with the rising edge of the CLKIN signal with a pre-determined phase shift. See the Applications Information section for details.

**SGND (F7):** Signal Ground Connection. SGND is connected to GND internally through single point. Use a separated SGND ground copper area for the ground of the feedback resistor and other components connected to signal pins. A second connection between the PGND plane and SGND plane is recommended on the backside of the PCB underneath the module.

**TEMP (F3):** Onboard Temperature Diode for Monitoring the VBE Junction Voltage Change with Temperature. See the Applications Information section.

## BLOCK DIAGRAM



## DECOUPLING REQUIREMENTS (per Channel)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $C_{IN}$ | External Input Capacitor Requirement ($V_{IN}$ = 4V to 20V, $V_{OUT}$ = 1.5V) | $I_{OUT}$ = 3A | 4.7 | 10 | | µF |
| $C_{OUT}$ | External Output Capacitor Requirement ($V_{IN}$ = 4V to 20V, $V_{OUT}$ = 1.5V) | $I_{OUT}$ = 3A | 22 | 47 | | µF |

## OPERATION

The LTM4643 is a quad output standalone non-isolated switch mode DC/DC power supply in 9mm × 15mm × 1.82mm ultrathin package. It has four separate regulator channels with each of them capable of delivering up to 3A continuous output current with few external input and output capacitors. Each regulator provides precisely regulated output voltage programmable from 0.6V to 3.3V via a single external resistor over 4V to 20V input voltage range. With an external bias voltage, this module can operate from an input voltage as low as 2.375V. The typical application schematic is shown in Figure 29.

The LTM4643 integrates four separate constant frequency controlled on-time valley current mode regulators, power MOSFETs, inductors, and other supporting discrete components. The typical switching frequency is set to 1.2MHz. For switching noise-sensitive applications, the µModule regulator can be externally synchronized to a clock from 850kHz to 1.5MHz. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4643 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides the flexibility of paralleling any of the separate regulator channels with accurate current sharing. With a built-in clock interleaving between regulator channels, the LTM4643 can easily be configured for 2+2, 3+1 or 4 channels parallel operation providing more design flexibility for multirail POL applications. Furthermore, the LTM4643 has CLKIN and CLKOUT pins for frequency synchronization or polyphasing multiple devices which allow up to 8 phases cascaded to run simultaneously.

Current mode control also provides cycle-by-cycle fast current monitoring. Foldback current limiting is provided in an overcurrent condition to reduce the inductor valley current to approximately 40% of the original value when $V_{FB}$ drops. An internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Continuous conduction mode (CCM) operation is forced during OV and UV conditions except during start-up when the TRACK pin is ramping up to 0.6V.

Pulling the RUN pin below 1.1V forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, discontinuous conduction mode (DCM) operation can be enabled to achieve higher efficiency compared to continuous conduction mode (CCM) by setting the MODE pin to SGND. The TRACK/SS pin is used for power supply tracking and soft-start programming. See the Applications Information section.

A temperature diode is included inside the module to monitor the temperature of the module. See the Applications Information section for details.

## APPLICATIONS INFORMATION

The typical LTM4643 application circuit is shown in Figure 29. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. Refer to Table 6 for specific external capacitor requirements for a particular application.

### $V_{IN}$ to $V_{OUT}$ Step-Down Ratios

There are restrictions in the maximum $V_{IN}$ and $V_{OUT}$ step-down ratio that can be achieved for a given input voltage due to the minimum off-time and minimum on-time limits of each regulator. The minimum off-time limit imposes a maximum duty cycle which can be calculated as:

$$D_{MAX} = 1 - t_{OFF(MIN)} \bullet f_{SW}$$

where $t_{OFF(MIN)}$ is the minimum off-time, 70ns typical for LTM4643, and $f_{SW}$ is the switching frequency. Conversely the minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated as:

$$D_{MIN} = t_{ON(MIN)} \bullet f_{SW}$$

where $t_{ON(MIN)}$ is the minimum on-time, 40ns typical for LTM4643. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. Note that additional thermal derating may be applied. See the Thermal Considerations and Output Current Derating section in this data sheet.

### Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k internal feedback resistor connects each regulator channel from $V_{OUT}$ pin to FB pin. Adding a resistor $R_{FB}$ from FB pin to GND programs the output voltage:

$$R_{FB} = \frac{60.4k}{\frac{V_{OUT}}{0.6} - 1}$$

**Table 1. $V_{FB}$ Resistor Table vs Various Output Voltages**

| $V_{OUT}$ (V) | 0.6 | 1.0 | 1.2 | 1.5 | 1.8 | 2.5 | 3.3 |
|---|---|---|---|---|---|---|---|
| $R_{FB}$ (k) | Open | 90.9 | 60.4 | 40.2 | 30.1 | 19.1 | 13.3 |

For parallel operation of N channels, use the following equation can be used to solve for $R_{FB}$. Tie the $V_{OUT}$ and the FB and COMP pins together for each paralleled output with a single resistor to GND as determined by:

$$R_{FB} = \frac{\left(\frac{60.4k}{N}\right)}{\left(\frac{V_{OUT}}{0.6} - 1\right)}$$

### Input Decoupling Capacitors

The LTM4643 module should be connected to a low AC-impedance DC source. For each regulator channel, a 10µF input ceramic capacitor is recommended for RMS ripple current decoupling. A bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor or polymer capacitor.

Without considering the inductor ripple current, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1 - D)}$$

where $\eta\%$ is the estimated efficiency of the power module.

### Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only single piece of low ESR output ceramic capacitor is required for each regulator channel to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 6 provides a reference matrix showing transient performance for different output capacitor configurations. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more a function of stability and transient response. The LTpowerCAD® Design Tool is available to download online for output ripple, stability and transient response analysis and calculating the output ripple reduction as the number of phases implemented increases by N times.

## APPLICATIONS INFORMATION

### Discontinuous Conduction Mode (DCM)

In applications where low output ripple and high efficiency at intermediate current are desired, discontinuous conduction mode (DCM) should be used by connecting the MODE pin to SGND. At light loads the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode.

### Force Continuous Conduction Mode (CCM)

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous conduction mode operation should be used. Forced continuous operation can be enabled by tying the MODE pin to $INTV_{CC}$. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4643's output voltage is in regulation.

### Operating Frequency

The operating frequency of the LTM4643 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. The default operating frequency is internally set to 1.2MHz. In most applications, no additional frequency adjusting is required.

If any operating frequency other than 1.2MHz is required by application, the µModule regulator can be externally synchronized to a clock from 850kHz to 1.5MHz.

Please note, a minimum switching frequency is required for given $V_{IN}$, $V_{OUT}$ operating conditions to keep a maximum peak-to-peak inductor ripple current below 2A for the LTM4643. The peak-to-peak inductor ripple current can be calculated as:

$$\Delta I_{PK-PK} = \frac{V_{OUT}}{F_S(MHz)} \bullet \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The maximum 2A peak-to-peak inductor ripple current is enforced due to the nature of the valley current mode control to maintain output voltage regulation at no load.

### Frequency Synchronization and Clock In

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows all internal top MOSFET turn-on to be locked to the rising edge of the same external clock. The external clock frequency range must be within ±30% around the 1.2MHz set frequency. A pulse detection circuit is used to detect a clock on the CLKIN pin to turn on the phase-locked loop. The pulse width of the clock has to be at least 100ns. The clock high level must be above 2V and clock low level below 0.3V. During the start-up of the regulator, the phase-locked loop function is disabled.

### Multichannel Parallel Operation

For loads that demand more than 3A of output current, the LTM4643 multiple regulator channels can be easily paralleled to provide more output current without increasing input and output voltage ripples. The LTM4643 has preset built-in phase shift between each two of the four regulator channels which is suitable to employ a 2+2, 3+1 or 4 channels parallel operation. Table 2 gives the phase difference between regulator channels.

**Table 2. Phase Difference Between Regulator Channels**

| CHANNEL | CH1 | CH2 | CH3 | CH4 |
|---|---|---|---|---|
| Phase Difference | 180° | 90° | 180° | |

Figure 1 shows a 2+2 and a 4-channels parallel concept schematic for clock phasing.

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

## APPLICATIONS INFORMATION

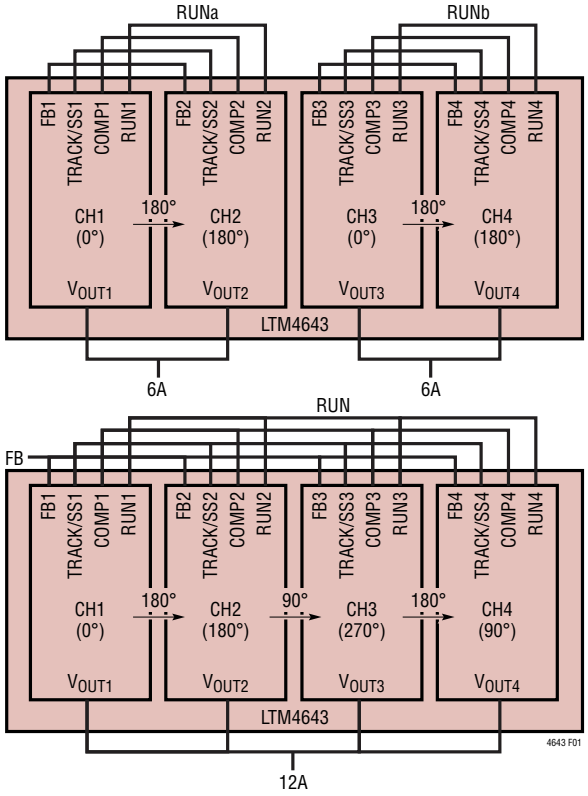



**Figure 1. 2+2 and 4 Channels Parallel Concept Schematic**

The LTM4643 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Please tie the RUN, TRACK/SS, FB and COMP pins of each paralleling channel together. Figure 31 and Figure 32 show an example of parallel operation and pin connection.

### Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 2 shows this graph.

### Soft-Start and Output Voltage Tracking

The TRACK/SS pin provides a means to either soft-start of each regulator channel or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the output voltage. An internal 2.5µA current source will charge up the external soft-start capacitor

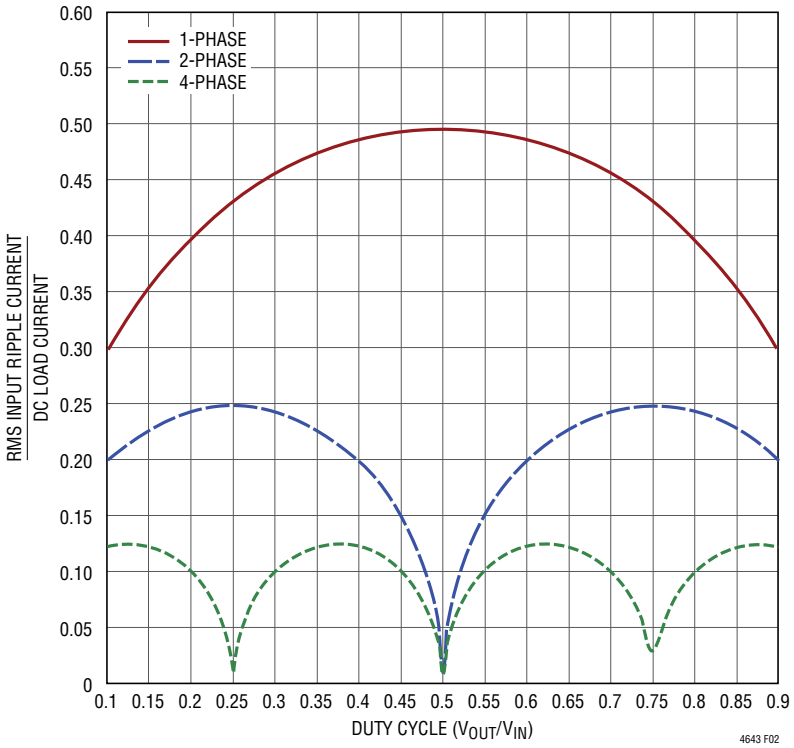



**Figure 2. Normalized RMS Ripple Current for Single Phase or Polyphase Applications**

## APPLICATIONS INFORMATION

towards the $INTV_{CC}$ voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated as:

$$t_{SS} = 0.6 \bullet \frac{C_{SS}}{2.5\mu A}$$

where $C_{SS}$ is the capacitance on the TRACK/SS pin. Current foldback and forced continuous mode are disabled during the soft-start process.

Output voltage tracking can also be programmed externally using the TRACK/SS pin of each regulator channel. The output can be tracked up and down with another regulator. Figure 3 and Figure 4 show an example waveform and schematic of a ratiometric tracking where the slave regulator's ($V_{OUT2}$, $V_{OUT3}$ and $V_{OUT4}$) output slew rate is proportional to the master's ($V_{OUT1}$).

Since the slave regulator's TRACK/SS is connected to the master's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the slave output

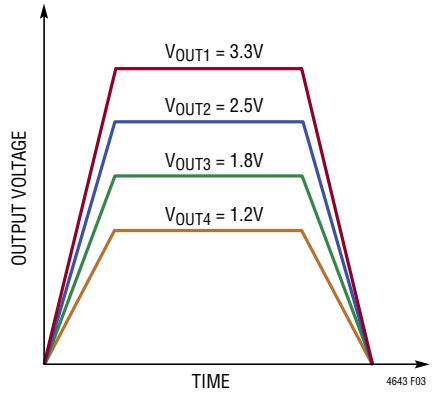



**Figure 3. Output Ratiometric Tracking Waveform**

voltage when TRACK/SS voltage is below 0.6V, the slave output voltage and the master output voltage should satisfy the following equation during the start-up.

$$V_{OUT(SL)} \bullet \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = V_{OUT(MA)} \bullet \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

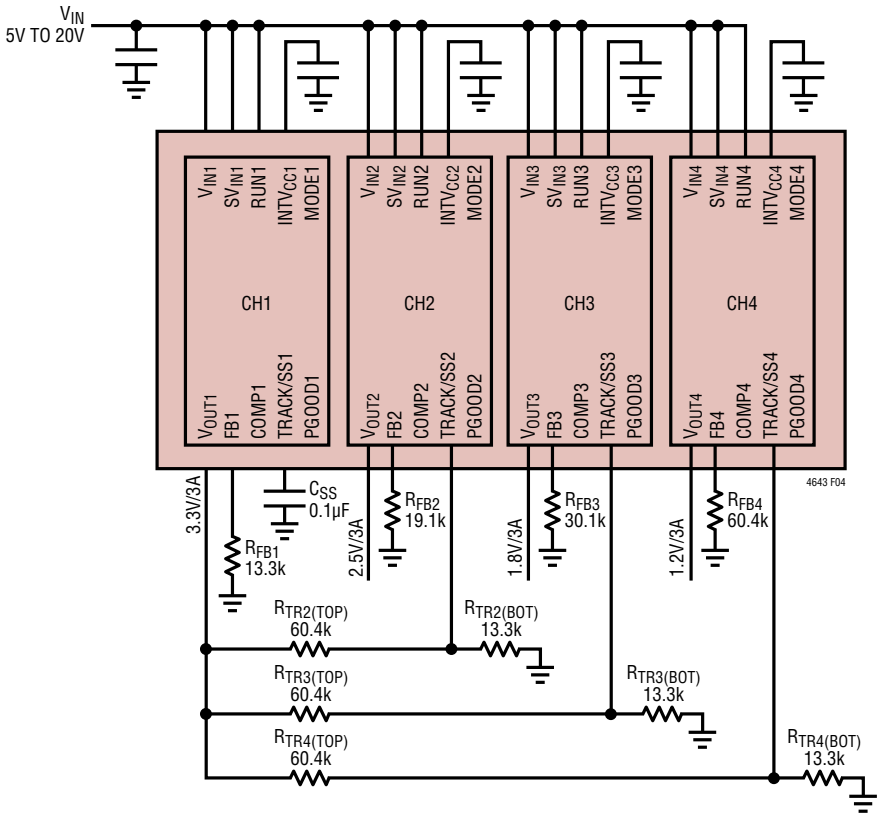



**Figure 4. Output Ratiometric Tracking Schematic**

## APPLICATIONS INFORMATION

The $R_{FB(SL)}$ is the feedback resistor and the $R_{TR(TOP)}$/$R_{TR(BOT)}$ is the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 4.

Following the upper equation, the master's output slew rate (MR) and the slave's output slew rate (SR) in volts/time is determined by:

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}}$$

For example, $V_{OUT(MA)}$ = 3.3V, MR = 3.3V/ms and $V_{OUT(SL)}$ = 1.2V, SR = 1.2V/ms as $V_{OUT1}$ and $V_{OUT4}$ shown in Figure 4. From the equation, we could solve out that $R_{TR4(TOP)}$ = 60.4k and $R_{TR4(BOT)}$ = 13.3k is a good combination. Follow the same equation, we can get the same $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider value for $V_{OUT2}$ and $V_{OUT3}$.

The TRACK pins will have the 2.5µA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller value resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK pin offset to a negligible value.

The coincident output tracking can be recognized as a special ratiometric output tracking which the master's output slew rate (MR) is the same as the slave's output slew rate (SR), as waveform shown in Figure 5.

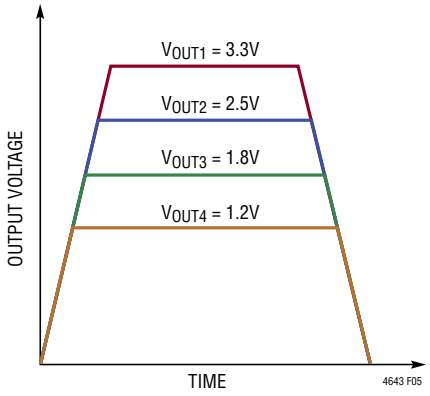



**Figure 5. Output Coincident Tracking Waveform**

From the equation we could easily find out that, in the coincident tracking, the slave regulator's TRACK/SS pin resistor divider is always the same as its output voltage divider.

$$\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

For example, $R_{TR4(TOP)}$ = 60.4k and $R_{TR4(BOT)}$ = 60.4k is a good combination for coincident tracking for $V_{OUT(MA)}$ = 3.3V and $V_{OUT(SL)}$ = 1.2V application.

### Power Good

The PGOOD pins are open drain pins that can be used to monitor each valid output voltage regulation. This pin monitors a ±10% window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. To prevent unwanted PGOOD glitches during transients or dynamic $V_{OUT}$ changes, the LTM4643's PGOOD falling edge includes a blanking delay of approximately 52 switching cycles.

### Stability Compensation

The LTM4643 module internal compensation loop of each regulator channel is designed and optimized for low ESR ceramic output capacitors only application. Table 6 is provided for most application requirements. An optional 100pF phase boost capacitor could help to boost up the phase margin in all ceramic output capacitors application. The LTpowerCAD Design Tool is available to download for control loop optimization.

### RUN Enable

Pulling the RUN pin of each regulator channel to ground forces the regulator into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 0.7V turns on the internal reference only, while still keeping the power MOSFETs off. Further increasing the RUN pin voltage above 1.2V will turn on the entire regulator channel.

## APPLICATIONS INFORMATION

### Pre-Biased Output Start-Up

There may be situations that require the power supply to start up with some charge on the output capacitors. The LTM4643 can safely power up into a pre-biased output without discharging it.

The LTM4643 accomplishes this by forcing discontinuous mode (DCM) operation until the TRACK/SS pin voltage reaches 0.6V reference voltage. This will prevent the BG from turning on during the pre-biased output start-up which would discharge the output.

Do not pre-bias LTM4643 with an output voltage higher than $INTV_{CC}$ (3.3V).

### Overtemperature Protection

The internal overtemperature protection monitors the junction temperature of the module. If the junction temperature reaches approximately 160°C, both power switches will be turned off until the temperature drops about 15°C cooler.

### Low Input Application

The LTM4643 module has a separate $SV_{IN}$ pin for each regulator channel which makes it compatible with operation from an input voltage as low as 2.375V. The $SV_{IN}$ pin is the signal input of the regulator control circuitry while the $V_{IN}$ pin is the power input which directly connected to the drain of the top MOSFET. In most application with input voltage ranges from 4V to 20V, connect the $SV_{IN}$ pin directly to the $V_{IN}$ pin of each regulator channel. An optional filter, consisting of a resistor (1Ω to 10Ω) between $SV_{IN}$ and $V_{IN}$ ground, can be placed for additional noise immunity. This filter is not necessary in most cases if good PCB layout practices are followed (see Figure 28). In a low input voltage (2.375V to 4V) application, or to reduce power dissipation by the internal bias LDO, connect $SV_{IN}$ to an external voltage higher than 4V with a 0.1µF local bypass capacitor. Figure 30 shows an example of a low input voltage application. Please note, $SV_{IN}$ voltage cannot go below $V_{OUT}$ voltage.

### Temperature Monitoring

A diode connected PNP transistor is used for the TEMP monitor function by monitoring its voltage over temperature. The temperature dependence of this diode voltage can be understood in the equation:

$$V_D = nV_T \ln\left(\frac{I_D}{I_S}\right)$$

where $V_T$ is the thermal voltage (kT/q), and n, the ideality factor, is 1 for the diode connected PNP transistor being used in the LTM4643. $I_S$ is expressed by the typical empirical equation:

$$I_S = I_0 \exp\left(\frac{-V_{G0}}{V_T}\right)$$

where $I_0$ is a process and geometry dependent current, ($I_0$ is typically around 20k orders of magnitude larger than $I_S$ at room temperature) and $V_{G0}$ is the band gap voltage of 1.2V extrapolated to absolute zero or –273°C.

If we take the $I_S$ equation and substitute into the $V_D$ equation, then we get:

$$V_D = V_{G0} - \left(\frac{kT}{q}\right)\ln\left(\frac{I_0}{I_D}\right),\ V_T = \frac{kT}{q}$$

The expression shows that the diode voltage decreases (linearly if $I_0$ were constant) with increasing temperature and constant diode current. Figure 6 shows a plot of $V_D$ vs Temperature over the operating temperature range of the LTM4643.

If we take this equation and differentiate it with respect to temperature T, then:

$$\frac{dV_D}{dT} = -\frac{V_{G0} - V_D}{T}$$

This $dV_D/dT$ term is the temperature coefficient equal to about –2mV/K or –2mV/°C. The equation is simplified for the first order derivation.

Solving for T, $T = -(V_{G0} - V_D)/(dV_D/dT)$ provides the temperature.

## APPLICATIONS INFORMATION

1st Example: Figure 6 for 27°C, or 300K the diode voltage is 0.598V, thus, 300K = –(1200mV – 598mV)/ –2.0 mV/K)

2nd Example: Figure 6 for 75°C, or 350K the diode voltage is 0.50V, thus, 350K = –(1200mV – 500mV)/ –2.0mV/K)

Converting the Kelvin scale to Celsius is simply taking the Kelvin temp and subtracting 273 from it.

A typical forward voltage is given in the Electrical Characteristics section of the data sheet, and Figure 6 is the plot of this forward voltage. Measure this forward voltage at 27°C to establish a reference point. Then using the above expression while measuring the forward voltage over temperature will provide a general temperature monitor. Connect a resistor between TEMP and $V_{IN}$ to set the current to 100µA. See Figure 31 for an example.

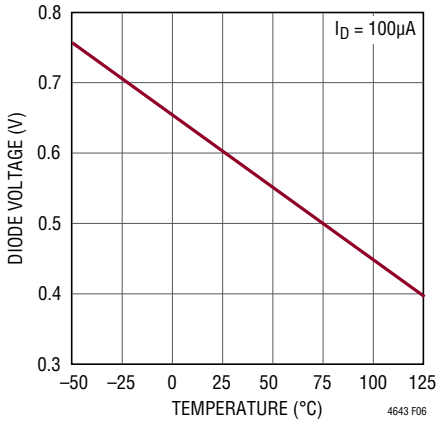



**Figure 6. Diode Voltage $V_D$ vs Temperature T(°C)**

### Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD 51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board: defined by JESD 51-9 (“Test Boards for Area Array Surface Mount Package Thermal Measurements”). The motivation for providing these thermal coefficients in found in JESD 51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. $\theta_{JA}$, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the page. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don’t generally match the user’s application.
3. $\theta_{JCtop}$, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the

## APPLICATIONS INFORMATION

package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4. $\theta_{JB}$, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package.

A graphical representation of the aforementioned thermal resistances is given in Figure 7; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for $\theta_{JCtop}$ and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4643, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4643 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD 51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4643 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss

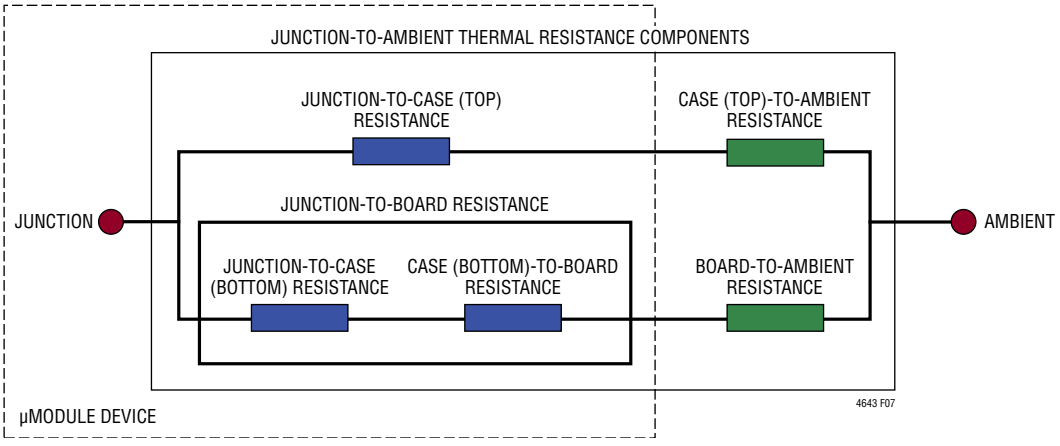



**Figure 7. Graphical Representation of JESD 51-12 Thermal Coefficients**

## APPLICATIONS INFORMATION

as that which was simulated. An outcome of this process and due diligence yields the set of derating curves shown in this data sheet.

The 1V to 3.3V power loss curves in Figures 8 to 13 can be used in coordination with the load current derating curves in Figures 14 to 25 for calculating an approximate $\theta_{JA}$ thermal resistance for the LTM4643 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with a multiplicative factor according to the junction temperature. This approximate factor is 1.3 for 120°C. The derating curves are plotted with the output current starting at 12A and the ambient temperature starting at 30°C. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example, in Figure 19 the load current is derated to 10A at ~67°C with 200LFM of airflow and no heat sink and the power loss for the 12V to 1.5V at 10A output is about 4.5W. The 4.5W loss is calculated with 4 times the 0.87W room temperature loss from the 12V to 1.5V power loss curve each channel at 2.5A, and the 1.3 multiplying factor at 120°C junction. If the 67°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 53°C divided by 4.5W equals 11.7°C/W $\theta_{JA}$ thermal resistance. Table 3 specifies a 12°C/W value which is very close. Tables 3 to 5 provide equivalent thermal resistances for the different outputs with and without airflow and heat sinking. The derived thermal resistances in Tables 3 to 6 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above junction temperature multiplicative factor. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm.

The 12A represents all four channels in parallel at 3A each. The four parallel channels have their currents reduced at the same rate to develop an equivalent $\theta_{JA}$ circuit evaluation with thermal couples or IR camera used to validate the thermal resistance values.

### Maximum Operating Ambient Temperature

Figures 26 and 27 display the Maximum Power Loss Allowance Curves vs ambient temperature with various heat sinking and airflow conditions. This data was derived from the thermal impedance generated by various thermal derating examinations with the junction temperature measured at 120°C. This maximum power loss limitation serves as a guideline when designing multiple output rails with different voltages and currents by calculating the total power loss.

For example, to determine the maximum ambient temperature when $V_{OUT1}$ = 2.5V at 0.6A, $V_{OUT2}$ = 3.3V at 3A, $V_{OUT3}$ = 1.8V at 1A, $V_{OUT4}$ = 1.2V at 3A, without a heat sink and 400LFM airflow, simply add up the total power loss for each channel read from Figure 8 to Figure 13 which in this example equals 3.0W, then multiply by the 1.3 coefficient for 120°C junction temperature and compare the total power loss number, 3.9W, with Figure 26. Figure 26 indicates with a 3.9W total power loss, the maximum ambient temperature for this particular application is around 77°C. Also from Figure 26, it is easy to determine with a 3.4W total power loss, the maximum ambient temperature is around 63°C with no airflow and 73°C with 200LFM airflow.

## APPLICATIONS INFORMATION

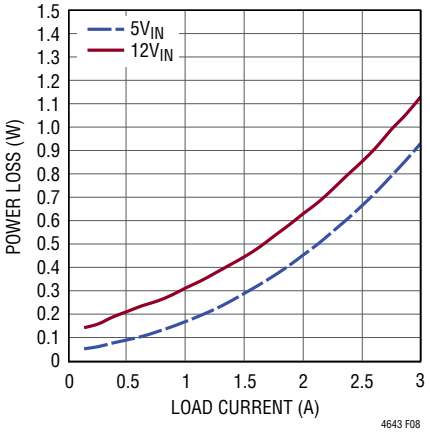



**Figure 8. Power Loss at 1.0V Output, (Each Channel, 25°C)**

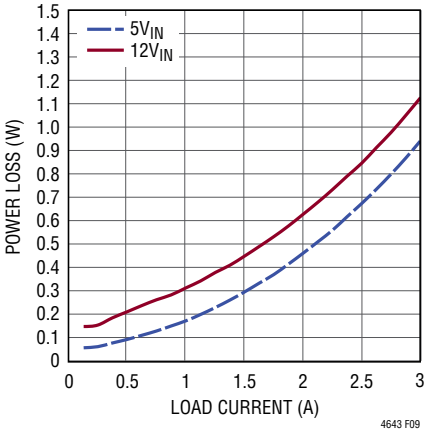



**Figure 9. Power Loss at 1.2V Output, (Each Channel, 25°C)**

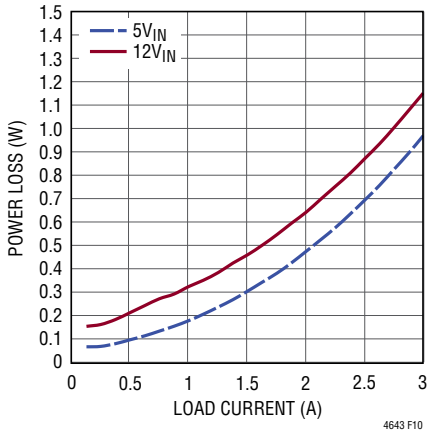



**Figure 10. Power Loss at 1.5V Output, (Each Channel, 25°C)**

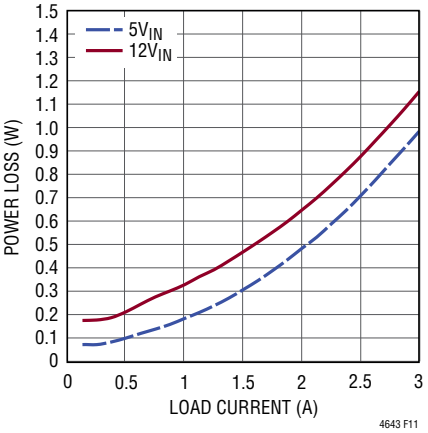



**Figure 11. Power Loss at 1.8V Output, (Each Channel, 25°C)**

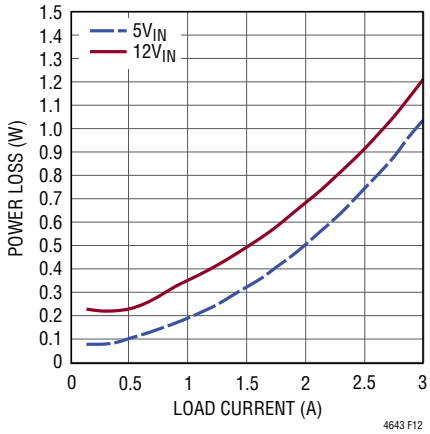



**Figure 12. Power Loss at 2.5V Output, (Each Channel, 25°C)**

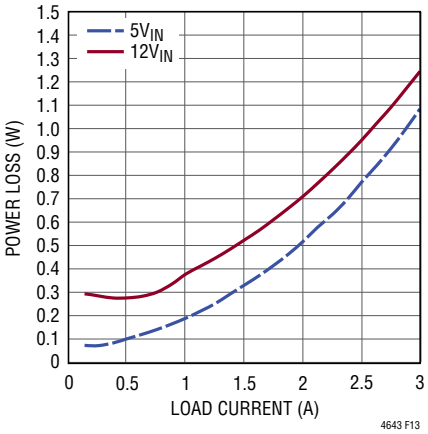



**Figure 13. Power Loss at 3.3V Output, (Each Channel, 25°C)**

## APPLICATIONS INFORMATION

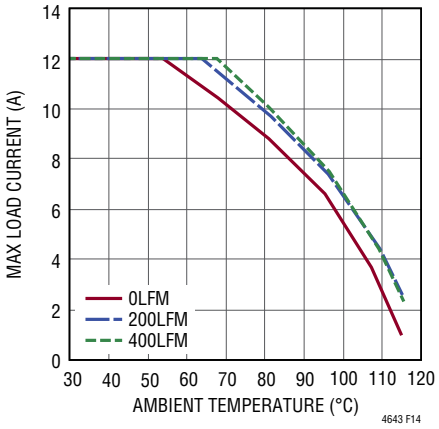



**Figure 14. $5V_{IN}$ to $1.0V_{OUT}$ Derating Curve, 4-Channel Paralleled, No Heat Sink**

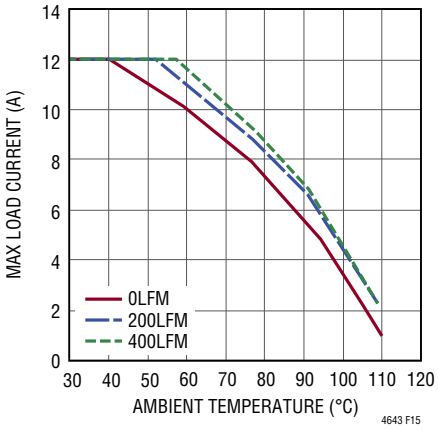



**Figure 15. $12V_{IN}$ to $1.0V_{OUT}$ Derating Curve, 4-Channel Paralleled, No Heat Sink**

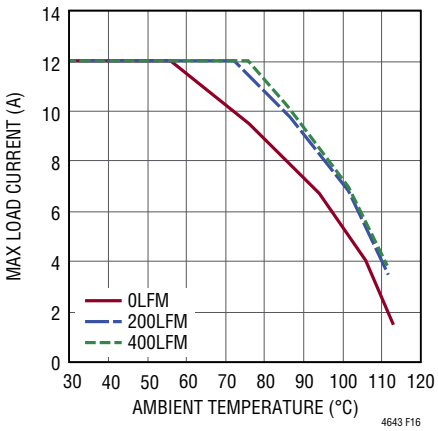



**Figure 16. $5V_{IN}$ to $1.0V_{OUT}$ Derating Curve, 4-Channel Paralleled, BGA Heat Sink**

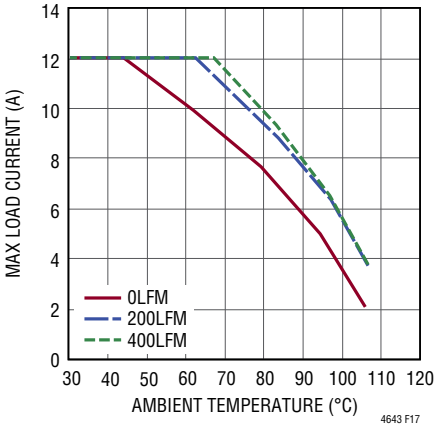



**Figure 17. $12V_{IN}$ to $1.0V_{OUT}$ Derating Curve, 4-Channel Paralleled, BGA Heat Sink**

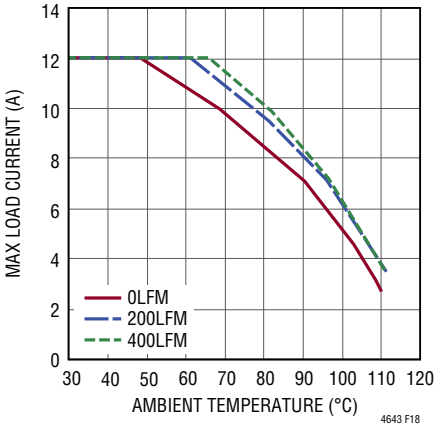



**Figure 18. $5V_{IN}$ to $1.5V_{OUT}$ Derating Curve, 4-Channel Paralleled, No Heat Sink**

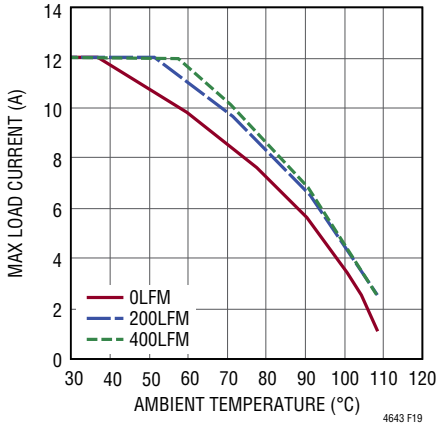



**Figure 19. $12V_{IN}$ to $1.5V_{OUT}$ Derating Curve, 4-Channel Paralleled, No Heat Sink**

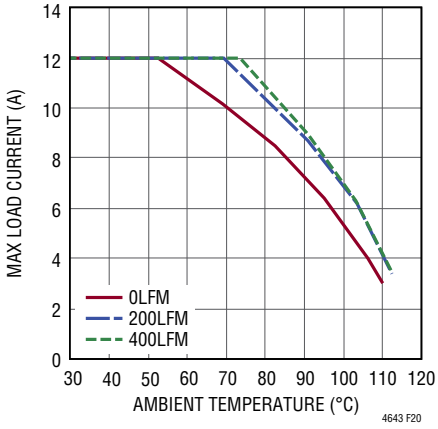



**Figure 20. $5V_{IN}$ to $1.5V_{OUT}$ Derating Curve, 4-Channel Paralleled, BGA Heat Sink**

Rev D

## APPLICATIONS INFORMATION

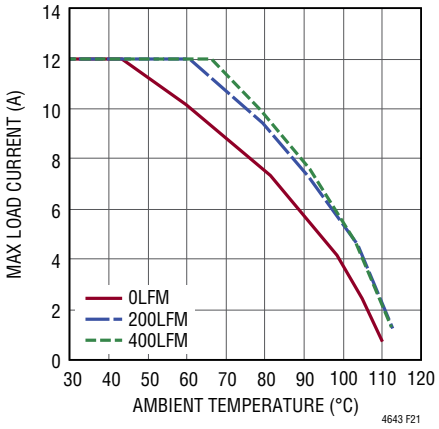



**Figure 21. $12V_{IN}$ to $1.5V_{OUT}$ Derating Curve, 4-Channel Paralleled, BGA Heat Sink**

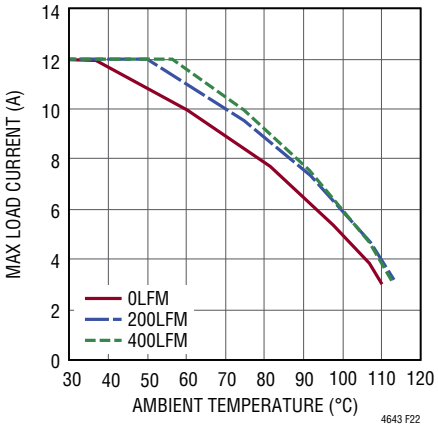



**Figure 22. $5V_{IN}$ to $3.3V_{OUT}$ Derating Curve, 4-Channel Paralleled, No Heat Sink**

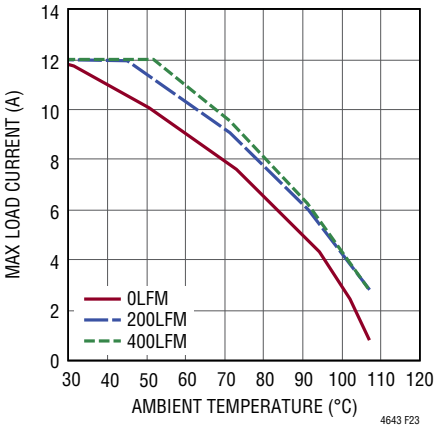



**Figure 23. $12V_{IN}$ to $3.3V_{OUT}$ Derating Curve, 4-Channel Paralleled, No Heat Sink**

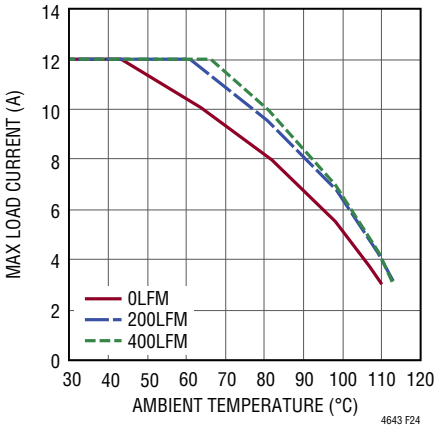



**Figure 24. $5V_{IN}$ to $3.3V_{OUT}$ Derating Curve, 4-Channel Paralleled, BGA Heat Sink**

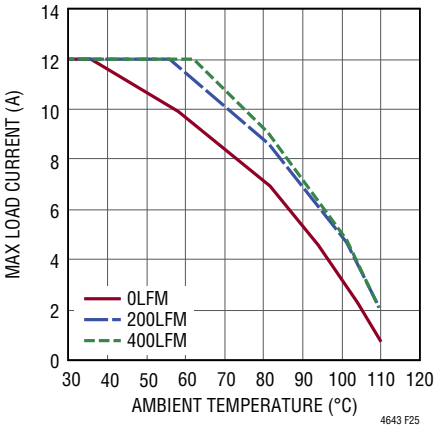



**Figure 25. $12V_{IN}$ to $3.3V_{OUT}$ Derating Curve, 4-Channel Paralleled, BGA Heat Sink**

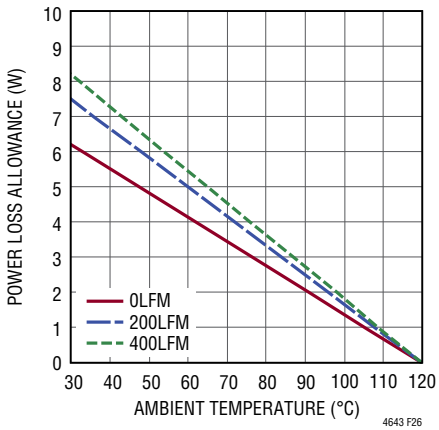



**Figure 26. Power Loss Allowance vs. Ambient Temperature, No Heat Sink**

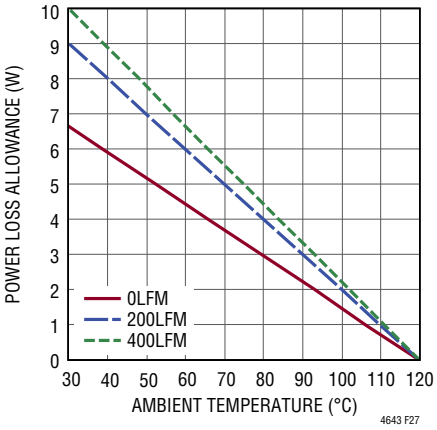



**Figure 27. Power Loss Allowance vs. Ambient Temperature, BGA Heat Sink**

## APPLICATIONS INFORMATION

**Table 3. 1.0V Output**

| DERATING CURVE | $V_{IN}$ (V) | POWER LOSS CURVE | AIR FLOW (LFM) | HEAT SINK | $\Theta_{JA}$ (°C/W) |
|---|---|---|---|---|---|
| Figures 14,15 | 5, 12 | Figure 8 | 0 | None | 14.5 |
| Figures 14, 15 | 5, 12 | Figure 8 | 200 | None | 12 |
| Figures 14, 15 | 5, 12 | Figure 8 | 400 | None | 11 |
| Figures 16, 17 | 5, 12 | Figure 8 | 0 | BGA Heat Sink | 13.5 |
| Figures 16, 17 | 5, 12 | Figure 8 | 200 | BGA Heat Sink | 10 |
| Figures 16, 17 | 5, 12 | Figure 8 | 400 | BGA Heat Sink | 9 |

**Table 4. 1.5V Output**

| DERATING CURVE | $V_{IN}$ (V) | POWER LOSS CURVE | AIR FLOW (LFM) | HEAT SINK | $\Theta_{JA}$ (°C/W) |
|---|---|---|---|---|---|
| Figures 18, 19 | 5, 12 | Figure 10 | 0 | None | 14.5 |
| Figures 18, 19 | 5, 12 | Figure 10 | 200 | None | 12 |
| Figures 18, 19 | 5, 12 | Figure 10 | 400 | None | 11 |
| Figures 20, 21 | 5, 12 | Figure 10 | 0 | BGA Heat Sink | 13.5 |
| Figures 20, 21 | 5, 12 | Figure 10 | 200 | BGA Heat Sink | 10 |
| Figures 20, 21 | 5, 12 | Figure 10 | 400 | BGA Heat Sink | 9 |

**Table 5. 3.3V Output**

| DERATING CURVE | $V_{IN}$ (V) | POWER LOSS CURVE | AIR FLOW (LFM) | HEAT SINK | $\Theta_{JA}$ (°C/W) |
|---|---|---|---|---|---|
| Figures 22, 23 | 5, 12 | Figure 13 | 0 | None | 14.5 |
| Figures 22, 23 | 5, 12 | Figure 13 | 200 | None | 12 |
| Figures 22, 23 | 5, 12 | Figure 13 | 400 | None | 11 |
| Figures 24, 25 | 5, 12 | Figure 13 | 0 | BGA Heat Sink | 13.5 |
| Figures 24, 25 | 5, 12 | Figure 13 | 200 | BGA Heat Sink | 10 |
| Figures 24, 25 | 5, 12 | Figure 13 | 400 | BGA Heat Sink | 9 |

# APPLICATIONS INFORMATION

**Table 6.**

| $C_{IN}$ | PART NUMBER | VALUE | $C_{OUT1}$ (CERAMIC) | PART NUMBER | VALUE | $C_{OUT1}$ (POSCAP) | PART NUMBER | VALUE |
|---|---|---|---|---|---|---|---|---|
| Murata | GRM21BR61E106KA73L | 10µF, 25V, 0805, X5R | Murata | GRM21BR60J476ME15 | 47µF, 6.3V, 0805, X5R | Sanyo | 4TPE100MZB | 4V 100µF |
| Taiyo Yuden | TMK212BBJ106KG-T | 10µF, 25V, 0805, X5R | Taiyo Yuden | JMK212BJ476MG-T | 47µF, 6.3V, 0805, X5R | | | |
| Murata | GRM31CR61C226ME15L | 22µF, 25V, 1206, X5R | | | | | | |
| Taiyo Yuden | TMK316BBJ226ML-T | 22µF, 25V, 1206, X5R | | | | | | |

| $V_{OUT}$ (V) | $C_{IN}$ (CERAMIC) (µF) | $C_{OUT1}$ (µF) | $C_{FF}$ (pF) | $V_{IN}$ (V) | DROOP (mv) | P-P DERIVATION (mV) | RECOVERY TIME (µs) | LOAD STEP (A) | LOAD STEP SLEW RATE (A/µs) | $R_{FB}$ (kΩ) |
|---|---|---|---|---|---|---|---|---|---|---|
| **CERAMIC ONLY** | | | | | | | | | | |
| 1 | 10 | 47 | 100 | 5, 12 | 1 | 59 | 40 | 2A to 3A | 0 | 90.9 |
| 1.2 | 10 | 47 | 100 | 5, 12 | 1 | 59 | 40 | 2A to 3A | 0 | 60.4 |
| 1.5 | 10 | 47 | 100 | 5, 12 | 1 | 66 | 40 | 2A to 3A | 0 | 40.2 |
| 1.8 | 10 | 47 | 100 | 5, 12 | 1 | 75 | 40 | 2A to 3A | 0 | 30.1 |
| 2.5 | 10 | 47 | 100 | 5, 12 | 2 | 108 | 50 | 2A to 3A | 0 | 19.1 |
| 3.3 | 10 | 47 | 100 | 5, 12 | 3 | 111 | 60 | 2A to 3A | 0 | 13.3 |
| **POSCAP** | | | | | | | | | | |
| 1 | 10 | 100 | | 5, 12 | 1 | 89 | 40 | 2A to 3A | 0 | 90.9 |
| 1.2 | 10 | 100 | | 5, 12 | 1 | 94 | 40 | 2A to 3A | 0 | 60.4 |
| 1.5 | 10 | 100 | | 5, 12 | 1 | 108 | 40 | 2A to 3A | 0 | 40.2 |
| 1.8 | 10 | 100 | | 5, 12 | 1 | 120 | 40 | 2A to 3A | 0 | 30.1 |
| 2.5 | 10 | 100 | | 5, 12 | 2 | 144 | 50 | 2A to 3A | 0 | 19.1 |
| 3.3 | 10 | 100 | | 5, 12 | 3 | 161 | 60 | 2A to 3A | 0 | 13.3 |

## APPLICATIONS INFORMATION

### Safety Considerations

The LTM4643 modules do not provide galvanic isolation from $V_{IN}$ to $V_{OUT}$. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and overcurrent protection.

### Layout Checklist/Example

The high integration of LTM4643 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including $V_{IN1}$ to $V_{IN4}$, GND, $V_{OUT1}$ to $V_{OUT4}$. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the $V_{IN}$, GND and $V_{OUT}$ pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the $V_{OUT}$, $V_{FB}$, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK/SS pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 28 gives a good example of the recommended layout.

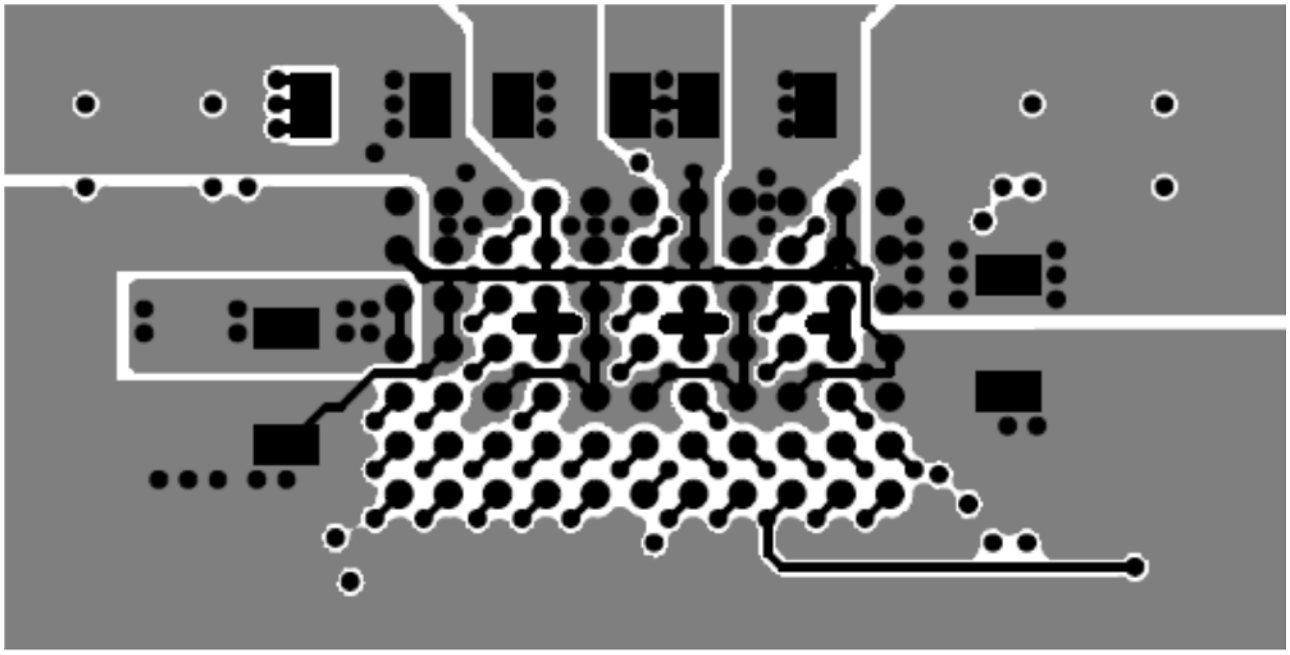


**Figure 28. Recommended PCB Layout**

## TYPICAL APPLICATIONS

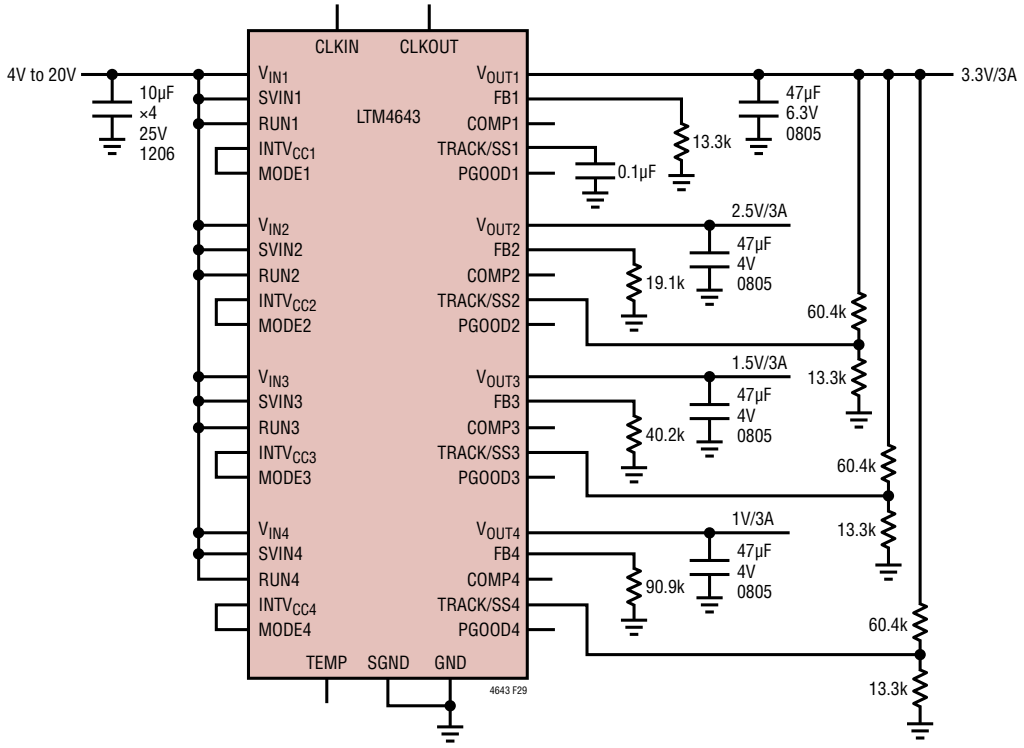



**Figure 29. 4V to 20V Input, Quad 1.0V, 1.5V, 2.5V and 3.3V Output with Ratiometric Tracking**

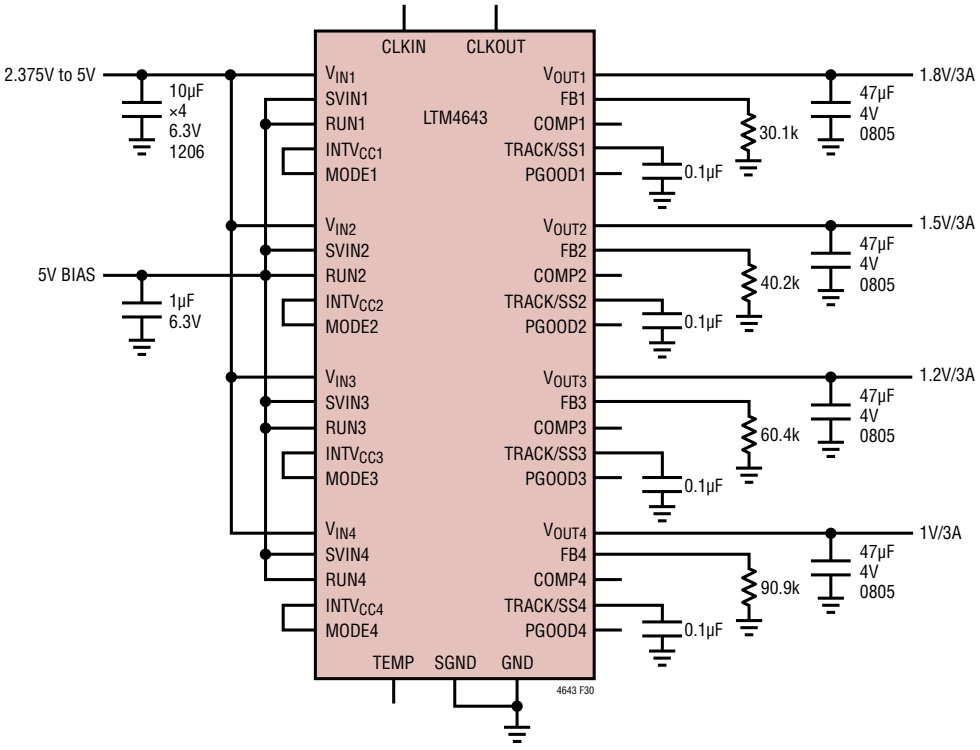



**Figure 30. 2.375V to 5V Input, Quad 1V, 1.2V, 1.5V, 1.8V Output**

## TYPICAL APPLICATIONS

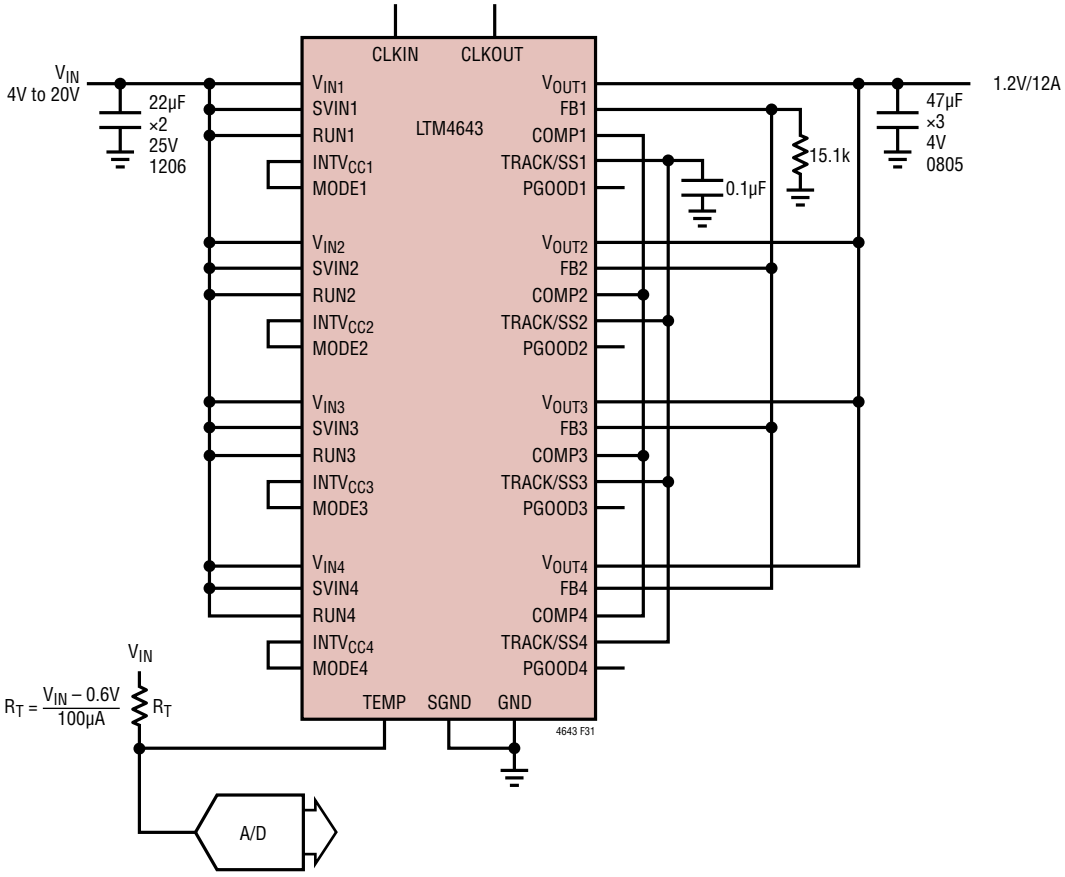



**Figure 31. 4V to 20V Input, 4-Phase, 1.2V at 12A Design with Temperature Monitoring**

## TYPICAL APPLICATIONS

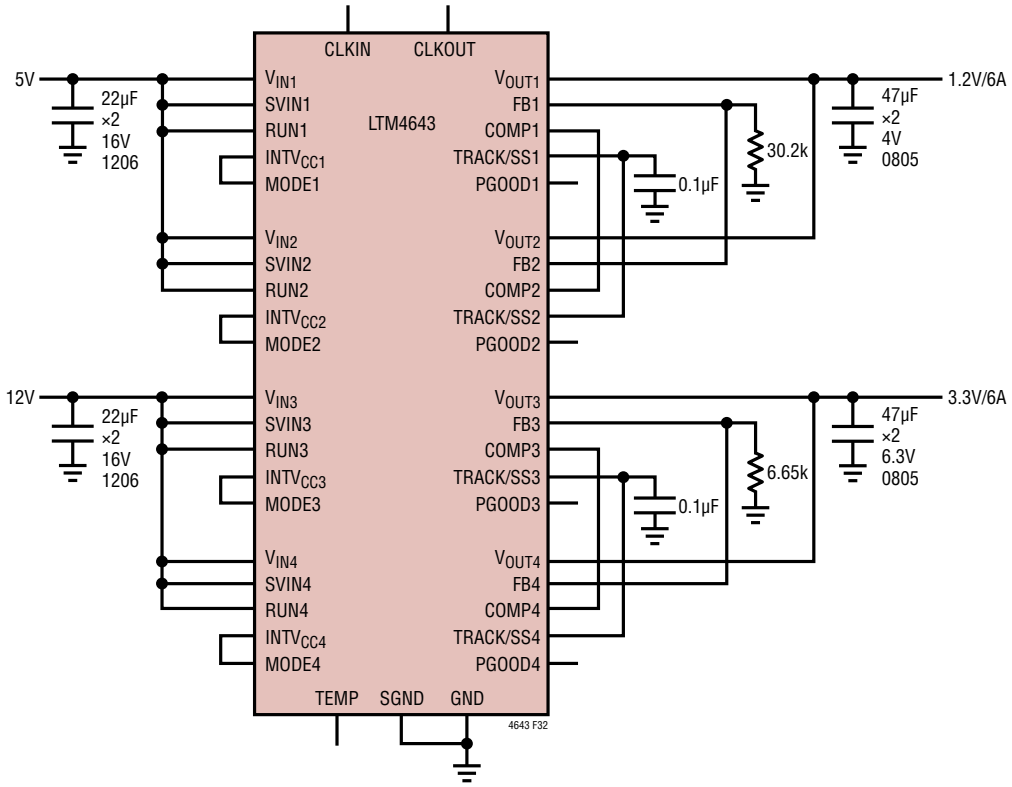



**Figure 32. 12V and 5V Two Separate Input Rails, 1.2V at 6A and 3.3V at 6A Output**

# PACKAGE DESCRIPTION

**PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.**

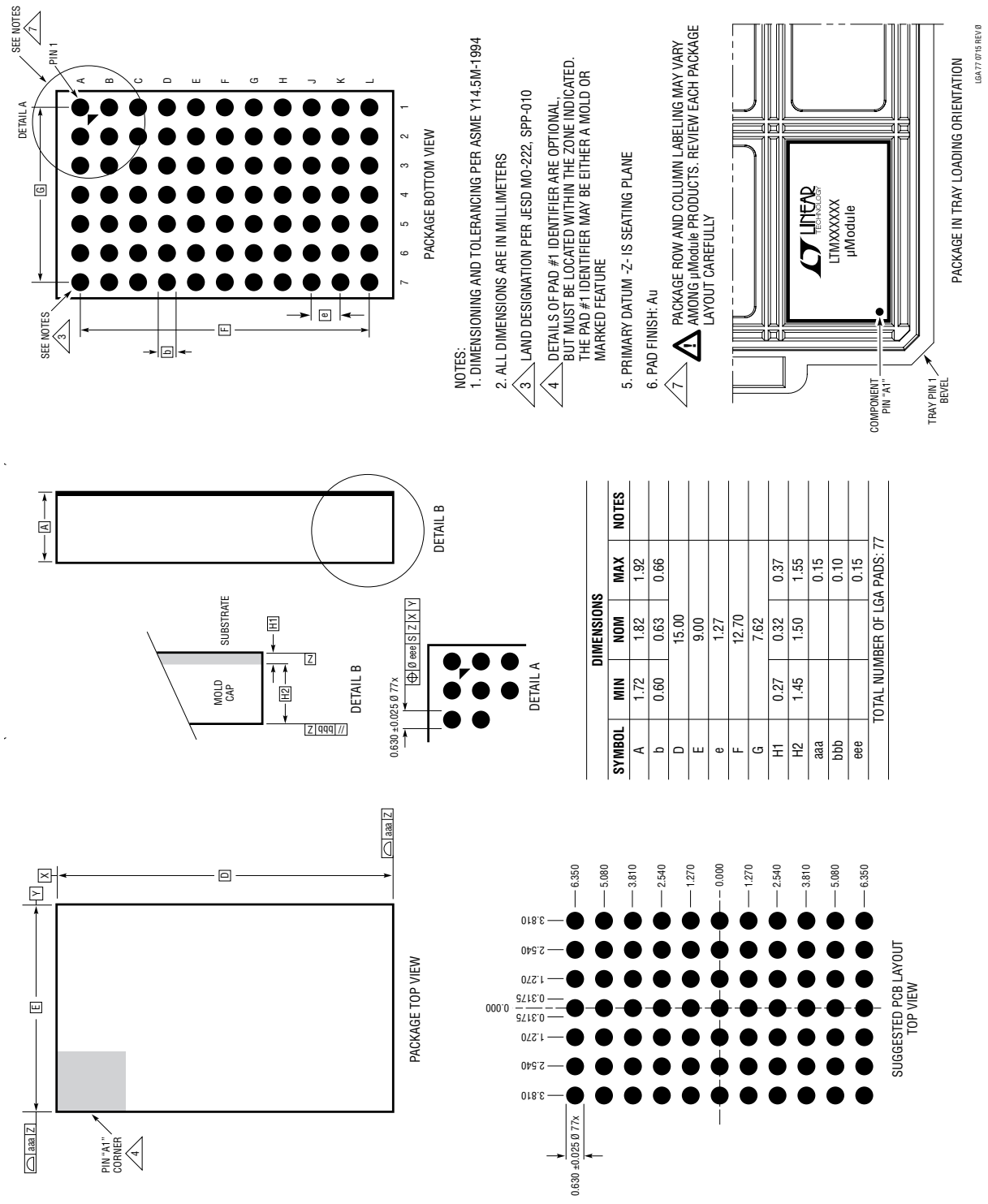
**LTM4643 Component LGA and BGA Pinout**

| PIN | NAME | PIN | NAME | PIN | NAME | PIN | NAME | PIN | NAME | PIN | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | $V_{OUT1}$ | B1 | GND | C1 | $V_{OUT2}$ | D1 | $V_{OUT2}$ | E1 | GND | F1 | $V_{OUT3}$ |
| A2 | $V_{OUT1}$ | B2 | GND | C2 | PGOOD2 | D2 | $V_{OUT2}$ | E2 | GND | F2 | PGOOD3 |
| A3 | $V_{OUT1}$ | B3 | $V_{IN1}$ | C3 | PGOOD1 | D3 | GND | E3 | $V_{IN2}$ | F3 | TEMP |
| A4 | GND | B4 | $V_{IN1}$ | C4 | $INTV_{CC1}$ | D4 | GND | E4 | $V_{IN2}$ | F4 | $INTV_{CC2}$ |
| A5 | GND | B5 | $SV_{IN1}$ | C5 | GND | D5 | GND | E5 | $SV_{IN2}$ | F5 | GND |
| A6 | TRACK/SS1 | B6 | MODE1 | C6 | RUN1 | D6 | TRACK/SS2 | E6 | MODE2 | F6 | RUN2 |
| A7 | FB1 | B7 | COMP1 | C7 | CLKIN | D7 | FB2 | E7 | COMP2 | F7 | SGND |

| PIN | NAME | PIN | NAME | PIN | NAME | PIN | NAME | PIN | NAME | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | $V_{OUT3}$ | H1 | GND | J1 | $V_{OUT4}$ | K1 | $V_{OUT4}$ | L1 | GND | | |
| G2 | $V_{OUT3}$ | H2 | GND | J2 | PGOOD4 | K2 | $V_{OUT4}$ | L2 | GND | | |
| G3 | GND | H3 | $V_{IN3}$ | J3 | CLKOUT | K3 | GND | L3 | $V_{IN4}$ | | |
| G4 | GND | H4 | $V_{IN3}$ | J4 | $INTV_{CC3}$ | K4 | GND | L4 | $V_{IN4}$ | | |
| G5 | GND | H5 | $SV_{IN3}$ | J5 | GND | K5 | $INTV_{CC4}$ | L5 | $SV_{IN4}$ | | |
| G6 | TRACK/SS3 | H6 | MODE3 | J6 | RUN3 | K6 | TRACK/SS4 | L6 | MODE4 | | |
| G7 | FB3 | H7 | COMP3 | J7 | FB4 | K7 | RUN4 | L7 | COMP4 | | |

# PACKAGE DESCRIPTION

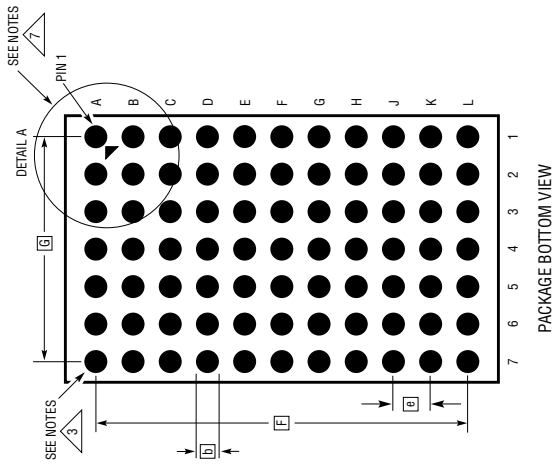
**LGA Package**
**77-Lead (15.00mm × 9.00mm ×1.82mm)**
(Reference LTC DWG # 05-08-1508 Rev Ø)



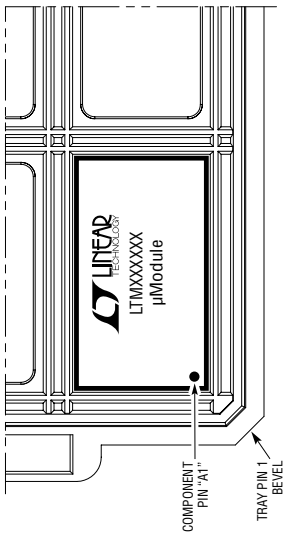

| DIMENSIONS | | | | |
|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | NOTES |
| A | 1.72 | 1.82 | 1.92 | |
| b | 0.60 | 0.63 | 0.66 | |
| D | | 15.00 | | |
| E | | 9.00 | | |
| e | | 1.27 | | |
| F | | 12.70 | | |
| G | | 7.62 | | |
| H1 | 0.27 | 0.32 | 0.37 | |
| H2 | 1.45 | 1.50 | 1.55 | |
| aaa | | | 0.15 | |
| bbb | | | 0.10 | |
| eee | | | 0.15 | |
| TOTAL NUMBER OF LGA PADS: 77 | | | | |

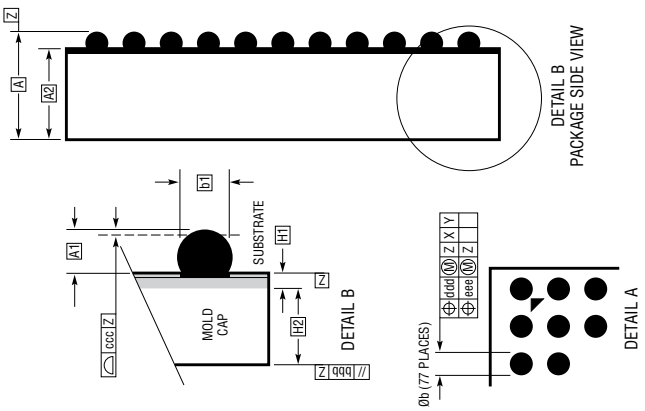
# PACKAGE DESCRIPTION

**BGA Package**
**77-Lead (15.00mm × 9.00mm × 2.42mm)**
(Reference LTC DWG# 05-08-1559 Rev Ø)

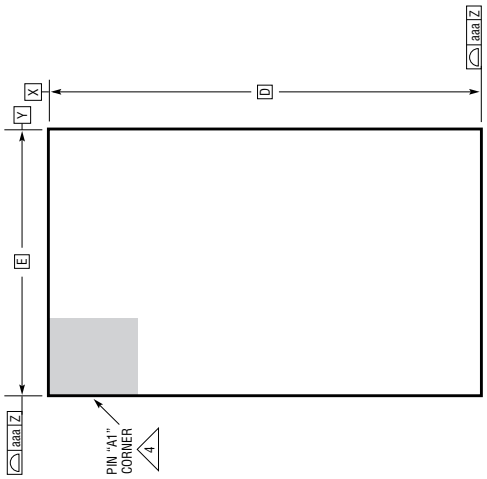


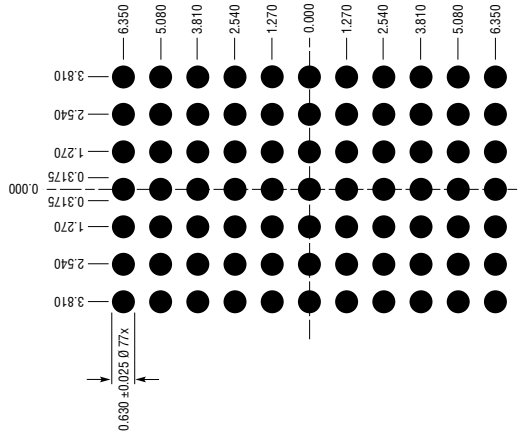

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION CAN BE 96.5% Sn/3.0% Ag/0.5% Cu OR Sn Pb EUTECTIC
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY




| DIMENSIONS | | | | |
|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | NOTES |
| A | 2.22 | 2.42 | 2.62 | |
| A1 | 0.50 | 0.60 | 0.70 | |
| A2 | 1.72 | 1.82 | 1.92 | |
| b | 0.60 | 0.75 | 0.90 | |
| b1 | 0.60 | 0.63 | 0.66 | |
| D | | 15.00 | | |
| E | | 9.00 | | |
| e | | 1.27 | | |
| F | | 12.70 | | |
| G | | 7.62 | | |
| H1 | 0.27 | 0.32 | 0.37 | |
| H2 | 1.45 | 1.50 | 1.55 | |
| aaa | | | 0.15 | |
| bbb | | | 0.10 | |
| ccc | | | 0.20 | |
| ddd | | | 0.30 | |
| eee | | | 0.15 | |
| TOTAL NUMBER OF BALLS: 77 | | | | |



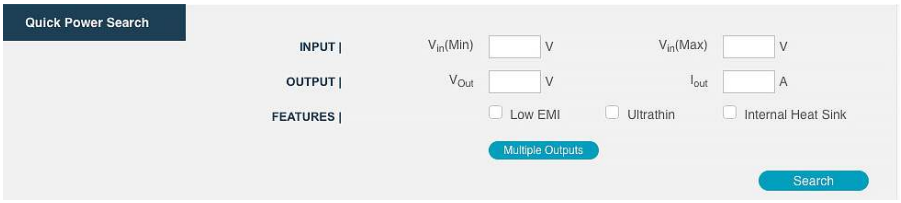



# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 03/17 | Added the BGA package | 1, 2, 28, 30 |
| B | 6/17 | Corrected Output Current from 4A to 3A on Figure 4 | 13 |
| | | Corrected Output Voltage from 1.2V to 1.0V on Title of Figure 29 | 25 |
| C | 5/18 | Changed Storage Temperature Range: –65°C to 150°C | 3 |
| D | 01/20 | Added text to CLKOUT in Pin Functions | 6 |

## PACKAGE PHOTOS


## DESIGN RESOURCES

| SUBJECT | DESCRIPTION | |
|---|---|---|
| µModule Design and Manufacturing Resources | Design:<br>• Selector Guides<br>• Demo Boards and Gerber Files<br>• Free Simulation Tools | Manufacturing:<br>• Quick Start Guide<br>• PCB Design, Assembly and Manufacturing Guidelines<br>• Package and Board Level Reliability |
| µModule Regulator Products Search | 1. Sort table of products by parameters and download the result as a spread sheet.<br>2. Search using the Quick Power Search parametric table.<br>  | |
| Digital Power System Management | Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging. | |



## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTM4644 | Higher Power, Quad | Quad 4A, Pin Compatible, 9mm × 15mm × 5.01mm BGA |
| LTM4623 | Single, Ultrathin | 3A, 6.25mm × 6.25mm × 1.8mm LGA and 6.25mm × 6.25mm × 2.42mm BGA |
| LTM4622 | Dual, Ultrathin | Dual 2.5A or Single 5A, , 6.25mm × 6.25mm × 1.8mm LGA and 6.25mm × 6.25mm × 2.42mm BGA |
| LTM4631 | Higher Power, Dual, Ultrathin | Dual 10A or Single 20A, , 16mm × 16mm × 1.91mm LGA |