

Vishay Siliconix

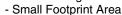
P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^{a, f}	Q _g (Typ.)		
- 30	$0.087 \text{ at V}_{GS} = -10 \text{ V}$	- 9	3.5 nC		
	0.158 at $V_{GS} = -4.5 \text{ V}$	- 7.2	3.5 110		

FEATURES

- · Halogen-free
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] SC-75 Package

Load Switch, PA Switch and Battery Switch for Portable

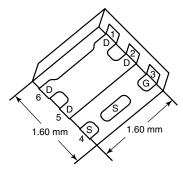


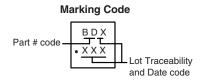


RoHS COMPLIANT

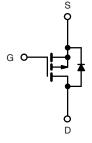
APPLICATIONS

PowerPAK SC-75-6L-Single





Ordering Information: SiB415DK-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V_{DS}	- 30	V	
Gate-Source Voltage		V_{GS}	± 20	7 v	
Continuous Drain Current (T _J = 150 °C)	$T_C = 25 \degree C$ $T_C = 70 \degree C$ $T_A = 25 \degree C$	I _D	- 9 ^a - 7.7 - 4.17 ^{a, b}		
Pulsed Drain Current		I _{DM}	- 3.36 ^{a, b} 15	A	
Continuous Source-Drain Diode Current	T _C = 25 °C T _A = 25 °C	I _S	- 9 ^a - 2 ^{a, b}		
Maximum Power Dissipation	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	P _D	13 8.4 2.4 ^{a, b} 1.6 ^{a, b}	w	
Operating Junction and Storage Temperature R	T _J , T _{stg}	- 55 to 150	-°C		
Soldering Recommendations (Peak Temperature) ^{c, d}			260		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, e}	t ≤ 5 s	R _{thJA}	41	51	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	7.5	9.5]	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. t = 5 s
- c. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- e. Maximum under Steady State conditions is 105 °C/W.
- f. Based on $T_C = 25$ °C.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1 0504		- 24.2		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	- I _D = - 250 μA		4			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1		- 3	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 30 V, V _{GS} = 0 V			- 1		
		V _{DS} = - 30 V, V _{GS} = 0 V, T _J = 55 °C			- 10	μΑ	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ 5 V, V _{GS} = - 10 V	5			Α	
	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 4.17 A		0.072	0.087	Ω	
Drain-Source On-State Resistance ^a		V _{GS} = - 4.5 V, I _D = - 3.1 A		0.130	0.158		
Forward Transconductance ^a	g _{fs}	V _{DS} = - 15 V, I _D = - 4.17 A		5.5		S	
Dynamic ^b		-				1	
Input Capacitance	C _{iss}			295			
Output Capacitance	C _{oss}	V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz		70		pF	
Reverse Transfer Capacitance	C _{rss}			50			
Total Gate Charge		V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 4.17 A		6.7	10.05	nC	
		30 00 0		3.5	5.25		
Gate-Source Charge	Q_{gs}	V _{DS} = - 15 V, V _{GS} = - 4.5 V, I _D = - 4.17 A		1			
Gate-Drain Charge	Q_{gd}			1.78			
Gate Resistance	R_{g}	f = 1 MHz		9.4		Ω	
Turn-On Delay Time	t _{d(on)}			43	64.5	-	
Rise Time	t _r	$V_{DD} = -15 \text{ V}, R_{L} = 6.07 \Omega$		55	82		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong -2.47 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$		13	19.5		
Fall Time	t _f			10	15		
Turn-On Delay Time	t _{d(on)}			6	9	ns	
Rise Time	t _r	$V_{DD} = -15 \text{ V}, R_{L} = 3.6 \Omega$		8.5	12.75		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 4.17 A, V_{GEN} = - 10 V, R_g = 1 Ω		14	21		
Fall Time	t _f			9	13.5		
Drain-Source Body Diode Characterist	ics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 9	۸	
Pulse Diode Forward Current	I _{SM}				15	A	
Body Diode Voltage	V_{SD}	I _S = - 3.2 A, V _{GS} = 0 V		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			14.63	22	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = - 3.2 A, di/dt = 100 A/μs, T _{.I} = 25 °C		8	12	nC	
Reverse Recovery Fall Time	t _a	$11F - 3.2 \text{ A}, \text{ u/u} = 100 \text{ A/} \mu \text{s}, \text{ IJ} = 25 \text{ C}$		9.13		ns	
Reverse Recovery Rise Time	t _b	†		5.5			

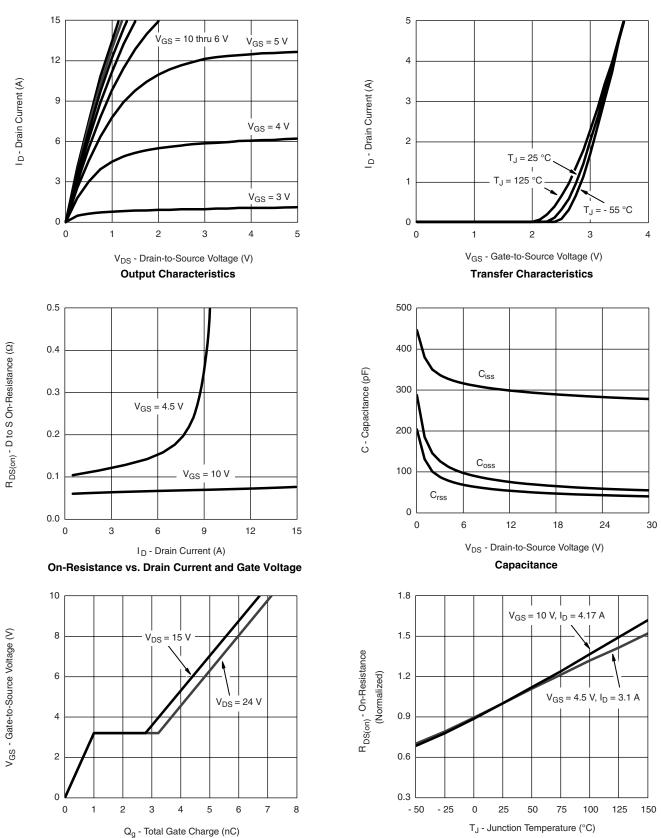
- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Gate Charge

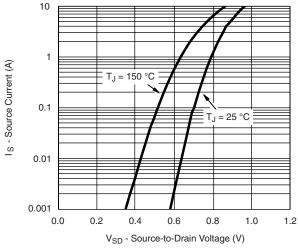
On-Resistance vs. Junction Temperature

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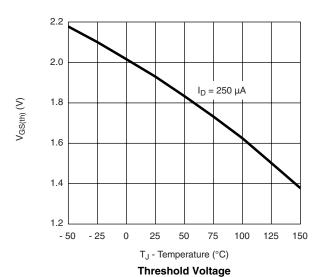
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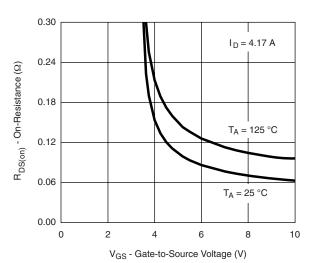
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

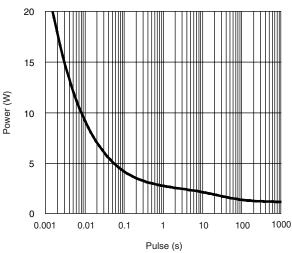


Soure-Drain Diode Forward Voltage

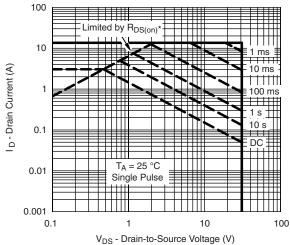




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



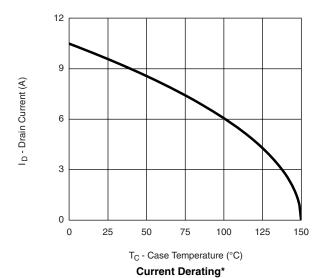
 * V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified

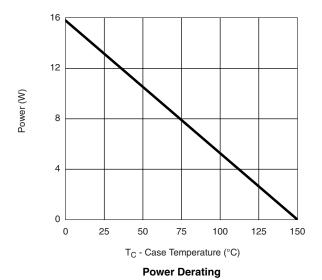
Safe Operating Area, Junction-to-Ambient



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





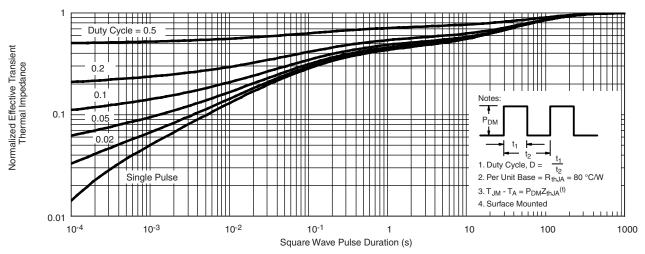
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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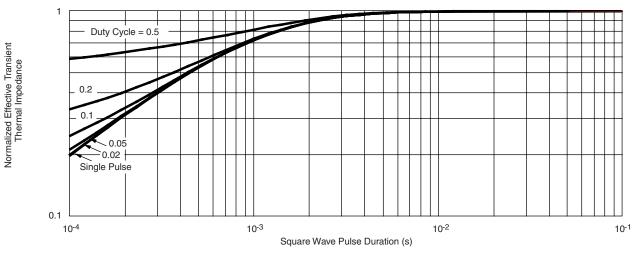
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70438.



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