Using the TPS40210EVM

User's Guide

Literature Number: SLUU308
April 2008

A 12-V Input, 24-V, 2-A Non-Synchronous Boost Converter

1 Introduction

The TPS40210EVM evaluation module (EVM) is a fixed frequency (600 kHz) non-synchronous boost converter providing fixed 24-V output at up to 2 A from a 12-V input bus. The EVM is designed to start up from a single supply, so no additional bias voltage is required for start-up. The module uses the TPS40210 Non-Synchronous Current Mode Control Boost Controller with integral N-channel FET driver.

1.1 Description

TPS40210EVM is designed to use a regulated 12-V (+10% / -20%) bus to produce a regulated power rail at 24 V at up to 2 A of load current each. TPS40210EVM is designed to demonstrate the TPS40210 in a typical 12-V bus system while providing a number of test points to evaluate the performance of the TPS40210 in a given application. The EVM can be modified to other input or output voltages by changing some of the components.

1.2 Applications

- Non-Isolated Low Current Point-of-Load and Voltage Bus Converters.
- Consumer Electronics
- LCD TV
- Computer Peripherals
- Digital Set Top Box

1.3 Features

- 12-V +10% / -20% input range
- 24-V fixed output voltage, adjustable with resistor change (May require compensation adjustment)
- 600-kHz switching frequency
- Single SO-8 switching MOSFET and rectifier diode.
- Double sided 2 active layer PCB with all components on top side (test point signals routed on internal layers)
- Active converter area of less than 2.5 square inch < 1.15” x 2.15”
- Convenient test points for probing switching waveforms and non-invasive loop response testing

2 TPS40210EVM Electrical Performance Specifications

Table 1. TPS40210EVM Electrical and Performance Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Input Characterstics						
V_{IN}	Input voltage		8	12	14	V
I_{IN}	Input current	V_{IN} = nom, I_{OUT} = max	-	4.3	4.5	A
	No load input current	V_{IN} = nom, I_{OUT} = 0 A	-	12	20	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = 100 mA	4	4.2	4.4	V
Output Characterstics						
V_{OUT1}	Output voltage 1	V_{IN} = nom, I_{OUT} = nom	24	24.5	25	V
	Line regulation	V_{IN} = min to max	-	-	1	%
	Load regulation	IOUT = min to max	-	-	1	
V_{OUT_ripple}	Output voltage ripple	V_{IN} = nom, I_{OUT} = max	-	-	500	mVpp
I_{OUT1}	Output current 1	V_{IN} = min to max	0		2	A
I_{OCP1}	Output over current Channel 1	V_{IN} = nom, V_{OUT} = VOUT1-5%	3.1	3.7	4.5	
I_{OCP2}	Output over current Channel 2	V_{IN} = nom, V_{OUT} = VOUT2-5%	3.1	3.7	4.5	
Systems Characterstics						
F_{SW}	Switching frequency		540	600	660	kHz
h_{pk}	Peak efficiency	V_{IN} = nom	-	90	-	%
h	Full load efficiency	V_{IN} = nom, I_{OUT} = max	-	85	-	

3 Schematic

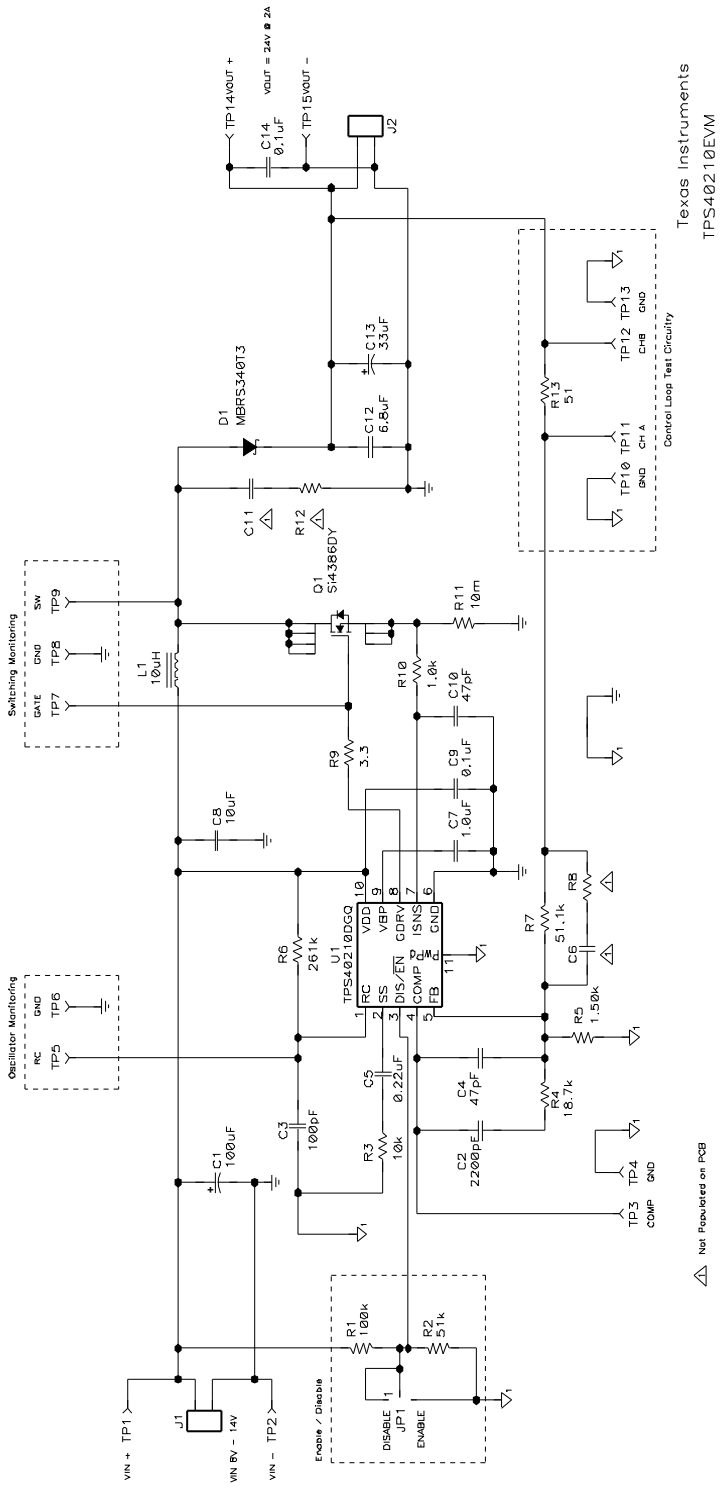

Figure 1. TPS40210EVM Schematic

Note: For reference only, See Table 3 List of Materials for specific values.

3.1 Enable Jumpers (JP1)

TPS40210EVM provides a 3-pin, 100-mil header and shunt for exercising the TPS40210 Enable function. When the JP1 shunt is removed, R1 and R2 pull up on the TPS40210 inverted Enable and turns OFF the TPS40210 switcher. Inserting a shunt in the LEFT (Enable) position pulls the TPS40210 inverted Enable to ground and turns ON the TPS40210 output. Due to diode D1, when the TPS40210 is “OFF” the output voltage will be maintained within 500 mV of the input voltage.

3.2 Test Point Descriptions

Table 2. Test Point Descriptions

TEST POINT	LABLE	USE	SECTION
TP1	VIN	Monitor input voltage	Section 3.2.1
TP2	GND	Ground for input voltage	Section 3.2.1
TP3	COMP	Monitor COMP voltage	Section 3.2.2, Section 3.2.5
TP4	GND	Ground for COMP voltage	Section 3.2.2, Section 3.2.5
TP5	RC	Monitor RC oscillator voltage	Section 3.2.3
TP6	GND	Ground for oscillator voltage	Section 3.2.3
TP7	GATE	Monitor GATE driver voltage	Section 3.2.4
TP8	GND	Ground for GATE and SW	Section 3.2.4
TP9	SW	Monitor switching node	Section 3.2.4
TP10	GND	Ground for Channel A loop monitoring	Section 3.2.5
TP11	CHA	Channel A for loop monitoring	Section 3.2.5
TP12	CHB	Channel B for loop monitoring	Section 3.2.5
TP13	GND	Ground for Channel B loop monitoring	Section 3.2.5
TP14	VOUT	Monitor VOUT voltage	Section 3.2.6
TP15	GND	Ground for VOUT voltage	Section 3.2.6

3.2.1 Input Voltage Monitoring (TP1 and TP2)

TPS40210EVM provides two test points for measuring the voltage applied to the module. This allows the user to measure the actual module voltage without losses from input cables and connectors. All input voltage measurements should be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive terminal to TP1 and negative terminal to TP2.

3.2.2 Control Voltage Monitoring (TP3 and TP4)

TPS40210EVM provides a test point for measuring the control voltage (COMP) returned to the TPS40210 for PWM generation. To measure the control voltage, connect an oscilloscope probe to TP3.

In addition to allowing the user to monitor the control voltage for signs of noise or unfiltered output ripple, this allows the user to directly measure the power stage gain as described in Section 3.2.5

3.2.3 Oscillator/Ramp Monitoring (TP5 and TP6)

TPS40210EVM provides a test point for monitoring the PWM oscillator (TP5) and a local ground connection (TP6) for the monitoring the oscillator and current mode control slope compensation. Connect an oscilloscope probe to TP5 to monitor the slope compensation ramp.

3.2.4 Switching Waveforms Monitoring (TP7, TP8 and TP9)

TPS40210EVM provides test points for monitoring the gate drive (TP7) and switch node (TP9) plus a local ground connection (TP8) for the monitoring the power stage switching waveforms. Connect an oscilloscope probe to TP7 to monitor the gate drive voltage and to TP9 to monitor the switch node voltage.

3.2.5 Loop Analysis (TP3, TP10, TP11, TP12 and TP13)

TPS40210EVM contains a 51-Ω series resistor (R13) in the feedback loop to allow for matched impedance signal injection into the feedback for loop response analysis. An isolation transformer should be used to apply a small (30 mV or less) signal across R13 through TP11 and TP12. By monitoring the ac injection level at TP11 and the returned ac level at TP13, the power supply loop response can be determined.

To measure the power stage transfer function, connect the isolation transformer as described above. Monitor the ac injection level at the control voltage (TP3) and the returned ac level at the output (TP13).

To measure the error amplifier transfer function, connect the isolation transformer as described above. Monitor the ac injection level at the output voltage (TP13) and the returned ac level at the control voltage (TP3).

3.2.6 Output Voltage Monitoring (TP14 and TP15)

TPS40210EVM provides two test points for measuring the voltage generated by the module. This allows the user to measure the actual module output voltage without losses from output cables and connectors. All output voltage measurements should be made between TP14 and TP15. To use TP14 and TP15, connect a voltmeter positive terminal to TP14 and negative terminal to TP15. For output ripple measurements, TP14 and TP15 allow a user to limit the ground loop area by using the tip and barrel measurement technique shown in Figure 3. All output ripple measurements should be made using the tip and barrel measurement.

4 Test Set Up

4.1 Equipment

4.1.1 Voltage Source

V_{IN} : The input voltage source (VIN) should be a 0-V to 15-V variable dc source capable of 8 A_{DC}. Connect VIN to J1 as shown in Figure 3.

4.1.2 Meters

- A1: 0 to 7-A_{DC}, ammeter
- V1: VIN, 0-V to 15-V voltmeter
- V2: VOUT 0-V to 25-V voltmeter

4.1.3 Loads

LOAD1: The Output1 Load (LOAD1) should be an electronic constant current mode load capable of 0-2 A_{DC} at 24.0 V

4.1.4 Oscilloscope

Oscilloscope: A digital or analog oscilloscope can be used to measure the ripple voltage on V_{OUT}. The oscilloscope should be set for 1-MΩ impedance, 20-MHz bandwidth, ac coupling, 1-µs/division horizontal resolution, 10-mV/division vertical resolution for taking output ripple measurements. TP14 and TP15 can be used to measure the output ripple voltages by placing the oscilloscope probe tip through TP14 and holding the ground barrel to TP15 as shown in Figure 3. For a hands free approach, the loop in TP15 can be cut and opened to cradle the probe barrel. Using a leaded ground connection may induce additional noise due to the large ground loop area.

4.1.5 Recommended Wire Gauge

VIN to J1: The connection between the source voltage, V_{IN} and J1 of HPA289 can carry as much as 8 A_{DC}. The minimum recommended wire size is AWG #14 with the total length of wire less than four feet (two feet input, two feet return).

J2 to LOAD1: The power connection between J2 of HPA289 and LOAD1 can carry as much as 2 A_{DC}. The minimum recommended wire size is AWG #18, with the total length of wire less than two feet (one foot output, one foot return).

4.1.6 Other

Fan: This evaluation module includes components that can get hot to the touch, because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 400 lfm is recommended to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered. The EVM should not be probed while the fan is not running.

4.2 Equipment Setup

Shown in Figure 2 is the basic test set up recommended to evaluate the TPS40210EVM. Please note that although the return for J1 and JP2 are the same system ground, the connections should remain separate as shown in Figure 2.

4.2.1 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the dc input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 8.0 A maximum. Make sure V_{IN} is initially set to 0 V and connected as shown in Figure 2.
3. Connect the ammeter A1 (0 A to 8 A range) between VIN and J1 as shown in Figure 2.
4. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 2.
5. Connect LOAD1 to J2 as shown in Figure 2. Set LOAD1 to constant current mode to sink 0 A_{DC} before V_{IN} is applied.
6. Connect voltmeter, V2 across TP14 and TP15 as shown in Figure 2.
7. Place fan as shown in Figure 3 and turn on, making sure air is flowing across the EVM.

4.2.2 Diagram

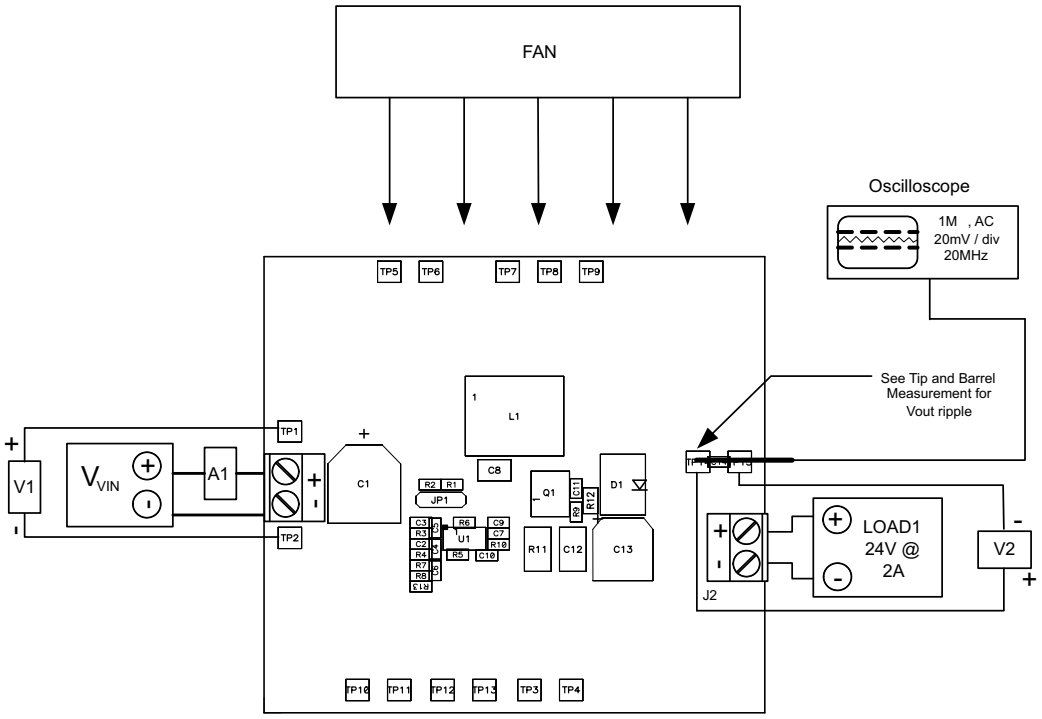

Figure 2. TPS40210EVM Recommended Test Set-Up

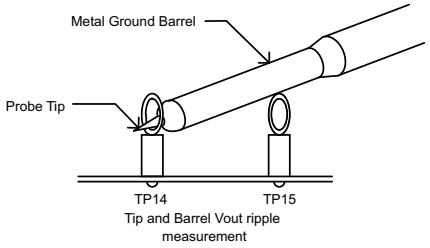

Figure 3. Output Ripple Measurement - Tip and Barrel Using TP14 and TP15

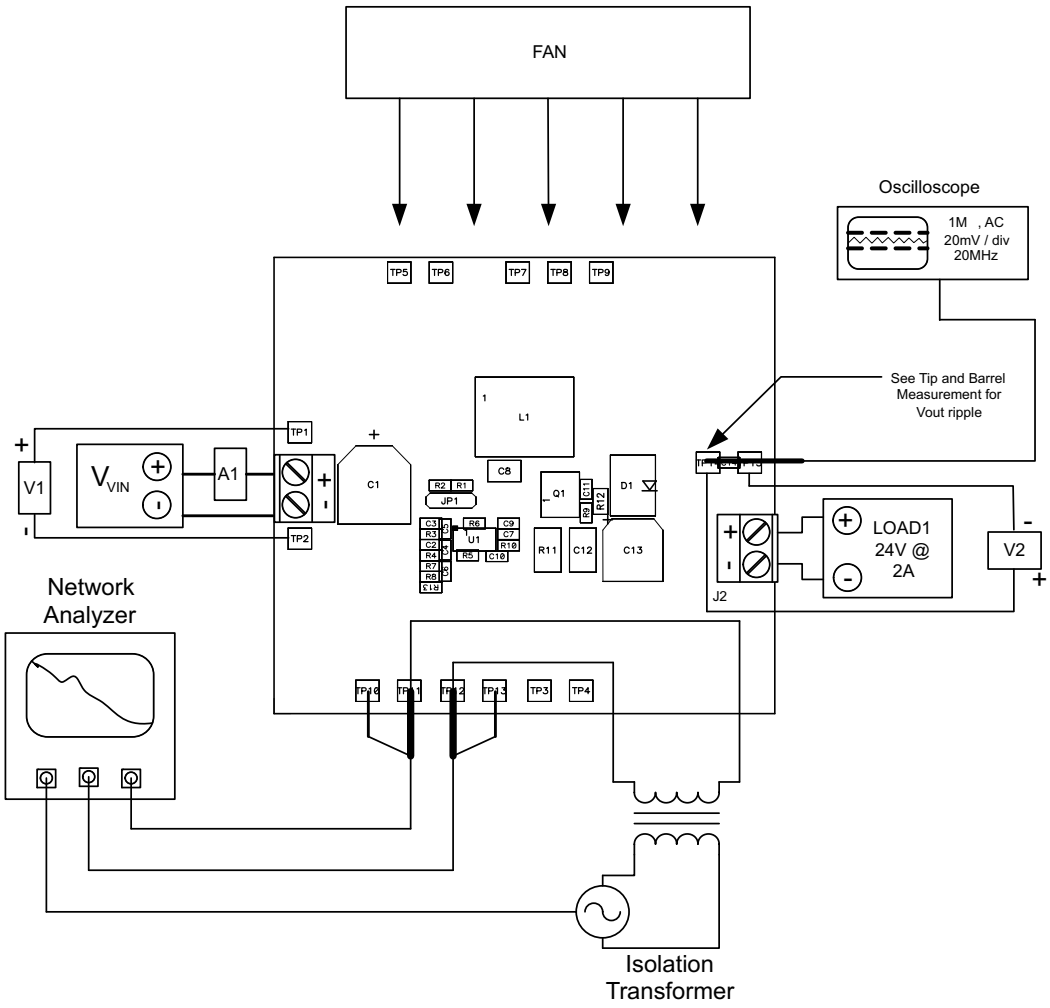

Figure 4. Control Loop Measurement Setup

4.3 Start Up / Shut Down Procedure

1. Increase V_{IN} from 0V to 12 V_{DC}
2. Vary LOAD1 from 0 – 2 A_{DC}
3. Vary V_{IN} from 8 V_{DC} to 14 V_{DC}
4. Decrease V_{IN} to 0 V_{DC}
5. Decrease LOAD1 to 0 A.

4.4 Output Ripple Voltage Measurement Procedure

1. Increase V_{IN} from 0 V to 12 V_{DC}
2. Adjust LOAD1 to desired load between 0 A_{DC} and 2 A_{DC}
3. Adjust V_{IN} to desired load between 8 V_{DC} and 14 V_{DC}
4. Connect oscilloscope probe to TP14 and TP15 as shown in Figure 3.
5. Measure output ripple
6. Decrease V_{IN} to 0 V_{DC}
7. Decrease LOAD1 to 0 A

4.5 Control Loop Gain and Phase Measurement Procedure

1. Connect 1-kHz to 1-MHz isolation transformer to TP11 and TP12 as show in Figure 4.
2. Connect input signal amplitude measurement probe (Channel A) to TP11 as shown in Figure 4.
3. Connect output signal amplitude measurement probe (Channel B) to TP13 as shown in Figure 4.
4. Connect ground lead of Channel A and Channel B to TP10 & TP13 as shown in Figure 4.
5. Inject 30 mV or less signal across R13 through isolation transformer.
6. Sweep frequency from 1 kHz to 1 MHz with 10 Hz or lower post filter.
7. Control loop gain can be measured by
8. Control loop phase is measured by the phase difference between Channel A and Channel B
9. The power stage transfer function can be measured by making the following substitutions:
   a. Connect Channel A to TP3
   b. Connect Channel A Ground Clip to TP4
   c. Connect Channel B as described in 4.5.3
10. The error amplifier transfer function can be measured by making the following substitutions :
    a. Connect Channel A as described in 4.5.2
    b. Connect Channel B to TP3
    c. Connect Channel B Ground Clip to TP4
11. Disconnect Isolation transformer before making any other measurements (signal injection into Feedback may interfere with accuracy of other measurements).

4.6 Equipment Shutdown

1. Shut Down Oscilloscope
2. Shut Down VIN
3. Shut Down LOAD1
4. Shut Down FAN

5 TPS40210EVM Typical Performance Data and Characteristic CURVES

Figure 5 through Figure 11 present typical performance curves for the TPS40210EVM. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

5.1 Efficiency

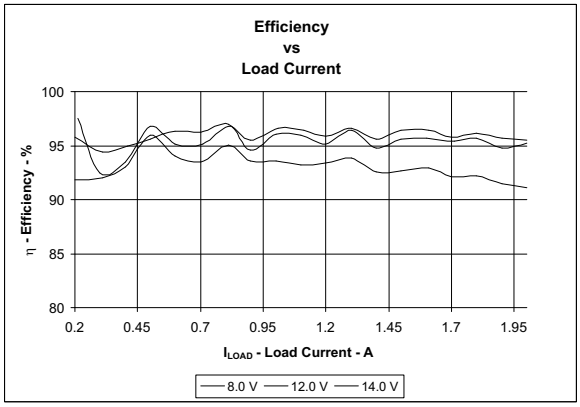

Figure 5. TPS40210EVM Efficiency vs. Load Current (V_{IN} = 8 V to 14 V, V_{OUT} = 24.0 V, I_{OUT} = 0 A to 2 A)

5.2 Line and Load Regulation

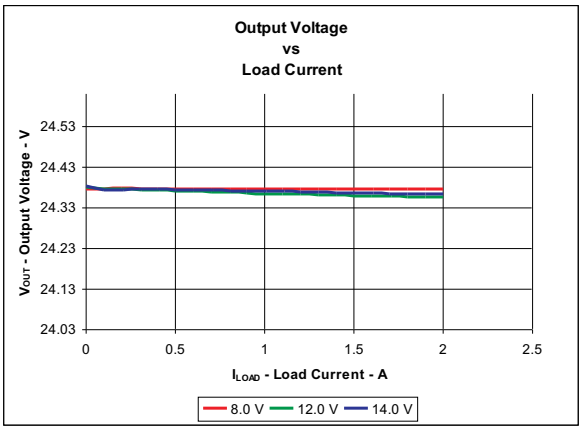

Figure 6. TPS40210EVM Output Voltage vs Load Current (V_{IN} = 8 V to 14 V, V_{OUT} = 24.0 V, I_{OUT} = 0 A to 2 A)

5.3 Output Voltage Ripple

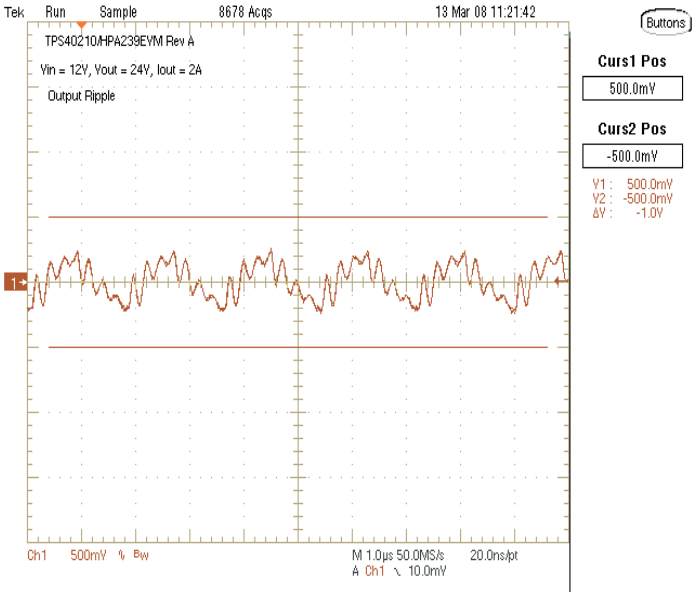

Figure 7. TPS40210EVM Output Voltage Ripple (V_{IN} = 12 V, V_{OUT} = 24.0 V, I_{OUT} = 2 A)

5.4 Switch Node

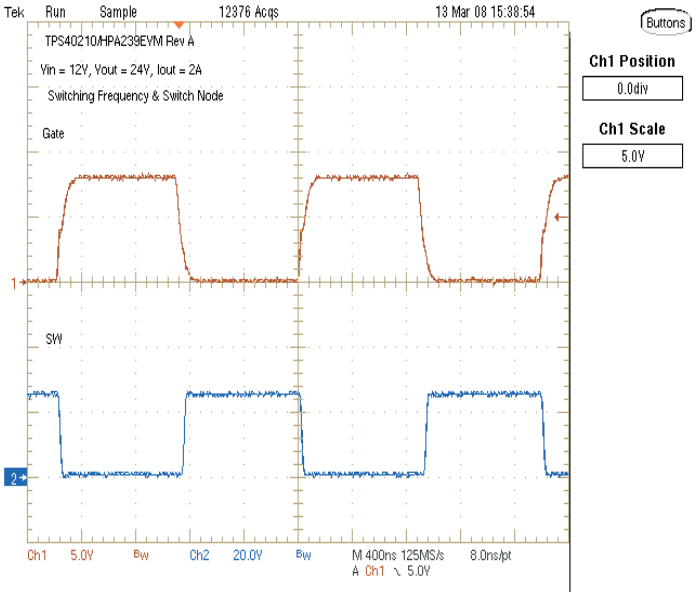

Figure 8. TPS40210EVM Switching Waveforms V_{IN} = 12 V, I_{OUT} = 2 A (Ch1: TP7 (GATE), Ch2: TP9 (SW))

5.5 Control Loop BODE Plot

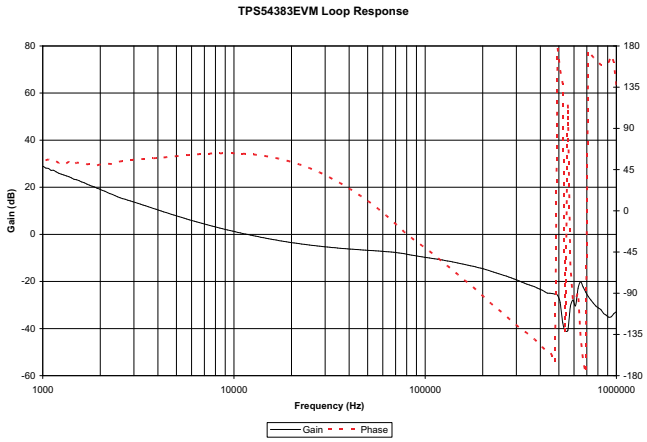

Figure 9. TPS40210EVM Gain/Phase vs Frequency (V_{IN} = 12 V, V_{OUT} = 24.0 V I_{OUT} = 2 A) (V_{OUT}: Bandwidth: 12 kHz Phase Margin: 62°)

5.6 Start Up and Soft Start

In a BOOST power stage, the rectifier diode connected the input voltage to the output voltage. During shut down, disable, UVLO and the start-up delay, this diode connects the input to the output, producing a plateau soft-state waveform. This is normal and an unavoidable result of the BOOST topology.

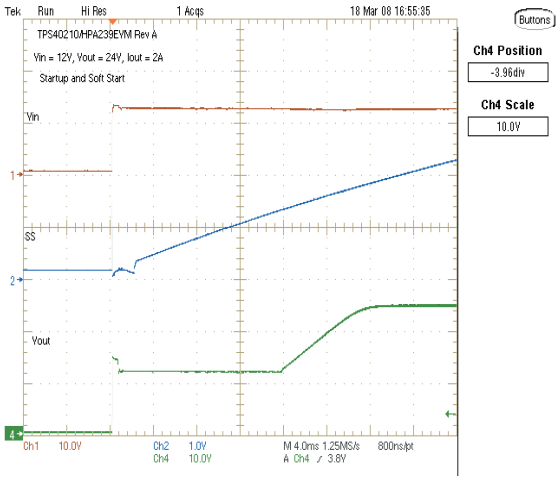

Figure 10. TPS40210EVM Power ON (UVLO) Soft Start (V_{IN} = 12 V, V_{OUT} = 24.0 V, I_{OUT} = 2 A)

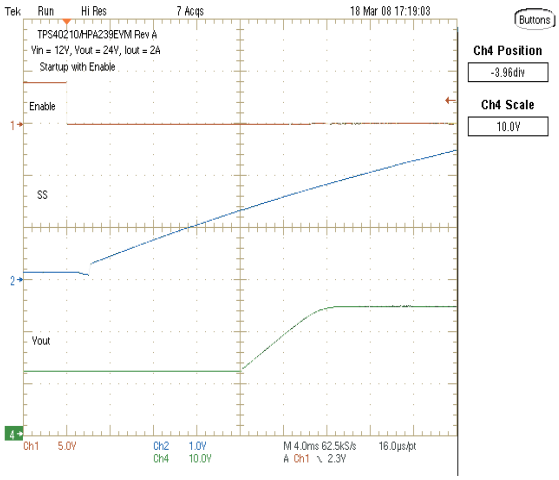

Figure 11. TPS40210EVM Enable ON Soft Start (V_{IN} = 12 V, V_{OUT} = 24.0 V I_{OUT} = 2 A)

6 EVM Assembly Drawings and Layout

The following figures (Figure 12 through Figure 17) show the design of the TPS40210EVM printed circuit board. The EVM has been designed using a 4-Layer, 2-oz copper-clad circuit board 3.0” x 3.0” with all components in a 1.15” x 2.15” active area on the top side and all active traces to the top and bottom layers to allow the user to easily view, probe and evaluate the TPS40210 control device in a practical double-sided application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

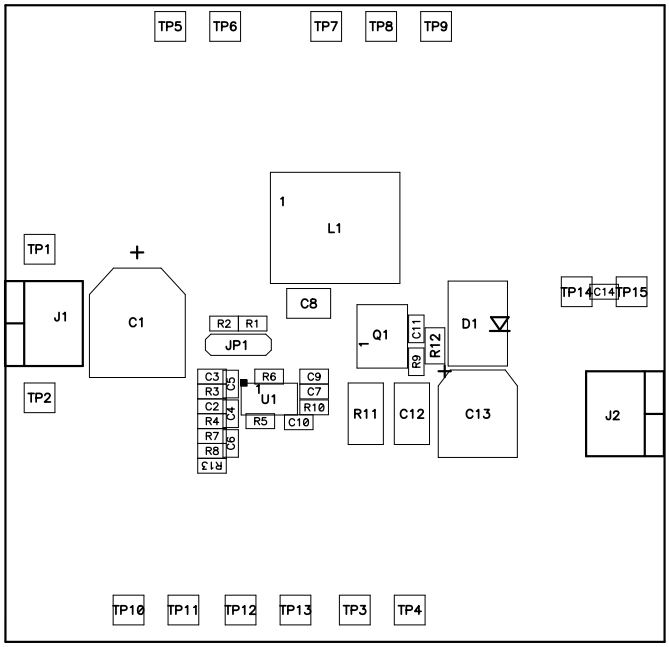

Figure 12. TPS40210EVM Component Placement (viewed from top)

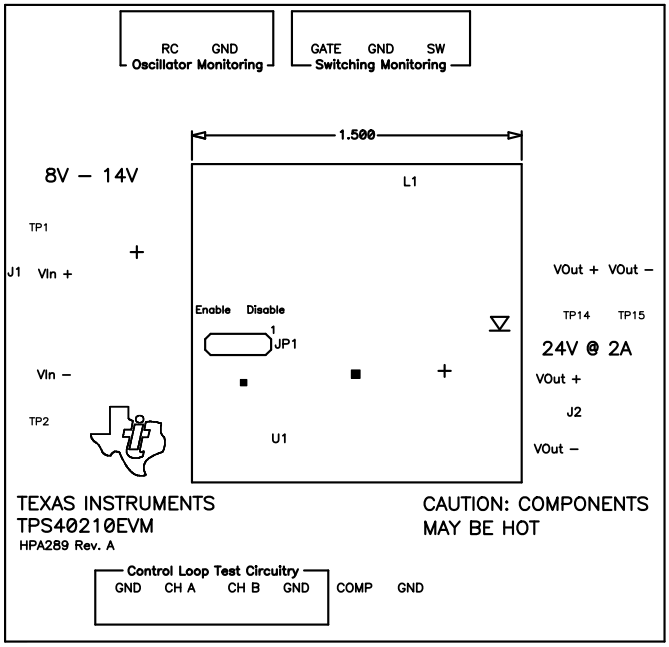

Figure 13. TPS40210EVM Silkscreen (viewed from top)

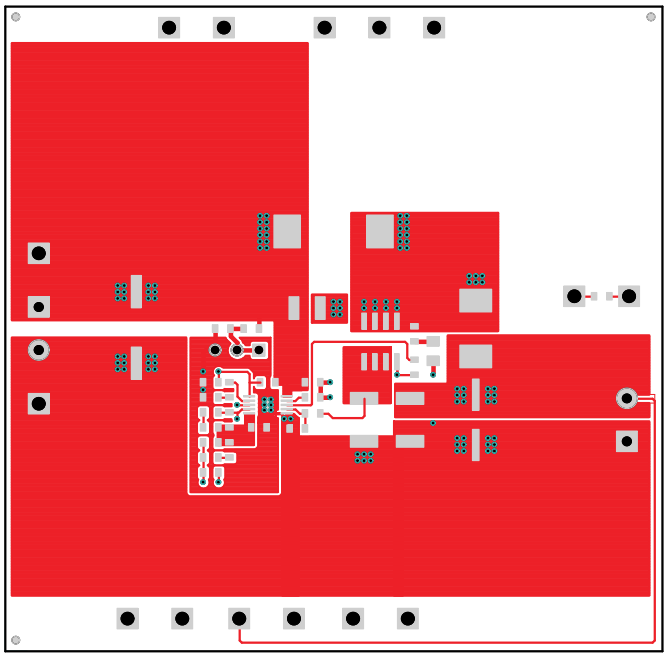

Figure 14. TPS40210EVM Top Copper (viewed from top)

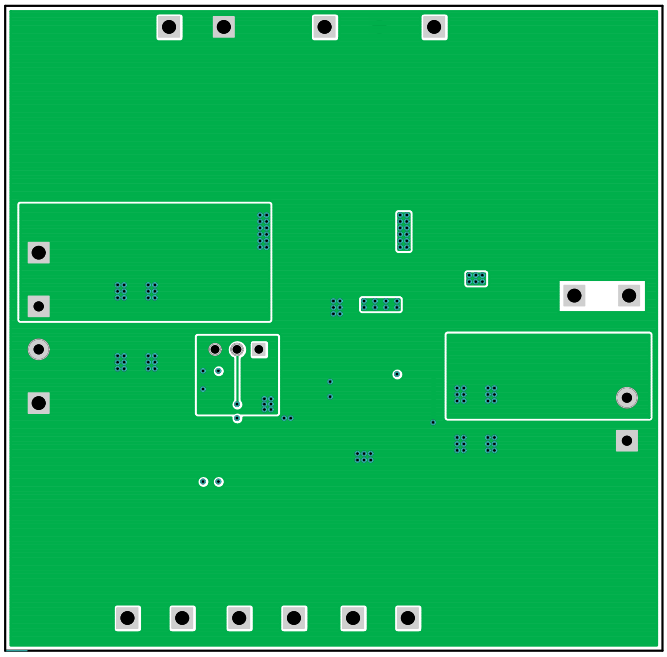

Figure 15. TPS40210EVM Bottom Copper (X-ray view from top)

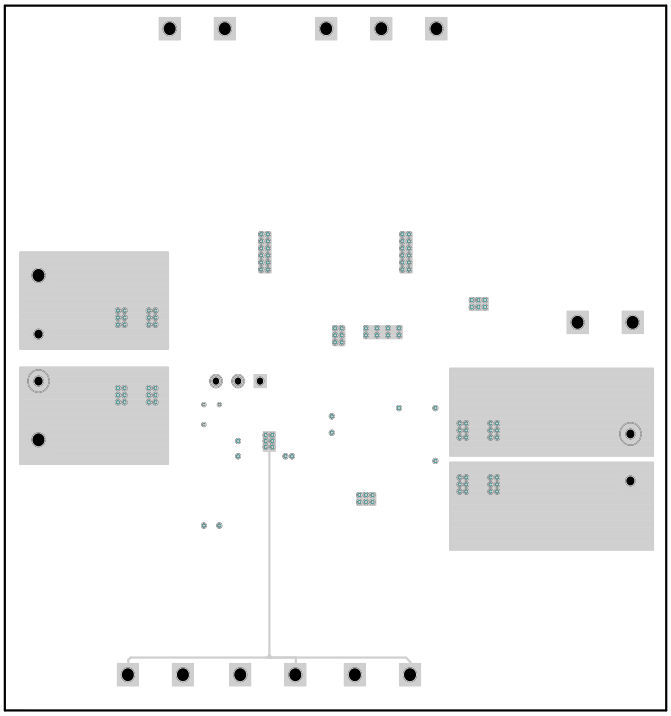

Figure 16. TPS40210EVM Internal 1 (X-ray view from top)

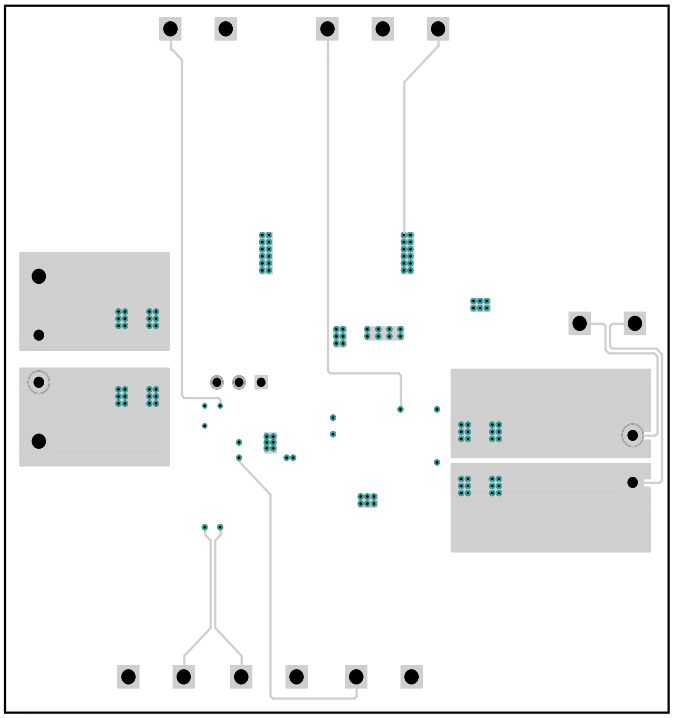

Figure 17. TPS40210EVM Internal 2 (X-ray view from top)

7 List of Materials

Table 3 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 3. TPS40210EVM List of Materials

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
1	C1	Capacitor, aluminum, SM, 20%, 35 V, 100 µF, 0.406 x 0.457 inch	EEEFC1V101P	Panasonic
0	C11	Capacitor, ceramic, 50 V, X5R, 20%, OPEN, 0603	Std	Std
1	C12	Capacitor, ceramic, 50 V, X7R, 20%, 6.8 µF, 1812	C4532X7R1H685M	TDK
1	C13	Capacitor, aluminum, SM, 20%, 35V, 33 µF, 0.328 x 0.328 inch	EEEFC1V330P	Panasonic
1	C2	Capacitor, ceramic, 25 V, X7R, 20%, 2200 pF, 0603	Std	Std
1	C3	Capacitor, ceramic, 16 V, C0G, 10%, 100 pF, 0603	Std	Std
2	C4, C10	Capacitor, ceramic, 25 V, C0G, 20%, 47 pF, 0603	Std	Std
1	C5	Capacitor, ceramic, 16 V, X7R, 20%, 0.22 µF, 0603	Std	Std
0	C6	Capacitor, ceramic, 25 V, X7R, 20%, OPEN, 0603	Std	Std
1	C7	Capacitor, ceramic, 16 V, X5R, 20%, 1.0 µF, 0603	Std	Std
1	C8	Capacitor, ceramic, 25 V, X7R, 20%, 10 µF, 1210	C3225X7R1E106M	TDK
2	C9, C14	Capacitor, ceramic, 50 V, X7R, 20%, 0.1 µF, 0603	Std	Std
1	D1	Diode, Schottky, 3 A, 40 V, SMC	MBRS340T3	On Semi
2	J1, J2	Terminal block, 2 pin, 15 A, 5.1 mm, 0.40 x 0.35 inch	D120/2DS	OST
1	JP1	Header, 3 pin, 100-mil spacing, (36-pin strip), 0.1 inch x 3	PTC36SAAN	Sullins
1	L1	Inductor, SMT, 7.5 A, 12.4 mΩ, 10 µH, 0.325 x 0.318 inch	RLF12560T-100M-7R5	TDK
1	Q1	Trans, MOSFET, N-channel reduced Qg, 30 V, 16 A, 7 mΩ, SO8	Si4386DY	Vishay
1	R1	Resistor, chip, 1/16 W, 5%, 100 kΩ, 0603	Std	Std
1	R10	Resistor, chip, 1/16 W, 5%, 1.0 kΩ, 0603	Std	Std
1	R11	Resistor, chip, 1/2 W, 2%, 10 mΩ, 1812	Std	Std
0	R12	Resistor, chip, 1/10 W, 5%, OPEN, 0805	Std	Std
1	R13	Resistor, chip, 1/16 W, 5%, 51Ω, 0603	Std	Std
1	R2	Resistor, chip, 1/16 W, 5%, 51 kΩ, 0603	Std	Std
1	R3	Resistor, chip, 1/16 W, 5%, 10 kΩ, 0603	Std	Std
1	R4	Resistor, chip, 1/16 W, 1%, 18.7 kΩ, 0603	Std	Std
1	R5	Resistor, chip, 1/16 W, 1%, 1.50 kΩ, 0603	Std	Std
1	R6	Resistor, chip, 1/16 W, 1%, 261 kΩ, 0603	Std	Std
1	R7	Resistor, chip, 1/16 W, 1%, 51.1 kΩ, 0603	Std	Std
0	R8	Resistor, chip, 1/16 W, 1%, OPEN, 0603	Std	Std
1	R9	Resistor, chip, 1/16 W, 5%, 3.3Ω, 0603	Std	Std
2	TP1, TP14	Test point, red, thru hole, 0.125 x 0.125 inch	5010	Keystone
7	TP2, TP4, TP6, TP8, TP10, TP13, TP15	Test point, black, thru hole, 0.125 x 0.125 inch	5011	Keystone
6	TP3, TP5, TP7, TP9, TP11, TP12	Test point, white, thru hole, 0.125 x 0.125 inch	5012	Keystone
1	U1	Device, 4.5 V to 52 V I/P, Current Mode Boost Controller, DGQ10	TPS40210DGQ	TI
1	--	Shunt, 100 mil, black, 0.1	929950-00	3M
1	--	PCB, 3 In x 3 In x 0.063 In,	HPA289	Any

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