MC14001B Series

B-Suffix Series CMOS Gates

MC14001B, MC14011B, MC14023B, MC14025B, MC14071B, MC14073B, MC14081B, MC14082B

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin–for–Pin Replacements for Corresponding CD4000 Series B Suffix Devices

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	–0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

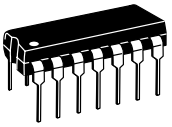
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

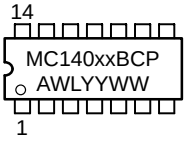
ON Semiconductor

http://onsemi.com

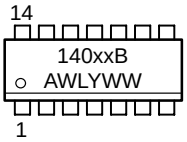
MARKING DIAGRAMS



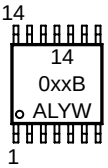
PDIP–14
P SUFFIX
CASE 646

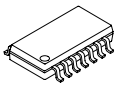


SOIC–14
D SUFFIX
CASE 751A

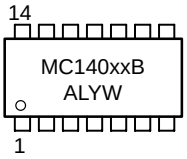


TSSOP–14
DT SUFFIX
CASE 948G





SOEIAJ–14
F SUFFIX
CASE 965



xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

DEVICE INFORMATION

Device	Description
MC14001B	Quad 2–Input NOR Gate
MC14011B	Quad 2–Input NAND Gate
MC14023B	Triple 3–Input NAND Gate
MC14025B	Triple 3–Input NOR Gate
MC14071B	Quad 2–Input OR Gate
MC14073B	Triple 3–Input AND Gate
MC14081B	Quad 2–Input AND Gate
MC14082B	Dual 4–Input AND Gate

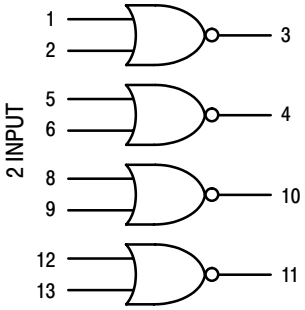
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

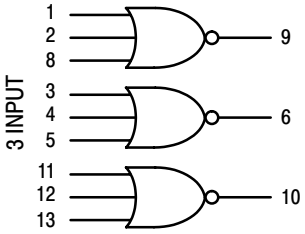
LOGIC DIAGRAMS

NOR

MC14001B
Quad 2–Input NOR Gate

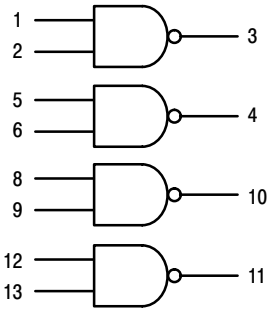


MC14025B
Triple 3–Input NOR Gate

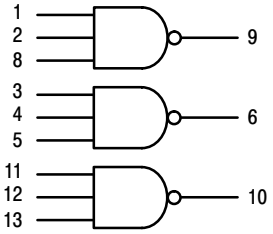


NAND

MC14011B
Quad 2–Input NAND Gate

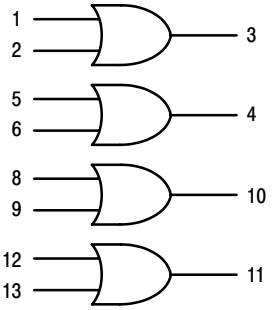


MC14023B
Triple 3–Input NAND Gate

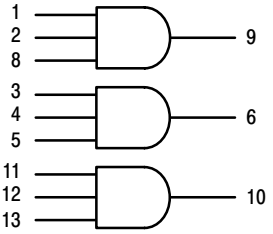


OR

MC14071B
Quad 2–Input OR Gate

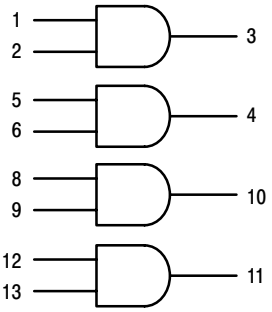


MC14073B
Triple 3–Input AND Gate

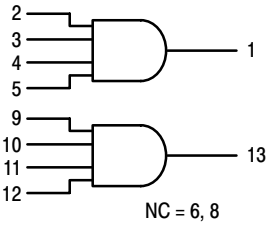


AND

MC14081B
Quad 2–Input AND Gate



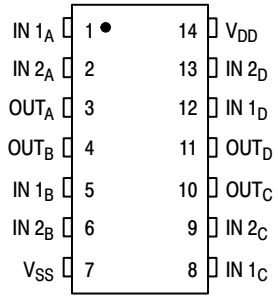
MC14082B
Dual 4–Input AND Gate



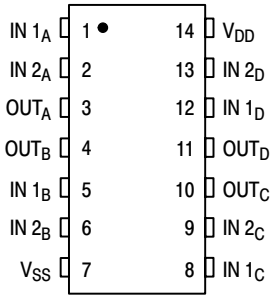
V_{DD} = PIN 14
V_{SS} = PIN 7
FOR ALL DEVICES

PIN ASSIGNMENTS

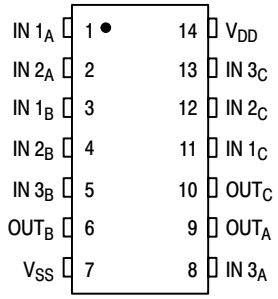
MC14001B
Quad 2–Input NOR Gate



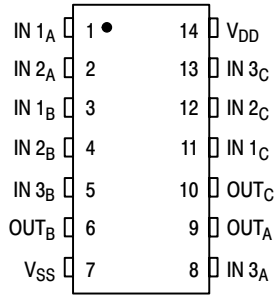
MC14011B
Quad 2–Input NAND Gate



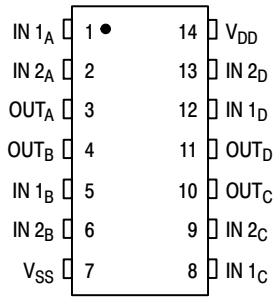
MC14023B
Triple 3–Input NAND Gate



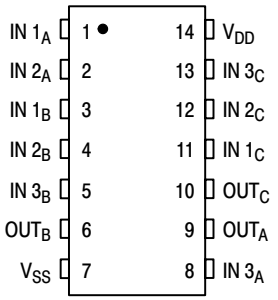
MC14025B
Triple 3–Input NOR Gate



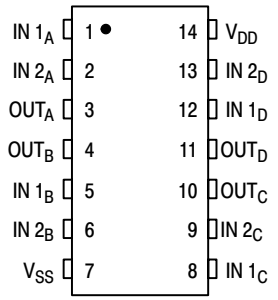
MC14071B
Quad 2–Input OR Gate



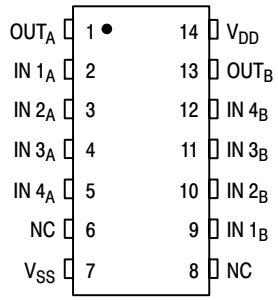
MC14073B
Triple 3–Input AND Gate



MC14081B
Quad 2–Input AND Gate



MC14082B
Dual 4–Input AND Gate



NC = NO CONNECTION

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
“1” Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	µAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}/N							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}/N							
		15	I_T = (0.9 µA/kHz) f + I_{DD}/N							

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

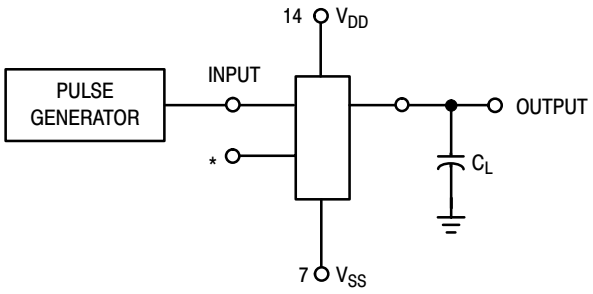
where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.

B–SERIES GATE SWITCHING TIMES

SWITCHING CHARACTERISTICS [6.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ [7.]	Max	Unit
Output Rise Time, All B–Series Gates	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH} = (0.40 ns/PF) C_L + 20 ns		15	—	40	80	
Output Fall Time, All B–Series Gates	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
MC14001B, MC14011B only						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 80 ns		5.0	—	125	250	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 32 ns		10	—	50	100	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 27 ns		15	—	40	80	
All Other 2, 3, and 4 Input Gates						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns		5.0	—	160	300	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns		10	—	65	130	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		15	—	50	100	
8–Input Gates (MC14068B, MC14078B)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 155 ns		5.0	—	200	350	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 62 ns		10	—	80	150	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	—	60	110	

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.



*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.

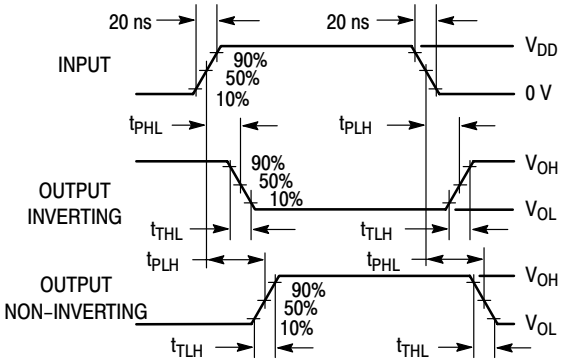
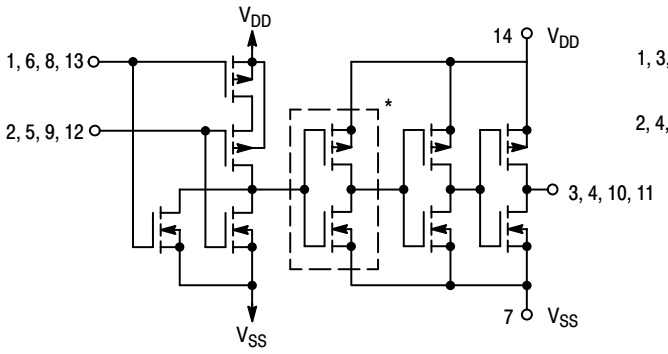


Figure 1. Switching Time Test Circuit and Waveforms

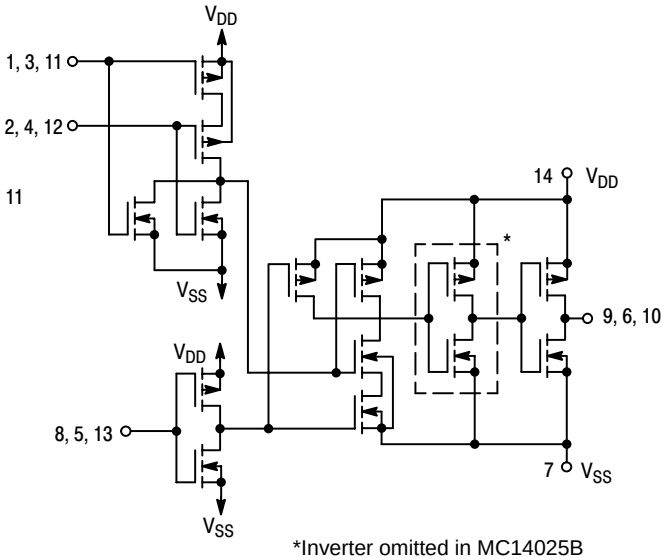
CIRCUIT SCHEMATIC
NOR, OR GATES

MC14001B, MC14071B
One of Four Gates Shown



*Inverter omitted in MC14001B

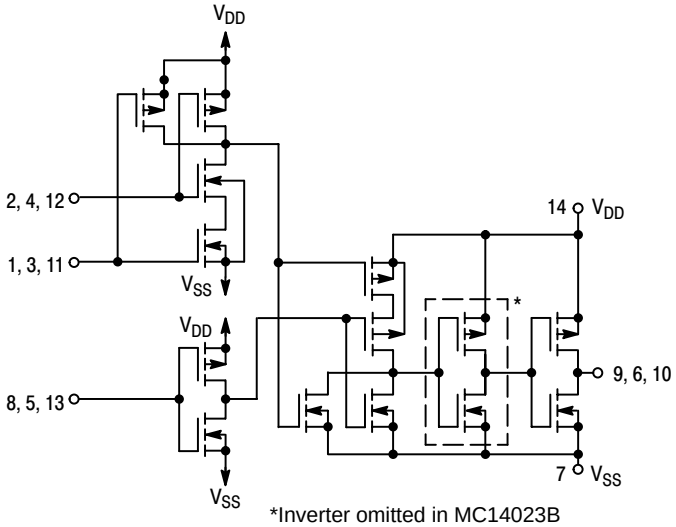
MC14025B
One of Three Gates Shown



*Inverter omitted in MC14025B

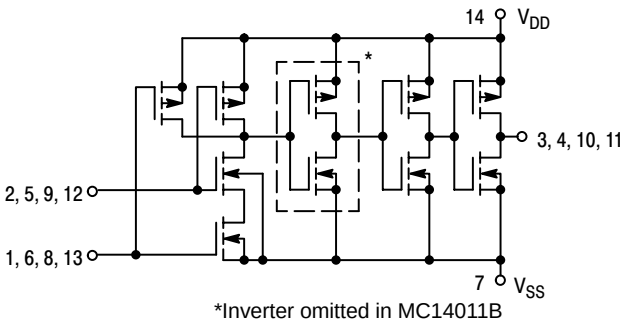
CIRCUIT SCHEMATIC
NAND, AND GATES

MC14023B, MC14073B
One of Three Gates Shown



*Inverter omitted in MC14023B

MC14011B, MC14081B
One of Four Gates Shown



*Inverter omitted in MC14011B

TYPICAL B–SERIES GATE CHARACTERISTICS

N–CHANNEL DRAIN CURRENT (SINK)

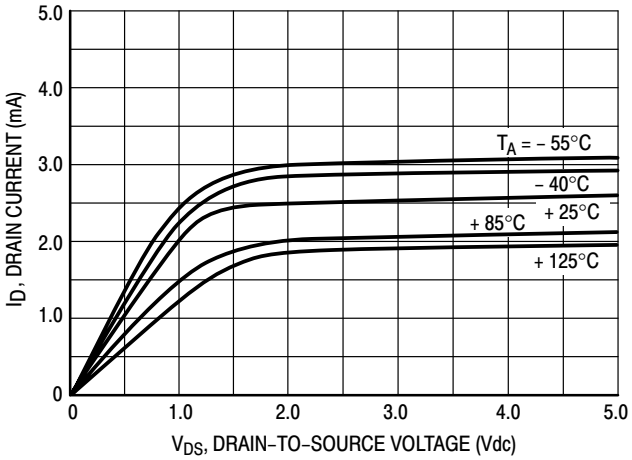


Figure 2. V_{GS} = 5.0 Vdc

P–CHANNEL DRAIN CURRENT (SOURCE)

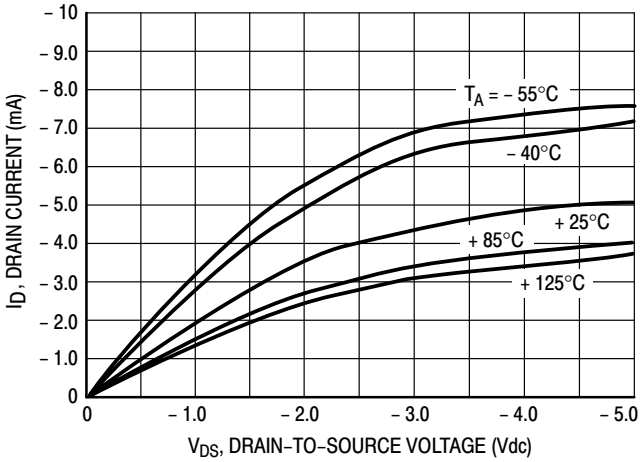


Figure 3. V_{GS} = – 5.0 Vdc

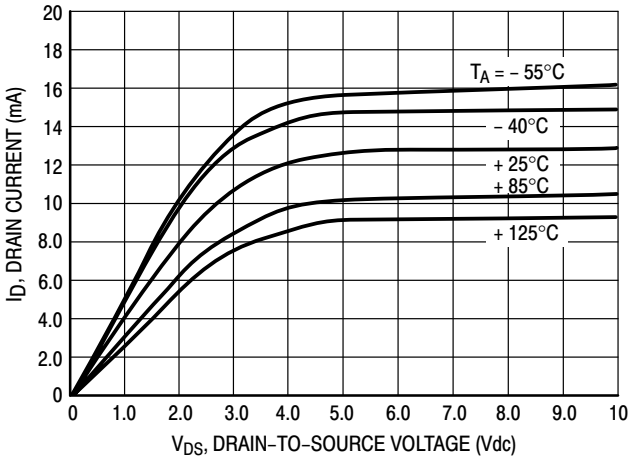


Figure 4. V_{GS} = 10 Vdc

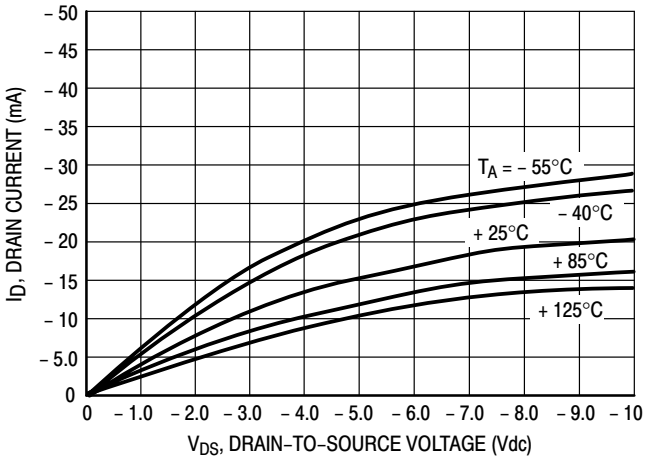


Figure 5. V_{GS} = – 10 Vdc

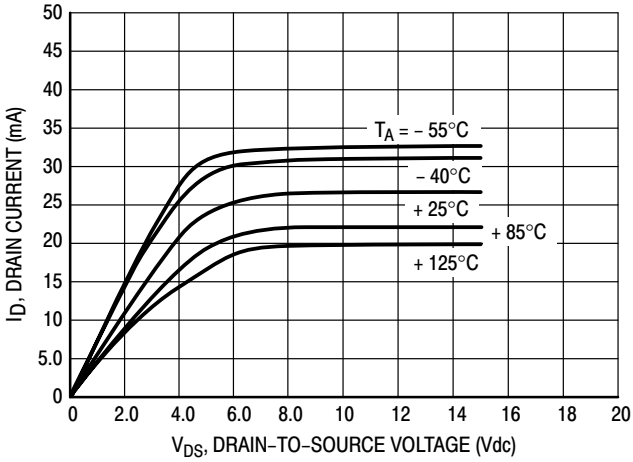


Figure 6. V_{GS} = 15 Vdc

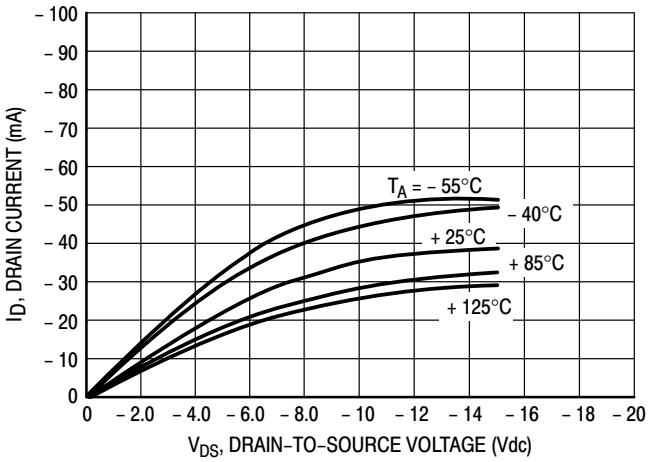


Figure 7. V_{GS} = – 15 Vdc

These typical curves are not guarantees, but are design aids.
Caution: The maximum rating for output current is 10 mA per pin.

TYPICAL B–SERIES GATE CHARACTERISTICS (cont'd)

VOLTAGE TRANSFER CHARACTERISTICS

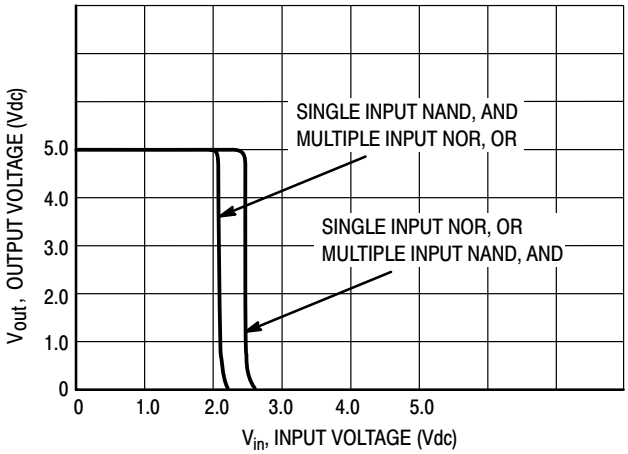


Figure 8. V_{DD} = 5.0 Vdc

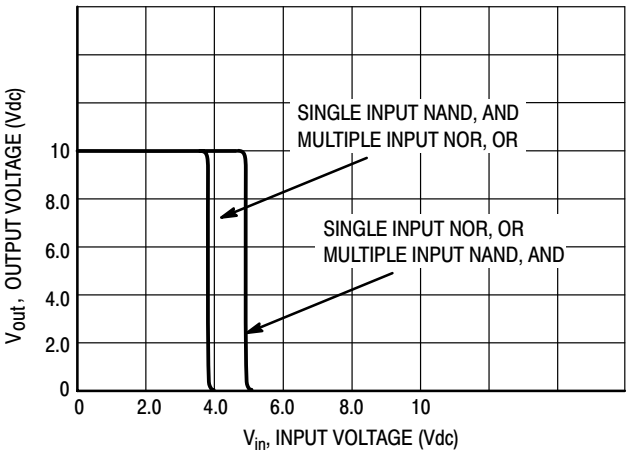


Figure 9. V_{DD} = 10 Vdc

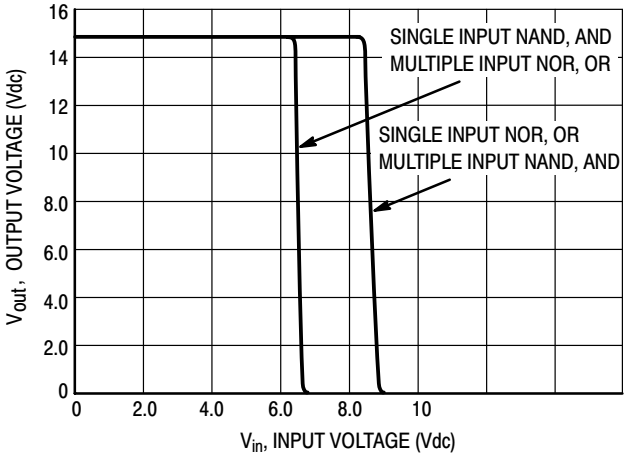


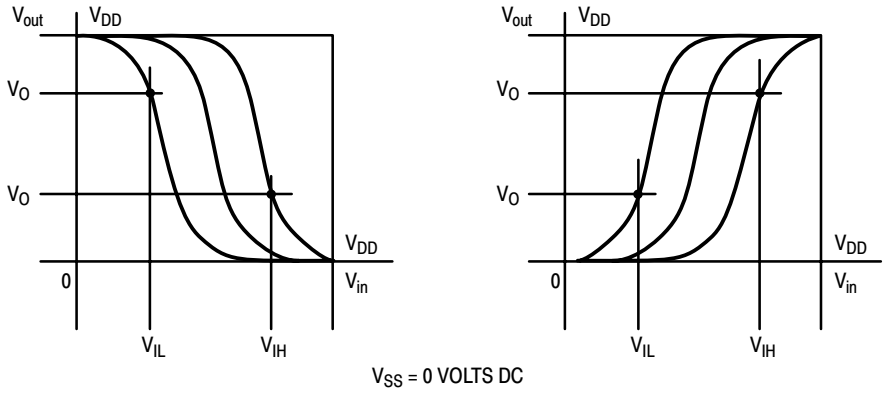
Figure 10. V_{DD} = 15 Vdc

DC NOISE MARGIN

The DC noise margin is defined as the input voltage range from an ideal "1" or "0" input level which does not produce output state change(s). The typical and guaranteed limit values of the input values V_{IL} and V_{IH} for the output(s) to be at a fixed voltage V_O are given in the Electrical Characteristics table. V_{IL} and V_{IH} are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the "1" and "0" levels =

1.0 V with a 5.0 V supply
2.0 V with a 10.0 V supply
2.5 V with a 15.0 V supply

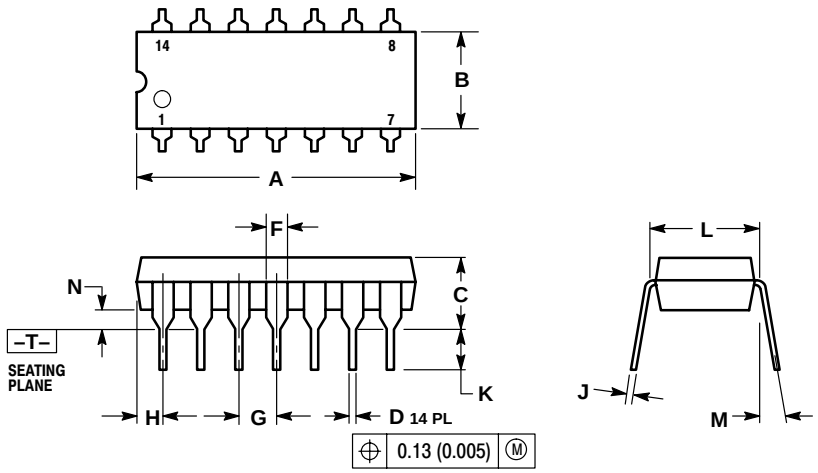


(a) Inverting Function **(b) Non–Inverting Function**

Figure 11. DC Noise Immunity

PACKAGE DIMENSIONS

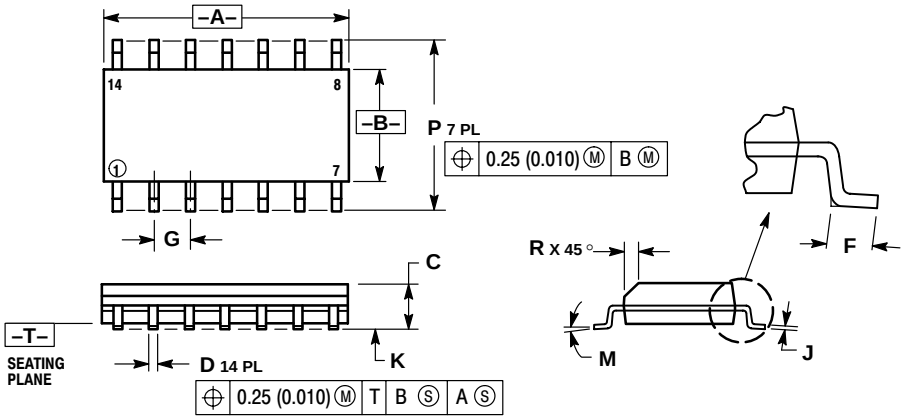
P SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F

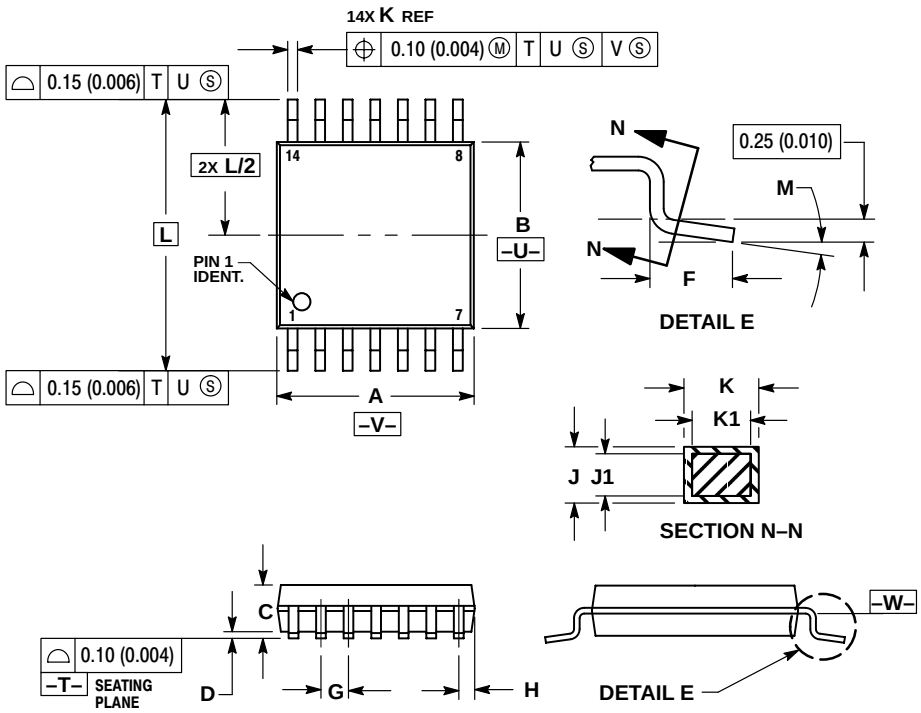


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O

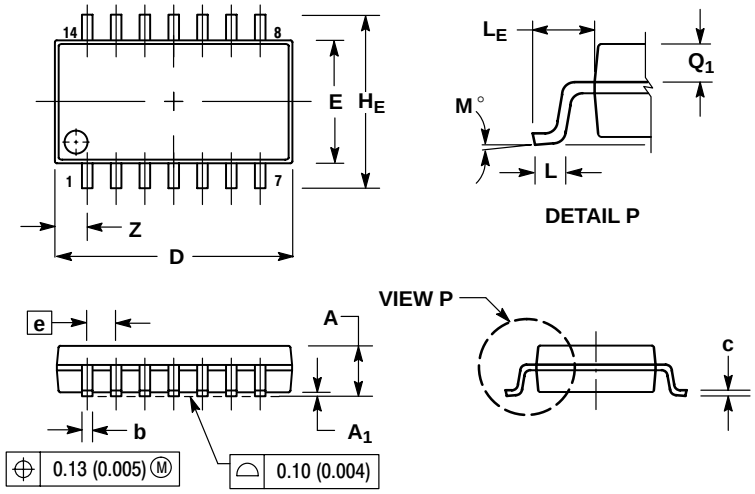


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 965–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

ORDERING & SHIPPING INFORMATION:

Device	Package	Shipping
MC14001BCP	PDIP–14	2000 Units per Box
MC14001BD	SOIC–14	2750 Units per Box
MC14001BDR2	SOIC–14	2500 Units / Tape & Reel
MC14001BDT	TSSOP–14	96 Units per Rail
MC14001BDTR2	TSSOP–14	96 Units per Rail
MC14011BCP	PDIP–14	2000 Units per Box
MC14011BD	SOIC–14	2750 Units per Box
MC14011BDR2	SOIC–14	2500 Units / Tape & Reel
MC14011BDT	TSSOP–14	96 Units per Rail
MC14011BDTEL	TSSOP–14	2000 Units / Tape & Reel
MC14011BDTR2	TSSOP–14	50 Units per Rail
MC14023BCP	PDIP–14	2000 Units per Box
MC14023BD	SOIC–14	2750 Units per Box
MC14023BDR2	SOIC–14	2500 Units / Tape & Reel
MC14025BCP	PDIP–14	2000 Units per Box
MC14025BD	SOIC–14	2750 Units per Box
MC14025BDR2	SOIC–14	2500 Units / Tape & Reel

ORDERING & SHIPPING INFORMATION:

Device	Package	Shipping
MC14071BCP	PDIP–14	2000 Units per Box
MC14071BD	SOIC–14	55 Units per Rail
MC14071BDR2	SOIC–14	2500 Units / Tape & Reel
MC14071BDT	TSSOP–14	96 Units per Rail
MC14071BDTR2	TSSOP–14	96 Units per Rail
MC14073BCP	PDIP–14	2000 Units per Box
MC14073BD	SOIC–14	55 Units per Rail
MC14073BDR2	SOIC–14	2500 Units / Tape & Reel
MC14081BCP	PDIP–14	2000 Units per Box
MC14081BD	SOIC–14	55 Units per Rail
MC14081BDR2	SOIC–14	2500 Units / Tape & Reel
MC14081BDT	TSSOP–14	96 Units per Rail
MC14081BDTR2	TSSOP–14	2500 Units / Tape & Reel
MC14082BCP	PDIP–14	2000 Units per Box
MC14082BD	SOIC–14	55 Units per Rail
MC14082BDR2	SOIC–14	2500 Units / Tape & Reel

For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

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For additional information, please contact your local
Sales Representative.

Associated Documents

Item	Short Desc
Application Notes	Using Power MOSFETS in Stepping Motor Control
Data Sheet	B-Suffix Series CMOS Gates

Device MC14071B

Quad 2-Input OR Gate

The B Series logic gates are constructed with P and N channel enhancement mod monolithic structure (Complementary MOS). Their primary use is where low power noise immunity is desired.

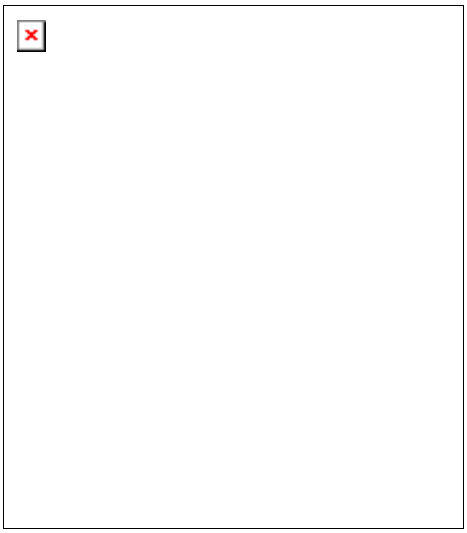
Features:

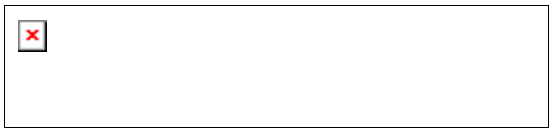
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices

Orderable Parts

Action	Orderable Part	Short Desc.	Package Desc.	Pin Count	Case Outline	Status

N/A	MC14071BDT	Quad 2-Input OR Gate	TSSOP	14	948G-01	Active
N/A	MC14071BCP	Quad 2-Input OR Gate	PDIP	14	646-06	Active
N/A	MC14071BD	Quad 2-Input OR Gate	SOIC	14	751A-03	Active
N/A	MC14071BDR2	Tape and Reel	SOIC	14	751A-03	Active
N/A	MC14071BDTR2	Tape and Reel	TSSOP	14	948G-01	Active
N/A	MC14071BF	Quad 2-Input OR Gate		14	965-01	Active
N/A	MC14071BFEL	Tape and Reel		14	965-01	Active
N/A	MC14071BFL1	Tape and Reel		14	965-01	LifeTime
N/A	MC14071BFL2	Tape and Reel		14	965-01	LifeTime
N/A	MC14071BFR2	Tape and Reel		14	965-01	LifeTime





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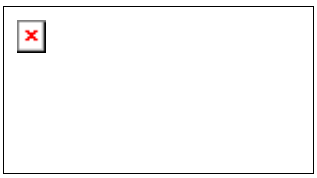

Product Quick Links

Associated Documents

Item	Short Desc	Size
Data Sheet	B-Suffix Series CMOS Gates	133

Device MC14073B

Triple 3-Input AND Gate

The B Series logic gates are constructed with P and N channel enhancement mod monolithic structure (Complementary MOS). Their primary use is where low power noise immunity is desired.

Features:

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices

Orderable Parts

Action	Orderable Part	Short Desc.	Package Desc.	Pin Count	Case Outline	Status	I
N/A	MC14073BCP	Triple 3-	PDIP	14	646-06	Active	

		Input AND Gate					
N/A	MC14073BD	Triple 3-Input AND Gate	SOIC	14	751A-03	Active	9
N/A	MC14073BDR2	Tape and Reel	SOIC	14	751A-03	Active	9
N/A	MC14073BF	Triple 3-Input AND Gate		14	965-01	Active	9
N/A	MC14073BFEL	Tape and Reel		14	965-01	Active	9
N/A	MC14073BFL1	Tape and Reel		14	965-01	LifeTime	
N/A	MC14073BFR1	Tape and Reel		14	965-01	LifeTime	

Associated Documents

Item	Short Desc
Application Notes	Infrared Sensing and Data Transmission Fundamentals
Application Notes	Using Power MOSFETS in Stepping Motor Control
Data Sheet	B-Suffix Series CMOS Gates

Device MC14081B

Quad 2-Input AND Gate

The B Series logic gates are constructed with P and N channel enhancement mod monolithic structure (Complementary MOS). Their primary use is where low power noise immunity is desired.

Features:

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices

Orderable Parts

Action	Orderable Part	Short	Package	Pin	Case	Status

Action	Orderable Part	Desc.	Desc.	Count	Outline	Status
N/A	MC14081BCP	CMOS Quad 2-Input AND Gate	PDIP	14	646-06	Active
N/A	MC14081BD	CMOS Quad 2-Input AND Gate	SOIC	14	751A-03	Active
N/A	MC14081BDR2	Tape and Reel	SOIC	14	751A-03	Active
N/A	MC14081BDTR2	Tape and Reel	TSSOP	14	948G-01	Active
N/A	MC14081BDT	CMOS Quad 2-Input AND Gate	TSSOP	14	948G-01	Active
N/A	MC14081BF	CMOS Quad 2-Input AND Gate		14	965-01	Active
N/A	MC14081BFEL	Tape and Reel		14	965-01	Active
N/A	MC14081BFL1	Tape and Reel		14	965-01	LifeTime
N/A	MC14081BFL2	Tape and Reel		14	965-01	LifeTime
N/A	MC14081BFR1	Tape and Reel		14	965-01	LifeTime
N/A	MC14081BFR2	Tape and Reel		14	965-01	LifeTime

Associated Documents

Item	Short Desc	Size
Data Sheet	B-Suffix Series CMOS Gates	133

Device MC14082B

Dual 4-Input AND Gate

The B Series logic gates are constructed with P and N channel enhancement mod monolithic structure (Complementary MOS). Their primary use is where low power noise immunity is desired.

Features:

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices

Orderable Parts

Action	Orderable Part	Short Desc.	Package Desc.	Pin Count	Case Outline	Status	I
N/A	MC14082BCP	Dual 4-	PDIP	14	646-06	Active	

		Input AND Gate					
N/A	MC14082BD	Dual 4-Input AND Gate	SOIC	14	751A-03	Active	9
N/A	MC14082BDR2	Tape and Reel	SOIC	14	751A-03	Active	9
N/A	MC14082BF	Dual 4-Input AND Gate		14	965-01	Active	9
N/A	MC14082BFR2	Tape and Reel		14	965-01	LifeTime	