Features

- **Usable for Automotive 12 V/24 V and Industrial Applications**
- **Maximum High-speed Data Transmissions up to 1 MBaud**
- **Fully Compatible with ISO 11898**
- **Controlled Slew Rate**
- **Standby Mode**
- **TXD Input Compatible to 3.3 V**
- **Short-circuit Protection**
- **Overtemperature Protection**
- **High Voltage Bus Lines Protection, -40 V to +40 V**
- **High Speed Differential Receiver Stage with a Wide Common Mode Range, -10 V to +10 V, for High Electromagnetic Immunity (EMI)**
- **Fully Controlled Bus Lines, CANH and CANL to Minimize Electromagnetic Emissions (EME)**
- **High ESD Protection at CANH, CANL HBM 8 kV, MM 300 V**

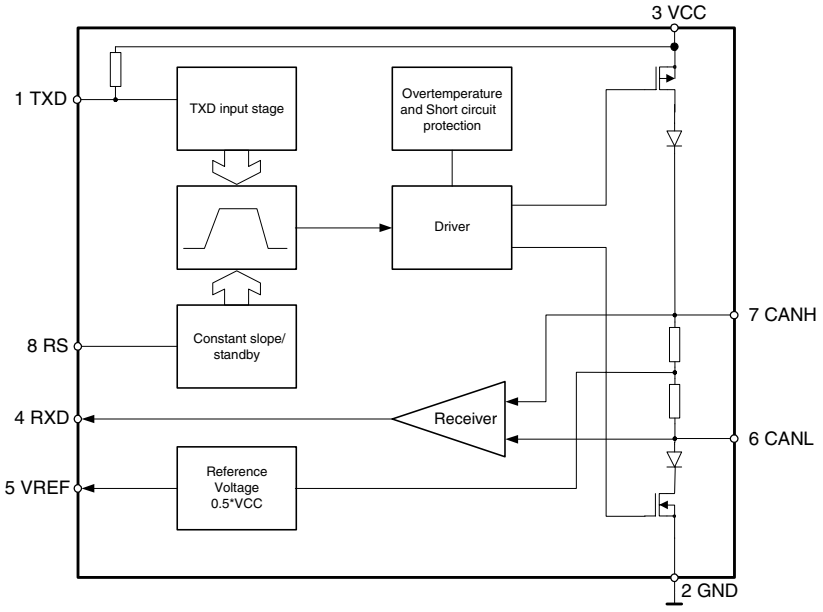
High-speed CAN Transceiver

ATA6660

Description

The ATA6660 is a monolithic circuit based on the Atmel's Smart Power BCD60-III technology. It is especially designed for high speed CAN-Controller (CAN-C) differential mode data transmission between CAN-Controllers and the physical differential bus lines.

Figure 1. Block Diagram



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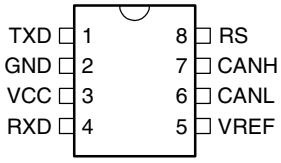
Pin Configuration

Figure 2. Pinning SO8



Pin Description

Pin	Symbol	Function
1	TXD	Transmit data input
2	GND	Ground
3	VCC	Supply voltage
4	RXD	Receive data output
5	VREF	Reference voltage output
6	CANL	Low level CAN voltage input/output
7	CANH	High level CAN voltage input/output
8	RS	Switch standby mode/normal mode

Functional Description

The ATA6660 is a monolithic circuit based on Atmel's Smart Power BCD60-III technology. It is especially designed for high-speed differential mode data transmission in harsh environments like automotive and industrial applications. Baudrate can be adjusted up to 1 Mbaud. The ATA6660 is fully compatible to the ISO11898, the developed standard for high speed CAN-C (Controller Area Network) communication.

Voltage Protection and ESD

High voltage protection circuitry on both line pins, CANH (Pin 7) and CANL (Pin 6), allow bus line voltages in the range of -40 V to +40 V. ESD protection circuitry on line pins allow HBM = 8 kV, MM = 300 V. The implemented high voltage protection on bus line output/input pins (7/6) makes the ATA6660 suitable for 12 V automotive applications as well as 24 V automotive applications.

Slope Control

A fixed slope is adjusted to prevent unsymmetrical transients on bus lines causing EMC problems. Controlled bus lines, both CANH and CANL signal, will reduce radio frequency interference to a minimum. In well designed bus configurations the filter design costs can be reduced dramatically.

Overcurrent Protection

In the case of a line shorts, like CANH to GND, CANL to VCC, integrated short current limitation allows a maximum current of I_{CANH_SC} or I_{CANL_SC}. If junction temperature rises above 165°C an internal overtemperature protection circuitry shuts down both output stages, the receiver will stay activated.

Standby Mode

The ATA6660 can be switched to standby mode by forcing the voltage VRS > 0.87 × VCC. In standby mode the supply current will reduce dramatically, supply current during standby mode is typical 600 µA (I_{VCC_stby}). Transmitting data function will not be supported, but the oppertunity will remain to receive data. A high-speed comparator is listening for activities on the bus. A dominant bus signal will force the output RXD to a low level in typical t_{dRXDL} = 400 ns. If the RS pin is not connected, causing through a broken connection to the controller, the ATA6660 will switch to standby mode automatically.

High-speed Receiver

In normal mode a fast receiver circuitry combined with a resistor network is able to detect differential bus line voltages V_{rec_th} > 0.9 V as dominant bit, differential bus line voltages V_{rec_th} < 0.5 V as recessive bit.

The wide receiver common mode range, -10 V to +10 V, combined with a symmetrical differential receiver stage offers high immunity against electromagnetic interference. A typical hysteresis of 70 mV is implemented. Dominant differential bus voltages forces RXD output (Pin 4) to low level, recessive differential bus voltages to high level.

TXD Input

The input stage Pin 1 (TXD) is compatible for 3.3 V output levels from new controller families. Pull-up resistance (25 kΩ) forces the IC to recessive mode, if TXD-Pin is not connected. TXD low signal drives the transmitter into dominant state.

Transmitter

A integrated complex compensation technique allows stable data transmission up to 1 MBaud. Low level on TXD input forces bus line voltages CANH to 3.5 V, CANL to 1.5 V with a termination resistor of 60 Ω. In the case of a line short circuit, like CANH to GND, CANL to VCC, integrated short current limitation circuitry allows a maximum current of 150 mA. If junction temperature rises above typical 163°C an internal overtemperature protection shuts down both output stages, the receive mode will stay activated.

Split Termination Concept

With a modified bus termination (see Figure 5) a reduction of emission and a higher immunity of the bus system can be achieved. The one 120 Ω resistor at the bus line end nodes is split into two resistors of equal value, i.e., two resistors of 60 Ω. The resistors for the stub nodes is recommended with two resistors of 1,3 kΩ. (for example 8 stub nodes and 2 bus end nodes) Notice: The bus load of all the termination resistors has to stay within the range of 50 Ω to 65 Ω.

The common mode signal at the centre tap of the termination is connected to ground via a capacitor of e.g., C_{split} = 10 nF to 100 nF. A seperate ground lead to the ground pin of the module connector is recommended.

Absolute Maximum Ratings

Parameters	Symbol	Conditions	Min.	Max.	Unit
Supply voltage	V_{CC}		-0.3	+6	V
DC voltage at Pins 1, 4, 5 and 8	V_{TXD}, V_{REF}, V_{RS}, V_{RXD}		-0.3	V_{CC} +0.3	V
DC voltage at Pins 6 and 7	V_{CANH}, V_{CANL}	0 V < V_{CC} < 5.25 V; no time limit	-40.0	+40.0	V
Transient voltage at Pins 6 and 7			-150	+100	V
Storage temperature	T_{Stg}		-55	+150	°C
Operating ambient temperature	T_{amb}		-40	+125	°C
ESD classification	All pins	HBM ESD S.5.1 MM JEDEC A115A	±3000 ±200		V V
ESD classification	Pin 6, 7 versus Pin 2	HBM 1.5 kΩ, 100 pF MM 0Ω, 200 pF	±8000 ±300		V V

Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance from junction to ambient	R_{thJA}	160	K/W

Truth Table

VCC	TXD	RS	CANH	CANL	Bus State	RXD
4.75 V to 5.25 V	0	< 0.3 × V_{CC}	3.5 V	1.5 V	Dominant	0
4.75 V to 5.25 V	1 (or floating)	< 0.3 × V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	Recessive	1
4.75 V to 5.25 V	X	> 0.87 × V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	Recessive	1

RS (Pin 8) Functionality

Slope Control	Mode	Voltage and Current Levels
V_{RS} > 0.87 × V_{CC}	Standby	I_{RS} < | 10 µA |
V_{RS} < 0.3 × V_{CC}	Constant slope control	I_{RS} ≤ 500 µA

Electrical Characteristics

V_{CC} = 4.75 V to 5.25 V; T_{amb} = -40°C to +125°C; R_{Bus} = 60 Ω; unless otherwise specified
All voltages referenced to ground (Pin 2); positive input current.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Supply Current**								
1.1	Supply current dominant	V_{TXD} = 0 V V_{RS} = 0 V	3	I_{vcc_dom}		45	60	mA	A
1.2	Supply current recessive	V_{TXD} = 5 V V_{RS} = 0 V	3	I_{vcc_rec}		10	15	mA	A
1.3	Supply current stand-by	V_{RS} = 5 V	3	I_{vcc_stby}		600	980	µA	A
2	**Transmitter Data Input TXD**								
2.1	HIGH level input voltage	V_{TXD} = 5 V V_{RS} = 0 V	1	V_{TXDH}	2		V_{CC}+0.3	V	A
2.2	LOW level input voltage	V_{TXD} = 0 V V_{RS} = 0 V	1	V_{TXDL}	-0.3		+1	V	A
2.3	HIGH level input current	V_{TXD} = V_{CC}	1	I_{IH}	-1		0	µA	A
2.4	LOW level input voltage	V_{TXD} = 0 V	1	I_{IL}	-500		-50	µA	A
3	**Receiver Data Output RXD**								
3.1	High level output voltage	I_{RXD} = -100 µA	4	V_{RXDH}	0.8 × V_{CC}		V_{CC}	V	A
3.2	Low level output voltage	I_{RXD} = 1 mA	4	V_{RXDL}	0		0.2 × V_{CC}	V	A
3.3	Short current at RXD	V_{TXD} = 5 V V_{RXD} = 0 V	4	I_{RXDs1}	-3		-1	mA	A
3.4	Short current at RXD	V_{TXD} = 0 V V_{RXD} = 5 V	4	I_{RXDs2}	2		6	mA	A
4	**Reference Output Voltage VREF**								
4.1	Reference output voltage normal mode	VRS = 0 V; -50 µA < I5 < 50 µA	5	V_{ref_no}	0.45 V_{CC}	-	0.55 V_{CC}	V	A
4.2	Reference output voltage standby mode	VRS = 5 V; -5µA < I5 < 5 µA	5	V_{ref_stby}	0.4 × V_{CC}	-	0.6 V_{CC}	V	A
5	**DC Bus Transmitter CANH; CANL**								
5.1	Recessive bus voltage	V_{TXD} = V_{CC}; no load	6, 7	V_{CANH}; V_{CANL}	2.0	2.5	3.0	V	A
5.2	$I_{O(CANH)(reces)}$ $I_{O(CANL)(reces)}$	-40 V < V_{CANH}; V_{CANL} < 40 V; 0 V < V_{CC} < 5.25 V	6, 7	I_{O_reces}	-5		+5	mA	A
5.3	CANH output voltage dominant	V_{TXD} = 0 V	6, 7	V_{CANH}	2.8	3.5	4.5	V	A
5.4	CANL output voltage dominant	V_{TXD} = 0 V	6, 7	V_{CANL}	0.5	1.5	2.0	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics (Continued)

V_{CC} = 4.75 V to 5.25 V; T_{amb} = -40°C to +125°C; R_{Bus} = 60 Ω; unless otherwise specified
All voltages referenced to ground (Pin 2); positive input current.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5.5	Differential bus output voltage ($V_{CANH} - V_{CANL}$)	V_{TXD} = 0 V; R_L = 45 Ω to 60 Ω; V_{CC} = 4.9 V	6, 7	$Vdiff_{dom}$	1.5	2	3.0	V	A
5.6		$V_{TXD} = V_{CC}$; no load	6, 7	$Vdiff_{rec}$	-500		+50	mV	A
5.7	Short-circuit CANH current	V_{CANH} = -10 V TXD = 0 V	6, 7	I_{CANH_SC}	-35		-100	mA	A
5.8	Short-circuit CANL current	V_{CANL} = 18 V TXD = 0 V	6, 7	I_{CANL_SC}	50	-	150	mA	A
6	**DC Bus Receiver CANH; CANL**								
6.1	Differential receiver threshold voltage normal mode	-10 V < V_{CANH} < +10 V -10 V < V_{CANL} < +10 V	6, 7	V_{rec_th}	0.5	0.7	0.9	V	A
6.2	Differential receiver threshold voltage stand-by mode	$V_{RS} = V_{CC}$	6, 7	$V_{rec\_th\_stby}$	0.5	0.7	0.9	V	A
6.3	Differential input hysteresis		6, 7	$V_{diff(hys)}$		70		mV	A
6.4	CANH and CANL common mode input resistance		6, 7	R_i	5	15	25	kΩ	A
6.5	Differential input resistance		6, 7	R_{diff}	10	30	100	kΩ	A
6.6	Matching between CANH and CANL common mode input resistance		6, 7	R_{i_m}	-3		+3	%	A
6.7	CANH, CANL input capacitance		6, 7	C_i			20	pF	D
6.8	Differential input capacitance		6, 7	C_{diff}			10	pF	D
6.9	CANH, CANL input leakage input current	V_{CC} = 0 V V_{CANH} = 3.5 V V_{CANL} = 1.5 V	6, 7	$I_{LI(CANH)}$; $I_{LI(CANL)}$			250	µA	A
7	**Thermal Shut-down**								
7.1	Shut-down junction temperature for CANH/CANL			$T_{J(SD)}$	150	163	175	°C	B
7.2	Switch on junction temperature for CANH/CANL			$T_{J(SD)}$	140	154	165	°C	B
7.3	Temperature hysteresis			T_{Hys}		10		K	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics (Continued)

V_{CC} = 4.75 V to 5.25 V; T_{amb} = -40°C to +125°C; R_{Bus} = 60 Ω; unless otherwise specified
All voltages referenced to ground (Pin 2); positive input current.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8	**Timing Characteristics Normal Mode , $V_{RS} \leq 0.3 \times V_{CC}$ (see Figure 3)**								
8.1	Delay TXD to bus active	V_{RS} = 0 V		$t_{d(TXD-BUS\_ON)}$		120	180	ns	A
8.2	Delay TXD to bus inactive	V_{RS} = 0 V		$t_{d(TXD-BUS\_OFF)}$		50	100	ns	A
8.3	Delay TXD to RXD, recessive to dominant	V_{RS} = 0 V	6, 7	$t_{d\_activ(TXD-RXD)}$		200	420	ns	A
8.4	Delay TXD to RXD, dominant to recessive	V_{RS} = 0 V		$t_{d\_inactiv(TXD-RXD)}$		180	460	ns	A
8.5	Difference between Delay TXD to RXD dominant to Delay recessive	$t_{diff} = t_{d\_activ(TXD-RXD)} - t_{d\_inactiv(TXD-RXD)}$		t_{diff}	-280		80	ns	A
9	**Timing Characteristics Stand-by Mode $V_{RS} \geq 0.87 \times V_{CC}$**								
9.1	Bus dominant to RXD low in stand-by mode	$V_{RS} = V_{CC}$	4	t_{dRxDL}	-	300	450	ns	A
9.2	Wake up time after stand-by mode (time delay between stand-by to normal mode and to bus dominant)	TXD = 0 V VRS from 0 V to V_{CC}	6, 7	T_{wake_up}			2	µs	A
10.1	**Standby/Normal Mode Selecteable via RS (Pin 8)**								
10.1	Input voltage for normal mode	$V_{RS} = V_{CC}$	8	V_{RS}	-	-	$0.3 \times V_{CC}$	V	A
10.2	Input current for normal mode	V_{RS} = 0 V	8	I_{RS}	-700			µA	A
10.3	Input voltage for stand-by mode		8	V_{stby}	$0.87 \times V_{CC}$			V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 3. Timing Diagrams

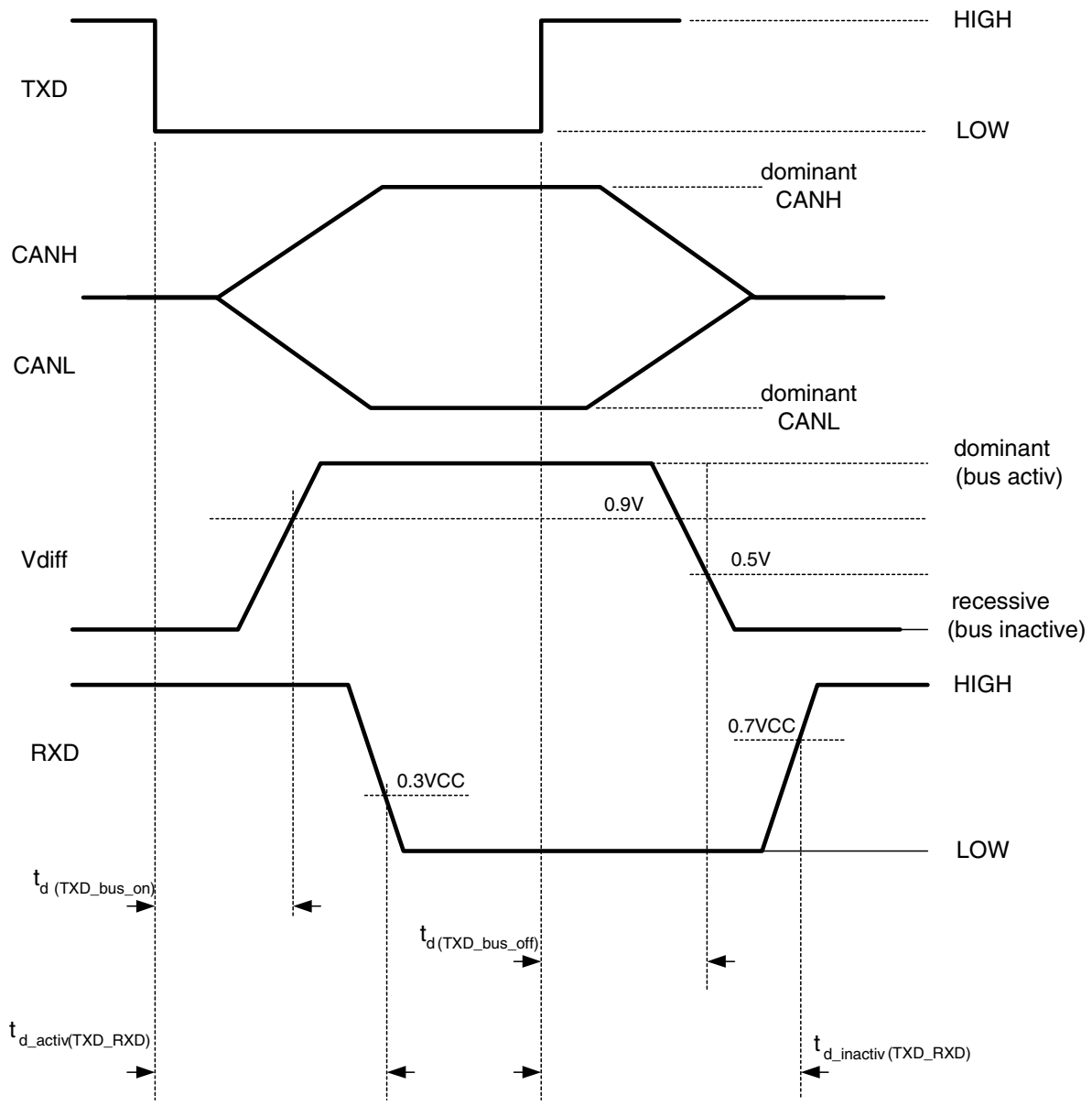


Figure 4. Test Circuit for Timing Characteristics

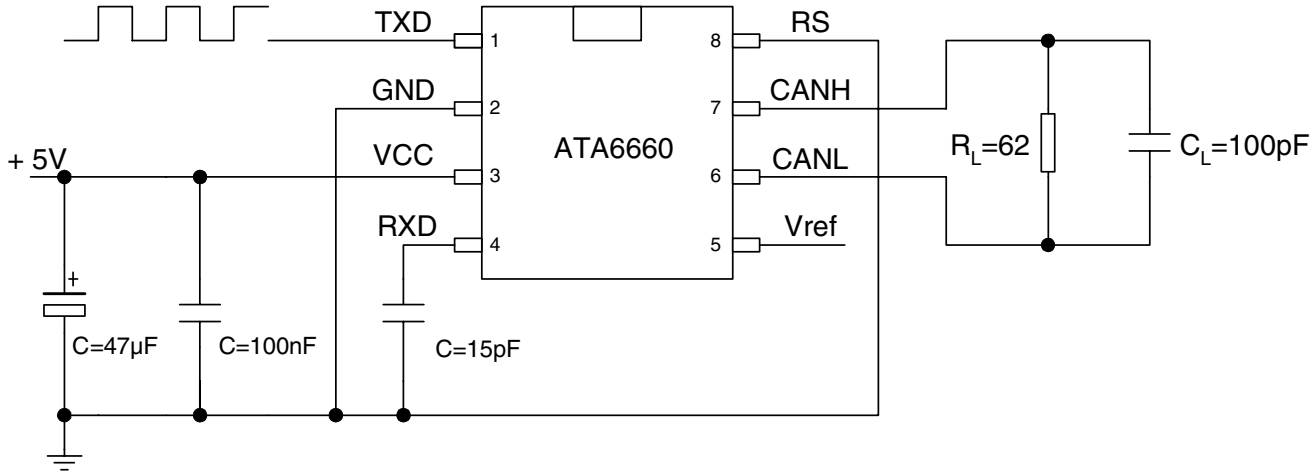
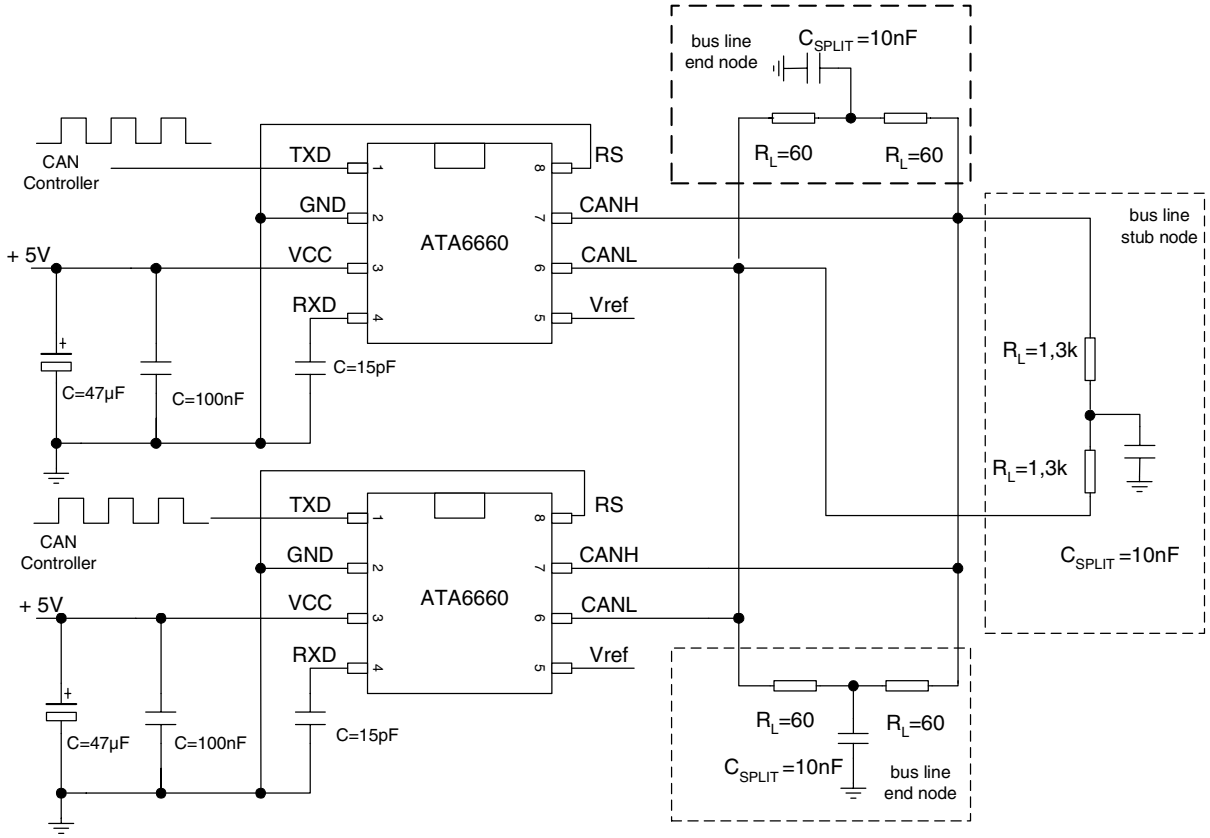


Figure 5. Bus Application with Split Termination Concept



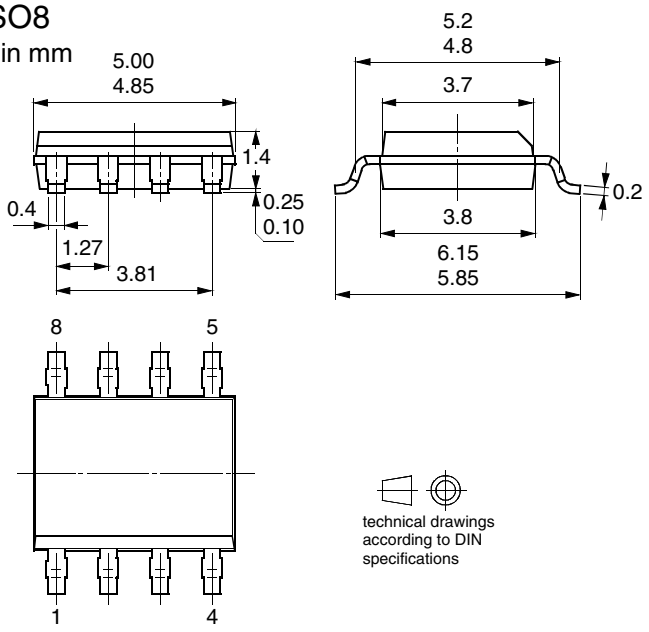
Ordering Information

Extended Type Number	Package	Remarks
ATA6660	SO8	–

Package Information

Package SO8

Dimensions in mm



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