ZiLOG

CUSTOMER PROCUREMENT SPECIFICATION

Z88C00/01

CMOS SUPER8® ROMLESS MCU

GENERAL DESCRIPTION

The CMOS Super8® offers new flexibility and sophistication in 8-bit microcontrollers. The Super8 offers all the features necessary for industrial, consumer, and automotive applications with an enhanced feature set in CMOS technology. At the same time, the CMOS Super8 retains full pin-for-pin compatibility with the NMOS Super8. Available in 48-pin DIP, and 44-, 68-pin PLCC, the CMOS Super8 is the last word in general purpose controllers.

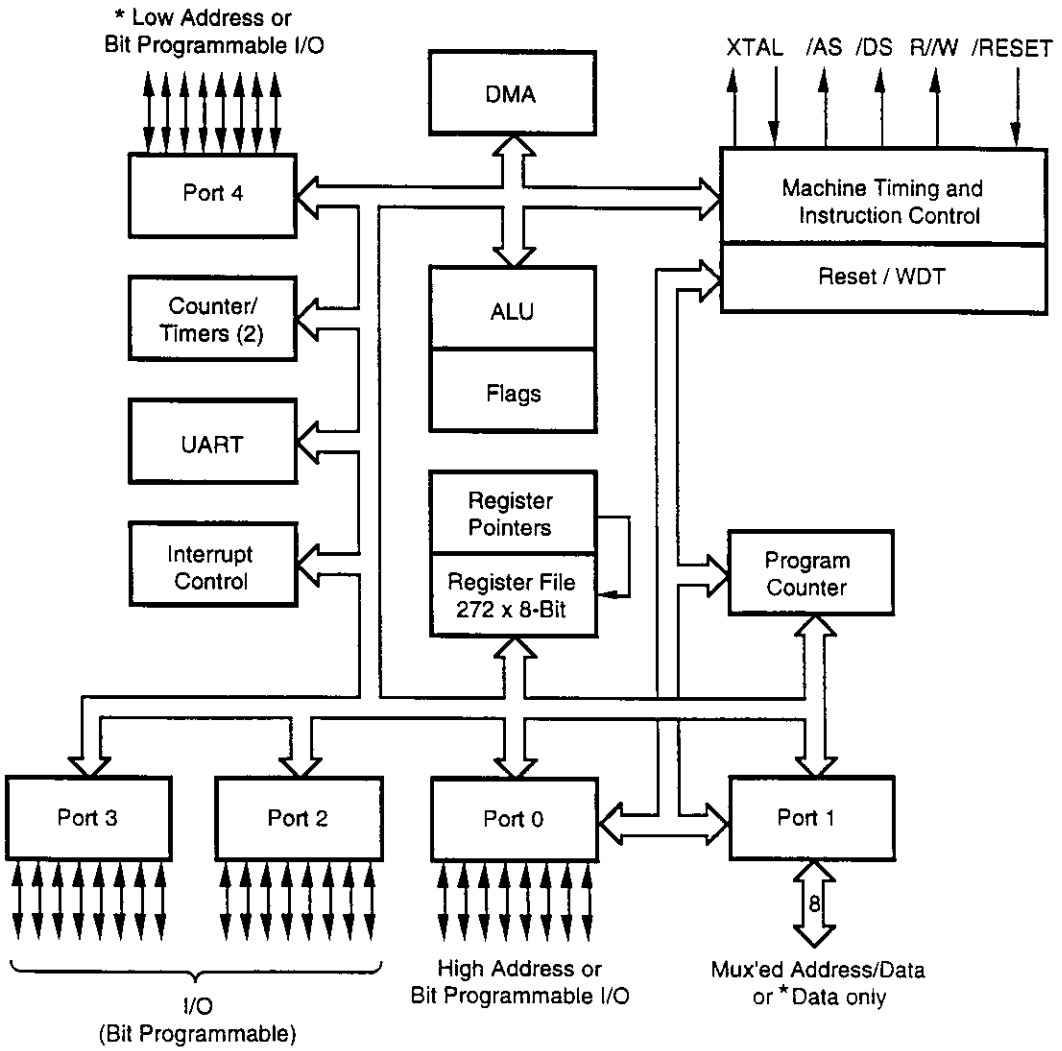
The Super8 features a full-duplex, Universal Asynchronous Receiver/Transmitter (UART) with on-chip baud rate generator, on-chip oscillator, and a Direct Memory Access controller (DMA).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

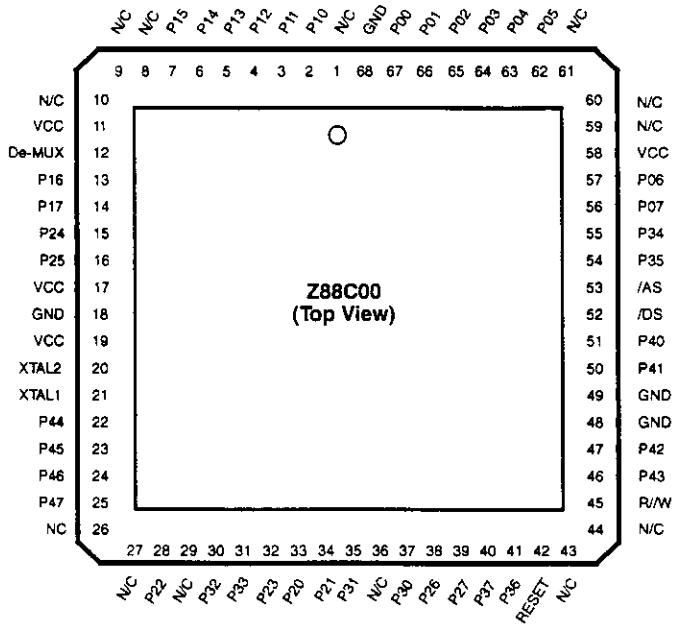
GENERAL DESCRIPTION (Continued)



* Only when used as demux'ed external memory bus.

Functional Block Diagram

GENERAL DESCRIPTION (Continued)

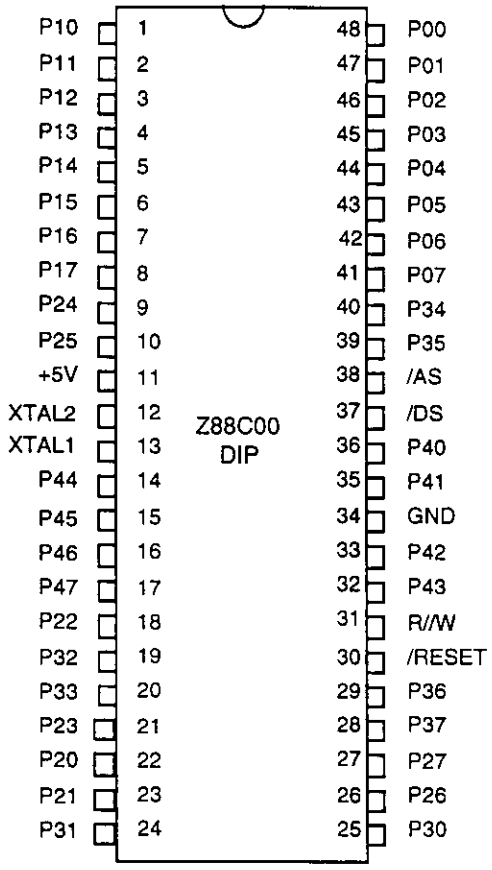


68-Lead PLCC Pin Identification

68-Lead PLCC Pin Assignments

Pin #	Symbol	Function	Direction
1	N/C	Not Connected	
2-7	P15-10	Port 1, Pins 0,1,2,3,4,5	In/Output
8-10	N/C	Not Connected	
11	V_{CC}	Power Supply	Input
12	De-Mux	De-multiplex Pin	Input
13-14	P17-16	Port 1, Pins 6,7	In/Output
15-16	P25-24	Port 2, Pins 4,5	In/Output
17	V_{CC}	Power Supply	Input
18	GND	Ground	Input
19	V_{CC}	Power Supply	Input
20	XTAL2	Crystal Oscillator	Output
21	XTAL1	Crystal Oscillator	Input
22-25	P47-44	Port 4, Pins 4,5,6,7	In/Output
26-27	N/C	Not Connected	
28	P22	Port 2, Pin 2	In/Output
29	N/C	Not Connected	
30-31	P33-32	Port 3, Pins 2,3	In/Output
32-34	P23-21	Port 2, Pins 3,0,1	In/Output
35	P31	Port 3, Pin 1	In/Output
36	N/C	Not Connected	

Pin #	Symbol	Function	Direction
37	P30	Port 3, Pin 0	In/Output
38-39	P27-26	Port 2, Pins 6,7	In/Output
40-41	P37-36	Port 3, Pins 7,6	In/Output
42	/RESET	RESET	Input
43-44	NC	Not Connected	
45	R/W	READ/WRITE	Output
46-47	P43-42	Port 4, Pins 3,2	In/Output
48-49	GND	Ground	Input
50-51	P41-40	Port 4, Pins 1,0	In/Output
52	/DS	Data Strobe	Output
53	/AS	Address Strobe	Output
54-55	P35-34	Port 3, Pins 4,5	In/Output
56-57	P07-06	Port 0, Pins 7,6	In/Output
58	V_{CC}	Power Supply	Input
59-61	N/C	Not Connected	
62-67	P05-00	Port 0, Pins 5,4,3,2,1,0	In/Output
68	GND	Ground	Input



48-Lead DIP Pin Identification

48-Lead DIP Pin Assignments

Pin #	Symbol	Function	Direction
1-8	P17-10	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
9-10	P25-24	Port 2, Pins 4,5	In/Output
11	V_{CC}	Power Supply	Input
12	XTAL2	Crystal Oscillator	Output
13	XTAL1	Crystal Oscillator	Input
14-17	P47-44	Port 4, Pins 4,5,6,7	In/Output
18	P22	Port 2, Pin 2	In/Output
19-20	P33-32	Port 3, Pins 2,3	In/Output
21-23	P23-21	Port 2, Pins 3,0,1	In/Output
24-25	P31-30	Port 3, Pins 1,0	In/Output
26-27	P27-26	Port 2, Pins 6,7	In/Output

Pin #	Symbol	Function	Direction
28-29	P37-36	Port 3, Pins 7,6	In/Output
30	/RESET	RESET	Input
31	R//W	READ/WRITE	Output
32-33	P43-42	Port 4, Pins 3,2	In/Output
34	GND	Ground	Input
35-36	P41-40	Port 4, Pins 1,0	In/Output
37	/DS	Data Strobe	Output
38	/AS	Address Strobe	Output
39-40	P35-34	Port 3, Pins 5,4	In/Output
41-48	P07-00	Port 0, Pins 7,6,5,4,3,2,1,0	In/Output

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp		†	C

Notes:

* Voltage on all pins with respect to GND.
† See Ordering Information.

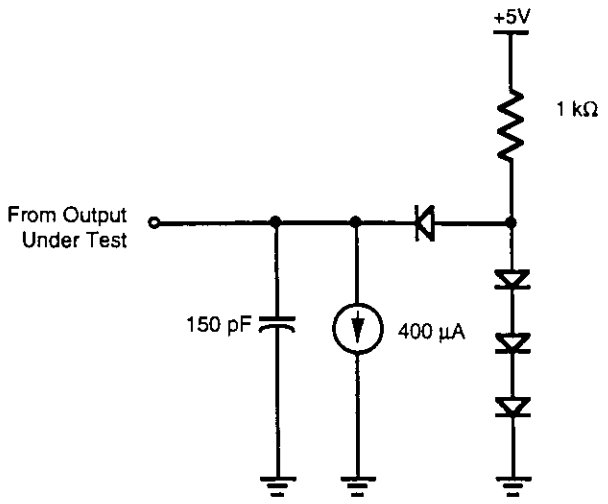
Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to V_{SS}. Positive current flows into the referenced pin (Standard Test Load).

Standard conditions are:

- $4.5V < V_{CC} < 5.5V$
- GND - 0V
- $-40°C < T_A < +105°C$

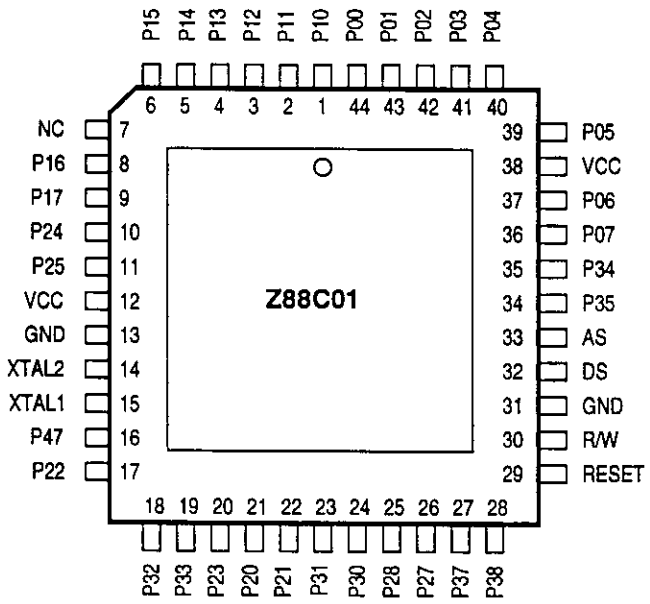


Standard Test Load

ADDITIONAL FEATURE

Weak Latches

All input pins on the Super8® will be provided with weak latches. Weak latches on inputs prevent them from floating and reduces unnecessary current flow. Weak latches on inputs are automatically disabled when the corresponding output is configured as open-drain.



44-Lead PLCC Pin Identification

44-Lead PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-6	P15-10	Port 1, Pins 0,1,2,3,4,5	In/Output
7	N/C	Not Connected	
8-9	P17-16	Port 1, Pins 6,7	In/Output
10-11	P25-24	Port 2, Pins 4,5	In/Output
12	V_{CC}	Power Supply	Input
13	GND	Ground	Input
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16	P47	Port 4, Pin 7	In/Output
17	P22	Port 2, Pin 2	In/Output
18-19	P33-32	Port 3, Pins 2,3	In/Output
20-22	P23-21	Port 2, Pins 3,0,1	In/Output

Pin #	Symbol	Function	Direction
23-24	P31-30	Port 3, Pins 1,0	In/Output
25-26	P27-26	Port 2, Pins 8,7	In/Output
27-28	P37-36	Port 3, Pins 7,8	In/Output
29	/RESET	Reset	Input
30	R/W	Read/Write	Output
31	GND	Ground	Input
32	/DS	Data Strobe	Output
33	/AS	Address Strobe	Output
34-35	P35-34	Port 3, Pins 5,4	In/Output
36-37	P07-06	Port 0, Pins 7,6	In/Output
38	V_{CC}	Power Supply	Input
39-44	P05-00	Port 0, Pins 5,4,3,2,1,0	In/Output

AC ELECTRICAL CHARACTERISTICS

External I/O or Memory Read and Write Timing

Number	Symbol	Parameter	Normal Min	Normal Max	Extended Min	Extended Max
1	TdA(AS)	Address valid to /AS Rise Delay	25		50	
2	ThAS(A)	/AS Rise to Address Valid Hold Time	35		85	
3	TdAS(DI)	/AS Rise to Data In Required Valid Delay		150		335
4	TwAS	/AS Low Width	35		85	
5	TdAZ (DSR)	Address Float to /DS (Read)	0		0	
6	TwDSR	/DS (Read) Low Width	125		275	
7	TwDSW	/DS (Write) Low Width	65		165	
8	TdDSR (DI)	/DS (Read) to Data In Required Valid Delay		80		225
9	ThDSR(DI)	/DS Rise (Read) to Data In Hold Time	0		0	
10	TdDS (A)	/DS Rise to Address Active Delay	20		70	
11	TdDA (AS)	/DS Rise to /AS Delay	30		80	
12	TdR/W (AS)	R/W to AS Rise Delay	20		70	
13	TdDS (R/W)	DS Rise to R/W Valid Delay	40		90	
14	TdDO (DSW)	Data Out to /DS (Write) Delay	10		50	
15	ThDSW (DO)	/DS Rise (Write) to Data Out Hold Time	20		85	
16	TdA (DI)	Address to Data In Required Valid Delay		205		385
17	TdAS (DSR)	/AS Rise to D/S (Read) Delay	50		95	
19	TdDM (AS)	/DM to /AS Rise Delay	28		70	
20	TdDS (DM)	/DS Rise to /DM Valid Delay	33		85	
21	ThDS (A)	/DS Rise to Address Valid Hold Time	36		90	
22	TwW	Wait Width (One Wait) Window	[1]		[1]	
23	TdAS (W)	/AS Rise to Wait Delay		90		335

Notes:

[1] Not characterized function, guaranteed by design.

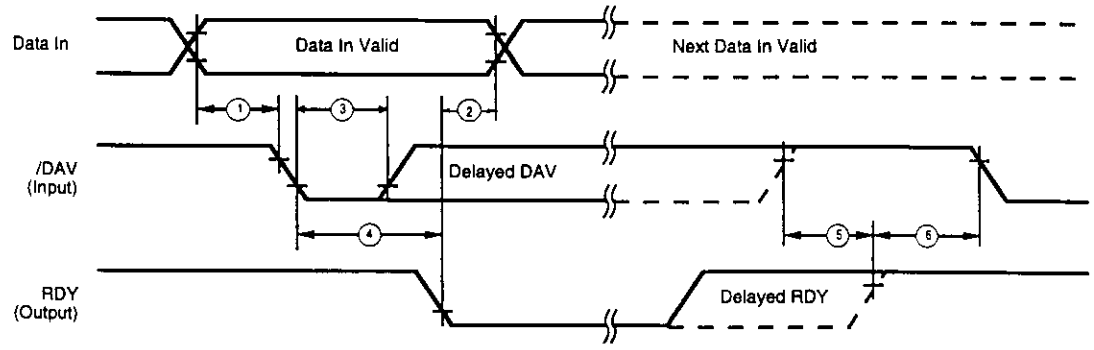
The value of TsDI (DSR) has been measured for the NMOS part as mentioned below as TsDI (DSR) old. This "old" value needs to be relaxed as to the value described as TsDI (DSR) new. This new value will allow the customer to use external memories with slower access times that immediately translates in lower cost.

DC CHARACTERISTICS

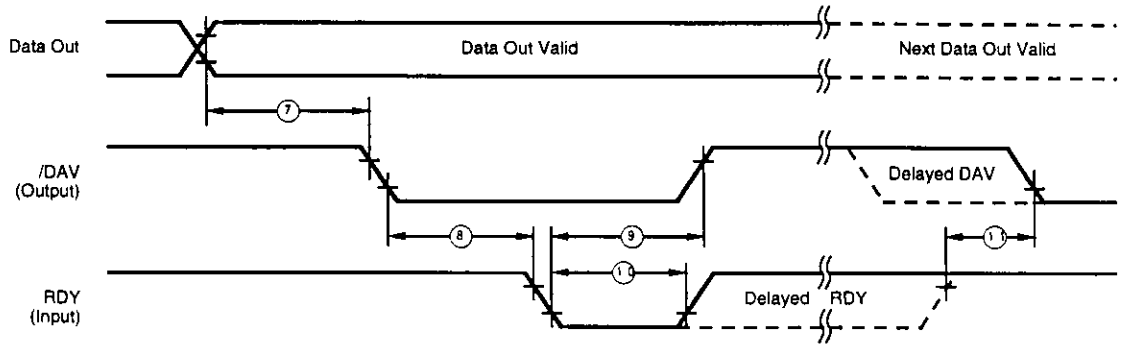
Symbol	Parameter	Min	Max	Unit	Condition
V_{CH}	Clock Input High Voltage	3.8	V_{CC}	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	–0.3	0.8	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC}	V	
V_{IL}	Input Low Voltage	–0.3	0.15 V_{CC}	V	
V_{RH}	Reset Input High Voltage	3.8	V_{CC}	V	
V_{RL}	Reset Input Low Voltage	–0.3	0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_{OH}=–400 µA
V_{OL}	Output Low Voltage		0.4	V	I_{OL}=+4.0 mA
V_{IL}	Input Leakage	–10	10	µA	
I_{OL}	Output Leakage	–10	10	µA	
I_{IR}	Reset Input Current		–50	µA	
I_{CC}	V_{CC} Standby Current		90	mA	[1]

Notes:
Estimated Values
[1] In this case all outputs and I/O pins are floating.

INTERLOCKED MODE HANDSHAKE TIMING



Input Handshake Timing Fully Interlocked Mode



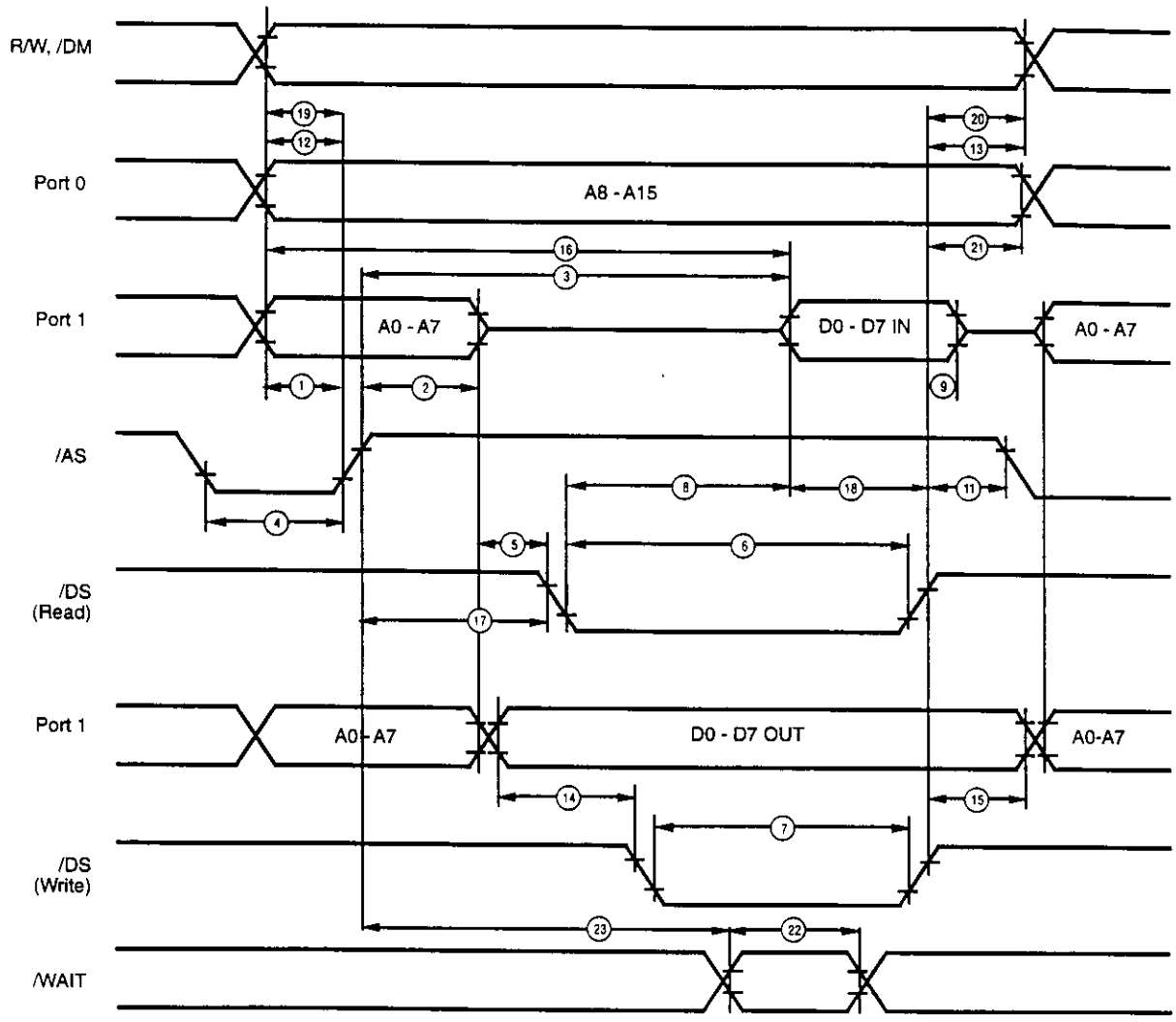
Output Handshake Timing Fully Interlocked Mode

AC ELECTRICAL CHARACTERISTICS

Interlocked Mode Handshake Timing

No.	Symbol	Parameter	Notes (Data Direction)
1	TsDI (DAV)	Data in Setup Time to /DAV	In
2	ThRDY (DI)	RDY to Data in Hold Time	In
3	TwDAV	/DAV Width	In
4	TdDAV (RDY)	/DAV to RDY Delay	In
5	TwDAV (RDY)	DAV^ to RDY Wait Time	In
6	TdRDY (DAV)	RDY^ to /DAV Delay	In
7	TdD0 (DAV)	Data Out to /DAV Delay	Out
8	TdDAVd (RDY)	DAV to RDY Delay	Out
9	TdRDY (DAV)	RDY to /DAV^ Delay	Out
10	TwRDY	RDY Width	Out
11	TwRDY (DAV)	RDY^ to /DAV Wait Time	Out

20 MHZ NORMAL TIMING



External Memory Read And Write

Z88C00 ERRATA

1. Handshake Port 4
   Input handshake (strobe and fully interlocked mode) with DMA is not functional.

2. UART Receive
   Upon receiving a character, the RCA (receive character available) interrupt is serviced twice. The time between two consecutive interrupts at 14 MHz is 53 µs. Although the UIO is read, which normally should clear the interrupt source, the RCA interrupt is asserted twice.

3. TTL Levels
   V_{iH}, V_{iL} do not meet the TTL specification when the port is used as control inputs for the counter/timers, UART, handshake, external wait and interrupts. Instead V_{iH} = 0.7 V_{cc} and V_{iL} = 0.15 V_{cc}.

4. DMA Usage
   No DMA can be performed to external memories if the wait feature (hardware wait and software wait) is used.

5. Reset Software Sequence
   After a hardware reset, program the P0M register before the PM register.

6. Counter/Timers
   To obtain a 2.5 MHz signal from the counter/timers, load the Counter/Timer registers with FFFFH and count up. The equivalent operations for the NMOS part to obtain the 2.5 MHz signal is to load the counter/timers with 0000H and count down.

Low Margin:
Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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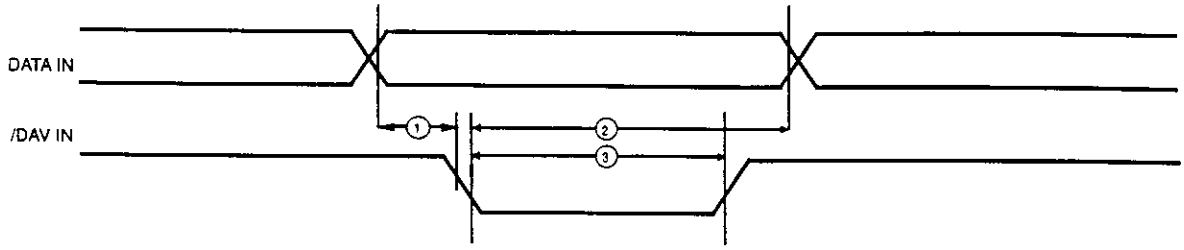
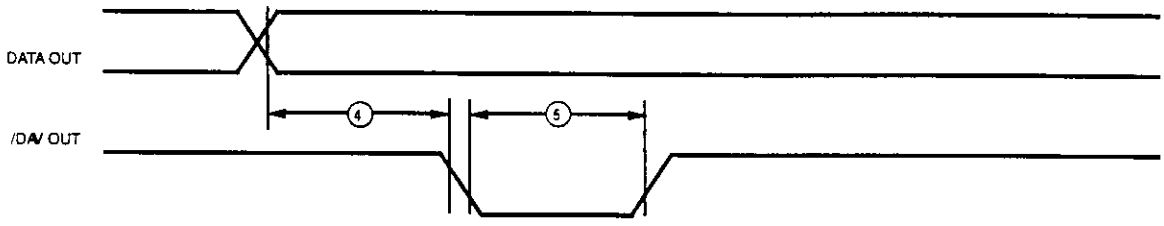
STROBE MODE HANDSHAKE TIMING



Input Handshake Timing Strobed Mode



Output Handshake Timing Strobed Mode

AC ELECTRICAL CHARACTERISTICS

Strobe Mode Handshake Timing

No.	Symbol	Parameter	Notes (Data Direction)
1	TsDI(DAV)	Data In to Setup Time /DAV	In
2	ThDAV(DI)	Data in Hold Time	In
3	TwDAV	/DAV Width	In
4	TdDO(DAV)	Data Out to /DAV Delay	Out
5	TwDAV	Data Available Width	Out