

## MC68HC16Z1

### *Technical Summary* **16-Bit Modular Microcontroller**

#### 1 Introduction

The MC68HC16Z1 is a high-speed 16-bit control unit that is upwardly code compatible with M68HC11 controllers. It is a member of the M68300/68HC16 Family of modular microcontrollers.

M68HC16 controllers are built up from standard modules that interface through a common internal bus. Standardization facilitates rapid development of devices tailored for specific applications.

The MC68HC16Z1 incorporates a true 16-bit central processing unit (CPU16), a system integration module (SIM), an 8/10-bit analog-to-digital converter (ADC), a queued serial module (QSM), a general-purpose timer (GPT), and a 2048-byte standby RAM (SRAM). These modules are interconnected by the intermodule bus (IMB).

Maximum system clock for the MC68HC16Z1 is 16.78 MHz. A phase-locked loop circuit synthesizes the clock from a frequency reference. Either a crystal (nominal frequency: 32.768 kHz) or an externally generated signal can be used. System hardware and software support changes in clock rate during operation. Because the MC68HC16Z1 is a fully static design, register and memory contents are not affected by clock rate changes.

High-density complementary metal-oxide semiconductor (HCMOS) architecture makes the basic power consumption of the MC68HC16Z1 low. Power consumption can be minimized by stopping the system clock. The M68HC16 instruction set includes a low-power stop (LPSTOP) command that efficiently implements this capability.



This document contains information about a new product. Specifications and information herein are subject to change without notice.



**MOTOROLA**

### Ordering Information

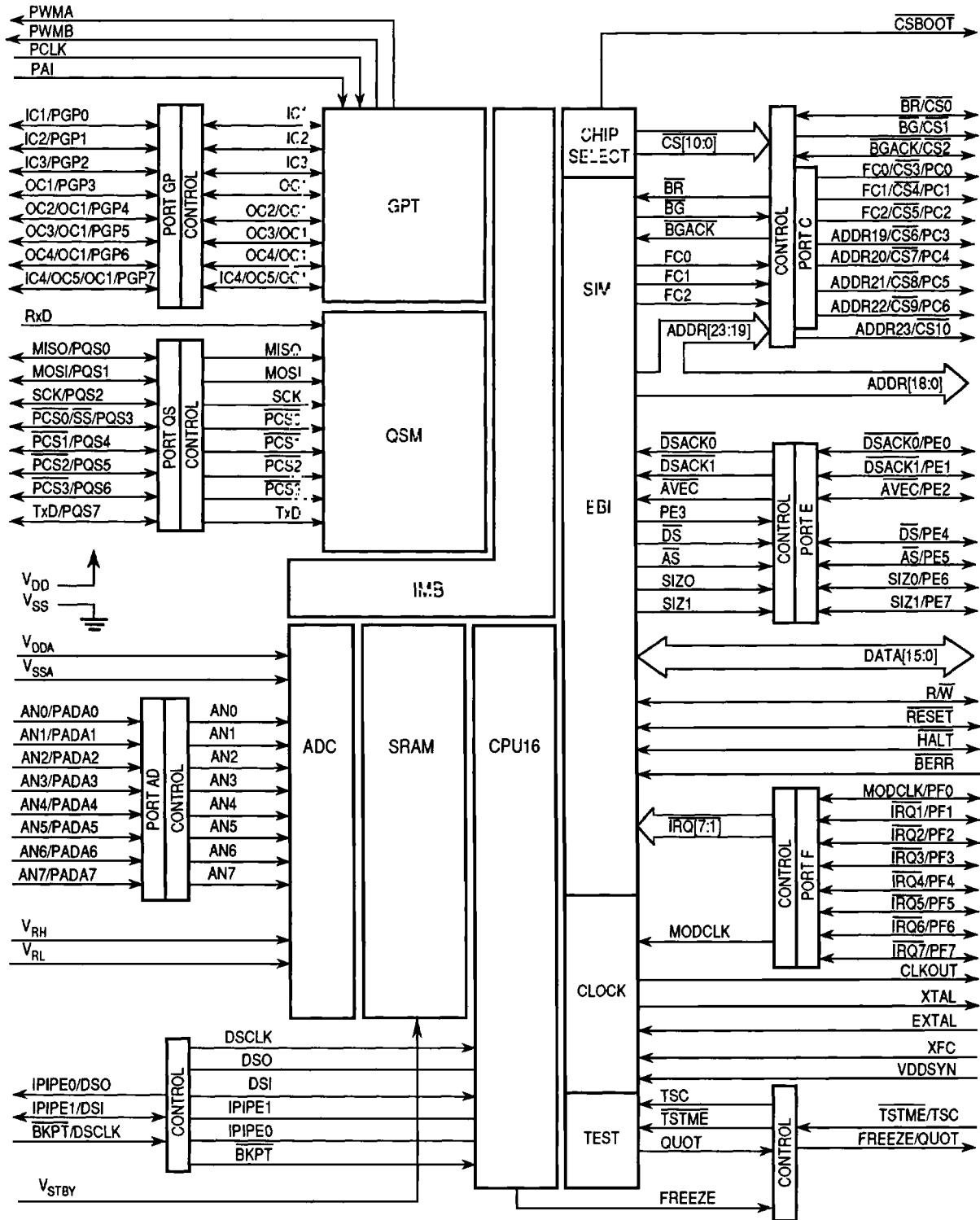
| Device Package                | Temperature Range (°C)        | Reference Frequency | Shipping Method | Order Number    |                 |
|-------------------------------|-------------------------------|---------------------|-----------------|-----------------|-----------------|
| 132-PIN PLASTIC SURFACE MOUNT | -40 to 85                     | 16.78 MHz           | 36 PER TRAY     | XC16Z1CFC16     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1CFC16 |                 |
|                               |                               | 20 MHz              | 36 PER TRAY     | XC16Z1CFC20     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1CFC20 |                 |
|                               |                               | 25 MHz              | 36 PER TRAY     | XC16Z1CFC25     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1CFC25 |                 |
|                               | -40 to 105                    | 16.78 MHz           | 36 PER TRAY     | XC16Z1VFC16     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1VFC16 |                 |
|                               |                               | 20 MHz              | 36 PER TRAY     | XC16Z1VFC20     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1VFC20 |                 |
|                               |                               | 25 MHz              | 36 PER TRAY     | XC16Z1VFC25     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1VFC25 |                 |
|                               | -40 to 125                    | 16.78 MHz           | 36 PER TRAY     | XC16Z1MFC16     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1MFC16 |                 |
|                               |                               | 20 MHz              | 36 PER TRAY     | XC16Z1MFC20     |                 |
| 2 PER TRAY                    |                               |                     | SPAKXC16Z1MFC20 |                 |                 |
| 25 MHz                        |                               | 36 PER TRAY         | XC16Z1MFC25     |                 |                 |
|                               |                               | 2 PER TRAY          | SPAKXC16Z1MFC25 |                 |                 |
| 132-PIN MOLDED CARRIER RING   | -40 to 85                     | 16.78 MHz           | 10 PER TUBE     | XC16Z1CFD16     |                 |
|                               |                               | 20 MHz              | 10 PER TUBE     | XC16Z1CFD20     |                 |
|                               |                               | 25 MHz              | 10 PER TUBE     | XC16Z1CFD25     |                 |
|                               | -40 to 105                    | 16.78 MHz           | 10 PER TUBE     | XC16Z1VFD16     |                 |
|                               |                               | 20 MHz              | 10 PER TUBE     | XC16Z1VFD20     |                 |
|                               |                               | 25 MHz              | 10 PER TUBE     | XC16Z1VFD25     |                 |
|                               | -40 to 125                    | 16.78 MHz           | 10 PER TUBE     | XC16Z1MFD16     |                 |
|                               |                               | 20 MHz              | 10 PER TUBE     | XC16Z1MFD20     |                 |
|                               |                               | 25 MHz              | 10 PER TUBE     | XC16Z1MFD25     |                 |
|                               | 144-PIN PLASTIC SURFACE MOUNT | -40 to 85           | 16.78 MHz       | 44 PER TRAY     | XC16Z1CFV16     |
|                               |                               |                     |                 | 2 PER TRAY      | SPAKXC16Z1CFV16 |
|                               |                               |                     | 20 MHz          | 44 PER TRAY     | XC16Z1CFV20     |
| 2 PER TRAY                    |                               |                     |                 | SPAKXC16Z1CFV20 |                 |
| 25 MHz                        |                               |                     | 44 PER TRAY     | XC16Z1CFV25     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1CFV25 |                 |
| -40 to 105                    |                               | 16.78 MHz           | 44 PER TRAY     | XC16Z1VfV16     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1VfV16 |                 |
|                               |                               | 20 MHz              | 44 PER TRAY     | XC16Z1VfV20     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1VfV20 |                 |
|                               |                               | 25 MHz              | 44 PER TRAY     | XC16Z1VfV25     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1VfV25 |                 |
| -40 to 125                    |                               | 16.78 MHz           | 44 PER TRAY     | XC16Z1MFV16     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1MFV16 |                 |
|                               |                               | 20 MHz              | 44 PER TRAY     | XC16Z1MFV20     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1MFV20 |                 |
|                               |                               | 25 MHz              | 44 PER TRAY     | XC16Z1MFV25     |                 |
|                               |                               |                     | 2 PER TRAY      | SPAKXC16Z1MFV25 |                 |
| 144-PIN MOLDED CARRIER RING   | -40 to 85                     | 16.78 MHz           | 13 PER TUBE     | XC16Z1CFM16     |                 |
|                               |                               | 20 MHz              | 13 PER TUBE     | XC16Z1CFM20     |                 |
|                               |                               | 25 MHz              | 13 PER TUBE     | XC16Z1CFM25     |                 |
|                               | -40 to 105                    | 16.78 MHz           | 13 PER TUBE     | XC16Z1VFM16     |                 |
|                               |                               | 20 MHz              | 13 PER TUBE     | XC16Z1VFM20     |                 |
|                               |                               | 25 MHz              | 13 PER TUBE     | XC16Z1VFM25     |                 |
|                               | -40 to 125                    | 16.78 MHz           | 13 PER TUBE     | XC16Z1MFM16     |                 |
|                               |                               | 20 MHz              | 13 PER TUBE     | XC16Z1MFM20     |                 |
|                               |                               | 25 MHz              | 13 PER TUBE     | XC16Z1MFM25     |                 |

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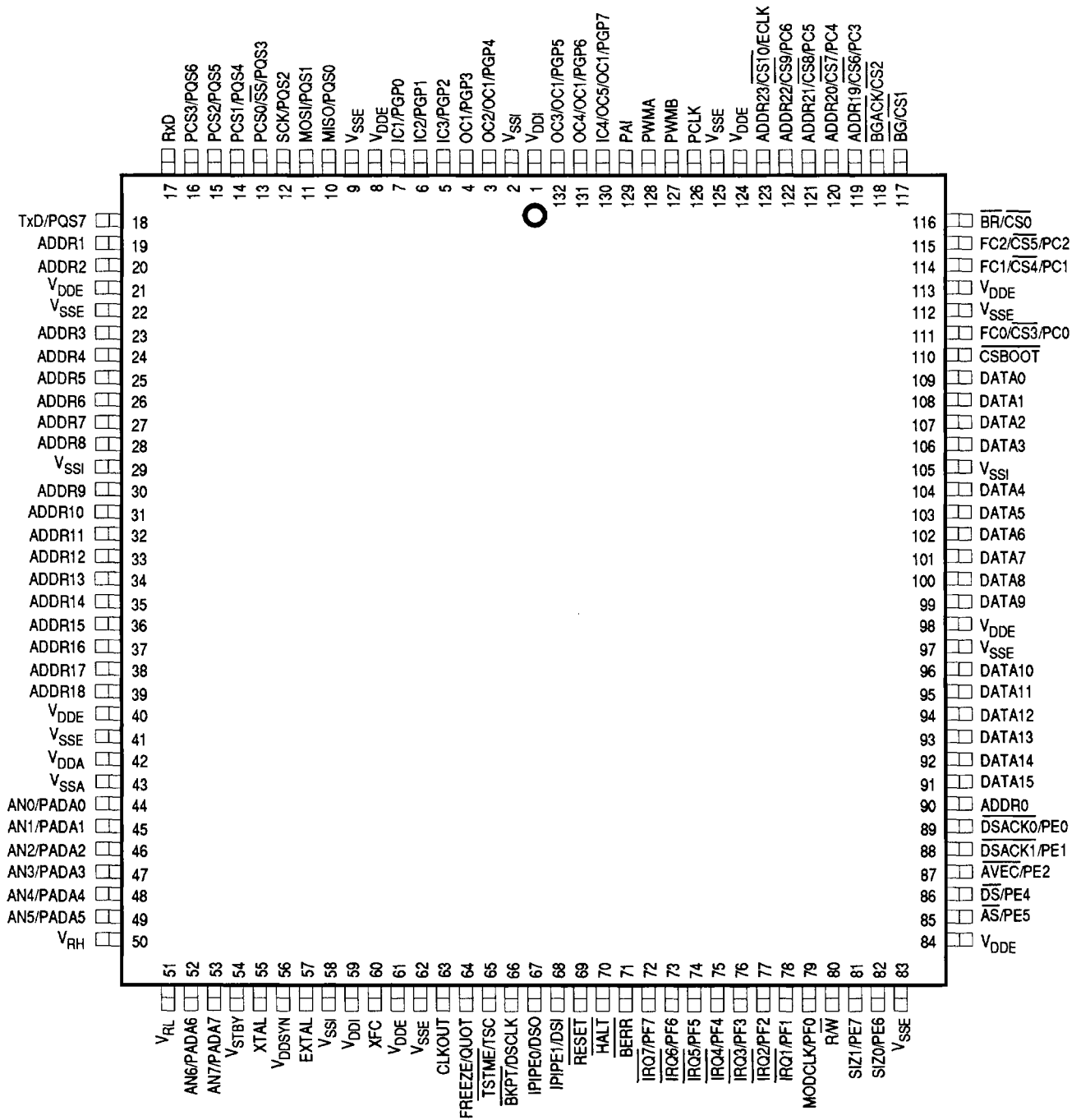
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## 1.1 Features

- CPU16
  - 16-Bit Architecture
  - Full Set of 16-Bit Instructions
  - Three 16-Bit Index Registers
  - Two 16-Bit Accumulators
  - Control-Oriented Digital Signal Processing Capability
  - 1 Megabyte of Program Memory and 1 Megabyte of Data Memory
  - High-Level Language Support
  - Fast Interrupt Response Time
  - Background Debugging Mode
  - Fully Static Operation
- System Integration Module
  - External Bus Support
  - Programmable Chip-Select Outputs
  - System Protection Logic
  - Watchdog Timer, Clock Monitor, and Bus Monitor
  - Two 8-Bit Dual Function Ports
  - One 7-Bit Dual Function Port
  - Phase-Locked Loop (PLL) Clock System
- 8/10-Bit Analog-to-Digital Converter
  - Eight Channels, Eight Result Registers
  - Eight Automated Modes
  - Three Result Alignment Modes
  - One 8-Bit Digital Input Port
- Queued Serial Module
  - Enhanced Serial Communication Interface
  - Queued Serial Peripheral Interface
  - One 8-Bit Dual Function Port
- General-Purpose Timer
  - Two 16-Bit Free-Running Counters with Prescaler
  - Three Input Capture Channels
  - Four Output Compare Channels
  - One Input Capture/Output Compare Channel
  - One Pulse Accumulator/Event Counter Input
  - Two Pulse Width Modulation Outputs
  - One 8-Bit Dual Function Port
  - Two Optional Discrete Inputs
  - Optional External Clock Input
- Standby RAM
  - 1024-Byte Static RAM
  - External Standby Voltage Supply Input



MC68HC16Z1 Block Diagram



MC68HC16Z1 132-Pin Package Pin Assignments

|             |     |                  |    |  |     |             |
|-------------|-----|------------------|----|--|-----|-------------|
| BRCS0       | 144 | NC               | 1  |  | 108 | VsSE        |
| FC2/CS5/PC2 | 143 | BG/CS1           | 2  |  | 107 | SIZ0/PE6    |
| FC1/CS4/PC1 | 142 | BGACK/CS2        | 3  |  | 106 | SIZ1/PE7    |
| VDDDE       | 141 | ADDR19/CS6/PC3   | 4  |  | 105 | R/W         |
| VsSSE       | 140 | ADDR20/CS7/PC4   | 5  |  | 104 | MODCLK/PF0  |
| FC0/CS3/PC0 | 139 | ADDR21/CS8/PC5   | 6  |  | 103 | IRQ1/PF1    |
| CSBOOT      | 138 | ADDR22/CS9/PC6   | 7  |  | 102 | IRQ2/PF2    |
| DATA0       | 137 | ADDR23/CS10      | 8  |  | 101 | IRQ3/PF3    |
| DATA1       | 136 | VDDDE            | 9  |  | 100 | IRQ4/PF4    |
| DATA2       | 135 | VsSSE            | 10 |  | 99  | IRQ5/PF5    |
| DATA3       | 134 | PCLK             | 11 |  | 98  | IRQ6/PF6    |
| NC          | 133 | PWMB             | 12 |  | 97  | IRQ7/PF7    |
| VsSSI       | 132 | PWMA             | 13 |  | 96  | BERR        |
| NC          | 131 | PAI              | 14 |  | 95  | HALT        |
| DATA4       | 130 | IC4/OC5/OC1/PGP7 | 15 |  | 94  | RESET       |
| DATA5       | 129 | OC4/OC1/PGP6     | 16 |  | 93  | IPIPE1/DS1  |
| DATA6       | 128 | OC3/OC1/PGP5     | 17 |  | 92  | IPIPE0/DS0  |
| DATA7       | 127 | NC               | 18 |  | 91  | BKPT/DSCLK  |
| DATA8       | 126 | VDDI             | 19 |  | 90  | NC          |
| DATA9       | 125 | VsSI             | 20 |  | 89  | TSTME/TSC   |
| VDDDE       | 124 | OC2/PGP4         | 21 |  | 88  | FREEZE/QUOT |
| NC          | 123 | OC1/PGP3         | 22 |  | 87  | CLKOUT      |
| VsSSE       | 122 | IC3/PGP2         | 23 |  | 86  | VsSSE       |
| DATA10      | 121 | IC2/PGP1         | 24 |  | 85  | VDDDE       |
| DATA11      | 120 | IC1/PGP0         | 25 |  | 84  | XFC         |
| DATA12      | 119 | VDDDE            | 26 |  | 83  | NC          |
| DATA13      | 118 | VsSSE            | 27 |  | 82  | VDDI        |
| DATA14      | 117 | MISO/PQS0        | 28 |  | 81  | VsSI        |
| DATA15      | 116 | MOSI/PQS1        | 29 |  | 80  | EXTAL       |
| ADDR0       | 115 | SCK/PQS2         | 30 |  | 79  | VDDSYN      |
| DSACK0/PE0  | 114 | PCS0/SS/PQS3     | 31 |  | 78  | XTAL        |
| DSACK1/PE1  | 113 | PCS1/PQS4        | 32 |  | 77  | VSTBY       |
| AVEC/PE2    | 112 | PCS2/PQS5        | 33 |  | 76  | AN7/PADA7   |
| DS/PE4      | 111 | PCS3/PQS6        | 34 |  | 75  | AN6/PADA6   |
| AS/PE5      | 110 | RxD              | 35 |  | 74  | VRLP        |
| VDDDE       | 109 | NC               | 36 |  | 73  | NC          |
|             |     | TxD/PQS7         | 37 |  |     |             |
|             |     | ADDR1            | 38 |  |     |             |
|             |     | ADDR2            | 39 |  |     |             |
|             |     | VDDDE            | 40 |  |     |             |
|             |     | VsSSE            | 41 |  |     |             |
|             |     | ADDR3            | 42 |  |     |             |
|             |     | ADDR4            | 43 |  |     |             |
|             |     | ADDR5            | 44 |  |     |             |
|             |     | ADDR6            | 45 |  |     |             |
|             |     | ADDR7            | 46 |  |     |             |
|             |     | ADDR8            | 47 |  |     |             |
|             |     | NC               | 48 |  |     |             |
|             |     | VsSI             | 49 |  |     |             |
|             |     | NC               | 50 |  |     |             |
|             |     | ADDR9            | 51 |  |     |             |
|             |     | ADDR10           | 52 |  |     |             |
|             |     | ADDR11           | 53 |  |     |             |
|             |     | ADDR12           | 54 |  |     |             |
|             |     | ADDR13           | 55 |  |     |             |
|             |     | ADDR14           | 56 |  |     |             |
|             |     | NC               | 57 |  |     |             |
|             |     | ADDR15           | 58 |  |     |             |
|             |     | ADDR16           | 59 |  |     |             |
|             |     | ADDR17           | 60 |  |     |             |
|             |     | ADDR18           | 61 |  |     |             |
|             |     | VDDDE            | 62 |  |     |             |
|             |     | VsSSE            | 63 |  |     |             |
|             |     | VDDA             | 64 |  |     |             |
|             |     | VSSA             | 65 |  |     |             |
|             |     | AN0/PADA0        | 66 |  |     |             |
|             |     | AN1/PADA1        | 67 |  |     |             |
|             |     | AN2/PADA2        | 68 |  |     |             |
|             |     | AN3/PADA3        | 69 |  |     |             |
|             |     | AN4/PADA4        | 70 |  |     |             |
|             |     | AN5/PADA5        | 71 |  |     |             |
|             |     | VrHP             | 72 |  |     |             |

MC68HC16Z1 144-Pin Package Pin Assignments

## 1.2 Pin Description

The following table shows MC68HC16Z1 pins and their characteristics. All inputs detect CMOS logic levels. All inputs can be put in a high-impedance state, but the method of doing this differs depending upon pin function. Refer to the table, MC68HC16Z1 Driver Types, for a description of output drivers. An entry in the discrete I/O column of the MC68HC16Z1 Pin Characteristics table indicates that a pin has an alternate I/O function. The port designation is given when it applies. Refer to the MC68HC16Z1 Block Diagram for information about port organization.

MC68HC16Z1 Pin Characteristics

| Pin Mnemonic            | Output Driver | Input Synchronized | Input Hysteresis | Discrete I/O | Port Designation |
|-------------------------|---------------|--------------------|------------------|--------------|------------------|
| ADDR23/CS10/ECLK        | A             | Y                  | N                | O            | —                |
| ADDR[22:19]/CS[9:6]     | A             | Y                  | N                | O            | C[6:3]           |
| ADDR[18:0]              | A             | Y                  | N                | —            | —                |
| AN[7:0] <sup>1</sup>    | —             | Y                  | N                | I            | ADA[7:0]         |
| AS                      | B             | Y                  | N                | I/O          | E5               |
| AVEC                    | B             | Y                  | N                | I/O          | E2               |
| BERR                    | B             | Y                  | N                | —            | —                |
| BG/CS1                  | B             | —                  | —                | —            | —                |
| BGACK/CS2               | B             | Y                  | N                | —            | —                |
| BKPT/DSCKL              | —             | Y                  | Y                | —            | —                |
| BR/CS0                  | B             | Y                  | N                | O            | Separate         |
| CLKOUT                  | A             | —                  | —                | —            | —                |
| CSBOOT                  | B             | —                  | —                | —            | —                |
| DATA[15:0] <sup>1</sup> | AW            | Y                  | N                | —            | —                |
| DS                      | B             | Y                  | N                | I/O          | E4               |
| DSACK1                  | B             | Y                  | N                | I/O          | E1               |
| DSACK0                  | B             | Y                  | N                | I/O          | E0               |
| DSI/IP1E1               | A             | Y                  | Y                | —            | Separate         |
| DSO/IP1E0               | A             | —                  | —                | —            | Separate         |
| EXTAL <sup>2</sup>      | —             | —                  | Special          | —            | —                |
| FC[2:0]/CS[5:3]         | A             | Y                  | N                | O            | C[2:0]           |
| FREEZE/QUOT             | A             | —                  | —                | —            | —                |
| HALT                    | Bo            | Y                  | N                | —            | —                |
| IC4/OC5                 | A             | Y                  | Y                | I/O          | GP4              |
| IC[3:1]                 | A             | Y                  | Y                | I/O          | GP[7:5]          |
| IRQ[7:1]                | B             | Y                  | Y                | I/O          | F[7:1]           |
| MISO                    | Bo            | Y                  | Y                | I/O          | QS0              |
| MODCLK <sup>1</sup>     | B             | Y                  | N                | I/O          | F0               |
| MOSI                    | Bo            | Y                  | Y                | I/O          | QS1              |
| OC[4:1]                 | A             | Y                  | Y                | I/O          | GP[3:0]          |
| PAI <sup>3</sup>        | —             | Y                  | Y                | I            | Separate         |
| PCLK <sup>3</sup>       | —             | Y                  | Y                | I            | Separate         |
| PCS0/SS                 | Bo            | Y                  | Y                | I/O          | QS3              |
| PCS[3:1]                | Bo            | Y                  | Y                | I/O          | QS[6:4]          |
| PWMA, PWMB <sup>4</sup> | A             | —                  | —                | O            | Separate         |
| R/W                     | A             | Y                  | N                | —            | —                |
| RESET                   | Bo            | Y                  | Y                | —            | —                |



### MC68HC16Z1 Pin Characteristics (Continued)

| Pin Mnemonic                 | Output Driver | Input Synchronized | Input Hysteresis | Discrete I/O | Port Designation |
|------------------------------|---------------|--------------------|------------------|--------------|------------------|
| RXD                          | —             | N                  | N                | —            | —                |
| SCK                          | Bo            | Y                  | Y                | I/O          | QS2              |
| SIZ[1:0]                     | B             | Y                  | N                | I/O          | E[7:6]           |
| TSTME/TSC                    | —             | Y                  | Y                | —            | —                |
| TXD                          | Bo            | Y                  | Y                | I/O          | QS7              |
| V <sub>RH</sub> <sup>5</sup> | —             | —                  | —                | —            | —                |
| V <sub>RL</sub> <sup>5</sup> | —             | —                  | —                | —            | —                |
| XFC <sup>2</sup>             | —             | —                  | —                | Special      | —                |
| XTAL <sup>2</sup>            | —             | —                  | —                | Special      | —                |

#### NOTES

1. DATA[15:0] are synchronized during reset only. MODCLK, MCC1 and ADC pins are synchronized only when used as input port pins.
2. EXTAL, XFC, and XTAL are clock reference connections.
3. PAI and PCLK can be used for discrete input, but are not part of an I/O port.
4. PWMA and PWMB can be used for discrete output, but are not part of an I/O port.
5. V<sub>RH</sub> and V<sub>RL</sub> are ADC reference voltage inputs.

### MC68HC16Z1 Power Connections

|                                    |   |
|------------------------------------|---|
| V <sub>STBY</sub>                  | Standby RAM Power/Clock Synthesizer Power   |
| V <sub>DDSYN</sub>                 | Clock Synthesizer Power                     |
| V <sub>DDA</sub> /V <sub>SSA</sub> | A/D Converter Power                         |
| V <sub>SSE</sub> /V <sub>DDE</sub> | External Periphery Power (Source and Drain) |
| V <sub>SSI</sub> /V <sub>DDI</sub> | Internal Module Power (Source and Drain)    |

### MC68HC16Z1 Driver Types

| Type | I/O | Description  |
|------|-----|--|
| A    | O   | Output-only signals that are always driven; no external pull-up required   |
| Aw   | O   | Type A output with weak P-channel pull-up during reset   |
| B    | O   | Three-state output that includes circuitry to pull up output before high impedance is established, to ensure rapid rise time. An external holding resistor is required to maintain logic level while the pin is in the high-impedance state. |
| Bo   | O   | Type B output that can be operated in an open-drain mode   |

### 1.3 Signal Description

Use the following tables as a quick reference to MC68HC16Z1 signal type and function.

**MC68HC16Z1 Signal Characteristics**

| Signal Name                    | MCU Module | Signal Type  | Active State  |
|--------------------------------|------------|--------------|---------------|
| ADDR[23:0]                     | SIM        | Bus          | —             |
| AN[7:0]                        | ADC        | Input        | —             |
| AS                             | SIM        | Output       | 0             |
| $\overline{\text{AVEC}}$       | SIM        | Input        | 0             |
| $\overline{\text{BERR}}$       | SIM        | Input        | 0             |
| $\overline{\text{BG}}$         | SIM        | Output       | 0             |
| $\overline{\text{BGACK}}$      | SIM        | Input        | 0             |
| $\overline{\text{BKPT}}$       | CPU16      | Input        | 0             |
| $\overline{\text{BR}}$         | SIM        | Input        | 0             |
| CLKOUT                         | SIM        | Output       | —             |
| CS[10:0]                       | SIM        | Output       | 0             |
| $\overline{\text{CSBOOT}}$     | SIM        | Output       | 0             |
| DATA[15:0]                     | SIM        | Bus          | —             |
| $\overline{\text{DS}}$         | SIM        | Output       | 0             |
| $\overline{\text{DSACK}}[1:0]$ | SIM        | Input        | 0             |
| DCLK                           | CPU16      | Input        | Serial Clock  |
| DSI                            | CPU16      | Input        | (Serial Data) |
| DSO                            | CPU16      | Output       | (Serial Data) |
| EXTAL                          | SIM        | Input        | —             |
| FC[2:0]                        | SIM        | Output       | —             |
| $\overline{\text{FREEZE}}$     | SIM        | Output       | 1             |
| HALT                           | SIM        | Input/Output | 0             |
| IC[4:1]                        | GPT        | Input        | —             |
| IPIPE0                         | CPU16      | Output       | —             |
| IPIPE1                         | CPU16      | Output       | —             |
| $\overline{\text{IRQ}}[7:1]$   | SIM        | Input        | 0             |
| MISO                           | QSM        | Input/Output | —             |
| MODCLK                         | SIM        | Input        | —             |
| MOSI                           | QSM        | Input/Output | —             |
| OC[5:1]                        | GPT        | Output       | —             |
| PADA[7:0]                      | ADC        | Input        | (Port)        |
| PAI                            | GPT        | Input        | —             |
| PC[6:0]                        | SIM        | Output       | (Port)        |
| PE[7:0]                        | SIM        | Input/Output | (Port)        |
| PF[7:0]                        | SIM        | Input/Output | (Port)        |
| PGP[7:0]                       | GPT        | Input/Output | (Port)        |
| PQS[7:0]                       | QSM        | Input/Output | (Port)        |
| PCLK                           | GPT        | Input        | —             |
| PCS[3:0]                       | QSM        | Input/Output | —             |
| PWMA, PWMB                     | GPT        | Output       | —             |
| QUOT                           | SIM        | Output       | —             |

### MC68HC16Z1 Signal Characteristics (Continued)

| Signal Name     | MCU Module | Signal Type  | Active State |
|-----------------|------------|--------------|--------------|
| R/W             | SIM        | Output       | 1/0          |
| RESET           | SIM        | Input/Output | 0            |
| RXD             | QSM        | Input        | —            |
| SCK             | QSM        | Input/Output | —            |
| SIZ[1:0]        | SIM        | Output       | —            |
| SS              | QSM        | Input        | 0            |
| TSC             | SIM        | Input        | —            |
| TSTME           | SIM        | Input        | 0            |
| TXD             | QSM        | Output       | —            |
| V <sub>RH</sub> | ADC        | Input        | —            |
| V <sub>RL</sub> | ADC        | Input        | —            |
| XFC             | SIM        | Input        | —            |
| XTAL            | SIM        | Output       | —            |

### MC68HC16Z1 Signal Function

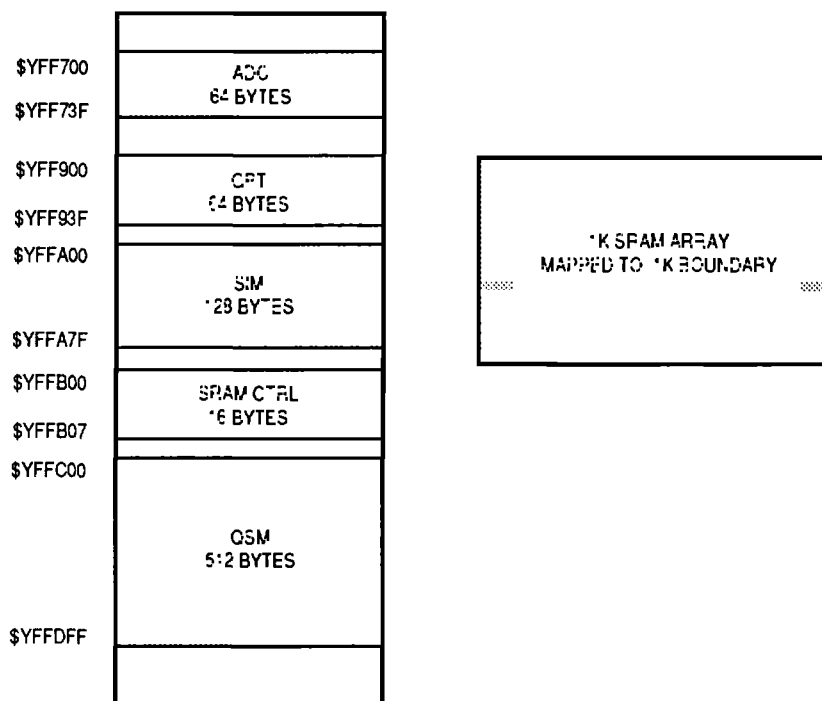
| Signal Name                       | Mnemonic        | Function   |
|-----------------------------------|-----------------|--|
| Address Strobe                    | AS              | Indicates that a valid address is on the address bus   |
| Autovector                        | AVEC            | Requests an automatic vector during interrupt acknowledge  |
| Bus Error                         | BERR            | Indicates that a bus error has occurred  |
| Bus Grant                         | BG              | Indicates that the MCU has relinquished the bus  |
| Bus Grant Acknowledge             | BGACK           | Indicates that an external device has assumed bus mastership   |
| Breakpoint                        | BKPT            | Signals a hardware breakpoint to the CPU   |
| Bus Request                       | BR              | Indicates that an external device requires bus mastership  |
| Chip Selects                      | CS[10:0]        | Select external devices at programmed addresses  |
| Boot Chip Select                  | CSBOOT          | Chip select for external boot startup ROM  |
| Address Bus                       | ADDR[19:0]      | 20-bit address bus used by CPU16   |
| Address Bus                       | ADDR[23:20]     | 4 MSB on IMB, test only, outputs follow ADDR19   |
| ADC Analog Input                  | AN[7:0]         | Inputs to ADC MUX  |
| System Clockout                   | CLKOUT          | System clock output  |
| Data Bus                          | DATA[15:0]      | 16-bit data bus  |
| Data Strobe                       | DS              | During a read cycle, indicates that an external device should place valid data on the data bus. During a write cycle, indicates that valid data is on the data bus |
| Halt                              | HALT            | Suspend external bus activity  |
| Interrupt Request Level           | IRQ[7:1]        | Provides an interrupt priority level to the CPU  |
| Data and Size Acknowledge         | DSACK[1:0]      | Provide asynchronous data transfers and dynamic bus sizing   |
| Peripheral Chip Select            | PCS[3:0]        | QSPI peripheral chip selects   |
| Reset                             | RESET           | System reset   |
| Test Mode Enable                  | TSTME           | Hardware enable for SIM test mode  |
| Development Serial In, Out, Clock | DSI, DSO, DSCLK | Serial I/O and clock for background debug mode   |

### MC68HC16Z1 Signal Function (Continued)

| Signal Name               | Mnemonic         | Function   |
|---------------------------|------------------|--|
| Crystal Oscillator        | EXTAL, XTAL      | Connections for clock synthesizer circuit reference; a crystal or an external oscillator can be used |
| Function Codes            | FC[2:0]          | Identify processor state and current address space   |
| Freeze                    | FREEZE           | Indicates that the CPU has entered background mode   |
| Instruction Pipeline      | PIPE[1:0]        | Indicate instruction pipeline activity   |
| Master In Slave Out       | MISO             | Serial input to QSPI in master mode; serial output from QSPI in slave mode                           |
| Clock Mode Select         | MODCLK           | Selects the source and type of system clock  |
| Master Out Slave In       | MOSI             | Serial output from QSPI in master mode; serial input to QSPI in slave mode                           |
| Port ADA                  | PADA[7:0]        | ADC digital input port signals   |
| Port C                    | PC[6:0]          | SIM digital output port signals  |
| Port E                    | PE[7:0]          | SIM digital I/O port signals   |
| Port F                    | PF[7:0]          | SIM digital I/O port signals   |
| Port GP                   | PGP[7:0]         | GPT digital I/O port signals   |
| Port QS                   | PQS[7:0]         | QSM digital I/O port signals   |
| Quotient Out              | QUOT             | Provides the quotient bit of the polynomial divider  |
| Read/Write                | $\overline{R/W}$ | Indicates the direction of data transfer on the bus  |
| SCI Receive Data          | RXD              | Serial input to the SCI  |
| QSPI Serial Clock         | SCK              | Clock output from QSPI in master mode; clock input to QSPI in slave mode                             |
| Size                      | SIZ[1:0]         | Indicates the number of bytes to be transferred during a bus cycle                                   |
| Slave Select              | $\overline{SS}$  | Causes serial transmission when QSPI is in slave mode; causes mode fault in master mode              |
| Three-State Control       | TSC              | Places all output drivers in a high-impedance state  |
| SCI Transmit Data         | TXD              | Serial output from the SCI   |
| ADC Reference Voltage     | $V_{RH}, V_{RL}$ | Provide precise reference for A/D conversion   |
| External Filter Capacitor | XFC              | Connection for external phase-locked loop filter capacitor   |

### 1.4 Internal Register Address Map

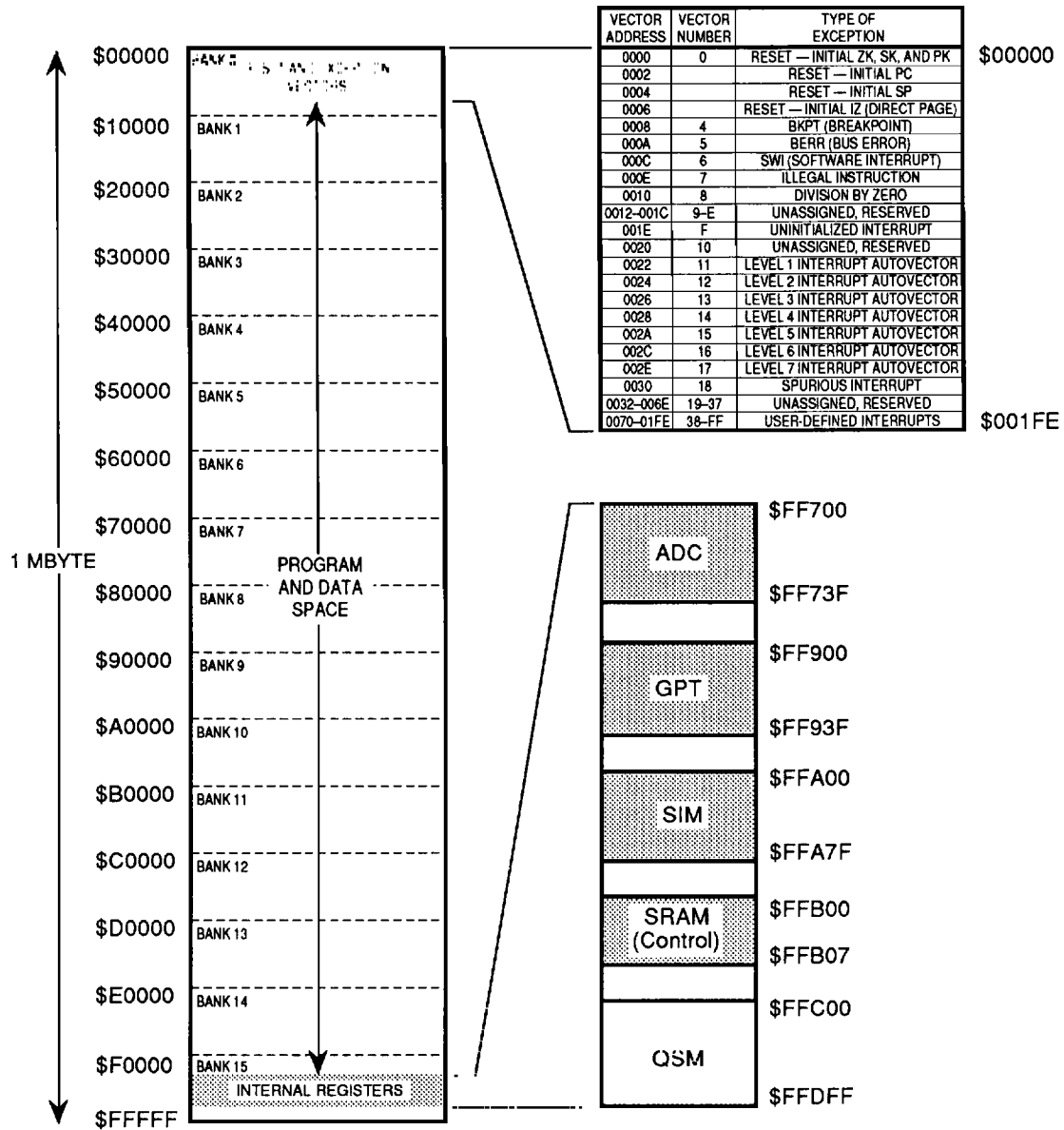
In the following figure, IMB ADDR[23:20] are represented by the letter Y. The value represented by Y determines the base address of MCU module control registers. In the MC68HC16Z1, Y is equal to M111, where M is the logic state of the module mapping (MM) bit in the system integration module configuration register (SIMCR). Since the CPU16 uses only ADDR[19:0], and ADDR[23:20] follow the logic state of ADDR19 when CPU driven, the CPU cannot access IMB addresses from \$080000 to \$F7FFFF. In order for the MCU to function correctly, MM must be set (Y must equal \$F). If M is cleared, internal registers are mapped to base address \$700000, and are inaccessible until a reset occurs. The SRAM array is positioned by a base address register in the SRAM CTRL block. Unimplemented blocks are mapped externally.



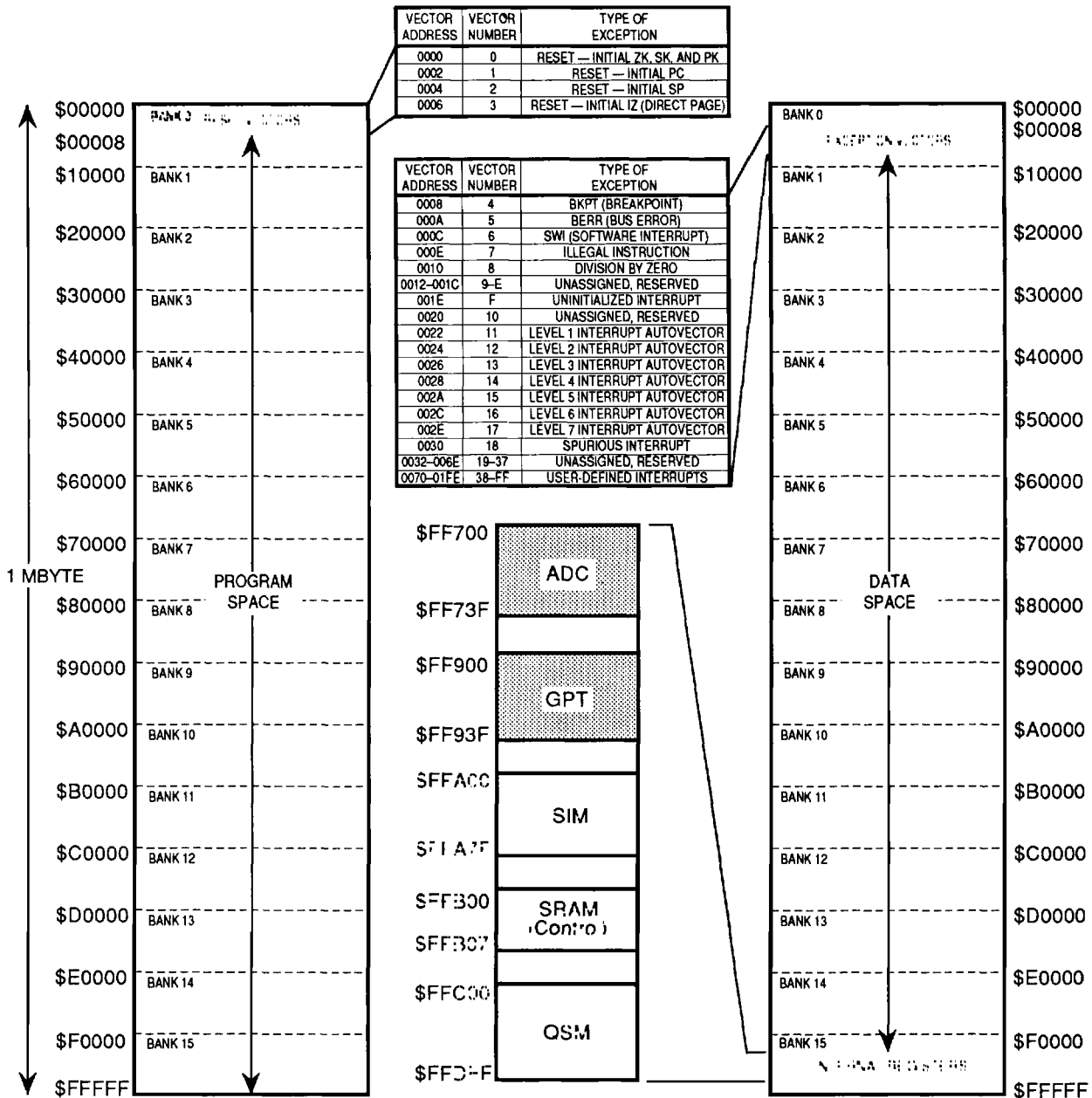
Internal Register Addresses

### 1.5 Pseudolinear Memory Maps

The following figures both show the complete CPU16 pseudolinear address space. Address space can be split into physically distinct program and data spaces by decoding the MCU function code outputs. The first figure shows the memory map of a system that has combined program and data spaces. The second figure shows the memory map when MCU function code outputs are decoded. Reset and exception vectors are mapped into bank 0 and cannot be relocated. The CPU16 program counter, stack pointer, and Z index register can be initialized to any address in pseudolinear memory, but exception vectors are limited to 16-bit addresses — to access locations outside of bank 0 during exception handler routines (including interrupt exceptions), a jump table must be used.



**Pseudolinear Addressing With Combined Program and Data Spaces**



Pseudolinear Addressing With Separated Program and Data Spaces