User's Guide

ADS1263EVM-PDK Evaluation Module

ABSTRACT

This user's guide describes the characteristics, operation, and use of the ADS1263 evaluation module (EVM). This EVM is an evaluation platform for the Texas Instruments ADS1263, a low-noise, 32-bit, 38-kSPS, 10-channel (multiplexed), delta-sigma (ΔΣ) analog-to-digital converter (ADC). The highly-integrated ADS1263 includes a programmable gain amplifier (PGA), a 2.5-V low-drift voltage reference, an internal oscillator, dual-sensor excitation current sources (IDAC), several system-monitoring features, and an auxiliary 24-bit ΔΣ ADC. The integrated features and excellent performance of the ADS1263 enable precision measurement of strain gauges, weigh scales, pressure sensors, thermocouples, thermistors, and resistance temperature detectors (RTDs). The ADS1263EVM eases the evaluation of the device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS1263EVM.

Note

The ADS1263EVM and software can also support the ADS1262, which is identical to the ADS1263 except that the ADS1262 does not include the auxiliary 24-bit ΔΣ ADC. However, the user must manually remove the ADS1263 and install the ADS1262. See Section 8.3 for the location of the ADS1263 on the EVM. The ADS1262 is not discussed further in this document.

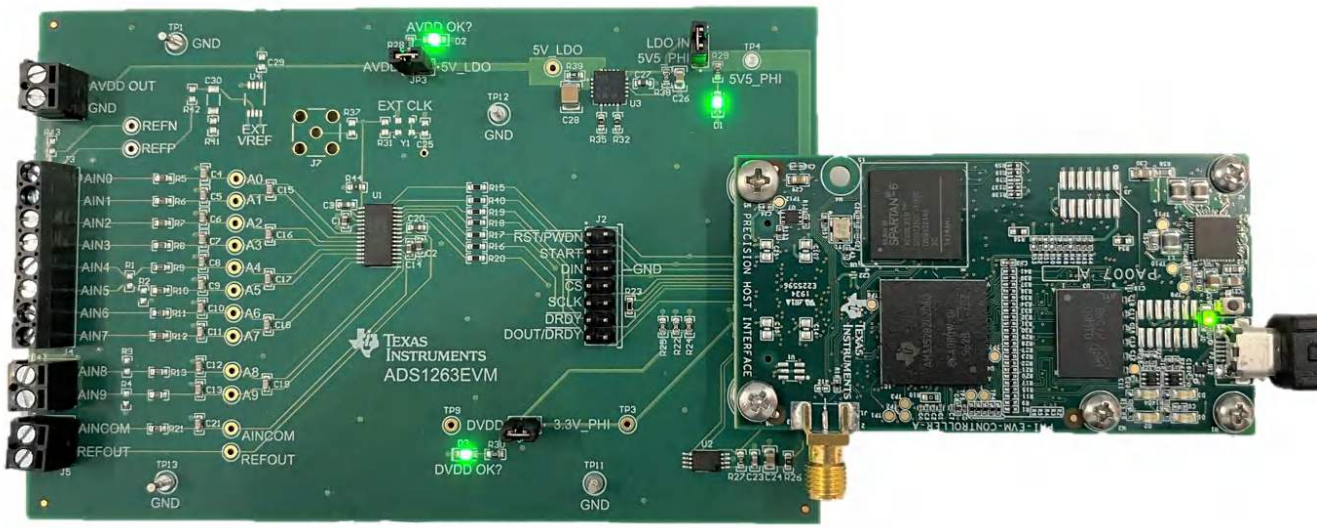

Table of Contents

Trademarks

LabVIEW™ is a trademark of National Instruments.
Microsoft® and Windows® are registered trademarks of Microsoft Corporation.
All trademarks are the property of their respective owners.

1 EVM Overview

The ADS1263EVM is a platform for evaluating the performance of the ADS1263, a 32-bit, 38-kSPS, 10-channel (multiplexed), ΔΣ ADC. The evaluation kit includes the ADS1263EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis. The ADS1263EVM board includes the ADS1263 as well as the high-performance peripheral analog circuits necessary to extract optimum performance from the ADC. The PHI board primarily serves three functions:

- Provide a communication interface from the EVM to the computer through a USB port
- Provide the digital input and output signals necessary to communicate with the ADS1263
- Supplies power to all circuitry on the ADS1263EVM board

1.1 ADS1263EVM Kit

The ADS1263 evaluation kit includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS1263 ADC.
- USB powered: No external power is required.
- PHI controller that provides a convenient communication interface to the ADS1263 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output.
- Microsoft® Windows® 8 and Windows 10 operating systems.
- Easy-to-use evaluation software for 64-bit Microsoft Windows.
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file post-processing.

Figure 1-1 shows system connections for the EVM.

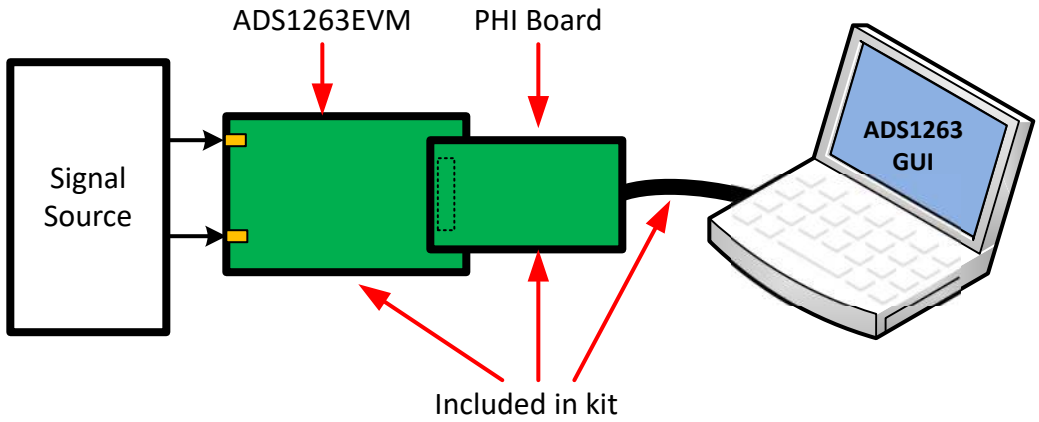

Figure 1-1. System Connection for Evaluation

1.2 ADS1263EVM Board

The ADS1263EVM board includes the following features and options:

- Ultra-low noise TPS7A4700, low-dropout (LDO) linear regulator supplies 5-V ADC analog voltage (AVDD), or use an external voltage supply
- 3.3-V ADC digital voltage (DVDD) supplied by PHI controller, or use external voltage supply
- Test points for power, GND, reference, and all digital signals to and from the PHI controller
- Optional external clocking and voltage reference footprints

2 Getting Started With the ADS1263EVM

The following list of instructions provides an overview to quickly get the ADS1263EVM set up and operational. The subsequent sections in this document expand on each step to explain in detail the available features on the EVM and the corresponding GUI. Links are provided to navigate from this quick-start guide to the appropriate sections at each applicable step.

1. Remove the ADS1263EVM, PHI board, and USB cable from the ADS1263EVM-PDK box.
2. If necessary, connect the PHI to the ADS1263EVM (see Figure 7-1).
3. Configure the ADS1263EVM:
   a. Power supplies (see Section 5).
   b. Clocking (see Section 3.3), if applicable.
   c. Voltage reference (see Section 3.4), if applicable.
4. Connect the micro-USB-to-USB cable from the PHI directly to a USB port on the computer. Do not connect the cable to the computer through a USB hub.
5. Open the latest version of the ADS1263EVM GUI on the connected computer:
   a. First-time users must download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS1263EVM and run the GUI installer to install the EVM GUI software on the host computer.
6. Connect your sensors or signals (see Section 3.1.2) to the input terminal blocks (J3-J6).
7. Capture and analyze data (see Section 7) using the GUI.

3 Analog Interface

The ADS1263EVM supports a wide variety of analog input configurations. Additional functionality enables precise measurement of many sensor types. The following sections discuss these features in more detail.

3.1 Analog Input Options

The ADS1263 has a total of 11 analog input pins: AIN0 through AIN9 plus a common input, AINCOM. This design allows the ADS1263 to be configured for up to five differential input pairs, 10 single-ended inputs referenced to a common voltage, or a combination of single-ended and differential inputs. The flexible input multiplexer of the ADS1263 allows any two inputs to be selected for either the positive or negative ADC input.

Any AINx pin can be used as a common input when measuring single-ended signals. However, AINCOM is specifically designed to serve this purpose because AINCOM can provide a bias voltage (level-shift function). This voltage biases floating sensors to help meet the common-mode voltage requirements of the AD1263 PGA.

All ADC analog inputs are pinned out on the ADS1263EVM. The supporting circuitry provides filtering and ratiometric connections for a variety of sensors. Additionally, terminal block J4 can be used for thermocouple inputs (see Section 3.1.2.1). Terminal block J5 shows the connection and input filter for AINCOM. Figure 3-1 shows the schematic of the ADS1263EVM analog input circuitry.

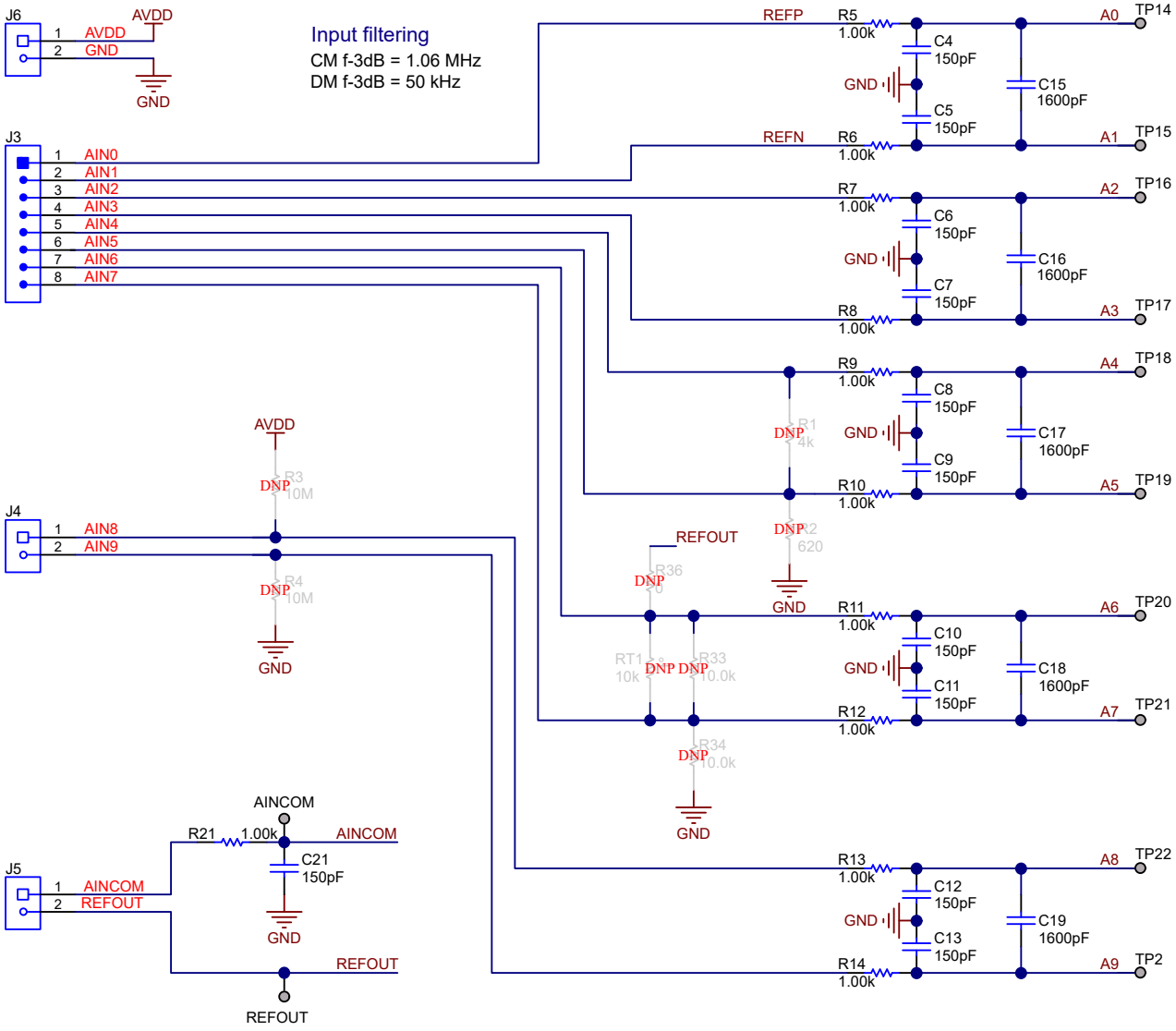

Figure 3-1. ADS1263EVM Analog Input Channels and Filtering

3.1.1 ADS1263 Integrated Input Functions

Each ADS1263 analog input pin has multipurpose functionality to support a wide variety of device applications. Table 3-1 summarizes the functions available for each ADC input pin.

Table 3-1. ADS1263 Analog Input Pin Functions

Input Pin	ADC Input	IDAC Output	VBIAS Output	External VREF Input	Test DAC Output	GPIO
AIN0	Yes	Yes	—	REF1 P	—	—
AIN1	Yes	Yes	—	REF1 N	—	—
AIN2	Yes	Yes	—	REF2 P	—	—
AIN3	Yes	Yes	—	REF2 N	—	Yes
AIN4	Yes	Yes	—	REF3 P	—	Yes
AIN5	Yes	Yes	—	REF3 N	—	Yes
AIN6	Yes	Yes	—	—	Yes	Yes
AIN7	Yes	Yes	—	—	Yes	Yes
AIN8	Yes	Yes	—	—	—	Yes
AIN9	Yes	Yes	—	—	—	Yes
AINCOM	Yes	Yes	Yes	—	—	Yes

3.1.1.1 ADC Inputs

The ADS1263 has a flexible input multiplexer with 11 analog inputs. Any input can connect to the positive input and any input can connect to the negative input. The ADS1263 also includes an auxiliary, 24-bit ΔΣ ADC with an independent flexible input multiplexer to all input pins. Configure the inputs to provide either single-ended or differential input measurements.

3.1.1.2 IDAC Output

The ADS1263 provides dual-matched current sources (IDAC1 and IDAC2) for biasing of RTDs, thermistors, and other resistive-biased sensors. The IDACs can be independently programmed and can be connected to any analog input. Each IDAC output is programmable from 50 µA to 3000 µA. The ADC internal reference must be enabled for IDAC operation.

3.1.1.3 VBIAS Output

For single-supply operation, the level-shift function (VBIAS) can offset the common input voltage on AINCOM to a mid-supply voltage ([AVDD + AVSS] / 2).

3.1.1.4 External Reference

The ADS1263 can accept an external reference in addition to the internal and supply reference options. The external reference inputs are shared with pins AIN0 through AIN5. ADC1 and ADC2 can share a reference source, though an independent reference source can also be selected for ADC2.

3.1.1.5 Test DAC Output

An internal test DAC (TDAC) provides a known voltage to the ADC to diagnose the operation of the signal chain. The positive and negative TDAC voltages are output on AIN6 (J3:7) and AIN7 (J3:8), respectively. Do not load AIN6 and AIN7 when the test signals are enabled because the TDAC outputs are unbuffered.

3.1.1.6 GPIO

Eight inputs (AIN3 through AINCOM) are configurable as general-purpose input/outputs (GPIO). The GPIO voltages are referenced to the analog power supply (AVDD and AVSS) and therefore must use 5-V logic. Use the GPIOs to control external devices or to read external logic signals.

3.1.2 Analog Sensor Connections

The ADS1263 is designed to easily interface with many types of analog sensors including weigh scales, strain gauge sensors, and analog temperature sensors. The following sections provide more detail for connecting and measuring temperature sensors, including thermocouples (see Section 3.1.2.1), thermistors (see Section

3.1.2.2), and RTDs (see Section 3.1.2.4). Connect these sensors as well as other similar devices across terminals J3-J6 on the ADS1263EVM, as per Figure 3-1.

3.1.2.1 Connecting a Thermocouple to J4 on the ADS1263EVM

Measure an external thermocouple by connecting the sensor directly to the J4:1 and J4:2 inputs on the J4 terminal block. The differential filter for this differential input pair has a cutoff frequency of 50 kHz. Additionally, each input has a common-mode filter with a cutoff frequency of 497.36 kHz. J4 is connected through the filter resistors to analog inputs AIN8 and AIN9 on the ADS1263. Figure 3-2 shows the portion of the ADS1263EVM schematic with J4 and the thermocouple input structure.

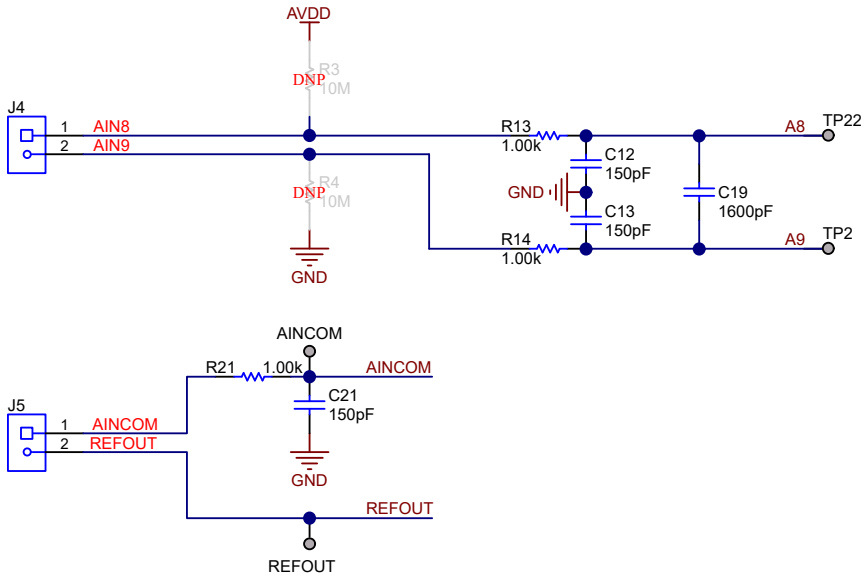

Figure 3-2. ADS1263EVM Thermocouple Input Structure

Although thermocouples are self-powered, these components must be biased to avoid floating beyond the input range of the PGA integrated into the ADC. Thermocouples are typically biased to AVDD / 2 because AVDD / 2 is also the middle of the PGA common-mode range. Designing a bias circuit at this voltage therefore enables the largest gain for any given thermocouple voltage. The ADS1263EVM offers multiple ways to bias the thermocouple so the output voltage can be successfully read by the ADS1263.

The first method uses pullup and pulldown resistors to center the thermocouple output voltage at AVDD / 2. Figure 3-2 shows that these resistors are designated R3 and R4 on the ADS1263EVM, but are not installed by default. Therefore, 1-MΩ to 10-MΩ resistors must be installed at R3 and R4 to use the pullup and pulldown resistor biasing scheme. One added benefit of using pullup and pulldown resistors is that these resistors enable continuous sensor break detection. If one of the thermocouple wires breaks, AIN8 is pulled up to AVDD and AIN9 is pulled to GND. These conditions cause the ADC to measure a full-scale input that is easily distinguishable from the normal, low-level thermocouple output voltage.

The second thermocouple biasing method that is supported by the ADS1263EVM uses the ADS1263 internal reference from REFOUT (J5:2). Figure 3-3 illustrates how to connect an external jumper between the AIN9 input (J4:2) and REFOUT output (J5:2) to bias the thermocouple input voltage to 2.5-V. One challenge with the configuration in Figure 3-3 is that this option does not offer continuous wire-break detection. Instead, perform wire-break detection using a separate diagnostic measurement or by installing pullup resistor R3.

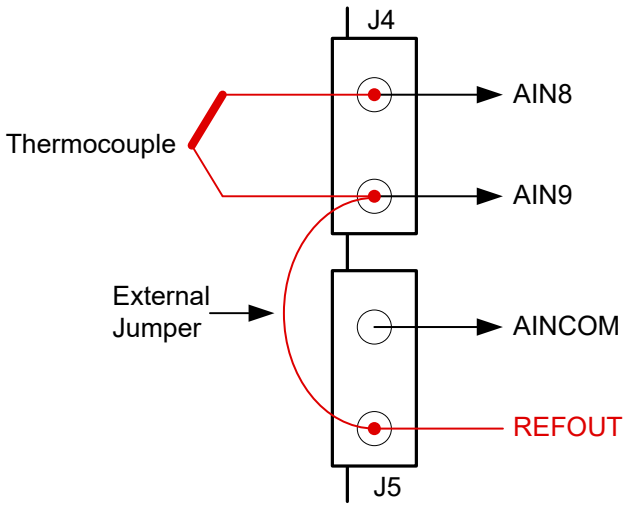

Figure 3-3. Using REFOUT (input J5:2) to Bias a Thermocouple

To learn more about the different thermocouple biasing schemes, as well as how to measure these sensors with precision ADCs, see the *A Basic Guide to Thermocouple Measurements application note*. This application note also discusses the need for cold-junction compensation (CJC), which uses a thermistor in conjunction with a thermocouple to derive the measured temperature. This process is described in Section 3.1.2.3.

3.1.2.2 Connecting a Thermistor to J3 on the ADS1263EVM

Unlike a thermocouple, thermistors are not self-powered and require a constant voltage or current source to operate. Constant voltage is typically preferred because the thermistor impedance can vary from hundreds of ohms at low temperature to hundreds of thousands of ohms at high temperature (or vice versa for a thermistor with a negative temperature coefficient). A resistor is added in series with the thermistor to create a resistor divider that can be measured by an ADC.

Connect an external thermistor directly to the J3:7 and J3:8 pins on the J3 terminal block, which corresponds to analog inputs AIN6 and AIN7, respectively. The differential filter for this differential input pair has a cutoff frequency of 50 kHz. Additionally, each input has a common-mode filter with a cutoff frequency of 497.36 kHz. AIN6 and AIN7 are connected through the filter resistors to the respective analog inputs on the ADS1263. Figure 3-4 shows the portion of the ADS1263EVM schematic with J3 and the thermistor input structure.

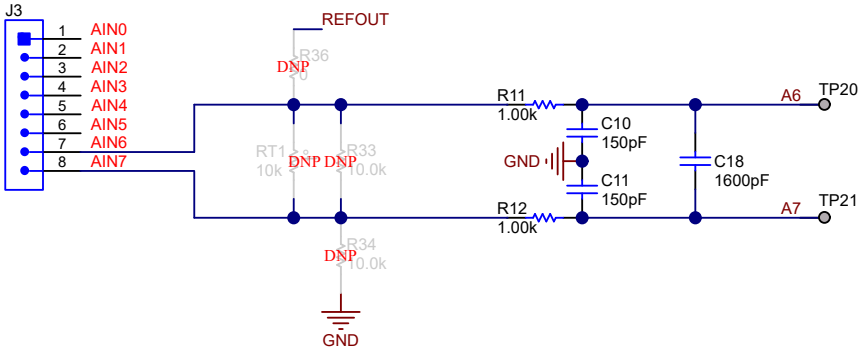

Figure 3-4. ADS1263EVM Thermistor Input Structure

Figure 3-4 shows four DNP components: a thermistor (RT1), a 10-kΩ linearization resistor (R33), a 10-kΩ bias resistor (R34), and a 0-Ω bias resistor (R36) connecting REFOUT to AIN6 to bias the sensor. Resistor R33 helps linearize the thermistor output voltage over a smaller temperature range. See section 2.8.2 in the *A Basic Guide to Thermocouple Measurements application note* to learn more about the benefits of using a linearization resistor when measuring a thermistor. Resistor R34 was chosen to be 10-kΩ because 10 kΩ is a commonly used nominal thermistor impedance. Choosing both resistors to have the same nominal impedance balances the resistor divider at 25°C.

As stated earlier in this section, thermistors are not self-powered and require a bias source to operate. The ADS1263EVM includes two methods to bias a thermistor using the 2.5-V reference output of the ADS1263. The first option requires populating the 0-Ω resistor (R36) in Figure 3-4. The second option requires installing an external jumper wire, as shown in Figure 3-5. In either case, make sure that the reference output (REFOUT) used to bias the resistor is selected as the reference source for the ADC measurements.

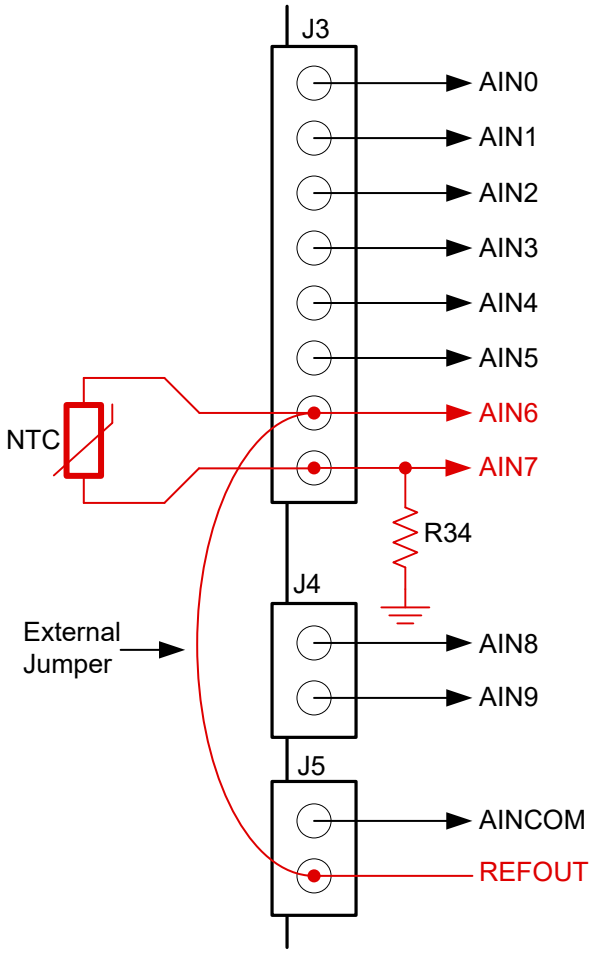

Figure 3-5. Using REFOUT (input J5:2) to Bias a Thermistor

3.1.2.3 Using Thermistor RT1 for Thermocouple Cold-Junction Compensation

The ADS1263EVM includes provisions for using a PCB-mounted thermistor to measure the cold junction of a thermocouple connected to the AIN8 and AIN9 inputs on J4. Figure 3-6 shows how top- and bottom-layer copper pours create an isothermal bridge between the AIN8 and AIN9 inputs. This bridge helps make sure that thermistor RT1 measures the same temperature as the thermocouple cold junction at inputs J4:1 and J4:2, enabling a more accurate thermocouple measurement.

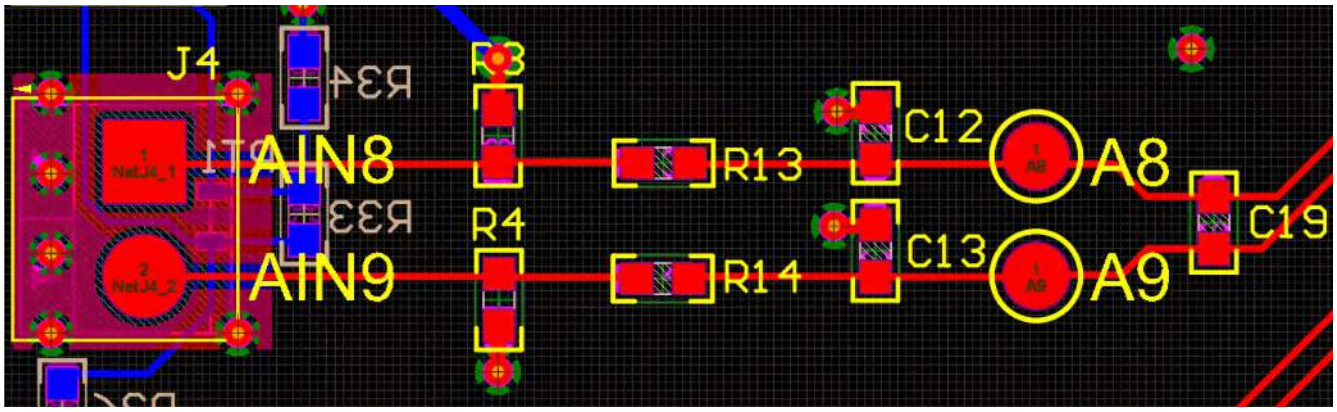

Figure 3-6. PCB Layout for J4 Showing Copper Pours for CJC Measurements

As discussed in Section 3.1.2.2, thermistor RT1 is not populated by default on the ADS1263EVM. Choose a 10-kΩ NTC thermistor in a 0603 package for this component. Additionally, populate the 10-kΩ bias resistor (R34) to create a valid resistor divider as well as the 0-Ω resistor (R36) to directly bias the sensor using the 2.5-V reference output of the ADS1263. Populating the linearization resistor (R33) is optional.

Measure the thermistor voltage as described in Section 3.1.2.2. However, note that the ADS1263 is a multiplexed ADC that can only measure one single-ended or differential input per conversion cycle. As a result, the thermocouple and CJC measurements must be taken separately and then manipulated in software to determine the resulting temperature. To learn more about CJC as well as how to use this value to determine the true measured temperature, see the *A Basic Guide to Thermocouple Measurements application note*.

3.1.2.4 Connecting an RTD to J3 on the ADS1263EVM

The ADS1263EVM provides the flexibility to measure multiple RTD types and configurations using differential pairs AIN0 and AIN1, AIN2 and AIN3, or AIN6 and AIN7 through terminal block J3. Each of these differential pairs has a differential filter with a cutoff frequency of 50 kHz. Additionally, each input has a common-mode filter with a cutoff frequency of 497.36 kHz. See Figure 3-1 for an overview of the ADS1263EVM analog input connections.

The ADS1263EVM also includes a placeholder for a precision reference resistor (R1) in series with the RTD. The ADS1263 integrated IDACs provide a constant current through both the RTD and R1 to establish a ratiometric reference voltage between AIN4 and AIN5 on the EVM. Any noise or drift in the IDAC occurs equally in the input and reference voltage, and therefore cancels out.

Choose resistor R1 to accommodate the RTD resistance across the entire temperature range. For example, a Pt1000 at 850°C has a typical impedance of approximately 3.9-kΩ. A 0-Ω resistor must also be installed at R2 to provide the IDAC a path to ground.

Choose the IDAC current magnitude and the total circuit impedance to make sure that the ADC IDAC compliance voltage is met. For additional information regarding ratiometric RTD measurement circuits using precision ADCs and for important specifications including compliance voltage, see the *A Basic Guide to RTD Measurements application note*.

The following sections detail how to connect a 2-wire, 3-wire, or 4-wire RTD to the ADS1263EVM.

3.1.2.4.1 Connecting a 2-Wire RTD

Connect a 2-wire RTD to any of the following differential pairs on terminal block J3: AIN0 and AIN1, AIN2 and AIN3, or AIN6 and AIN7. Figure 3-7 shows an example where the 2-wire RTD is connected to differential pair AIN6 and AIN7.

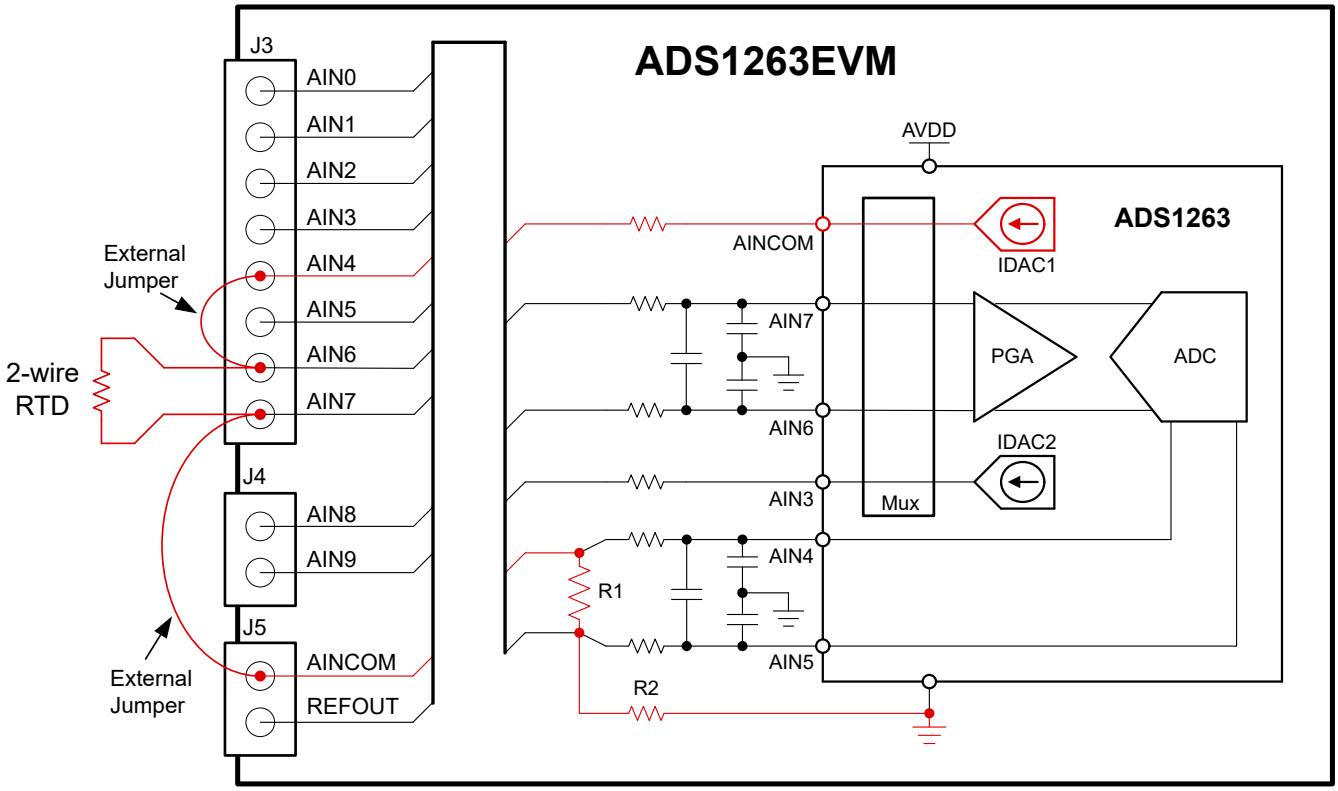

Figure 3-7. 2-Wire RTD Ratiometric Connection Example

In this configuration, connect external jumper wires between AIN4 (J3:5) and AIN6 (J3:7) as well as AIN7 (J3:8) to AINCOM (J5:1). These jumper wires route the IDAC current on AINCOM around the input filtering to prevent voltage drops in the input signal path. IDAC current flows across the RTD and then through R1. The ratiometric reference voltage is generated between AIN4 and AIN5. The IDAC current is then routed to GND through resistor R2 when populated.

3.1.2.4.2 Connecting a 3-Wire RTD

Connect the two measurement leads of a 3-wire RTD to any of the following differential pairs on terminal block J3: AIN0 and AIN1, AIN2 and AIN3, or AIN6 and AIN7. Connect the remaining common lead to AIN4. Figure 3-8 shows an example where the 3-wire RTD is connected to differential pair AIN6 and AIN7. Two IDACs are used in this example, though this approach is not strictly necessary.

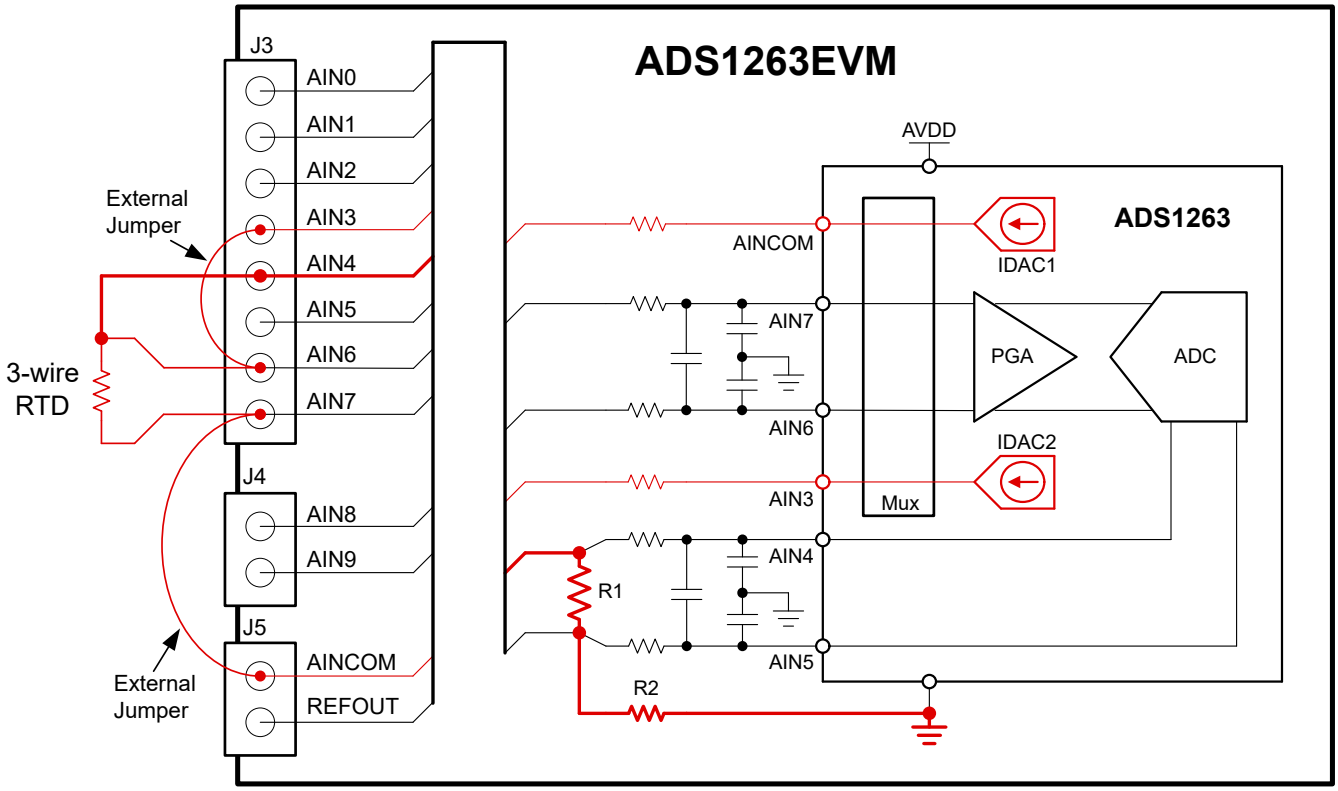

Figure 3-8. 3-Wire RTD Ratiometric Connection Example

In this configuration, connect external jumper wires between AIN7 (J3:8) to AINCOM (J5:1). An additional jumper wire is required between AIN6 (J3:7) to AIN3 (J3:4) if two IDACs are used. These jumper wires route the IDAC currents on AINCOM and AIN3 around the input filtering to prevent voltage drops in the input signal path. IDAC1 current flows across the RTD and then the combined current of IDAC1 and IDAC2 flows through R1. The ratiometric reference voltage is generated between AIN4 and AIN5. The IDAC currents are then routed to GND through resistor R2 when populated.

3.1.2.4.3 Connecting a 4-Wire RTD

Connect the two measurement leads of a 4-wire RTD to any of the following differential pairs on terminal block J3: AIN0 and AIN1, AIN2 and AIN3, or AIN6 and AIN7. Connect the remaining common leads to AIN4 and AINCOM. Figure 3-9 shows an example where the 4-wire RTD is connected to differential pair AIN6 and AIN7.

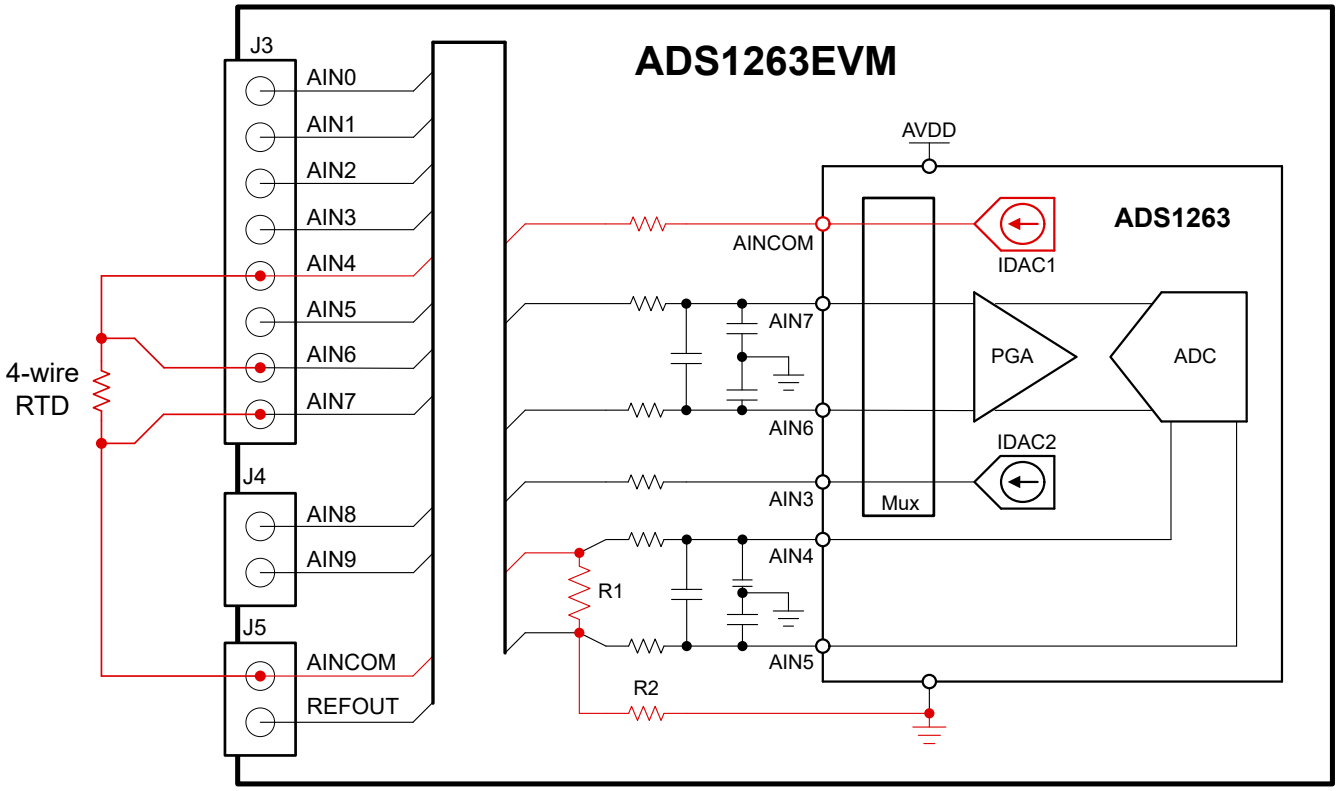

Figure 3-9. 4-Wire RTD Ratiometric Connection Example

In this configuration, no external jumper wires are necessary. IDAC current flows across the RTD and then through R1. The ratiometric reference voltage is generated between AIN4 and AIN5. The IDAC current is then routed to GND through resistor R2 when populated.

3.2 ADC Connections and Decoupling

Figure 3-10 shows all ADC connections. Each power-supply and reference connection has a 1-µF decoupling capacitor. Place these capacitors as close as possible to the ADC pins and make sure each component has a low-impedance connection to the GND plane.

Each ADC digital pin has a 49.9-Ω series resistor in series with the trace. These resistors smooth the edges of the digital signals to minimize overshoot and ringing. A resistor is most important on the serial clock (SCLK) trace because the SCLK signal can toggle as quickly as 40 MHz. Resistors on the other pins are not strictly required, though these components can be included in the final design to improve digital signal integrity.

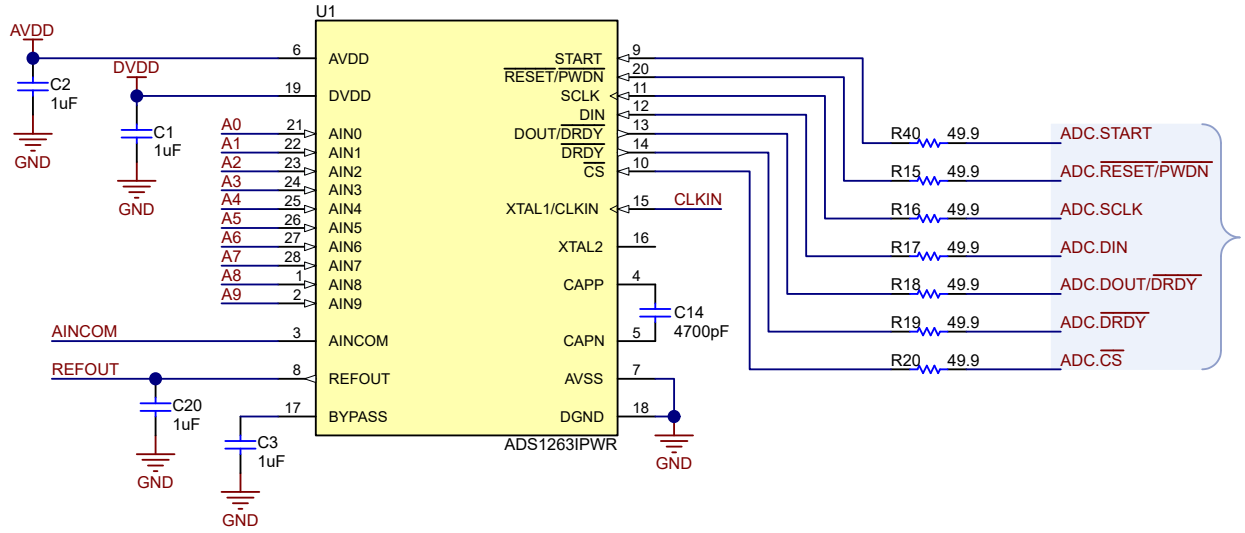

Figure 3-10. ADS1263EVM ADC Power-Supply Decoupling and Analog and Digital Connections

3.3 Clocking

Figure 3-11 shows the different clocking options for the ADS1263EVM. The default configuration connects a 0-Ω resistor (R44) between the ADS1263 CLKIN pin and ground. Shorting CLKIN to ground automatically chooses the ADS1263 internal 7.3728-MHz oscillator to be the ADC clock source.

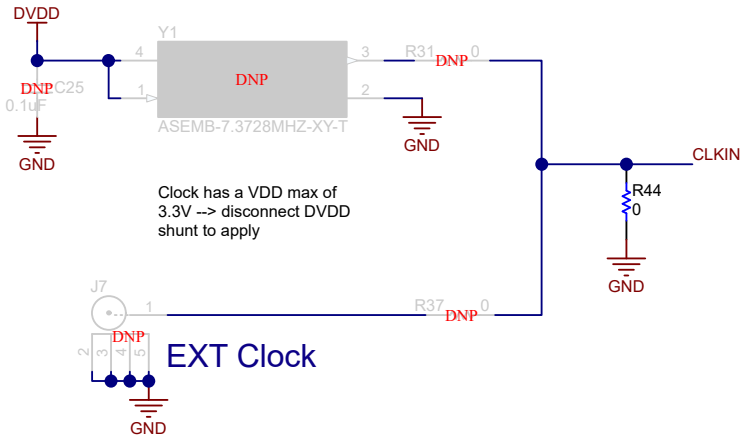

Figure 3-11. ADS1263EVM External Voltage Reference Circuit (Optional)

An external clock can also be provided to the ADC. Figure 3-11 shows multiple ways to apply an external clock. First, an external 7.3728-MHz oscillator can be installed by using component Y1. The supply voltage for the recommended clocking component can be a maximum of 3.3 V and is tied to DVDD as a result. Review the data sheet parameters for any alternate components to confirm operation with these settings. See Section 5 if the selected clock requires a different DVDD voltage. In all cases, using an external clock at Y1 requires installing a 0-Ω resistor at R31 and removing R44.

The ADS1263EVM also offers the option of connecting an external clock using SMA connector J7. Choosing this clock option also requires installing a 0-Ω resistor at R37 and removing R44. However, neither of these external clock options are installed by default.

3.4 Voltage Reference

The ADS1263 can accept an external reference in addition to the internal and supply reference options. The external reference inputs are shared with pins AIN0 through AIN5. See Table 3-1 to determine which pins correspond to RMUXP and RMUXN. ADC1 and ADC2 can share a reference source, though an independent reference source can be selected for ADC2.

Figure 3-12 shows that the ADS1263EVM also includes an optional external voltage reference circuit that is not installed by default.

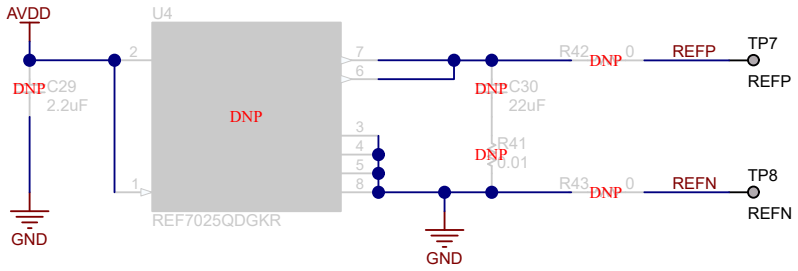

Figure 3-12. ADS1263EVM External Voltage Reference Circuit (Optional)

The external reference circuit includes several resistors and capacitors that are not installed by default. A discrete voltage reference is also required. The recommended component is Texas Instruments' REF7025. This voltage reference offers very low noise, a very low temperature drift coefficient (2 ppm/°C), and high accuracy (±0.025%). Use the REF7025 with the ADS1263 in precision applications where performance is critical. The REF7025 output voltage is connected to analog inputs AIN0 and AIN1.

4 Digital Interface

As noted in Section 1 and Section 2, the EVM interfaces with the PHI and communicates with the host over USB. Figure 4-1 shows how the PHI communicates with two devices on the EVM: the ADS1263 using the serial peripheral interface (SPI) and the EEPROM using the inter-integrated circuit (I^2C) interface. The EEPROM comes preprogrammed with the information required to configure and initialize the ADS1263EVM. When the hardware is initialized, no further communication with the EEPROM is necessary and this device can be ignored by the user.

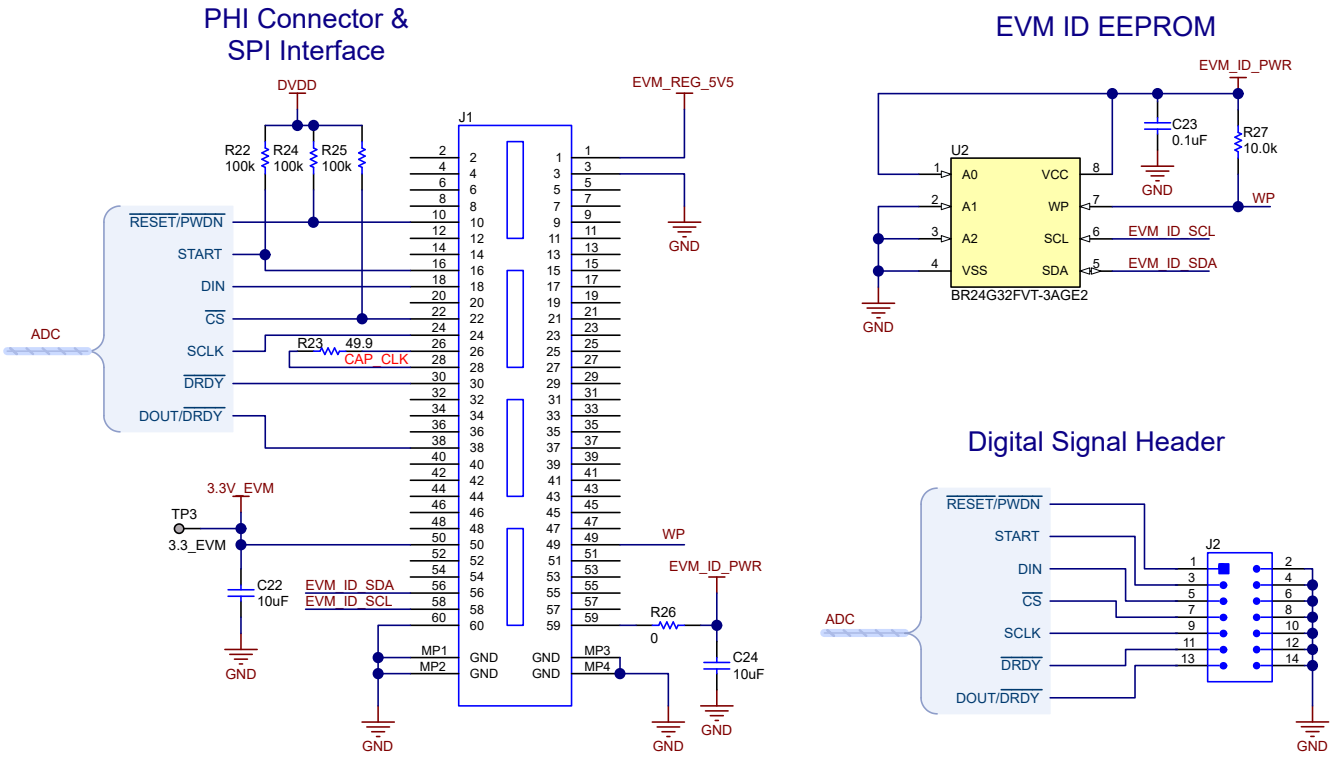

Figure 4-1. ADS1263EVM Digital Interface Connections

The ADS1263 uses SPI serial communication in mode 01 where CPOL = 0 and CPHA = 1. Header J2 in Figure 4-1 provides test points for all digital signals to and from the PHI controller. The test points can be connected to a logic analyzer for convenient visualization of the digital signals. These test points can also be used to communicate with the ADS1263EVM using an external controller.

Pullup resistor R22 drives the START pin high and puts ADC1 in continuous conversion mode. The ADC then continuously converts until the START pin is returned low. Pullup resistor R24 drives the $\overline{\text{RESET}}$/$\overline{\text{PWDN}}$ pin high to hold the ADC in conversion mode. A momentary low pulse resets the ADC. Holding $\overline{\text{RESET}}$/$\overline{\text{PWDN}}$ low enables the ADC power-down mode. Pullup resistor R35 brings the chip-select ($\overline{\text{CS}}$) pin high, which resets the serial interface. The $\overline{\text{CS}}$ pin must be pulled low during the entire data transaction. More information about the specifics of the digital pins can be found in the ADS1263 data sheet.

5 Power Supplies

The default ADC power-supply voltages (DVDD and AVDD) are generated by the PHI controller using power from the USB. The PHI provides 3.3-V and 5.5-V power rails. The 3.3-V power rail directly supplies the ADC DVDD voltage. The 5.5-V power rail is supplied to the input of the TPS7A4700, a low-noise, configurable-output LDO, to supply AVDD. The LDO output voltage depends on the internal reference voltage (V_{LDO_REF}) of 1.4 V and the pin connections. Grounding any LDO pin between pin 4 through pin 12 adds that pin voltage to V_{LDO_REF} and increases the LDO output voltage, LDO_{VOUT}. Figure 5-1 shows that the ADS1263EVM grounds pin 6 and pin 10 (3P2V and 0P4V, respectively) to set LDO_{VOUT} to 5 V.

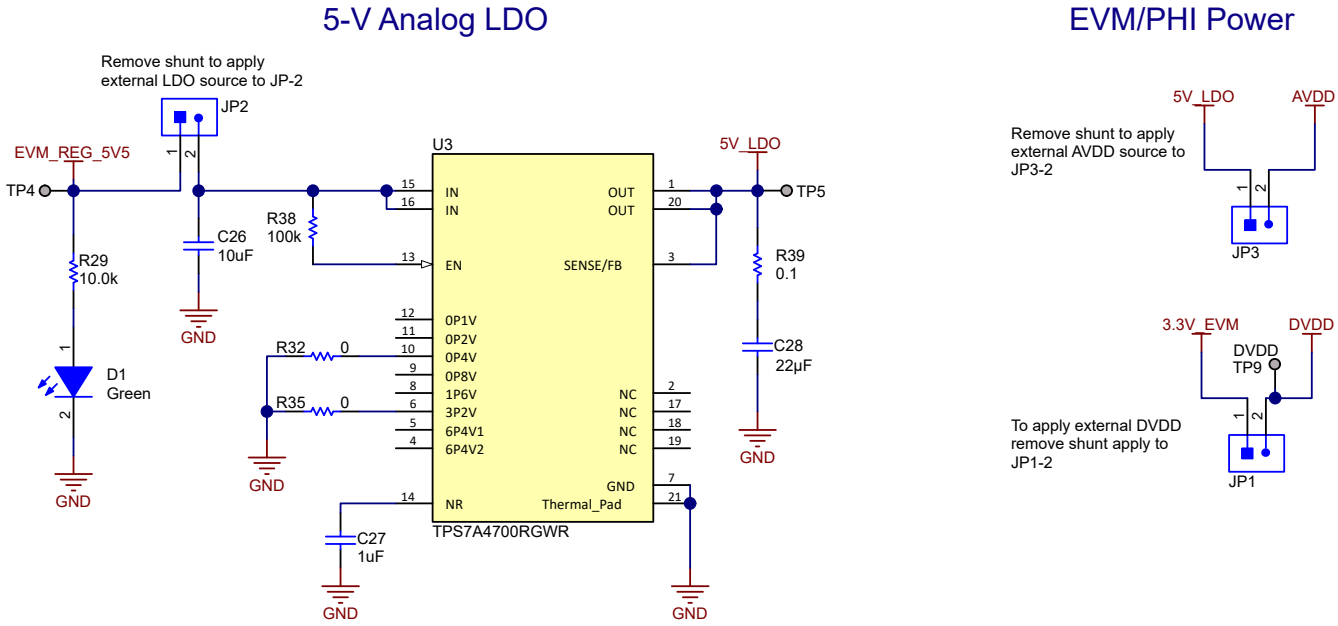

Figure 5-1. ADS1263EVM LDO Circuit and External Power Source Connections

Figure 5-1 also shows that the 5V_LDO output is used for the AVDD connections across the EVM. Additionally, the user can measure the AVDD current by connecting an ammeter between pins 1 and 2 of JP1 or the DVDD current by connecting an ammeter between pins 1 and 2 of JP3.

External power sources can also be provided for each supply voltage:

- LDO: Remove the shunt on JP2 and connect external power to JP2:2
- AVDD: Remove the shunt on JP3 and connect external power to JP3:2
- DVDD: Remove the shunt on JP1 and connect external power to JP1:2

When using either internal or external power supplies, LEDs D2 and D3 indicate if power is connected to AVDD and DVDD, respectively. These LEDs do not necessarily indicate if AVDD is 5 V or if DVDD is 3.3 V. Check the AVDD voltage using terminal JP6:1 and check the DVDD voltage using test point TP9. Figure 5-2 shows the portion of the schematic that includes the AVDD and DVDD LEDs.

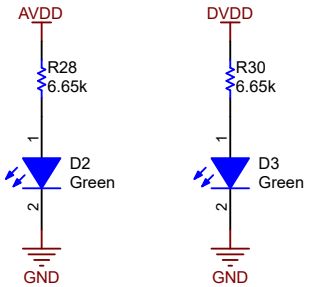

Figure 5-2. ADS1263EVM AVDD and DVDD Indicator LEDs and Shunts

6 Software Installation

Download the latest version of the EVM GUI installer from the ADS1263EVM tool folder. Run the program to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message may appear or the *installer.exe* file may be deleted.

As shown in Figure 6-1, accept the license agreements and follow the on-screen instructions to complete the installation.

Figure 6-1. Software Installation and Prompts

As shown in Figure 6-2, a prompt with a *Device Driver Installation* appears on the screen as part of the ADS1263EVM GUI installation. Click *Next* to continue.

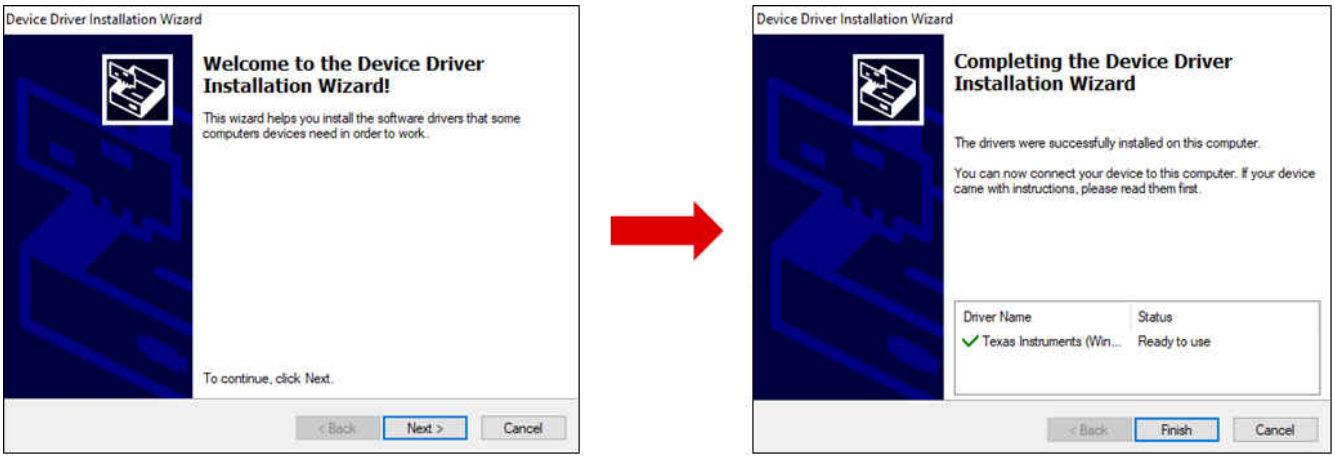

Figure 6-2. Device Driver Installation and Prompts

The ADS1263EVM requires the LabVIEW™ run-time engine and can prompt for the installation of this software if not already installed. Figure 6-3 shows the LabVIEW installation prompts.

Figure 6-3. LabVIEW Run-Time Engine Installation

7 EVM Operation and GUI

7.1 Connecting the EVM Hardware

After installing the EVM software, connect the EVM as shown in Figure 7-1 and as described in the following steps:

1. Physically connect P2 of the PHI to J1 of the ADS1263EVM. Install the screws to provide a robust connection.
2. Connect the USB cable from the computer to the PHI.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC. Figure 7-1 shows the resulting LED indicators.
3. Start the software GUI as shown in Figure 7-2. The LEDs blink slowly as the FPGA firmware is loaded on the PHI. This loading takes a few seconds and then the AVDD and DVDD power supplies turn on, as indicated by LEDs D1, D2, and D3 on the ADS1263EVM.
4. Connect external sensors to terminal blocks J3-J6 in accordance with the examples given in Section 3.1.2.

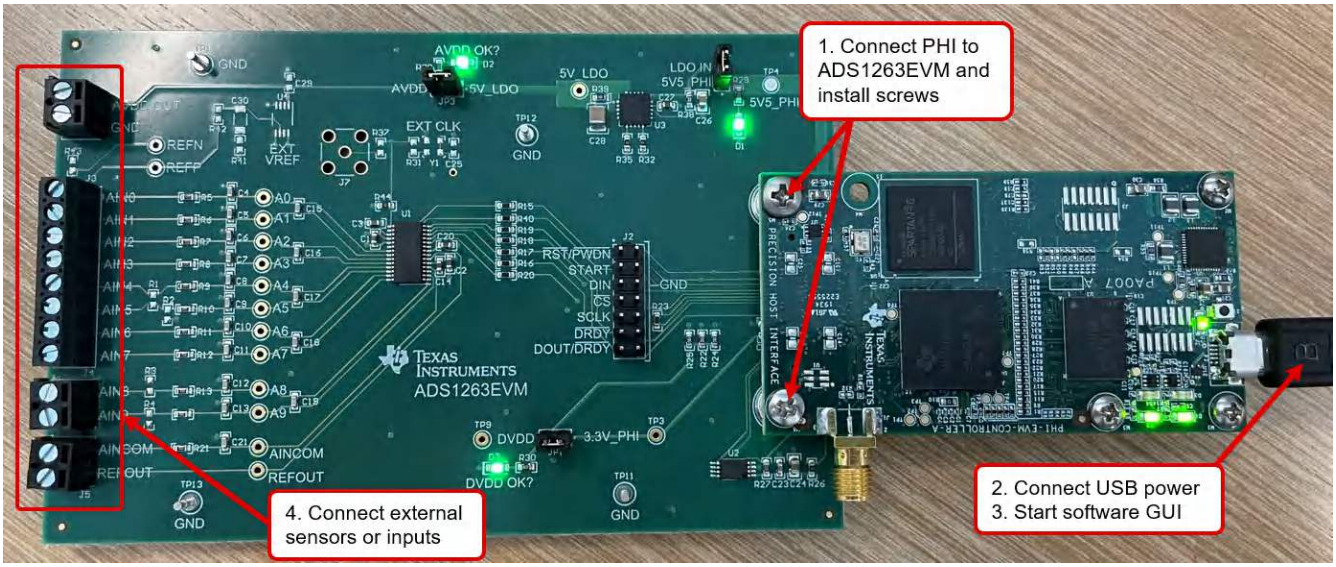

Figure 7-1. ADS1263EVM Hardware Connections

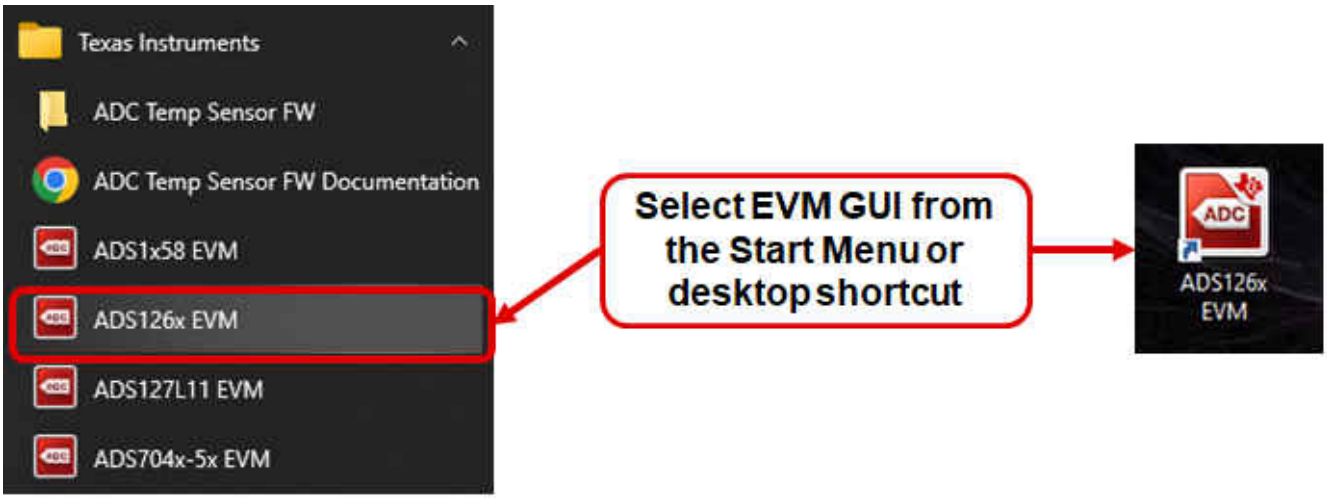

Figure 7-2. Launch the EVM GUI Software

7.2 EVM GUI Global Settings for ADC Control

Figure 7-3 shows that the EVM global controls are located on the left side of the GUI. These controls include the filter type, data rate, PGA gain, input channels, number of samples, and others. The *Pages* control in the upper-left allows access to the other pages in the GUI. Figure 7-3 also shows the ADC register settings. The registers can be used to set the different device modes such as power, PGA, and ADC selection. Change the register settings by clicking on each bit, typing a value directly into the *Value* column, or by selecting from the drop-down menus in the *Field View* control.

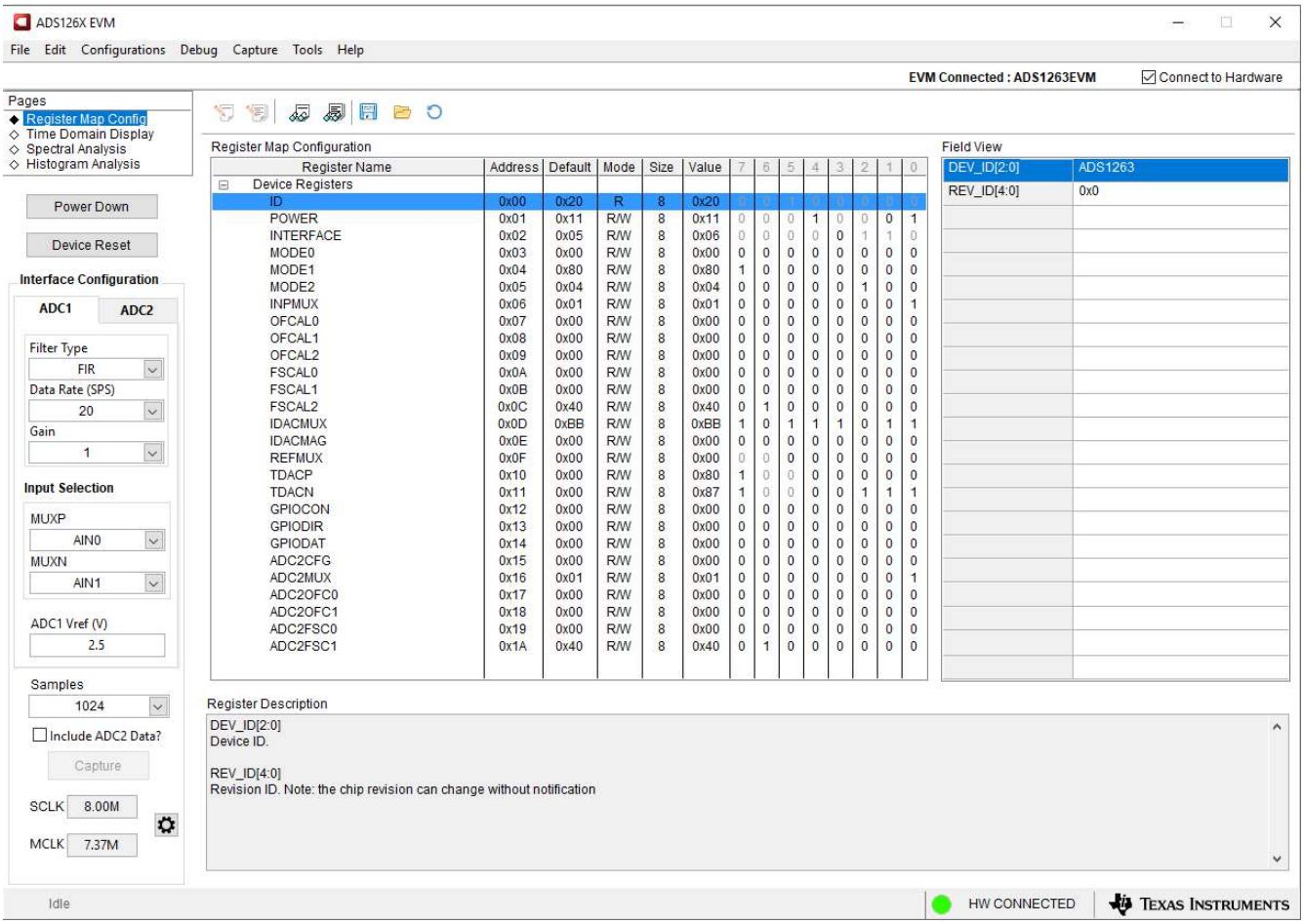

Figure 7-3. ADS1263EVM GUI Global Settings for the ADC Control Page

7.3 Time Domain Display

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior of and debugging any gross problems with the ADC or drive circuits. Trigger a data capture of the selected number of samples from the ADS1263EVM by using the *Capture* button in Figure 7-4. The captured data are subject to the current interface mode settings. The time-domain plot has *Samples* on the x-axis and by default shows the corresponding *Codes* on the y-axis relative to the specified reference voltage. The y-axis units can be changed to *Voltage/Temp* using the *Unit* control in the bottom right. The *Temp* units are only used with the Temp channel selection.

The *Measurements* control on the bottom of Figure 7-4 calculates the code range, the mean code, and the code standard deviation. Switching pages to any of the *Analysis* tools described in the subsequent sections causes calculations to be performed on the same set of data.

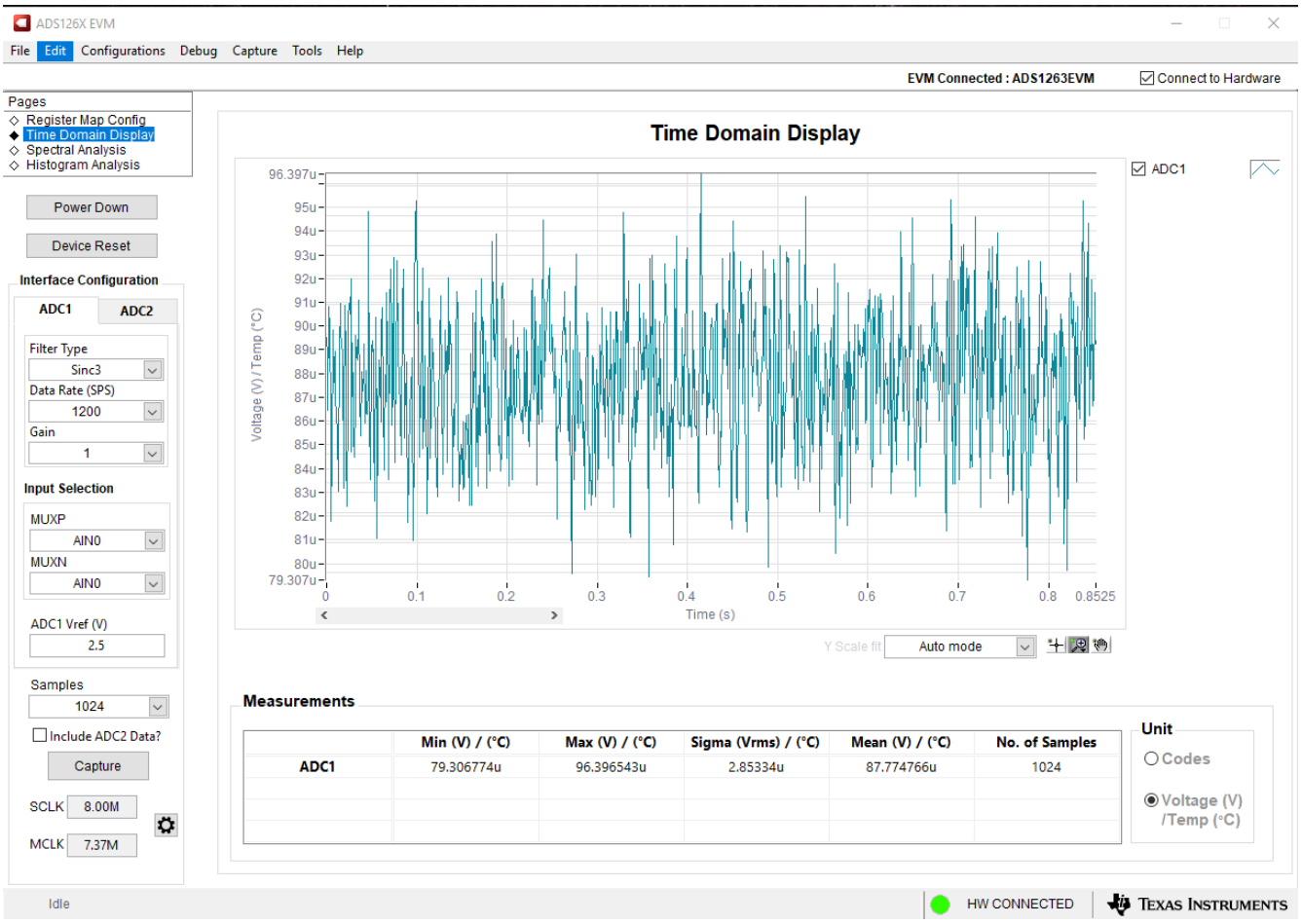

Figure 7-4. ADS1263EVM GUI Time Domain Display Page

7.4 Frequency Domain Display

Figure 7-5 shows the spectral analysis tool that evaluates the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS1263. This dynamic performance is calculated by single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-term Blackman-Harris window is the default option and has sufficient dynamic range to resolve the frequency components of a 32-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

Figure 7-5. ADS1263EVM GUI Frequency Domain Display Page

7.5 Histogram Display

Noise degrades ADC resolution and the histogram tool shown in Figure 7-6 can be used to estimate effective resolution. Effective resolution is a metric describing the ADC resolution loss resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

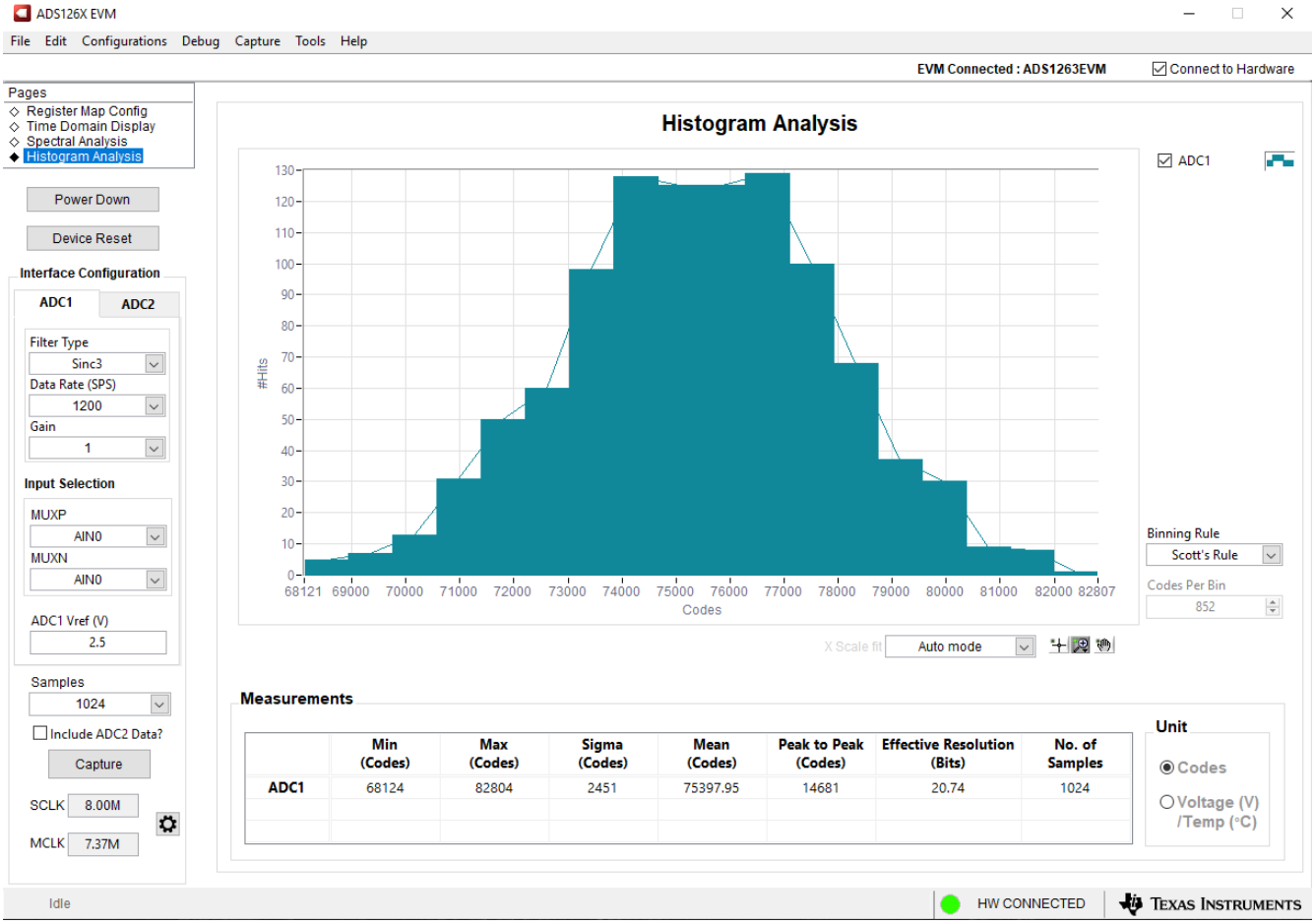

Figure 7-6. ADS1263EVM GUI Histogram Display Page

7.6 Using the GUI to Control ADC2

As noted throughout this document, the ADS1263 includes two ADCs: a 32-bit primary device (ADC1), and a 24-bit secondary converter (ADC2). The ADS1263EVM GUI is capable of controlling both ADC1 and ADC2 using the global settings on the left side of the GUI. Figure 7-7 highlights the controls for ADC2.

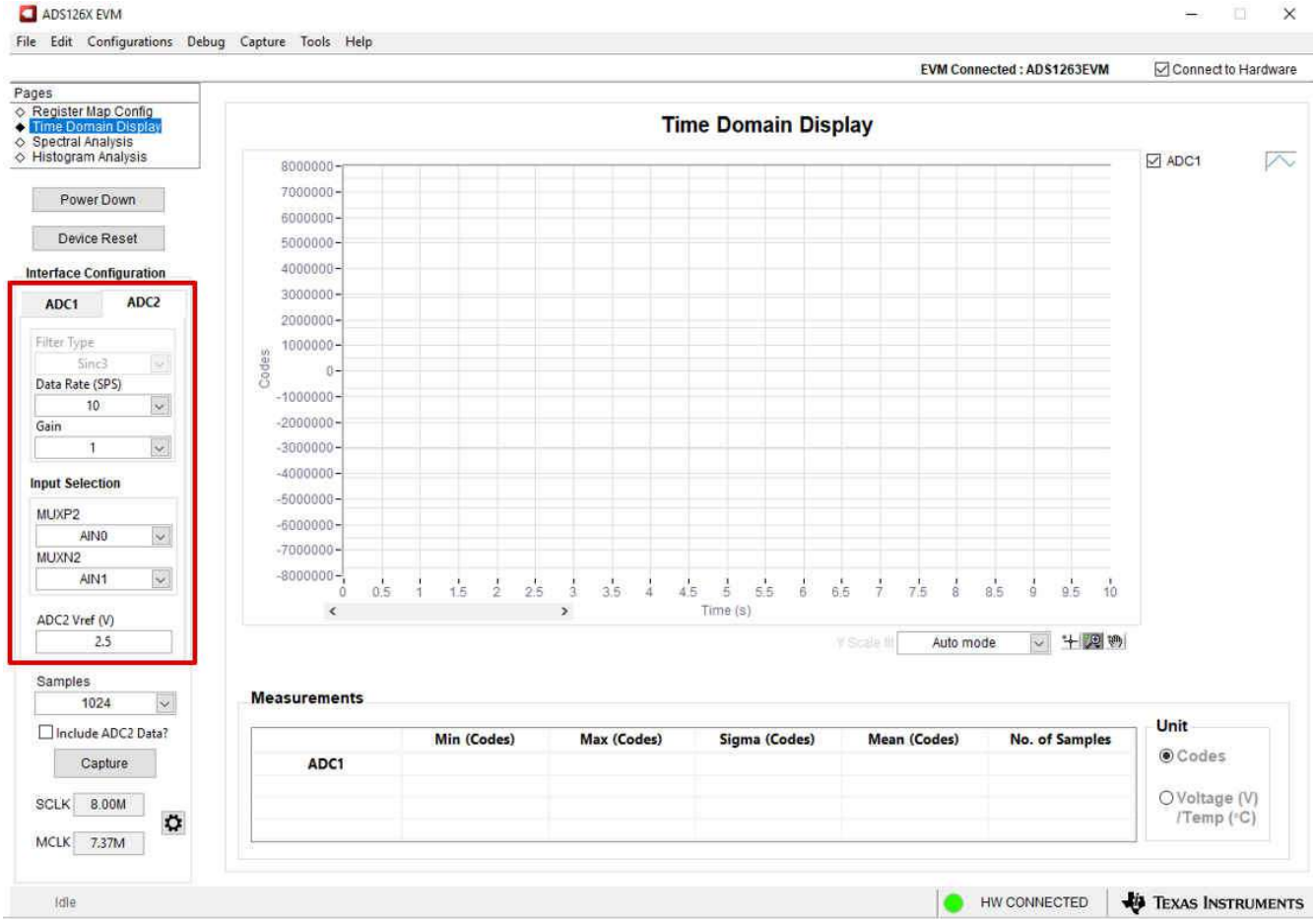

Figure 7-7. ADS1263EVM GUI Global Settings for ADC2

As Figure 7-7 shows, ADC2 can use a different data rate, gain, input channels, and reference voltage compared to ADC1. However, ADC2 can only use the *Sinc3* filter, and both ADCs must use the same number of *Samples*. To view both ADC1 and ADC2 data in the GUI, select the *Include ADC2 data?* check box.

The GUI operates by converting samples at the data rate specified by ADC1, which can be different from ADC2. Therefore:

- If the data rate for ADC2 is greater than the data rate for ADC1, some new samples for ADC2 are not captured by the GUI. The GUI provides a warning when these conditions are met.
- If the data rate for ADC2 is less than the data rate for ADC1, repeat values are sampled for ADC2. These values are not shown in the GUI such that ADC2 data is only updated when the data are new.

See the ADC2 section of the ADS1263 data sheet for more information about how to configure and retrieve data from ADC2.

8 Bill of Materials, PCB Layout, and Schematics

This section contains the ADS1263EVM bill of materials, PCB layout, and the EVM schematics.

8.1 Bill of Materials

Table 8-1 lists the bill of materials (BOM) for the ADS1263EVM.

Table 8-1. Bill of Materials

Designator	Quantity	Value	Part Number	Manufacturer	Description
C1, C2, C3, C20, C27	5	1uF	C0603C105K3RACTU	Kemet	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603
C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C21	11	150pF	C0603C151J5GACTU	Kemet	CAP, CERM, 150 pF, 50 V, +/- 5%, C0G/NP0, 0603
C14	1	4700pF	C0603C472J1GAC7867	Kemet	CAP, CERM, 4700 pF, 100 V, +/- 5%, C0G/NP0, 0603
C15, C16, C17, C18, C19	5	1600pF	GRM1885C1H162JA01D	MuRata	CAP, CERM, 1600 pF, 50 V, +/- 5%, C0G/NP0, 0603
C22, C24, C26	3	10uF	CL21A106KAFN3NE	Samsung Electro-Mechanics	CAP, CERM, 10 uF, 25 V, +/- 10%, X5R, 0805
C23	1	0.1uF	C0603C104J3RAC	Kemet	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603
C28	1	22uF	CL32B226KAJNFNE	Samsung Electro-Mechanics	CAP, CERM, 22 µF, 25 V,+/- 10%, X7R, 1210
D1, D2, D3	3	Green	APT2012LZGCK	Kingbright	LED, Green, SMD
H1, H2, H3, H4	4		SJ61A1	3M	Bumpon, Cylindrical, 0.312 X 0.200, Black
H5, H6	2		RM3X4MM 2701	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
H7, H8	2		9774050360R	Wurth Elektronik	ROUND STANDOFF M3 STEEL 5MM
J1	1		QTH-030-01-L-D-A	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT
J2	1		TSW-107-07-G-D	Samtec	Header, 100mil, 7x2, Gold, TH
J3	1		ED555/8DS	On-Shore Technology	Terminal Block, 3.5mm, 8-Pos, TH
J4, J5, J6	3		ED555/2DS	On-Shore Technology	Terminal Block, 3.5mm Pitch, 2x1, TH
JP1, JP2, JP3	3		TSW-102-07-G-S	Samtec	Header, 100mil, 2x1, Gold, TH
R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R21	11	1.00k	RT0603BRD071KL	Yageo America	RES, 1.00 k, 0.1%, 0.1 W, 0603
R15, R16, R17, R18, R19, R20, R23, R40	8	49.9	RT0603BRD0749R9L	Yageo America	RES, 49.9, 0.1%, 0.1 W, 0603
R22, R24, R25, R38	4	100k	CRCW0603100KJNEA	Vishay-Dale	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
R26, R32, R35, R44	4	0	RC0603JR-070RL	Yageo	RES, 0, 5%, 0.1 W, 0603
R27, R29	2	10.0k	RC0603FR-0710KL	Yageo	RES, 10.0 k, 1%, 0.1 W, 0603
R28, R30	2	6.65k	RT0603DRE076K65L	Yageo America	RES, 6.65 k, 0.5%, 0.1 W, 0603
R39	1	0.1	ERJ-L03KF10CV	Panasonic	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 1, 0603
SH-JP1, SH-JP2, SH-JP3	3	1x2	SPC02SYAN	Sullins Connector Solutions	Shunt, 100mil, Flash Gold, Black
TP1, TP11, TP12, TP13	4		1573-2	Keystone	Terminal, Turret, TH, Double

Table 8-1. Bill of Materials (continued)

Designator	Quantity	Value	Part Number	Manufacturer	Description
U1	1		ADS1263IPWR	Texas Instruments	High Resolution, 32-bit, 38-kSPS, ADC with PGA, Int Reference and Auxiliary ADC, PW0028A (TSSOP-28)
U2	1		BR24G32FVT-3AGE2	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8
U3	1		TPS7A4700RGWR	Texas Instruments	36-V, 1-A, 4.17-μVRMS, RF low-dropout (LDO) voltage regulator 20-VQFN -40 to 125
C25	0	0.1uF	C0603C104J3RAC	Kemet	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603
C29	0	2.2uF	GRM188R71A225KE15D	MuRata	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7R, 0603
C30	0	22uF	LMK316AB7226KL-TR	Taiyo Yuden	CAP, CERM, 22 uF, 10 V, +/- 10%, X7R, 1206
J7	0		901-144-8RFX	Amphenol RF	SMA Straight Jack, Gold, 50 Ohm, TH
R1	0	4k	Y16364K00000F9R	Vishay Foil Resistors	RES, 4k, 1%, 0.1 W, 0603
R2	0	620	RG1608P-621-B-T5	Susumu Co Ltd	RES, 620, 0.1%, 0.1 W, 0603
R3, R4	0	10Meg	CRCW060310M0DHEAP	Vishay-Dale	RES, 10 M, 0.5%, 0.1 W, AEC-Q200 Grade 0, 0603
R31, R36, R37, R42, R43	0	0	RC0603JR-070RL	Yageo	RES, 0, 5%, 0.1 W, 0603
R33, R34	0	10.0k	RT0603BRD0710KL	Yageo America	RES, 10.0 k, 0.1%, 0.1 W, 0603
R41	0	0.01	WSL0603R0100FEA	Vishay-Dale	RES, 0.01, 1%, 0.1 W, 0603
RT1	0	10k	NCP18XH103F03RB	MuRata	Thermistor NTC, 10.0k ohm, 1%, 0603
U4	0		REF7025QDGKR	Texas Instruments	REF7025QDGK, DGK0008A (VSSOP-8)
Y1	0		ASEMB-7.3728MHZ-XY-T	Abracon Corporation	OSC, 7.3728 MHz, 1.8 - 3.3V, SMD

8.2 PCB Layout

Figure 8-1 shows the EVM printed circuit board (PCB) layout for the ADS1263EVM.

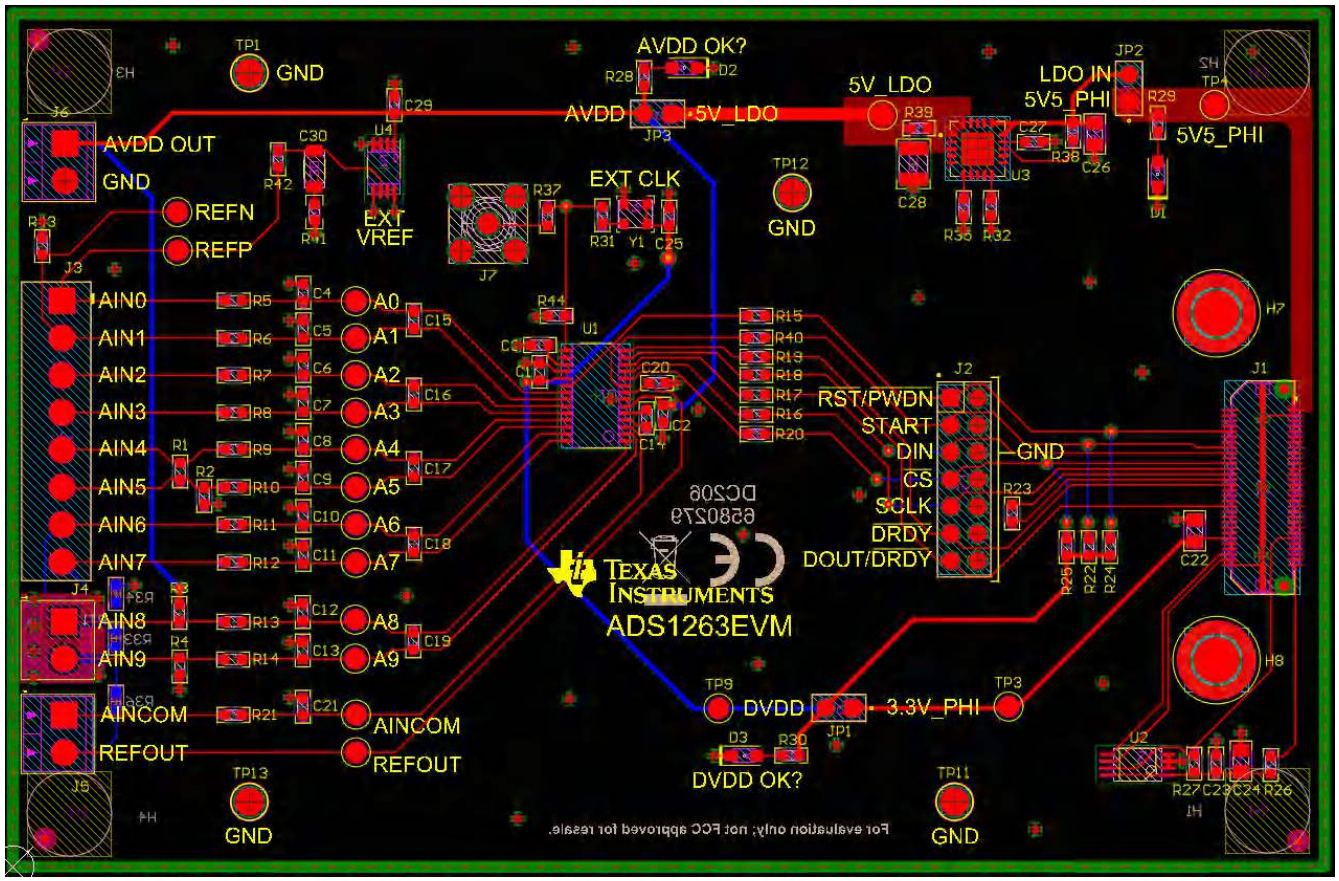

Figure 8-1. ADS1263EVM PCB Layout

8.3 Schematics

This section provides the schematics for the ADS1263EVM.

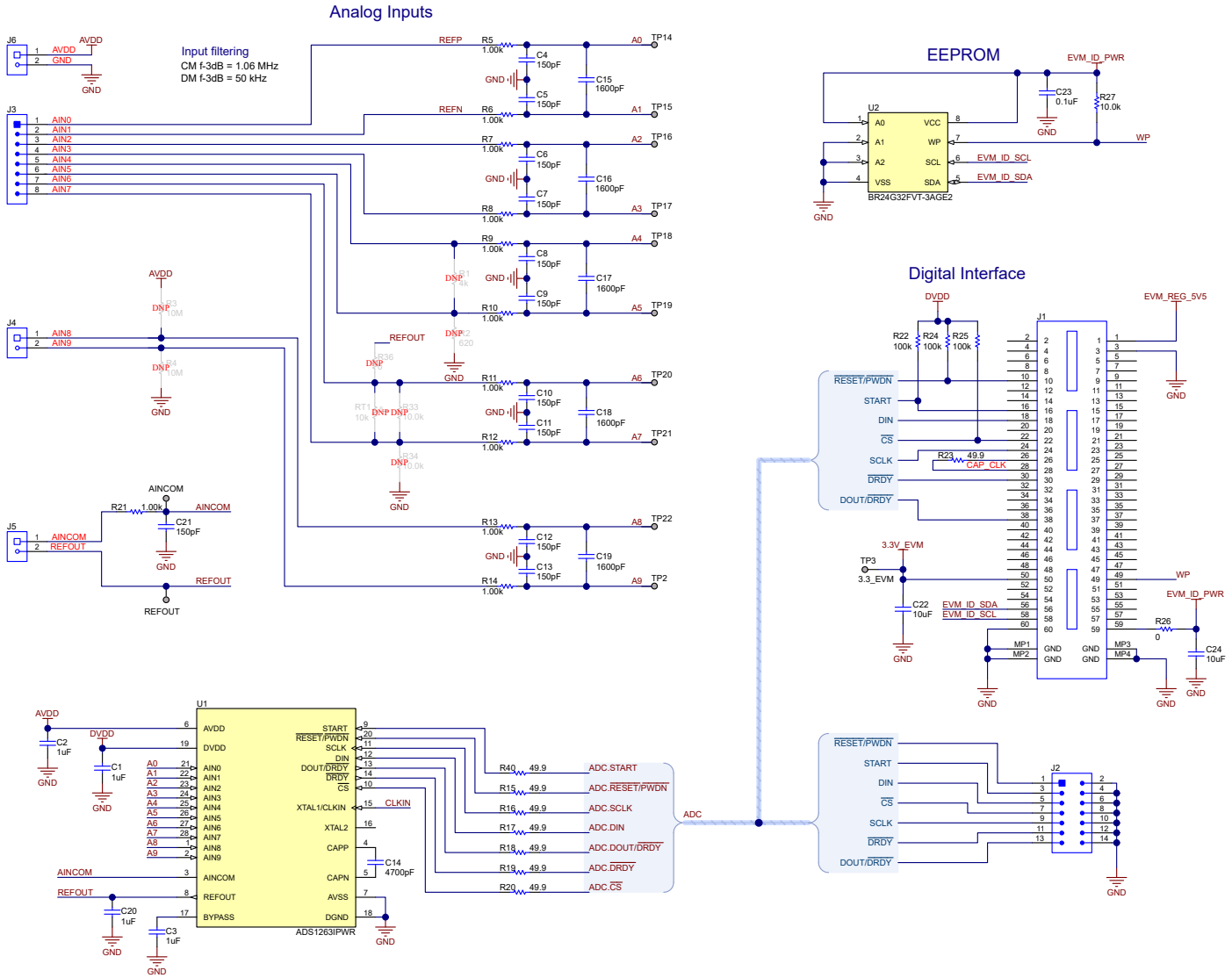

Figure 8-2. ADS1263EVM ADC, Analog Input, EEPROM, and Digital Interface Circuits

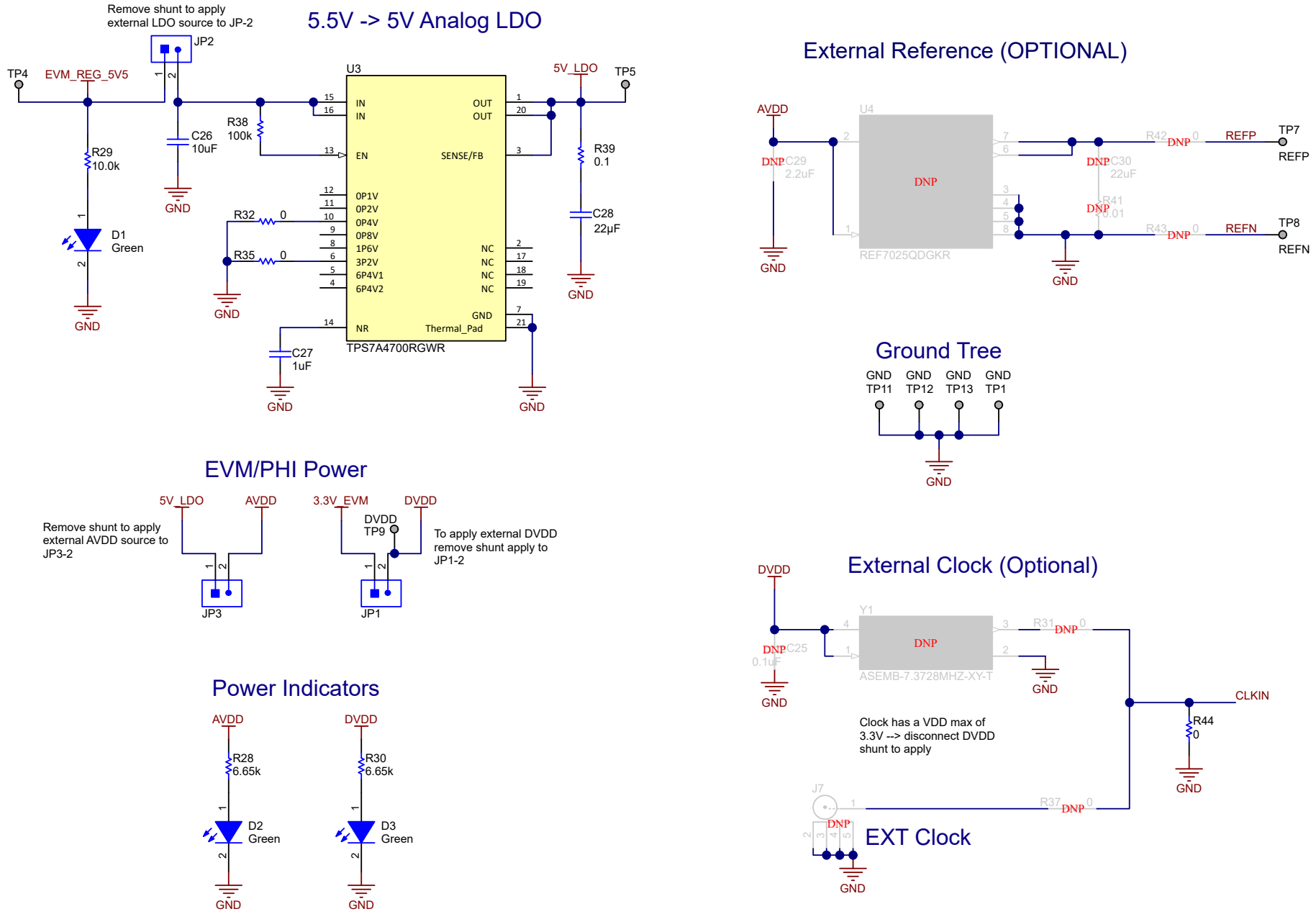

Figure 8-3. ADS1263EVM Power, Clock, and Voltage Reference Circuits

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2015) to Revision B (May 2023)	Page
• Changed entire document to reflect changes made in EVM moving to a new platform	3

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265