



## 54F/74F373 Octal Transparent Latch with TRI-STATE® Outputs

### General Description

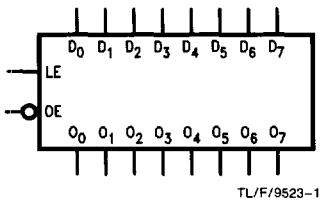
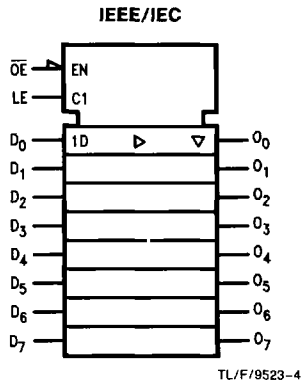
The 'F373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH the bus output is in the high impedance state.

### Features

- Eight latches in a single package
- TRI-STATE outputs for bus interfacing

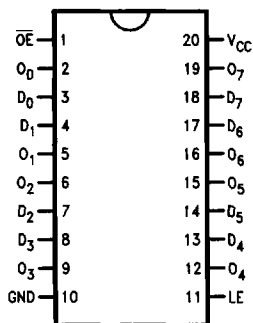
**Ordering Code:** See Section 5

### Logic Symbols

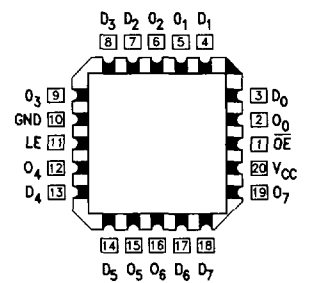


### Connection Diagrams

**Pin Assignment  
for DIP, SOIC and Flatpak**



**Pin Assignment  
for LCC and PCC**



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0$ - $D_7$	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
LE	Latch Enable Input (Active HIGH)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$O_0$ - $O_7$	TRI-STATE Latch Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

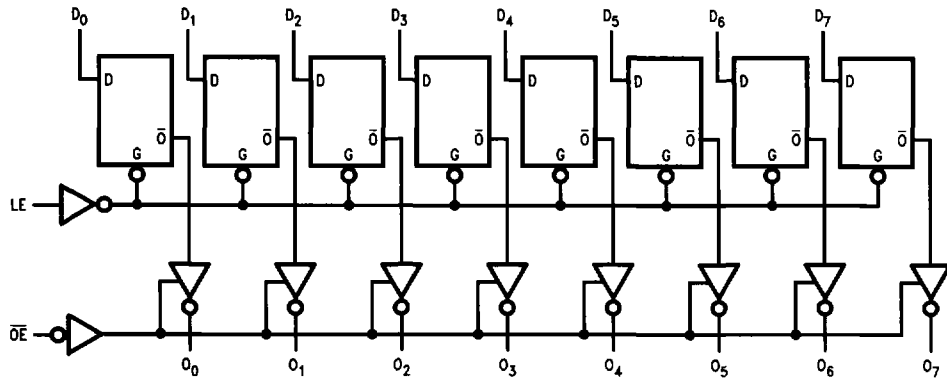
The 'F373 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

## Truth Table

Inputs			Output
LE	$\overline{OE}$	$D_n$	$O_n$
H	L	H	H
H	L	L	L
L	L	X	$O_n$ (no change)
X	H	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance State

## Logic Diagram



TL/F/9523-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LCW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEX</sub>	Output HIGH Leakage Current			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>CCZ</sub>	Power Supply Current		38	55	mA	Max	V <sub>O</sub> = HIGH Z

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig No
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $O_n$	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.5 7.0	3.0 2.0	8.0 6.0	ns	2-3
$t_{PLH}$ $t_{PHL}$	Propagation Delay LE to $O_n$	5.0 3.0	9.0 5.2	11.5 7.0	5.0 3.0	15.0 8.5	5.0 3.0	13.0 8.0	ns	2-3
$t_{PZH}$ $t_{PZL}$	Output Enable Time	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	13.5 10.0	2.0 2.0	12.0 8.5	ns	2-5
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time	1.5 1.5	4.5 3.8	6.5 5.0	1.5 1.5	10.0 7.0	1.5 1.5	7.5 6.0	ns	2-5

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig No
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $D_n$ to LE	2.0 2.0		2.0 2.0		2.0 2.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $D_n$ to LE	3.0 3.0		3.0 4.0		3.0 3.0			
$t_w(\text{H})$	LE Pulse Width, HIGH	6.0		6.0		6.0		ns	2-4