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Apacer Technology Inc.

CUSTOMER: 研華股份有限公司

APPROVAL SHEET

APPROVED NO.	**:**	**90004-T0014**
ISSUE DATE	**:**	**May-17-2012**
MODULE PART NO.	**:**	**78.B2GCJ.AF10C**
PCB PART NO.	**:**	**48.18220.091**
IC Brand	**:**	**Hynix**
DESCRIPTION	**:**	**DDR3 SODIMM 12800-11 256x8 4GB HYN G**

CUSTOMER APPROVAL :

Apacer Technology Inc.

Authorized by : Steven Wang

4GB DDR3 SDRAM SODIMM with SPD

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency	Density	Organization	Component Composition	Number of Rank
78.B2GCJ.AF10C	12.8GB/sec	1600Mbps	800MHz	CL11	4GB	512Mx64	256Mx8*16EA	2

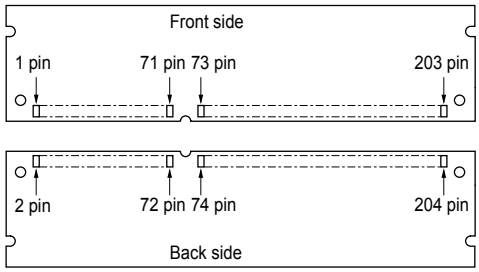
Specifications

- On Dimm Thermal Sensor: No
- Density: 4GB
- Organization
— 512M words · 64 bits, 2 ranks
- Mounting 16 pieces of 2G bits DDR3 SDRAM sealed in FBGA
- Package: 204-pin socket type small outline dual in line memory module (SO-DIMM)
— PCB height: 30.0mm
— Lead pitch: 0.6mm (pin)
— Lead-free (RoHS compliant)
- Power supply: VDD = 1.5V ± 0.075V
- Eight internal banks for concurrent operation (components)
- Interface: SSTL_15
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- /CAS Latency (CL): 6, 7, 8, 9, 10, 11
- /CAS write latency (CWL): 5, 6, 7, 8
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles
— Average refresh period
7.8∝s at 0°C ≤ TC ≤ +85°C
3.9∝s at +85°C < TC ≤ +95°C
- Operating case temperature range
— TC = 0°C to +95°C

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die-Termination (ODT) for better signal quality
— Synchronous ODT
— Dynamic ODT
— Asynchronous ODT
- Multi Purpose Register (MPR) for temperature read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
— Normal/extended
— Auto/manual self-refresh
- Programmable Output driver impedance control

Pin Configurations



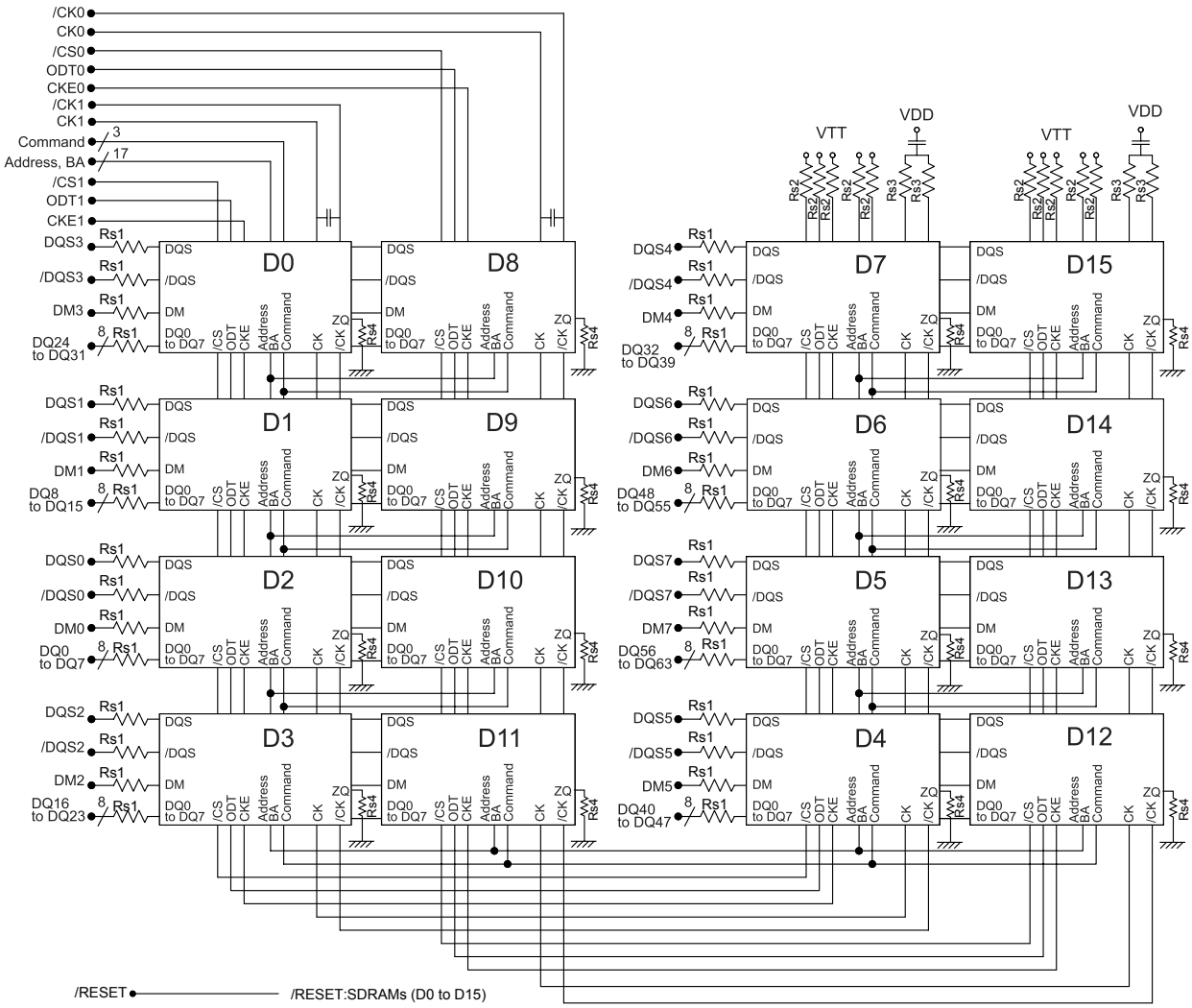
Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREFDQ	103	/CK0	2	VSS	104	/CK1
3	VSS	105	VDD	4	DQ4	106	VDD
5	DQ0	107	A10 (AP)	6	DQ5	108	BA1
7	DQ1	109	BA0	8	VSS	110	/RAS
9	VSS	111	VDD	10	/DQS0	112	VDD
11	DM0	113	/WE	12	DQS0	114	/CS0
13	VSS	115	/CAS	14	VSS	116	ODT0
15	DQ2	117	VDD	16	DQ6	118	VDD
17	DQ3	119	A13	18	DQ7	120	ODT1
19	VSS	121	/CS1	20	VSS	122	NC
21	DQ8	123	VDD	22	DQ12	124	VDD
23	DQ9	125	NC	24	DQ13	126	VREFCA
25	VSS	127	VSS	26	VSS	128	VSS
27	/DQS1	129	DQ32	28	DM1	130	DQ36
29	DQS1	131	DQ33	30	/RESET	132	DQ37
31	VSS	133	VSS	32	VSS	134	VSS
33	DQ10	135	/DQS4	34	DQ14	136	DM4
35	DQ11	137	DQS4	36	DQ15	138	VSS
37	VSS	139	VSS	38	VSS	140	DQ38
39	DQ16	141	DQ34	40	DQ20	142	DQ39
41	DQ17	143	DQ35	42	DQ21	144	VSS
43	VSS	145	VSS	44	VSS	146	DQ44
45	/DQS2	147	DQ40	46	DM2	148	DQ45
47	DQS2	149	DQ41	48	VSS	150	VSS
49	VSS	151	VSS	50	DQ22	152	/DQS5
51	DQ18	153	DM5	52	DQ23	154	DQS5
53	DQ19	155	VSS	54	VSS	156	VSS
55	VSS	157	DQ42	56	DQ28	158	DQ46
57	DQ24	159	DQ43	58	DQ29	160	DQ47
59	DQ25	161	VSS	60	VSS	162	VSS
61	VSS	163	DQ48	62	/DQS3	164	DQ52
63	DM3	165	DQ49	64	DQS3	166	DQ53
65	VSS	167	VSS	66	VSS	168	VSS
67	DQ26	169	/DQS6	68	DQ30	170	DM6

Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
69	DQ27	171	DQS6	70	DQ31	172	VSS
71	VSS	173	VSS	72	VSS	174	DQ54
73	CKE0	175	DQ50	74	CKE1	176	DQ55
75	VDD	177	DQ51	76	VDD	178	VSS
77	NC	179	VSS	78	NC	180	DQ60
79	BA2	181	DQ56	80	NC	182	DQ61
81	VDD	183	DQ57	82	VDD	184	VSS
83	A12 (/BC)	185	VSS	84	A11	186	/DQS7
85	A9	187	DM7	86	A7	188	DQS7
87	VDD	189	VSS	88	VDD	190	VSS
89	A8	191	DQ58	90	A6	192	DQ62
91	A5	193	DQ59	92	A4	194	DQ63
93	VDD	195	VSS	94	VDD	196	VSS
95	A3	197	SA0	96	A2	198	/EVENT
97	A1	199	VDDSPD	98	A0	200	SDA
99	VDD	201	SA1	100	VDD	202	SCL
101	CK0	203	VTT	102	CK1	204	VTT

Pin Description

Pin name	Function
A0 to A14	Address input Row address A0 to A14 Column address A0 to A9
A10 (AP)	Auto precharge
A12 (/BC)	Burst chop
BA0, BA1, BA2	Bank select address
DQ0 to DQ63	Data input/output
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/CS0, /CS1	Chip select
CKE0, CKE1	Clock enable
CK0, CK1	Clock input
/CK0, /CK1	Differential clock input
DQS0 to DQS7, /DQS0 to /DQS7	Input and output data strobe
DM0 to DM7	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0, SA1	Serial address input
VDD	Power for internal circuit
VDDSPD	Power for serial EEPROM
VREFCA	Reference voltage for CA
VREFDQ	Reference voltage for DQ
VSS	Ground
VTT	I/O termination supply for SDRAM
/RESET	Set DRAM to known state
ODT0, ODT1	ODT control
/EVENT	Temperature event pin
NC	No connection

Block Diagram

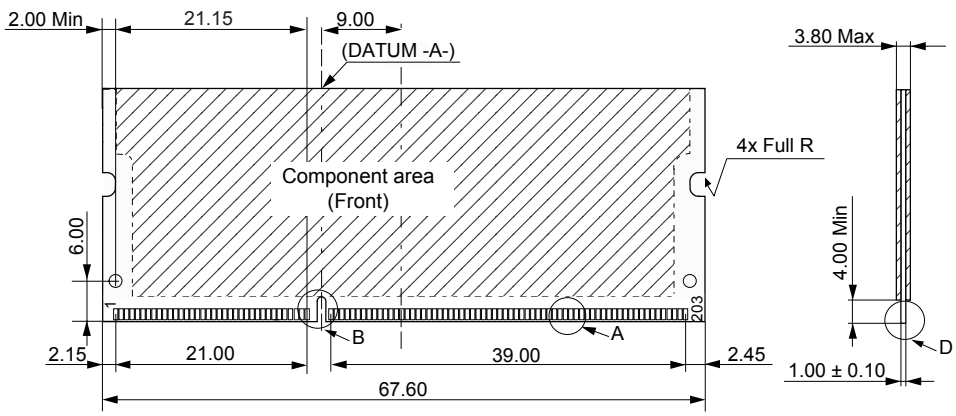


Notes :
1. DQ wiring may be changed within a byte.
2. DQ, DQS, /DQS, ODT, DM, CKE, /CS relationships must be maintained as shown.

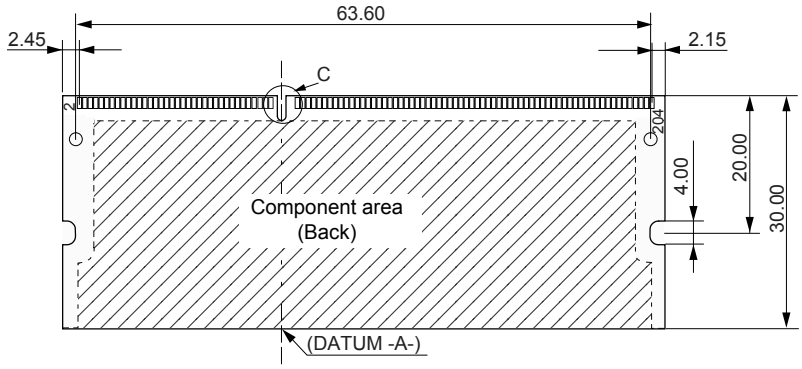
* D0 to D15: 2G bits DDR3 SDRAM
Address, BA: A0 to A14, BA0 to BA2
Command: /RAS, /CAS, /WE
U1: 256 bytes EEPROM
Rs1: 15Ω
Rs2: 36Ω
Rs3: 30Ω
Rs4: 240Ω

Unit: mm

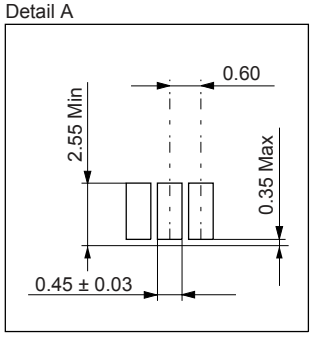
Front side



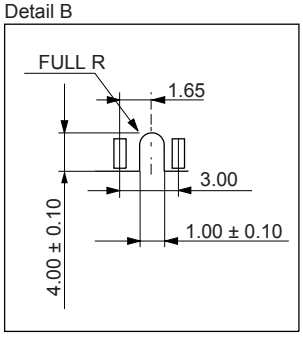
Back side



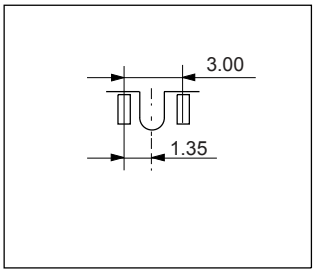
Detail A



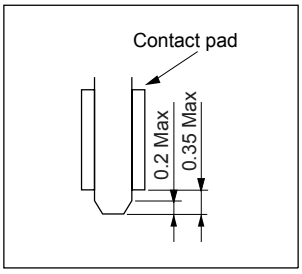
Detail B



Detail C



Detail D



(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)