19-4909; Rev 0; 10/09

EVALUATION KIT AVAILABLE

Low-Jitter, Wide Frequency Range, Programmable Clock Generator with 10 Outputs

MAX3637

General Description

The MAX3637 is a highly flexible, precision phase-locked loop (PLL) clock generator optimized for the next generation of network equipment that demands low-jitter clock generation and distribution for robust high-speed data transmission. The device features subpicosecond jitter generation, excellent power-supply noise rejection, and pin-programmable LVDS/LVPECL output interfaces. The MAX3637 provides nine differential outputs and one LVCMOS output, divided into three banks. The frequency and output interface of each output bank can be individually programmed, making this device an ideal replacement for multiple crystal oscillators and clock distribution ICs on a system board, saving cost and space.

This 3.3V IC is available in a 7mm x 7mm, 48-pin TQFN package and operates from -40°C to +85°C.

Applications

Ethernet Switch/Router	Fibre Channel SAN
Wireless Base Station	SONET Line Cards

Typical Application Circuits and Pin Configuration appear at end of data sheet.

Features

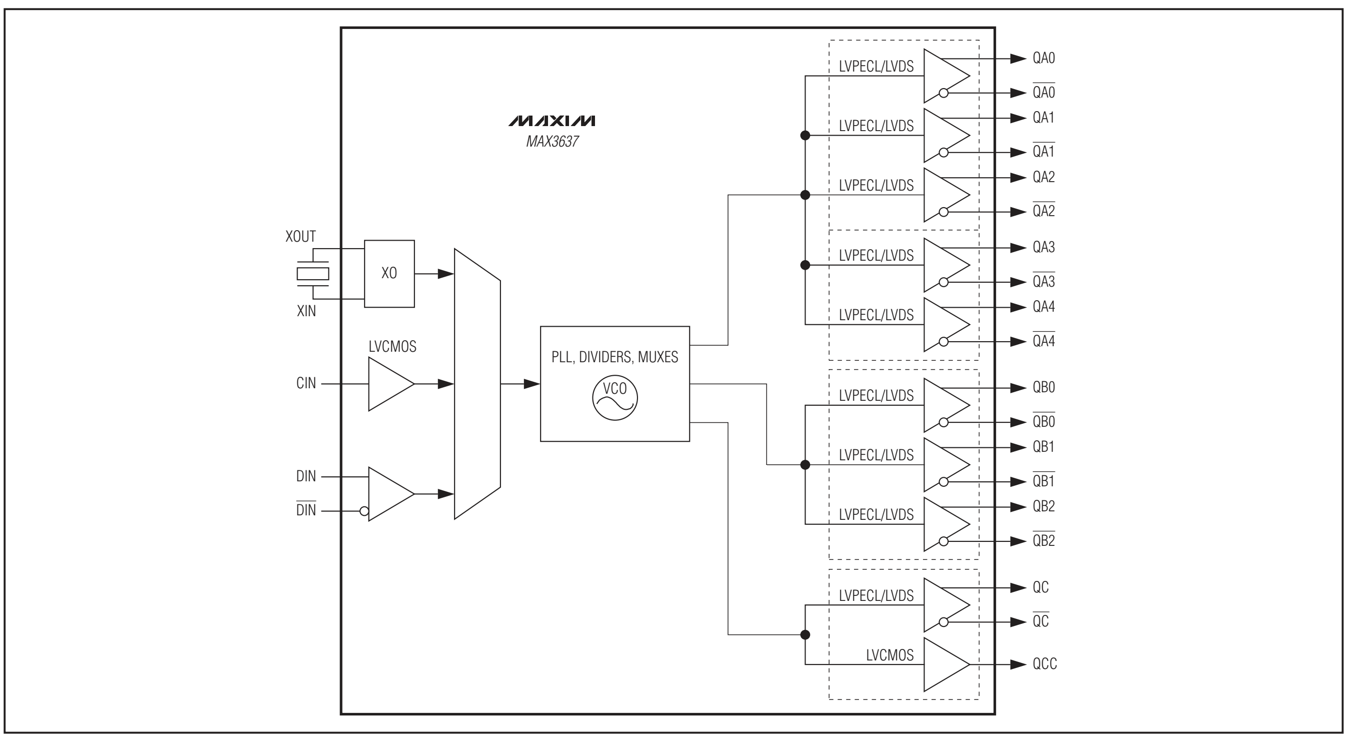
- **Inputs**
  - **Crystal Interface: 18MHz to 33.5MHz**
  - **LVCMOS Input: 15MHz to 160MHz**
  - **Differential Input: 15MHz to 350MHz**
- **Outputs**
  - **LVCMOS Output: Up to 160MHz**
  - **LVPECL/LVDS Outputs: Up to 800MHz**
- **Three Individual Output Banks**
  - **Pin-Programmable Dividers**
  - **Pin-Programmable Output Interface**
- **Wide VCO Tuning Range (3.60GHz to 3.83GHz)**
- **Low Phase Jitter**
  - **0.34ps$_{RMS}$ (12kHz to 20MHz)**
  - **0.14ps$_{RMS}$ (1.875MHz to 20MHz)**
- **Excellent Power-Supply Noise Rejection**
- **-40°C to +85°C Operating Temperature Range**
- **+3.3V Supply**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3637ETM+	-40°C to +85°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (V_{CC}, V_{CCA}, V_{CCQA}, V_{CCQB}, V_{CCQC}, V_{CCQCC}) ....-0.3V to +4.0V
Voltage Range at CIN, IN_SEL, DM, DF[1:0], DP, PLL_BP, DA[1:0], DB[1:0], DC[1:0], QA_CTRL1, QA_CTRL2, QB_CTRL, QC_CTRL, QCC, RES .... -0.3V to (V_{CC} + 0.3V)
Voltage Range at DIN, $\overline{DIN}$........ (V_{CC} - 2.35V) to (V_{CC} - 0.35V)
Voltage Range at QA[4:0], $\overline{QA[4:0]}$, QB[2:0], $\overline{QB[2:0]}$, QC, $\overline{QC}$ when LVDS Output... -0.3V to (V_{CC} + 0.3V)
Current into QA[4:0], $\overline{QA[4:0]}$, QB[2:0], $\overline{QB[2:0]}$, QC, $\overline{QC}$ when LVPECL Output .... -56mA
Current into QCC.. ±50mA
Voltage Range at XIN...-0.3V to +1.2V
Voltage Range at XOUT............................-0.3V to (V_{CC} - 0.6V)
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFN (derate 40mW/°C above +70°C)..........3200mW
Operating Junction Temperature Range .... -55°C to +150°C
Storage Temperature Range........................... -65°C to +160°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. Signal applied to CIN or DIN/$\overline{DIN}$ only when selected as the reference clock.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current with PLL Enabled (Note 2)	I_{CC}	Configured with LVPECL outputs		170	215	mA
		Configured with LVDS outputs		290	365	
Supply Current with PLL Bypassed (Note 2)		Configured with LVPECL outputs		110		mA
		Configured with LVDS outputs		230		
LVCMOS/LVTTL CONTROL INPUTS (IN_SEL, DM, DF[1:0], DA[1:0], DB[1:0], DC[1:0], PLL_BP, DP, QA_CTRL1, QA_CTRL2, QB_CTRL, QC_CTRL)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IN} = V_{CC}			80	µA
Input Low Current	I_{IL}	V_{IN} = 0V	-80			µA
LVCMOS/LVTTL CLOCK INPUT (CIN)						
Reference Clock Input Frequency	f_{REF}		15		160	MHz
Input Amplitude Range		Internally AC-coupled (Note 3)	1.2		3.6	V_{P-P}
Input High Current	I_{IH}	V_{IN} = V_{CC}			80	µA
Input Low Current	I_{IL}	V_{IN} = 0V	-80			µA
Reference Clock Input Duty-Cycle Distortion			40		60	%
Input Capacitance				1.5		pF
DIFFERENTIAL CLOCK INPUT (DIN, $\overline{DIN}$) (Note 4)						
Differential Input Frequency	f_{REF}		15		350	MHz
Input Bias Voltage	V_{CMI}		V_{CC} - 1.8	V_{CC} - 1.3		V
Input Differential Voltage Swing			150		1800	mV_{P-P}
Single-Ended Voltage Range			V_{CC} - 2.0		V_{CC} - 0.7	V
Input Differential Impedance			80	100	120	Ω
Differential Input Capacitance				1.5		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. Signal applied to CIN or DIN/$\overline{DIN}$ only when selected as the reference clock.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS OUTPUTS (QA[4:0], $\overline{QA[4:0]}$, QB[2:0], $\overline{QB[2:0]}$, QC, $\overline{QC}$) (Note 5)						
Output Frequency					800	MHz
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage	$\vert V_{OD}\vert$		250		400	mV
Change in Magnitude of Differential Output for Complementary States	$\Delta\vert V_{OD}\vert$				25	mV
Output Offset Voltage	V_{OS}		1.125		1.3	V
Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\vert V_{OS}\vert$				25	mV
Differential Output Impedance			80	100	140	Ω
Output Current		Short together		3		mA
		Short to ground		6		
Output Current When Disabled		$V_{Q\_\_} = V_{\overline{Q\_\_}}$ = 0V to V_{CC}		10		µA
Output Rise/Fall Time		20% to 80%		160	240	ps
Output Duty-Cycle Distortion		PLL enabled	48	50	52	%
		PLL bypassed (Note 6)		50		
LVPECL OUTPUTS (QA[4:0], $\overline{QA[4:0]}$, QB[2:0], $\overline{QB[2:0]}$, QC, $\overline{QC}$) (Note 7)						
Output Frequency					800	MHz
Output High Voltage	V_{OH}		V_{CC} - 1.13	V_{CC} - 0.98	V_{CC} - 0.83	V
Output Low Voltage	V_{OL}		V_{CC} - 1.85	V_{CC} - 1.70	V_{CC} - 1.55	V
Output-Voltage Swing (Single-Ended)			0.5	0.7	0.9	V_{P-P}
Output Current When Disabled		V_O = 0V to V_{CC}		10		µA
Output Rise/Fall Time		20% to 80%, differential load = 100Ω		140	240	ps
Output Duty-Cycle Distortion		PLL enabled	48	50	52	%
		PLL bypassed (Note 6)		50		
LVCMOS/LVTTL OUTPUT (QCC)						
Output Frequency					160	MHz
Output High Voltage		I_{OH} = -12mA	2.6		V_{CC}	V
Output Low Voltage		I_{OL} = 12mA			0.4	V
Output Rise/Fall Time		20% to 80% (Note 8)	150	400	850	ps
Output Duty-Cycle Distortion		PLL enabled	42	50	58	%
		PLL bypassed (Note 6)		50		
Output Impedance				15		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. Signal applied to CIN or DIN/$\overline{DIN}$ only when selected as the reference clock.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PLL SPECIFICATIONS							
VCO Frequency Range	f_{VCO}			3600	3750	3830	MHz
Phase-Frequency Detector Compare Frequency	f_{PFD}			15		42	MHz
PLL Jitter Transfer Bandwidth					130		kHz
Integrated Phase Jitter	RJ	25MHz crystal input (Note 9)	12kHz to 20MHz		0.34	1.0	ps_{RMS}
			1.875MHz to 20MHz		0.14		
		25MHz LVCMOS or differential input (Notes 9, 10)			0.34		
Supply-Noise Induced Phase Spur at LVPECL/LVDS Output		(Note 11)			-56		dBc
Supply-Noise Induced Phase Spur at LVCMOS Output		(Note 11)			-45		dBc
Determinisitic Jitter Induced by Power-Supply Noise		LVPECL or LVDS (Note 11)			6		ps_{P-P}
Nonharmonic and Subharmonic Spurs		(Note 12)			-70		dBc
SSB Phase Noise at 622.08MHz		f_{OFFSET} = 1kHz			-109		dBc/Hz
		f_{OFFSET} = 10kHz			-112		
		f_{OFFSET} = 100kHz			-118		
		f_{OFFSET} = 1MHz			-134		
		f_{OFFSET} ≥ 10MHz			-146		
SSB Phase Noise at 212.5MHz		f_{OFFSET} = 1kHz			-119		dBc/Hz
		f_{OFFSET} = 10kHz			-121		
		f_{OFFSET} = 100kHz			-127		
		f_{OFFSET} = 1MHz			-143		
		f_{OFFSET} ≥ 10MHz			-151		
SSB Phase Noise at 156.25MHz		f_{OFFSET} = 1kHz			-122		dBc/Hz
		f_{OFFSET} = 10kHz			-123		
		f_{OFFSET} = 100kHz			-129		
		f_{OFFSET} = 1MHz			-145		
		f_{OFFSET} ≥ 10MHz			-152		
SSB Phase Noise at 125MHz		f_{OFFSET} = 1kHz			-123		dBc/Hz
		f_{OFFSET} = 10kHz			-124		
		f_{OFFSET} = 100kHz			-130		
		f_{OFFSET} = 1MHz			-147		
		f_{OFFSET} ≥ 10MHz			-153		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. Signal applied to CIN or DIN/$\overline{DIN}$ only when selected as the reference clock.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SSB Phase Noise at 62.5MHz		f_{OFFSET} = 1kHz		-129		dBc/Hz
		f_{OFFSET} = 10kHz		-130		
		f_{OFFSET} = 100kHz		-137		
		f_{OFFSET} = 1MHz		-152		
		f_{OFFSET} ≥ 10MHz		-156		

Note 1: A series resistor of up to 10.5Ω is allowed between V_{CC} and V_{CCA} for filtering supply noise when system power-supply tolerance is V_{CC} = 3.3V ±5%. See Figure 3.
Note 2: Measured with all outputs enabled and unloaded.
Note 3: CIN can be AC- or DC-coupled. See Figure 8. Input high voltage must be ≤ V_{CC} + 0.3V.
Note 4: DIN can be AC- or DC-coupled. See Figure 10.
Note 5: Measured with 100Ω differential load.
Note 6: Measured with crystal input, or with 50% duty cycle LVCMOS or differential input.
Note 7: Measured with output termination of 50Ω to V_{CC} - 2V or Thevenin equivalent.
Note 8: Measured with a series resistor of 33Ω to a load capacitance of 3.0pF. See Figure 1.
Note 9: Measured at 156.25MHz output.
Note 10: Measured using LVCMOS/LVTTL input with slew rate ≥ 1.0V/ns, or differential input with slew rate ≥ 0.5V/ns.
Note 11: Measured at 156.25MHz output with 200kHz, 50mV_{P-P} sinusoidal signal on the supply using the crystal input and the power-supply filter shown in Figure 3. See the *Typical Operating Characteristics* for other supply noise frequencies. Deterministic jitter is calculated from the measured power-supply-induced spurs. For more information, refer to Application Note 4461: *HFAN-04.5.5: Characterizing Power-Supply Noise Rejection in PLL Clock Synthesizers*.
Note 12: Measured with all outputs enabled and all three banks at different frequencies.

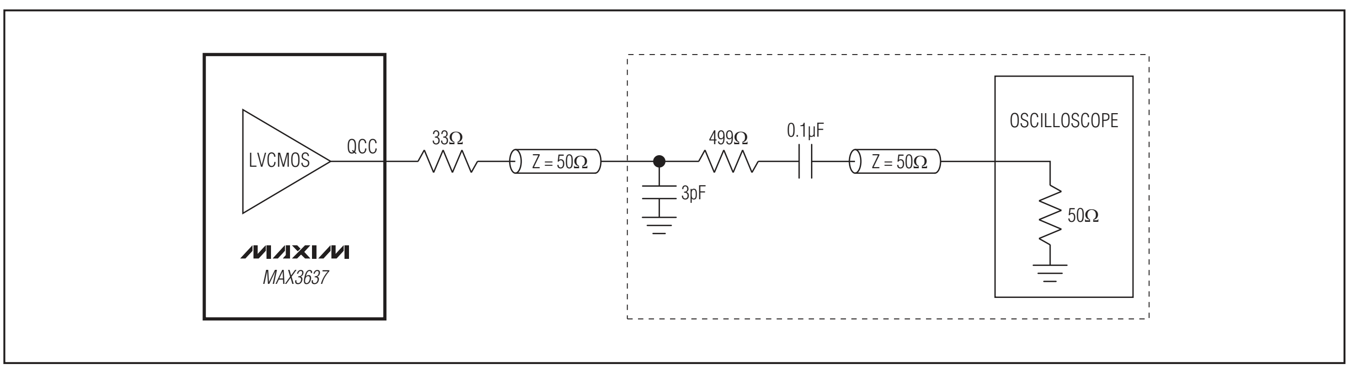


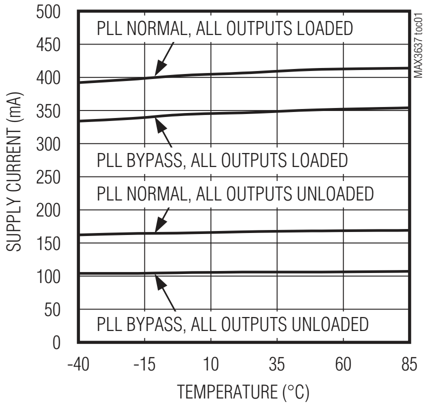
Figure 1. LVCMOS Output Measurement Setup

Low-Jitter, Wide Frequency Range, Programmable Clock Generator with 10 Outputs

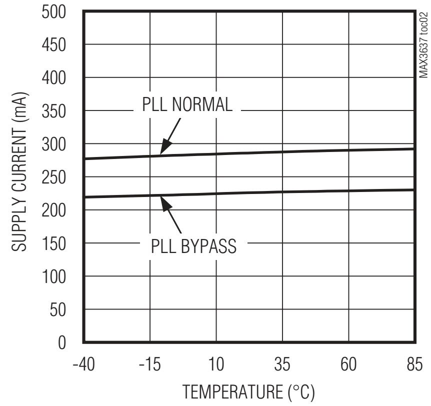
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

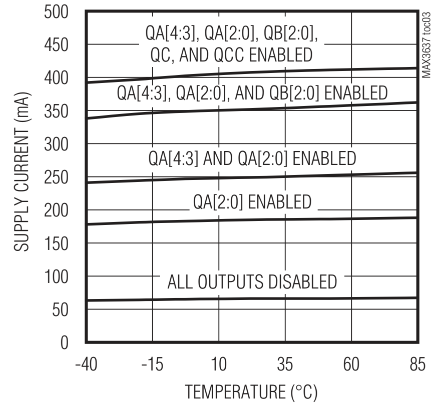
SUPPLY CURRENT vs. TEMPERATURE (LVPECL OUTPUTS, ALL ENABLED)



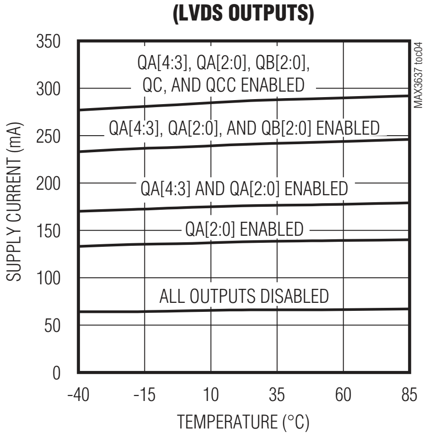
SUPPLY CURRENT vs. TEMPERATURE (LVDS OUTPUTS, ALL ENABLED)



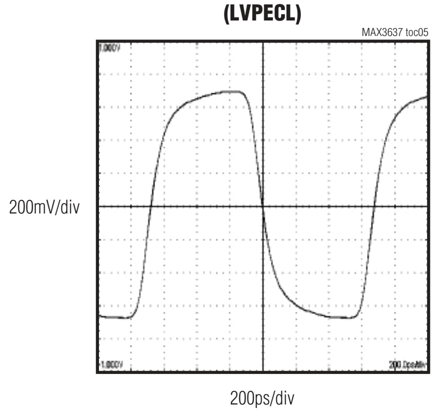
SUPPLY CURRENT vs. TEMPERATURE (LVPECL OUTPUTS, ALL LOADED)



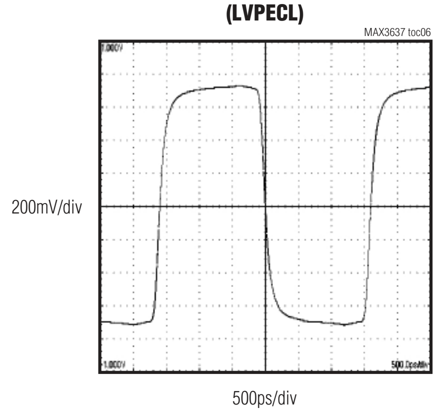
SUPPLY CURRENT vs. TEMPERATURE (LVDS OUTPUTS)



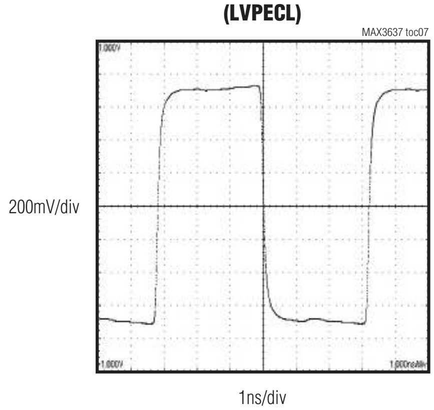
DIFFERENTIAL OUTPUT AT 737.28MHz (LVPECL)



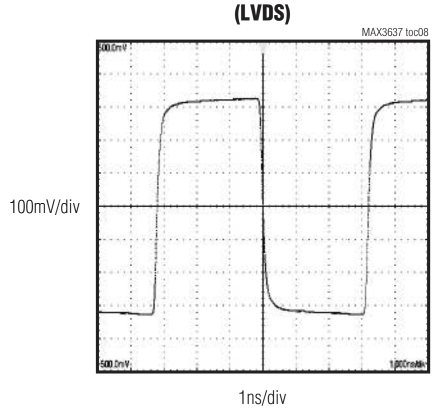
DIFFERENTIAL OUTPUT AT 312.5MHz (LVPECL)



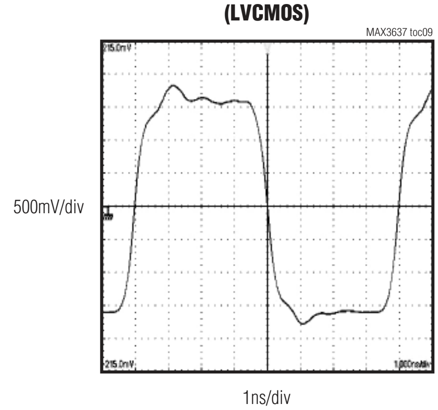
DIFFERENTIAL OUTPUT AT 156.25MHz (LVPECL)



DIFFERENTIAL OUTPUT AT 156.25MHz (LVDS)



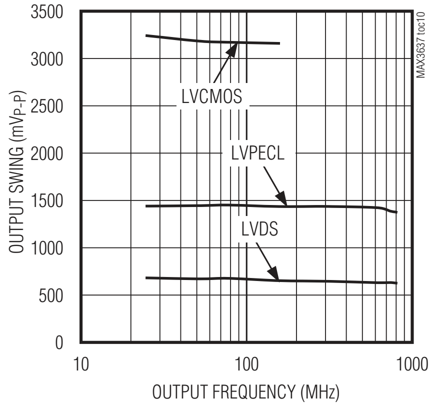
QCC OUTPUT AT 125MHz (LVCMOS)



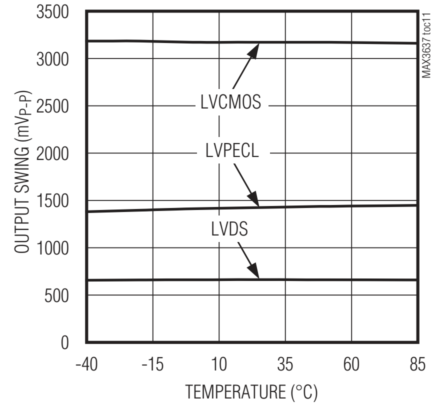
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

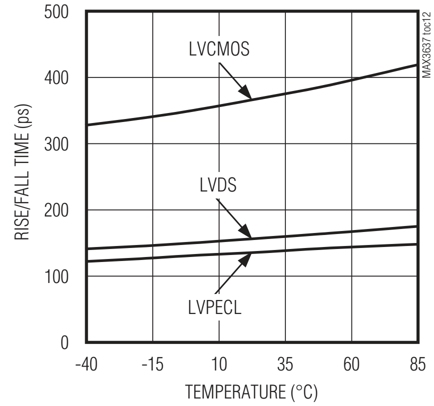
OUTPUT SWING vs. OUTPUT FREQUENCY



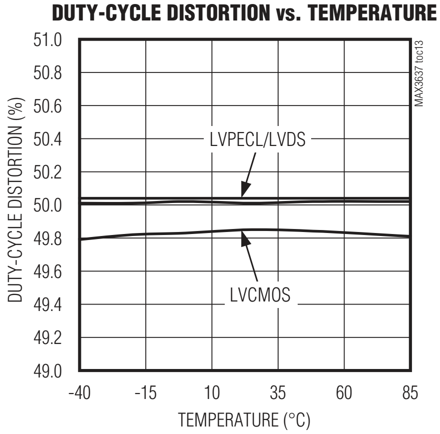
OUTPUT SWING vs. TEMPERATURE



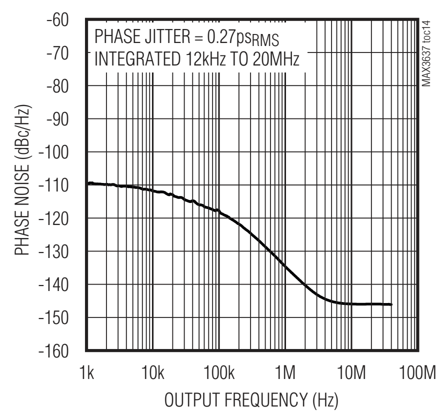
RISE/FALL TIME vs. TEMPERATURE (20% TO 80%)



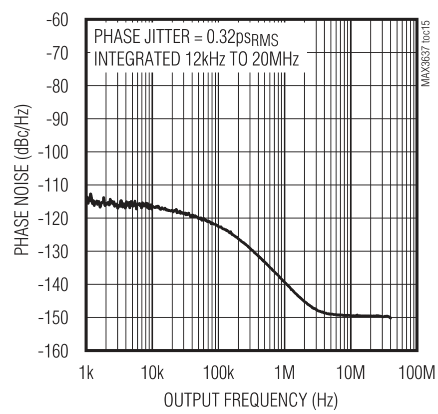
DUTY-CYCLE DISTORTION vs. TEMPERATURE



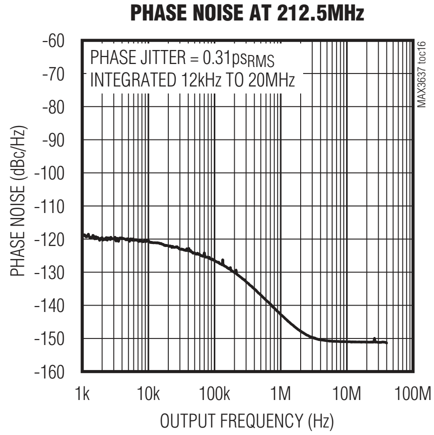
PHASE NOISE AT 622.08MHz



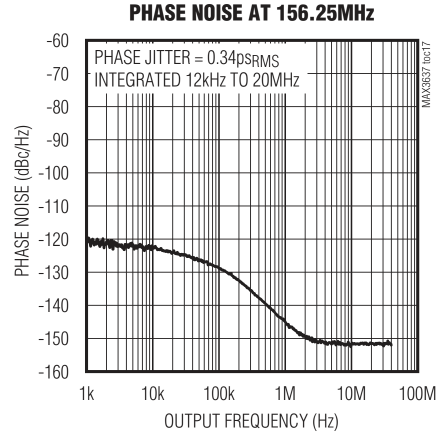
PHASE NOISE AT 312.5MHz



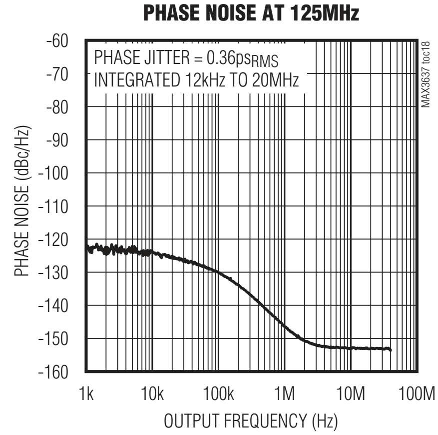
PHASE NOISE AT 212.5MHz



PHASE NOISE AT 156.25MHz



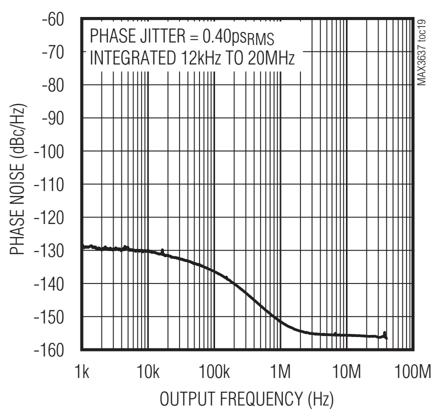
PHASE NOISE AT 125MHz



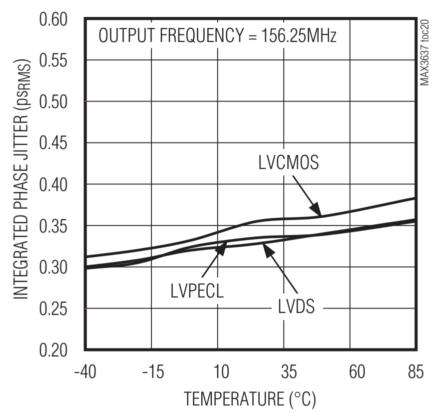
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

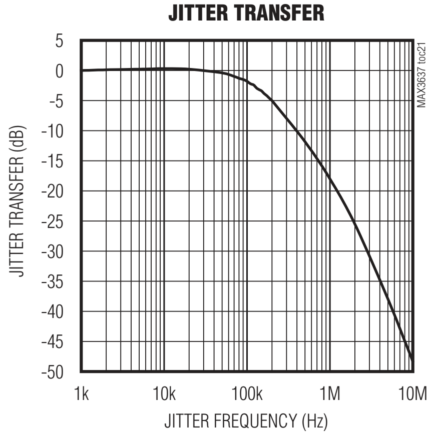
PHASE NOISE AT 62.5MHz



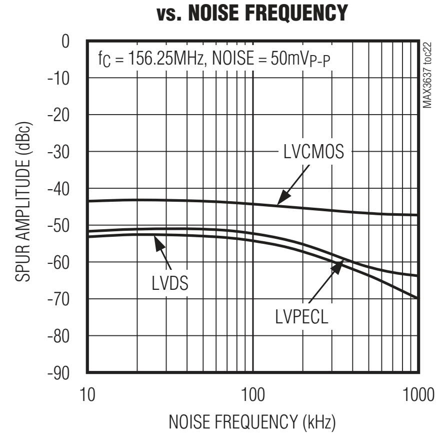
INTEGRATED PHASE JITTER (12kHz TO 20MHz) vs. TEMPERATURE



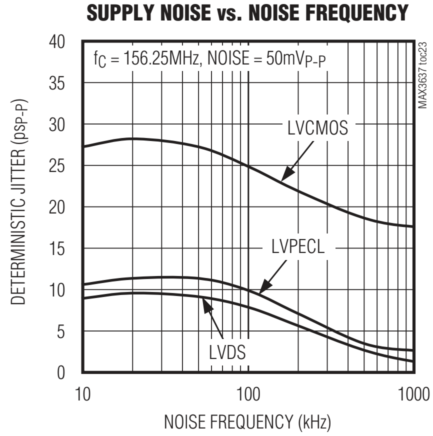
JITTER TRANSFER



SPURS INDUCED BY POWER-SUPPLY NOISE vs. NOISE FREQUENCY



DETERMINISTIC JITTER INDUCED BY POWER-SUPPLY NOISE vs. NOISE FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	DM	LVCMOS/LVTTL Input. Three-level control for input divider M. See Table 3.
2	XIN	Crystal Oscillator Input
3	XOUT	Crystal Oscillator Output
4	V_{CC}	Core Power Supply. Connect to +3.3V.
5	IN_SEL	LVCMOS/LVTTL Input. Three-level control for input mux. See Table 1.
6	PLL_BP	LVCMOS/LVTTL Input. Three-level control for PLL bypass mode. See Table 2.
7, 8	DF1, DF0	LVCMOS/LVTTL Inputs. Three-level controls for feedback divider F. See Table 4.
9	QC_CTRL	LVCMOS/LVTTL Input. Three-level control input for C-bank output interface. See Table 10.
10	V_{CCA}	Power Supply for Internal Voltage-Controlled Oscillators (VCOs). See Figure 3.
11	RES	Reserved. Connect to GND for normal operation.
12	DP	LVCMOS/LVTTL Input. Three-level control for prescale divider P. See Table 7.
13, 14	DB1, DB0	LVCMOS/LVTTL Inputs. Three-level controls for output divider B. See Table 5.
15, 16	DA1, DA0	LVCMOS/LVTTL Inputs. Three-level controls for output divider A. See Table 5.
17, 18	DC1, DC0	LVCMOS/LVTTL Inputs. Three-level controls for output divider C. See Table 6.
19	QA_CTRL2	LVCMOS/LVTTL Input. Three-level control for QA[4:3] output interface. See Table 8.
20	V_{CCQCC}	Power Supply for QCC Output. Connect to +3.3V.
21	QCC	C-Bank LVCMOS Clock Output
22, 23	$\overline{QC}$, QC	C-Bank Differential Output. Configured as LVPECL or LVDS with the QC_CTRL pin.
24	V_{CCQC}	Power Supply for C-Bank Differential Output. Connect to +3.3V.
25, 36	V_{CCQA}	Power Supply for A-Bank Differential Outputs. Connect to +3.3V.
26, 27	$\overline{QA4}$, QA4	A-Bank Differential Output. Configured as LVPECL or LVDS with the QA_CTRL2 pin.
28, 29	$\overline{QA3}$, QA3	A-Bank Differential Output. Configured as LVPECL or LVDS with the QA_CTRL2 pin.
30, 31	$\overline{QA2}$, QA2	A-Bank Differential Output. Configured as LVPECL or LVDS with the QA_CTRL1 pin.
32, 33	$\overline{QA1}$, QA1	A-Bank Differential Output. Configured as LVPECL or LVDS with the QA_CTRL1 pin.
34, 35	$\overline{QA0}$, QA0	A-Bank Differential Output. Configured as LVPECL or LVDS with the QA_CTRL1 pin.
37	V_{CCQB}	Power Supply for B-Bank Differential Outputs. Connect to +3.3V.
38, 39	$\overline{QB0}$, QB0	B-Bank Differential Output. Configured as LVPECL or LVDS with the QB_CTRL pin.
40, 41	$\overline{QB1}$, QB1	B-Bank Differential Output. Configured as LVPECL or LVDS with the QB_CTRL pin.
42, 43	$\overline{QB2}$, QB2	B-Bank Differential Output. Configured as LVPECL or LVDS with the QB_CTRL pin.
44	QA_CTRL1	LVCMOS/LVTTL Input. Three-level control for QA[2:0] output interface. See Table 8.
45	QB_CTRL	LVCMOS/LVTTL Input. Three-level control for B-bank output interface. See Table 9.
46, 47	$\overline{DIN}$, DIN	Differential Clock Input. Operates up to 350MHz. This input can accept DC-coupled LVPECL signals, and is internally biased to accept AC-coupled LVDS, CML, and LVPECL signals.
48	CIN	LVCMOS Clock Input. Operates up to 160MHz.
—	EP	Exposed Pad. Connect to supply ground for proper electrical and thermal performance.

Low-Jitter, Wide Frequency Range, Programmable Clock Generator with 10 Outputs

Detailed Description

The MAX3637 is a low-jitter clock generator designed to operate over a wide range of frequencies. It consists of a selectable reference clock (on-chip crystal oscillator, LVCMOS input, or differential input), PLL with on-chip VCO, pin-programmable dividers and muxes, and three banks of clock outputs. See Figure 2. The output banks include nine pin-programmable LVDS/LVPECL output buffers and one LVCMOS output buffer. The frequency, enabling, and output interface of each output bank can be individually programmed. In addition the A-bank is split into two banks with programmable enabling and

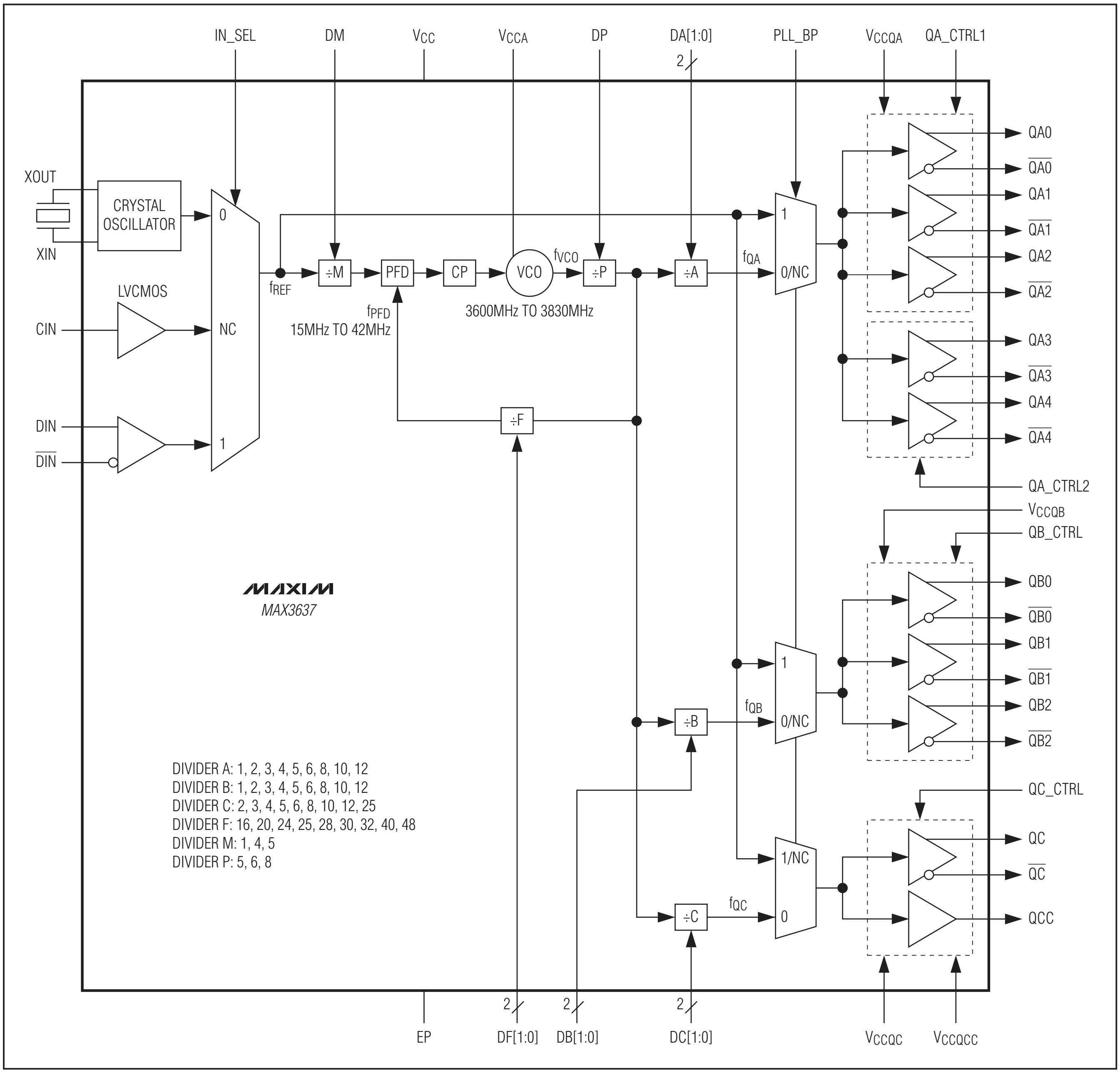


Figure 2. Detailed Functional Diagram

output interface. A PLL bypass mode is also available for system testing or clock distribution.

Crystal Oscillator

The on-chip crystal oscillator provides the low-frequency reference clock for the PLL. This oscillator requires an external crystal connected between XIN and XOUT. See the *Crystal Selection and Layout* section for more information. The XIN and XOUT pins can be left open if not used.

LVCMOS Clock Input

An LVCMOS-compatible clock source can be connected to CIN to serve as the PLL reference clock. The input is internally biased to allow AC- or DC-coupling (see the *Applications Information* section). It is designed to operate from 15MHz to 160MHz. No signal should be applied to CIN if not used.

Differential Clock Input

A differential clock source can be connected to DIN to serve as the PLL reference clock. This input operates from 15MHz to 350MHz and contains an internal 100Ω differential termination. This input can accept DC-coupled LVPECL signals, and is internally biased to accept AC-coupled LVDS, CML, and LVPECL signals (see the *Applications Information* section). No signal should be applied to DIN if not used.

Phase-Locked Loop (PLL)

The PLL takes the signal from the crystal oscillator, LVCMOS clock input, or differential clock input and synthesizes a low-jitter, high-frequency clock. The PLL contains a phase-frequency detector (PFD), a charge pump (CP), and a low phase noise VCO with a wide 3.60GHz to 3.83GHz frequency range. The high-frequency VCO output is divided by prescale divider P, then is connected to the PFD input through a feedback divider. The PFD compares the reference frequency to the divided-down VCO output and generates a control signal that keeps the VCO locked to the reference clock. The high-frequency VCO/P output clock is sent to the output dividers. To minimize noise-induced jitter, the VCO supply (V_{CCA}) is isolated from the core logic and output buffer supplies.

Dividers and Muxes

The dividers and muxes are set with three-level control inputs. Leakage in the NC case must be less than 1µA. Divider settings and routing information are given in Tables 1 to 7. See Table 11 for example divider configurations used in various applications.

Table 1. PLL Input

IN_SEL	INPUT
0	Crystal Input. XO circuit is disabled when not selected.
1	Differential Input. No signal should be applied to DIN if not selected.
NC	LVCMOS Input. No signal should be applied to CIN if not selected.

Table 2. PLL Bypass

PLL_BP	PLL OPERATION
0	PLL Enabled for Normal Operation. All outputs from the A, B, and C banks are derived from the VCO.
1	PLL Bypassed. Selected input passes directly to the outputs. The VCO is disabled to minimize power consumption and intermodulation spurs. Used for system testing or clock distribution.
NC	The outputs from A-bank and B-bank are derived from the VCO, but the C-bank outputs are directly driven from the input signal for purposes of daisy chaining.

Low-Jitter, Wide Frequency Range, Programmable Clock Generator with 10 Outputs

Table 3. Input Divider M

DM	M DIVIDER RATIO
0	÷1
1	÷5
NC	÷4

Note: *When the on-chip XO is selected (IN_SEL = 0), the setting DM = 0 is required.*

Table 4. PLL Feedback Divider F

DF1	DF0	F DIVIDER RATIO
0	0	÷25
0	1	÷20
1	0	÷16
1	1	÷32
1	NC	÷24
NC	1	÷30
0	NC	÷40
NC	0	÷48
NC	NC	÷28

Table 5. Output Divider A, B

DA1/DB1	DA0/DB0	A, B DIVIDER RATIO
0	0	÷2
0	1	÷3
1	0	÷4
1	1	÷5
1	NC	÷6
NC	1	÷8
0	NC	÷10
NC	0	÷12
NC	NC	÷1

Table 6. Output Divider C

DC1	DC0	C DIVIDER RATIO
0	0	÷2
0	1	÷3
1	0	÷4
1	1	÷5
1	NC	÷6
NC	1	÷8
0	NC	÷10
NC	0	÷12
NC	NC	÷25

Table 7. Prescale Divider P

DP	P DIVIDER RATIO
0	÷5
1	÷6
NC	÷8

Table 8. A-Bank Output Interface

QA_CTRL1	QA[2:0] OUTPUT
0	QA[2:0] = LVDS
1	QA[2:0] = LVPECL
NC	QA[2:0] disabled to high impedance
QA_CTRL2	**QA[4:3] OUTPUT**
0	QA[4:3] = LVDS
1	QA[4:3] = LVPECL
NC	QA[4:3] disabled to high impedance

Table 9. B-Bank Output Interface

QB_CTRL	QB[2:0] OUTPUT
0	QB[2:0] = LVDS
1	QB[2:0] = LVPECL
NC	QB[2:0] disabled to high impedance

Table 10. C-Bank Output Interface

QC_CTRL	QC AND QCC OUTPUT
0	QC = LVDS, QCC = LVCMOS
1	QC = LVPECL, QCC = LVCMOS
NC	QC and QCC disabled to high impedance

LVDS/LVPECL Clock Outputs

The differential clock outputs (QA[4:0], QB[2:0], QC) operate up to 800MHz and have a pin-programmable LVDS/LVPECL output interface. See Tables 8 to 10. When configured as LVDS, the buffers are designed to drive transmission lines with a 100Ω differential termination. When configured as LVPECL, the buffers are designed to drive transmission lines terminated with 50Ω to V_{CC} - 2V. Unused output banks can be disabled to high impedance and unused outputs can be left open.

LVCMOS Clock Output

The LVCMOS clock output operates up to 160MHz and is designed to drive a single-ended high-impedance load. If unused, this output can be left open or the C-bank can be disabled to high impedance.

Internal Reset

During power-on, a power-on reset (POR) signal is generated to synchronize all dividers. A reset signal is also generated if any control pin is changed. Outputs within a bank are phase aligned, but outputs bank-to-bank may not be phase aligned.

Applications Information

Output Frequency Configuration

The MAX3637 output frequencies (f_{QA}, f_{QB}, f_{QC}) are functions of the reference frequency (f_{REF}) and the pin-programmable dividers (A, B, C, F, M). The relationships can be expressed as:

$$f_{QA} = \frac{f_{REF}}{M} \times \frac{F}{A} \qquad (1)$$

$$f_{QB} = \frac{f_{REF}}{M} \times \frac{F}{B} \qquad (2)$$

$$f_{QC} = \frac{f_{REF}}{M} \times \frac{F}{C} \qquad (3)$$

The frequency ranges for the selected reference clocks are 18MHz to 33.5MHz for the crystal oscillator input, 15MHz to 160MHz for the LVCMOS input, and 15MHz to 350MHz for the differential input. The available dividers are given in Tables 3 to 6.

For a given reference frequency f_{REF}, the input divider M, the PLL feedback divider F, and VCO prescale divider P must be configured so the VCO frequency (f_{VCO}) falls within the specified ranges. Invalid PLL configuration leads to VCO frequencies beyond the specified ranges and can result in loss of lock. An expression for the VCO frequency along with the specified ranges is given by:

$$f_{VCO} = \frac{f_{REF}}{M} \times F \times P \qquad (4)$$

$$3600\text{MHz} \le f_{VCO} \le 3830\text{MHz} \quad (5)$$

The prescale divider P is set by DP as given in Table 7.

In addition, the reference clock frequency and input divider M must also be selected so the PFD compare frequency (f_{PFD}) falls within the specified range of 15MHz to 42MHz. If applicable, the higher f_{PFD} should be selected for optimal jitter performance.

$$f_{PFD} = \frac{f_{REF}}{M} = \frac{f_{VCO}}{P \times F} \qquad (6)$$

$$15\text{MHz} \le f_{PFD} \le 42\text{MHz} \quad (7)$$

Note that the reference clock frequency is not limited by the f_{PFD} range when the PLL is in bypass mode.

Example Frequency Configuration

The following is an example of how to find divider ratios for a valid PLL configuration, given a requirement of input and output frequencies.

1) Select input and output frequencies for system clocking.

   f_{REF} = 25MHz

   f_{QA} = 312.5MHz

   f_{QB} = 156.25MHz

   f_{QC} = 125MHz

2) Find the input divider M for a valid PFD compare frequency. Using Table 3 and equations (6) and (7), it is determined that M = ÷1 is the only valid option.
3) Find the feedback divider F and prescale divider P for a valid f_{VCO}. Using Tables 4 and 7 along with equations (4) and (5), it is determined that F = ÷25 and P = ÷6 results in f_{VCO} = 3750MHz, which is within the valid range of the low VCO.
4) Find the output dividers A, B, C for the required output frequencies. Using Tables 5 and 6 and equations (1), (2), and (3), it is determined that A = ÷2 gives f_{QA} = 312.5MHz, B = ÷4 gives f_{QB} = 156.25MHz, and C = ÷5 gives f_{QC} = 125MHz.

Table 11 provides input and output frequencies along with valid divider ratios for a variety of applications.

Low-Jitter, Wide Frequency Range, Programmable Clock Generator with 10 Outputs

Table 11. Reference Frequencies and Divider Ratios for Various Applications

f_{REF} (MHz)	INPUT DIVIDER (M)	PLL FEEDBACK DIVIDER (F)	VCO FREQUENCY (MHz)	VCO PRESCALE DIVIDER (P)	OUTPUT DIVIDER (A, B, C)	OUTPUT FREQUENCY (MHz)	APPLICATIONS
15.36	1	48	3686.4	5	1	737.28	Wireless Base Station: WCDMA, cdma2000®, LTE, TD_SCDMA, WiMAX™, GSM
				5	2	368.64	
30.72	1	24		5	3	245.76	
				5	4	184.32	
61.44	4	48		5	6	122.88	
122.88	4	24		5	8	92.16	
				5	12	61.44	
15.36	1	40	3686.4	6	1	614.4	
19.2	1	32		6	2	307.2	
30.72	1	20		6	3	204.8	
38.4	1	16		6	4	153.6	
61.44	4	40		6	5	122.88	
122.88	4	20		6	6	102.4	
153.6	4	16		6	8	76.8	
				6	12	51.3	
25/31.25/ 62.5/125/ 156.25	1/1/4/5/5	25/20/40/ 25/20	3750	6	1	625	Ethernet
				6	2	312.5	
26.04166	1	24		6	4	156.25	
				6	5	125	
				6	10	62.5	
				6	20	31.25	
				6	25	25	
25/31.25/ 125	1/1/4	30/24/24	3750	5	3	250	
				5	4	187.5	
				5	5	150	
				5	6	125	
				5	12	62.5	
26.5625	1	24	3825	6	2	318.75	FC-SAN
				6	3	212.5	
				6	4	159.375	
				6	6	106.25	
				6	12	53.125	
19.44	1	32	3732.48	6	1	622.08	SONET/SDH, STM-N
38.88	1	16		6	2	311.04	
155.52	4	16		6	4	155.52	
				6	8	77.76	

cdma2000 is a registered trademark of the Telecommunications Industry Association.
WiMAX is a trademark of WiMAX Forum.

Power-Supply Filtering

The MAX3637 is a mixed analog/digital IC. The PLL contains analog circuitry susceptible to random noise. To take full advantage of on-board filtering and noise attenuation, in addition to excellent on-chip power-supply rejection, this part provides a separate power-supply pin, V_{CCA}, for the VCO circuitry. Figure 3 illustrates the recommended power-supply filter network for V_{CCA}. The purpose of this design technique is to ensure clean input power supply to the VCO circuitry and to improve the overall immunity to power-supply noise. This network requires that the power supply is +3.3V ±5%. Decoupling capacitors should be used on all other supply pins for best performance. All supply connections should be driven from the same source.

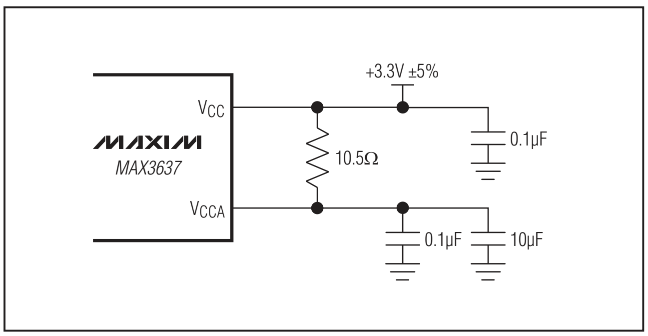


Figure 3. Power-Supply Filter

Ground Connection

The 48-pin TQFN package features an exposed pad (EP), which provides a low resistance thermal path for heat removal from the IC and also the electrical ground. For proper operation, the EP must be connected to the circuit board ground plane with multiple vias.

Crystal Selection and Layout

The MAX3637 features an integrated on-chip crystal oscillator to minimize system implementation cost. The crystal oscillator is designed to drive a fundamental mode, AT-cut crystal resonator. See Table 12 for recommended crystal specifications. See Figure 4 for the crystal equivalent circuit and Figure 5 for the recommended external capacitor connections. The crystal, trace, and two external capacitors should be placed on the board as close as possible to the XIN and XOUT pins to reduce crosstalk of active signals into the oscillator. The total load capacitance for the crystal is a combination of external and on-chip capacitance. The layout shown in Figure 6 gives approximately 1.7pF of trace plus footprint capacitance per side of the crystal. Note the ground plane is removed under the crystal to minimize capacitance. There is approximately 2.5pF of on-chip capacitance between XIN and XOUT. With an external 27pF capacitor connected to XIN and a 33pF external capacitor connected to XOUT, the total load capacitance for the crystal is approximately 18pF. The XIN and XOUT pins can be left open if not used.

Table 12. Crystal Selection Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Oscillation Frequency	f_{OSC}	18	25	33.5	MHz
Shunt Capacitance	C_0		2.0	7.0	pF
Load Capacitance	C_L		18		pF
Equivalent Series Resistance (ESR)	R_S		10	50	Ω
Maximum Crystal Drive Level				200	µW

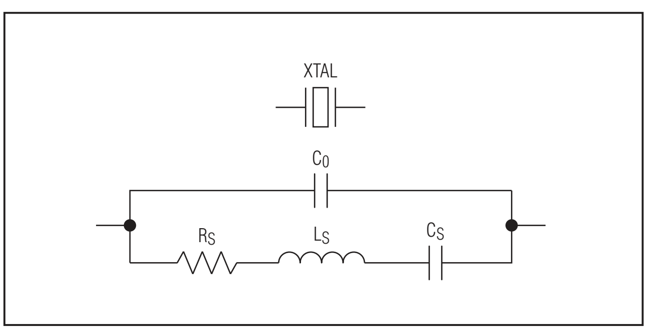


Figure 4. Crystal Equivalent Circuit

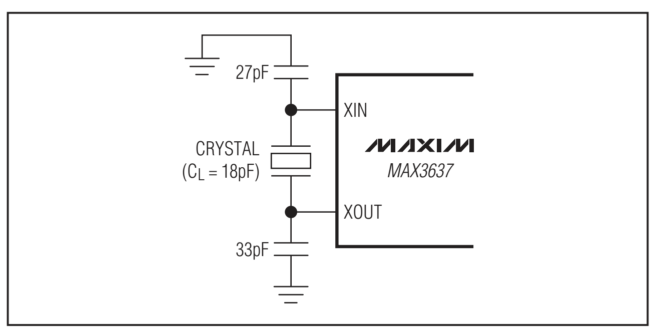


Figure 5. Crystal, Capacitor Connections

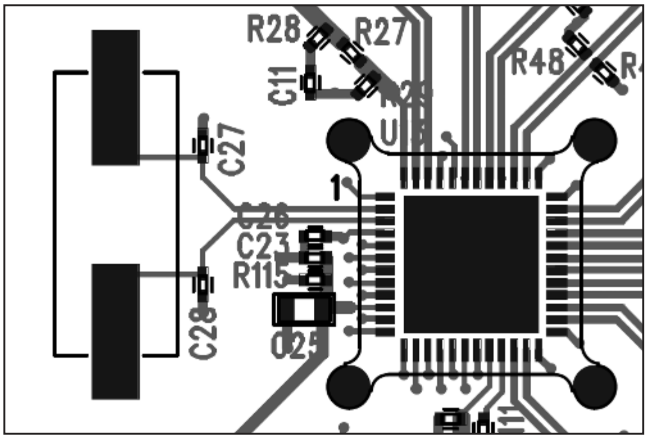


Figure 6. Crystal Layout

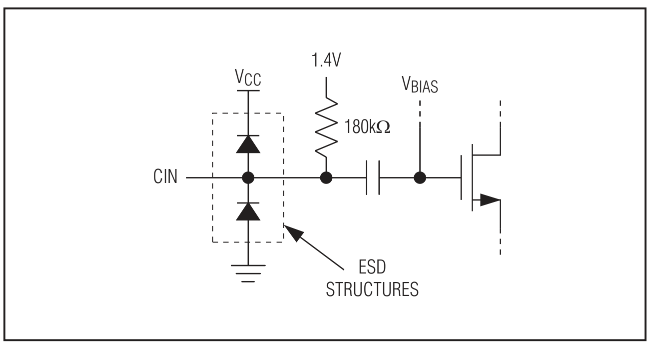


Figure 7. Equivalent CIN Circuit

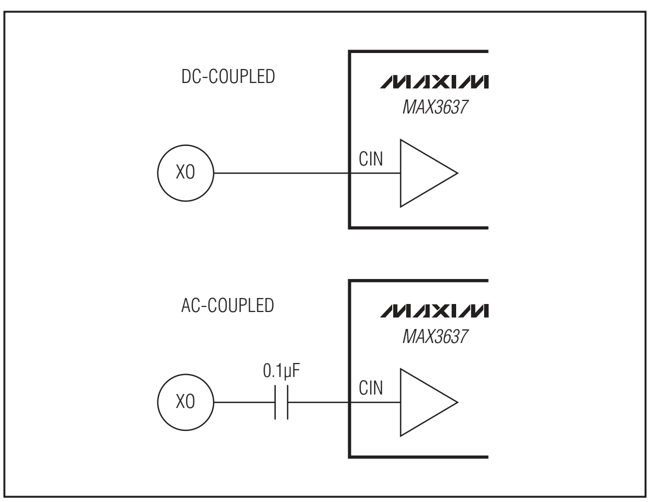


Figure 8. Interface to CIN

Interfacing with LVCMOS Input

The equivalent LVCMOS input circuit for CIN is given in Figure 7. This input is internally biased to allow AC- or DC-coupling, and has 180kΩ input impedance. See Figure 8 for the interface circuit. No signal should be applied to CIN if not used.

Interfacing with Differential Input

The equivalent input circuit for DIN is given in Figure 9. This input operates up to 350MHz and contains an internal 100Ω differential termination as well as a 35Ω common-mode termination. The common-mode termination ensures good signal integrity when connected to a source with large common-mode signals. The input can accept DC-coupled LVPECL signals, and is internally biased to accept AC-coupled LVDS, CML, and LVPECL signals (Figure 10). No signal should be applied to DIN if not used.

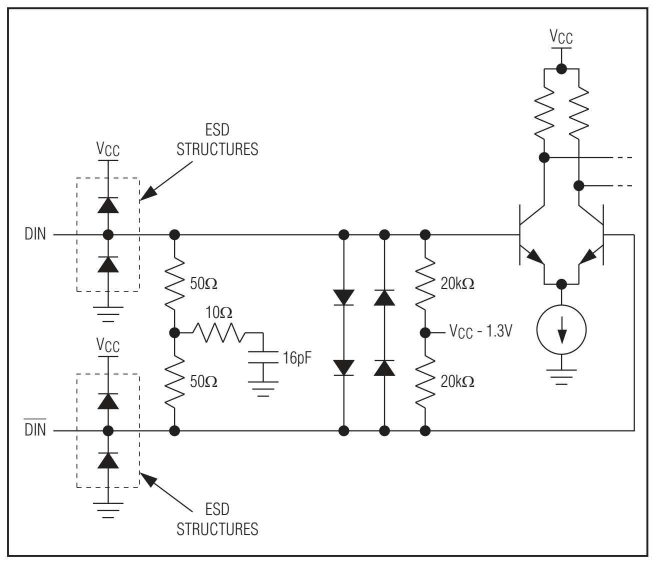


Figure 9. Equivalent DIN Circuit

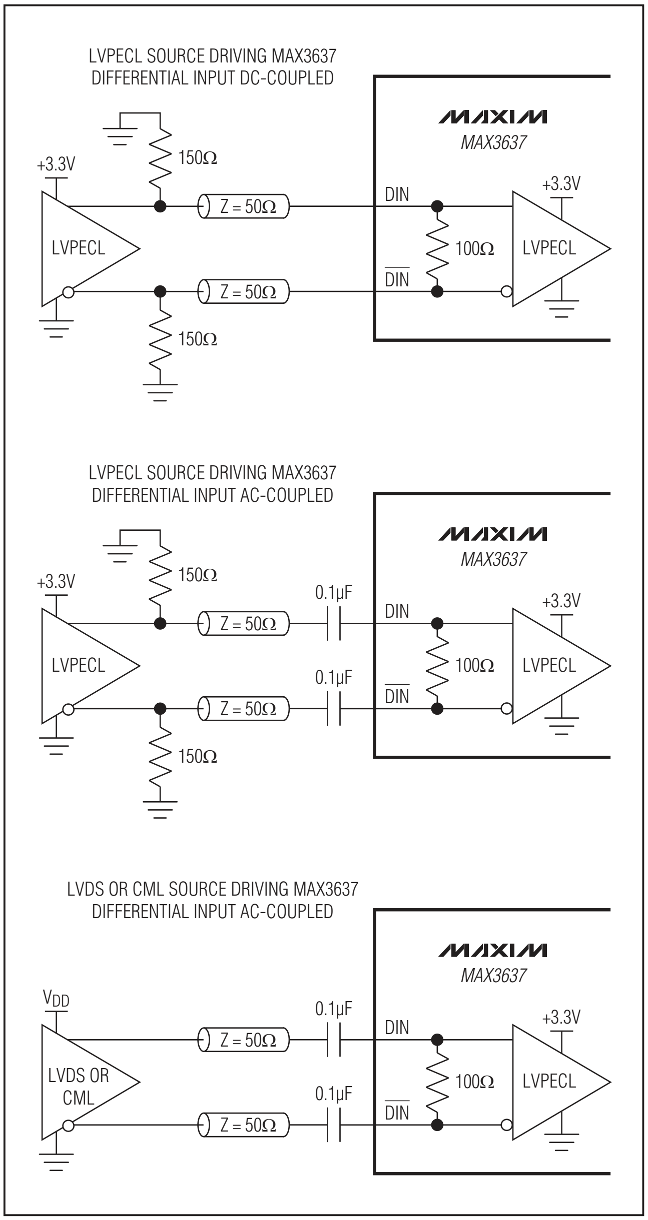


Figure 10. Interfacing to DIN

Interfacing with LVPECL Outputs

The equivalent LVPECL output circuit is given in Figure 11. These outputs are designed to drive a pair of 50Ω transmission lines terminated with 50Ω to V_{TT} = V_{CC} - 2V. If a separate termination voltage (V_{TT}) is not available, other terminations methods can be used, as shown in Figure 12. For more information on LVPECL terminations and how to interface with other logic families, refer to Application Note 291: *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

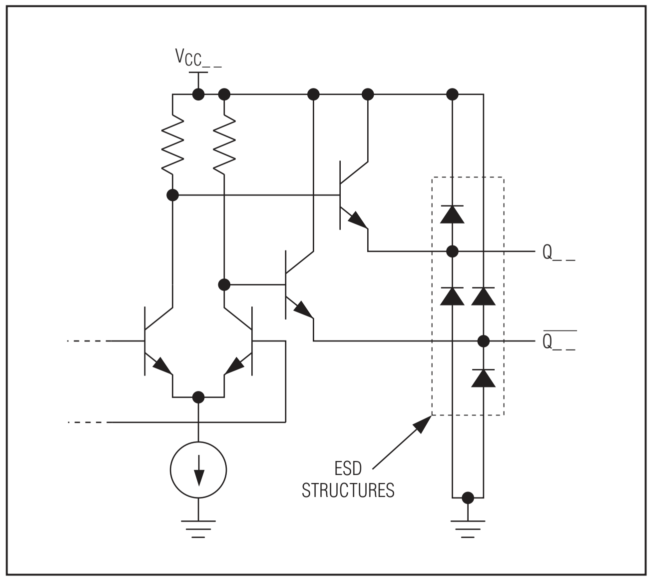


Figure 11. Equivalent LVPECL Output Circuit

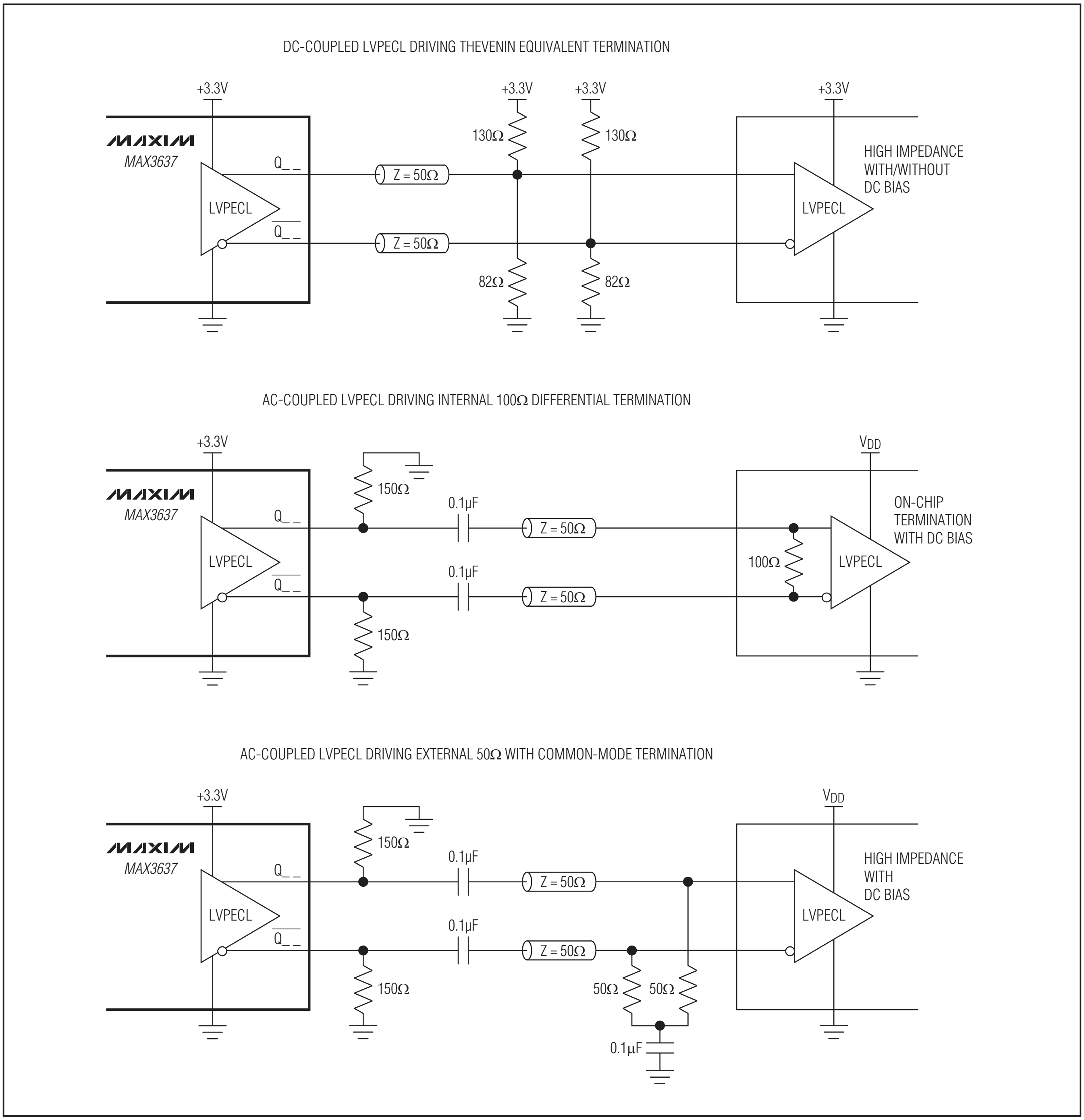


Figure 12. Interface to LVPECL Outputs

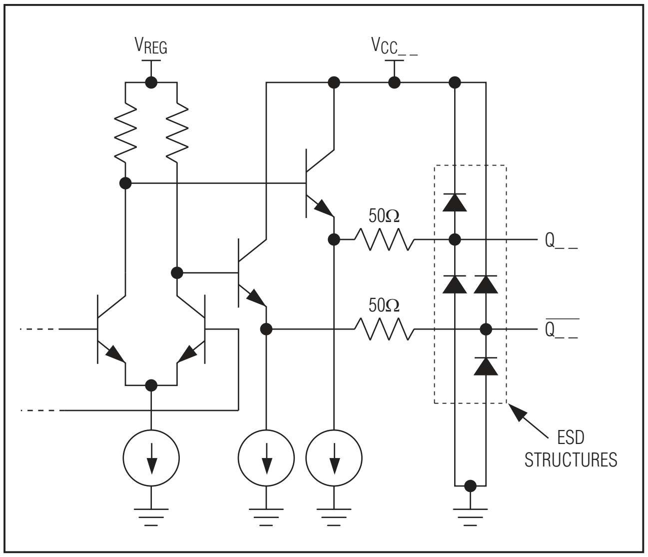


Figure 13. Equivalent LVDS Output Circuit

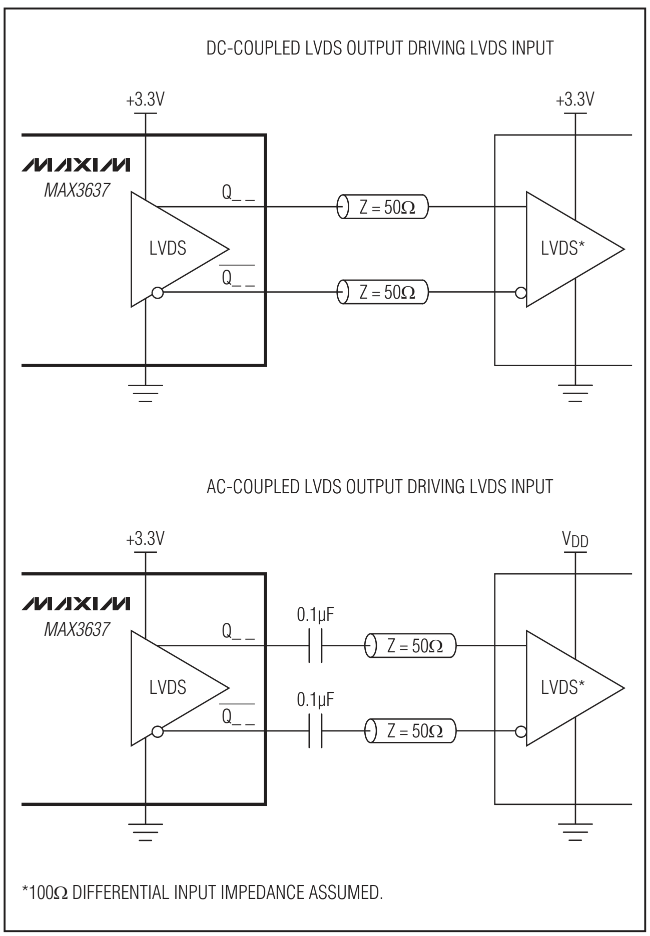


Figure 14. Interface to LVDS Outputs

Interfacing with LVDS Outputs

The equivalent LVDS output circuit is given in Figure 13. These outputs provide 100Ω differential output impedance designed to drive a 100Ω differential transmission line terminated with a 100Ω differential load. Example interface circuits are shown in Figure 14. For more information on LVDS terminations and how to interface with other logic families, refer to Application Note 291: *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

Interfacing with LVCMOS Output

The equivalent LVCMOS output circuit is given in Figure 15. This output provides 15Ω output impedance and is designed to drive a high-impedance load. A series resistor of 33Ω is recommended at the LVCMOS output before the transmission line. An example interface circuit is shown in Figure 16.

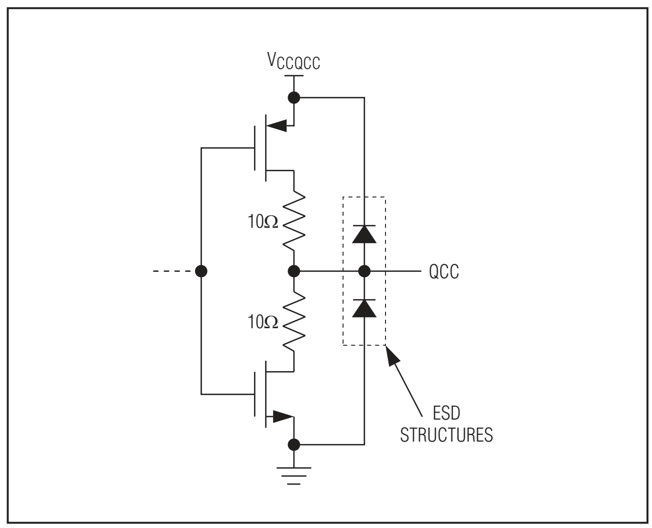


Figure 15. Equivalent LVCMOS Output Circuit

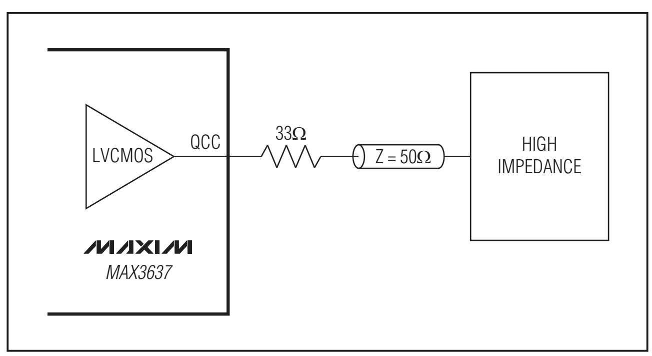


Figure 16. Interface to LVCMOS Output

Layout Considerations

The inputs and outputs are the most critical paths for the MAX3637; great care should be taken to minimize discontinuities on the transmission lines. Here are some suggestions for maximizing the performance of the MAX3637:

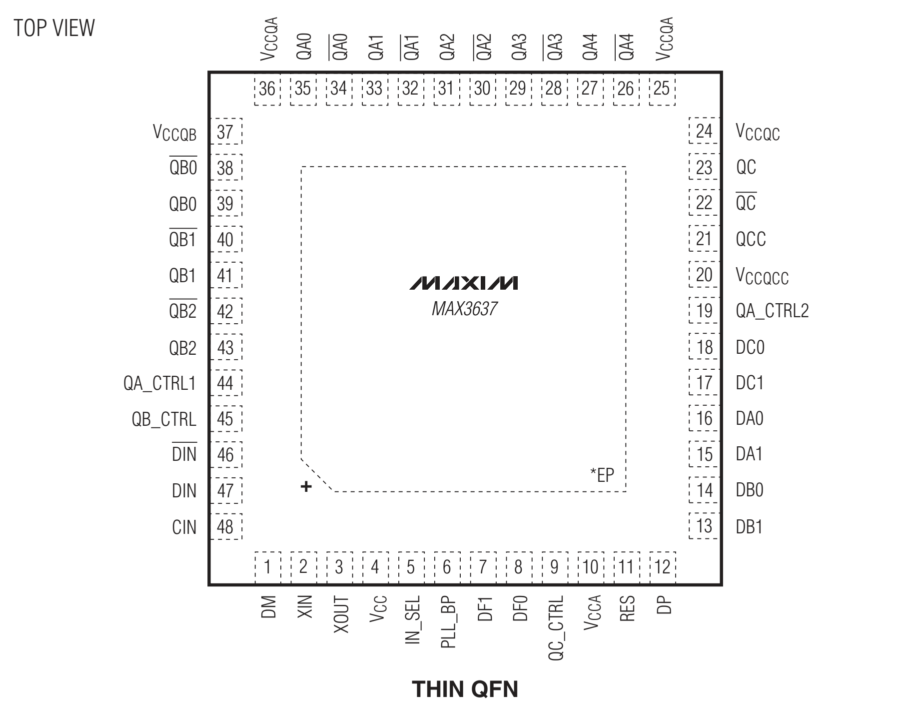
- An uninterrupted ground plane should be positioned beneath the clock outputs. The ground plane under the crystal should be removed to minimize capacitance.
- Supply decoupling capacitors should be placed close to the supply pins, preferably on the same side of the board as the MAX3637.
- Take care to isolate input traces from the MAX3637 outputs.
- The crystal, trace, and two external capacitors should be placed on the board as close as possible to the XIN and XOUT pins to reduce crosstalk of active signals into the oscillator.
- Maintain 100Ω differential (or 50Ω single-ended) transmission line impedance into and out of the part.
- Provide space between differential output pairs to reduce crosstalk, especially if the outputs are operating at different frequencies.
- Use multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.

Refer to the MAX3637 evaluation kit for more information.

Chip Information

PROCESS: BiCMOS

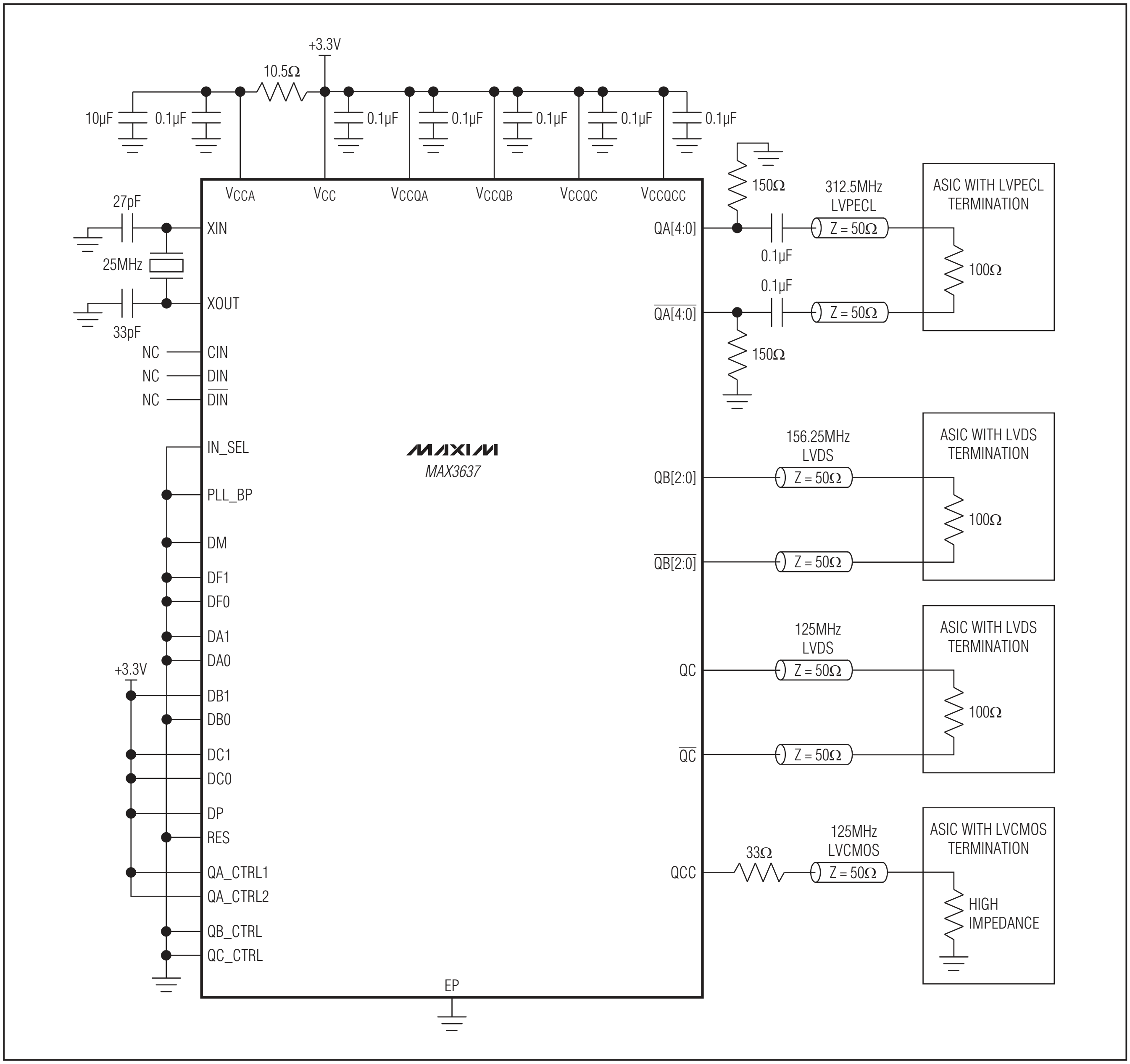
Pin Configuration



THIN QFN
(7mm × 7mm × 0.8mm)

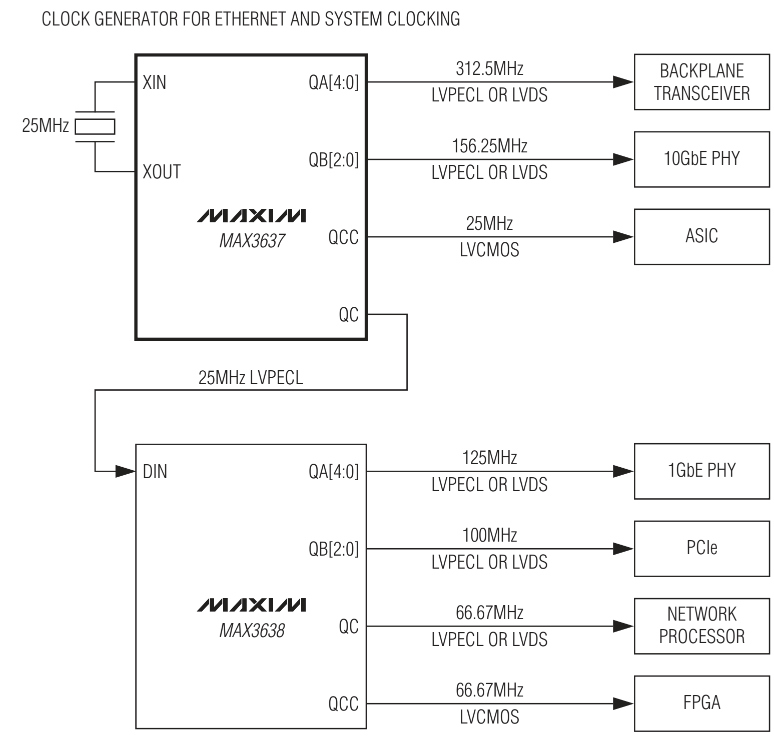
*THE EXPOSED PAD OF THE QFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL AND ELECTRICAL OPERATION.

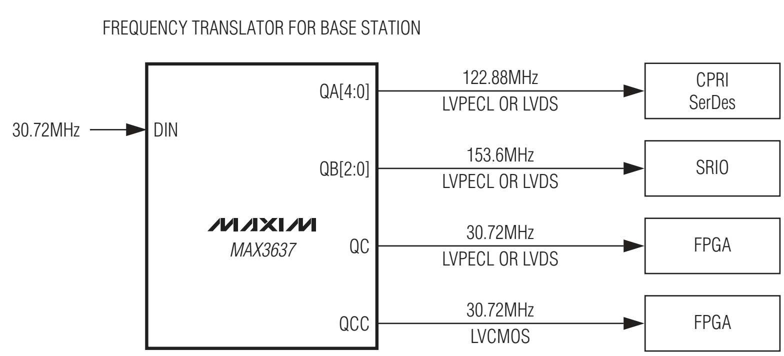
Typical Application Circuits



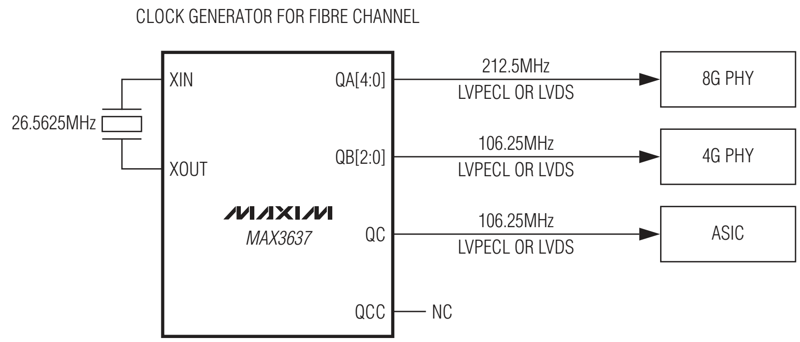
Low-Jitter, Wide Frequency Range, Programmable Clock Generator with 10 Outputs

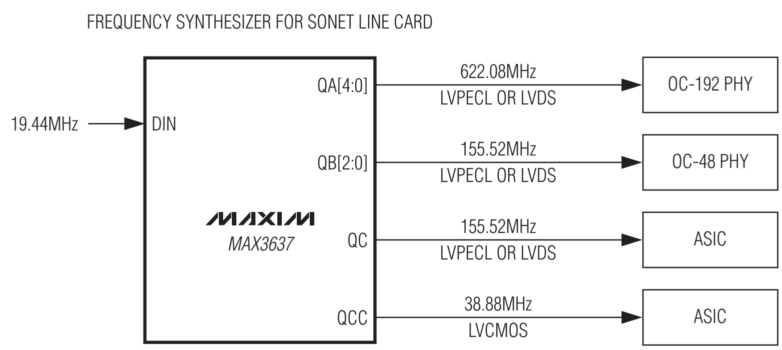
Typical Application Circuits (continued)





Typical Application Circuits (continued)





Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFN-EP	T4877+4	21-0144