Quasi-Resonant Controller

Product Highlights

- Novel Quasi-resonant operation and proprietary implementation for low EMI
- Enhanced Active Burst Mode with selectable entry and exit standby power
- Active Burst Mode to reach the lowest standby power <100 mW
- Fast startup achieved with cascode configuration
- Digital frequency reduction for better overall system efficiency
- Robust line protection with input OVP and brownout
- Comprehensive protection
- Pb-free lead plating, halogen free mold compound, RoHS compliant

PG-DSO-8

Features

- Minimum switching frequency difference between low & high line for higher efficiency & better EMI
- Enhanced Active Burst Mode with selectable entry and exit standby power
- Active Burst Mode to reach the lowest standby power <100 mW
- Fast startup achieved with cascode configuration
- Digital frequency reduction up to 10 zero crossings
- Built-in digital soft start
- Cycle-by-cycle peak current limitation
- Maximum on/off time limitation to avoid audible noise during start up and power down
- Robust line protection with input OVP and brownout
- Auto restart mode protection for VCC Over Voltage, VCC Under Voltage, Over load/Open Loop, Output Over Voltage, Over Temperature
- Limited charging current for VCC short to GND
- Pb-free lead plating, halogen free mold compound, RoHS compliant

Applications

- Auxiliary power supply for Home Appliances/white Goods, TV, PC & Server
- Blu-ray player, Set-top box & LCD/LED Monitor

Description

The Quasi-Resonant, ICE5QSAG is the 5th generation of quasi-resonant controller optimized for off-line switch power supply in cascode configuration. The improved digital frequency reduction with proprietary novel Quasi-Resonant operation offers lower EMI and higher efficiency for wide AC range by reducing the switching frequency difference between low and high line. The enhanced active burst mode enables flexibility in standby power range selection. The product has a wide operating range (10~25.5 V) of IC power supply and lower power consumption. The numerous protection functions including the robust line protection (both input OVP and brownout) to support the protections of the power supply system in failure situations. All of these make the ICE5QSAG an outstanding controller for Quasi-Resonant flyback converter in the market.

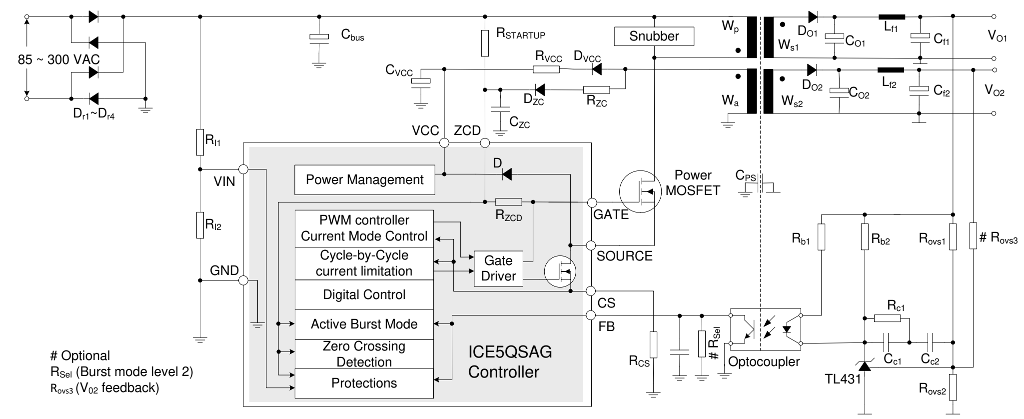

Figure 1 Typical application

Table 1 Output Power of 5th generation Quasi-Resonant Controller

Type	Package	Marking	$220V_{AC}$ ±20%[1]	85-300 V_{AC}[1]
ICE5QSAG	PG-DSO-8	5QSAG	109 W	60 W

[1] Calculated maximum output power rating in an open frame design at T_a=50°C, T_J=125°C. The output power figure is for reference purpose only. The actual power can vary depending on particular designs. Please contact to a technical expert from Infineon for more information.

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1 Pin Configuration and Functionality

The pin configuration is shown in Figure 2 and the functions are described in Table 2.

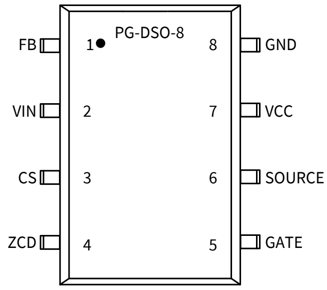

Figure 2 Pin Configuration

Table 2 Pin Definitions and Functions

Pin	Symbol	Function
1	FB	**Feedback & Burst entry/exit control** **FB** pin combines the functions of feedback control, selectable burst entry/exit control and overload/open loop protection.
2	VIN	**Input Line OVP & Brownout** **VIN** pin is connected to the bus via resistor divider (see Figure 1) to sense the line voltage. This pin combines the functions of input Line OVP, Brownout, minimum and maximum ZC count setting for low and high line.
3	CS	**Current Sense** The **CS** pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the feedback voltage) internally.
4	ZCD	**Zero Crossing Detection** **ZCD** pin combines the functions of start up, zero crossing detection and output over voltage protection. During the start up, it is used to provide a voltage level to the gate of power switch Q1 (see Figure 1) to charge V_{CC} capacitor.
5	GATE	**Gate Drive Output** This output signal drives the external main power switch Q1 (see Figure 1).
6	SOURCE	**SOURCE** The **SOURCE** pin is connected to the source of external power switch Q1 (see Figure 1) which is in series connection with internal low side MOSFET and internal VCC diode D.
7	VCC	**VCC(Positive Voltage Supply)** The **VCC** pin is the positive voltage supply to the IC. The operating range is between V_{VCC_OFF} and V_{VCC_OVP}.
8	GND	**Ground** The **GND** pin is the common ground of the controller.

2 Representative Block Diagram

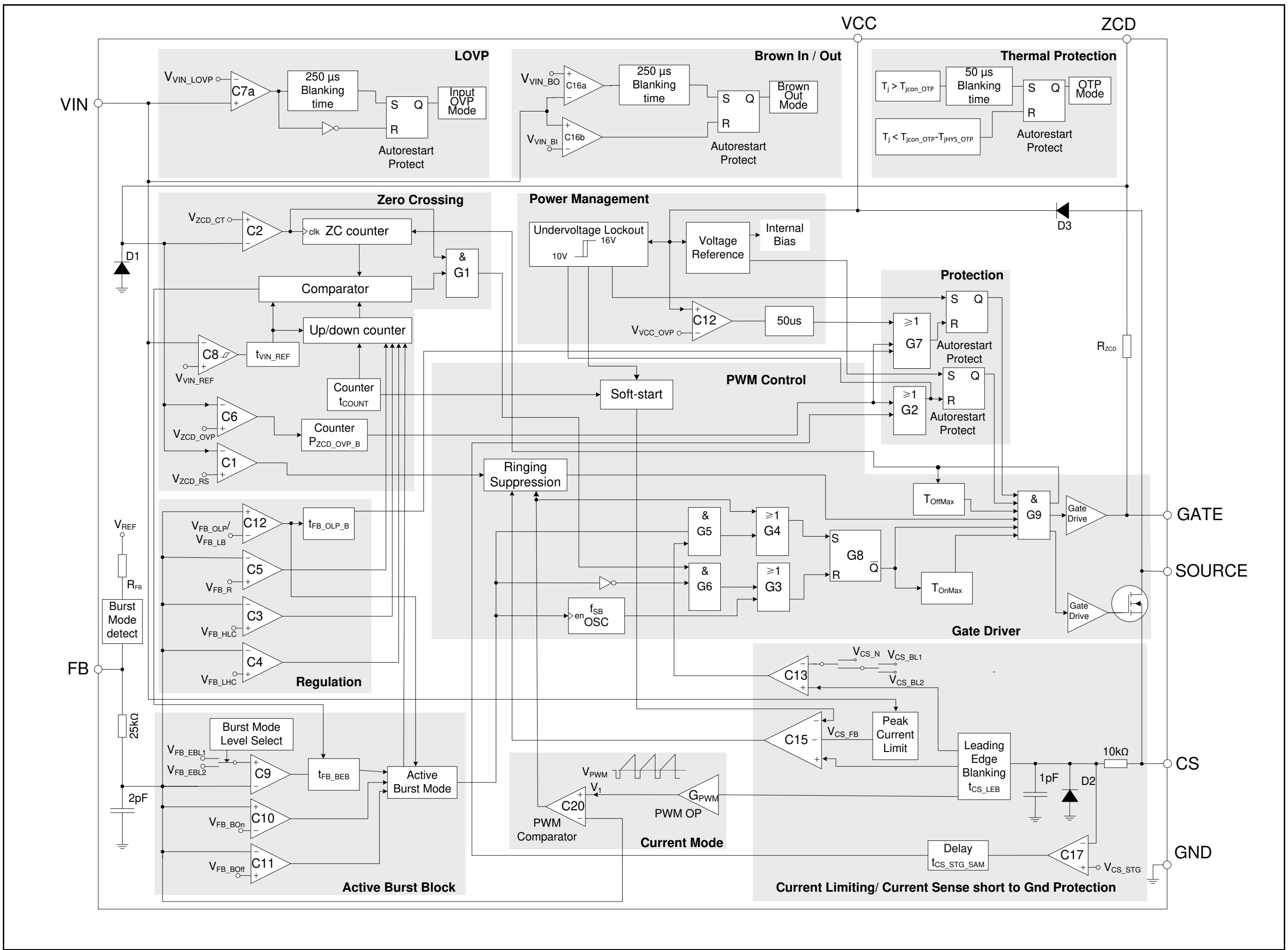

Figure 3 Representative Block Diagram

3 Functional Description

3.1 V_{CC} Pre-Charging and Typical V_{CC} Voltage during Start-up

As shown in Figure 1, once the line input voltage is applied, a rectified voltage appears across the capacitor $C_{BUS.}$ The pull up resistor $R_{STARTUP}$ provides a current to charge the C_{iss} (input capacitance) of CoolMOS™ and gradually generate one voltage level. If the voltage over C_{iss} is high enough, CoolMOS™ on and V_{CC} capacitor will be charged through primary inductance of transformer $L_{P,}$ CoolMOS™ and internal diode D_3 with two steps constant current source $I_{VCC\_Charge1}$[1] and $I_{VCC\_Charge3}$[1].

A very small constant current source ($I_{VCC\_Charge1}$) is charged to the V_{CC} capacitor till V_{CC} reach V_{CC_SCP} to protect the controller from V_{CC} pin short to ground during the start up. After this, the second step constant current source ($I_{VCC\_Charge3}$) is provided to charge the V_{CC} capacitor further, until the V_{CC} voltage exceeds the turned-on threshold V_{VCC_ON}. As shown in the time phase I in Figure 4, the V_{CC} voltage increase almost linearly with two steps.

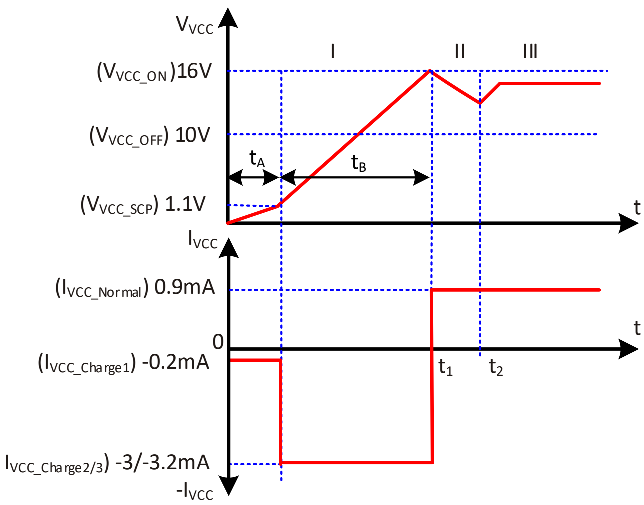

Figure 4 VCC voltage and current at start up

The time taking for the V_{CC} pre-charging can then be approximately calculated as:

$$t_1 = t_A + t_B = \frac{V_{VCC\_SCP} \cdot C_{VCC}}{I_{VCC\_Charge1}} + \frac{(V_{VCC\_ON} - V_{VCC\_SCP}) \cdot C_{VCC}}{I_{VCC\_Charge3}} \quad (1)$$

When the V_{CC} voltage exceeds the V_{CC} turned on threshold V_{VCC_ON} at time t_1, the IC begins to operate with soft start. Due to power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the V_{CC} capacitor before the output voltage is built up, the V_{CC} voltage drops (Phase II). Once the output voltage is high enough, the V_{CC} capacitor receives the energy from the auxiliary winding from the time t_2 onward and delivering the I_{VCC_Normal}[2] to the controller. The V_{CC} then will reach a constant value depending on output load.

3.2 Soft-start

As shown in Figure 5, at the time t_{on}, the IC begins to operate with a soft-start. By this soft-start the switching stresses for the MOSFET, diode and transformer are minimized. The soft-start implemented in ICE5QSAG is a digital time-based function. The preset soft-start time is t_{SS} (12 ms) with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.3 V to 1 V finally. During the first 3 ms of

[1] $I_{VCC\_Charge1/2/3}$ is charging current from the controller to VCC capacitor during start up

[2] I_{VCC_Normal} is supply current from VCC capacitor or auxiliary winding to the controller during normal operation

soft start, the ringing suppression time is set to *25 μs* to avoid irregular switching due to switch off oscillation noise.

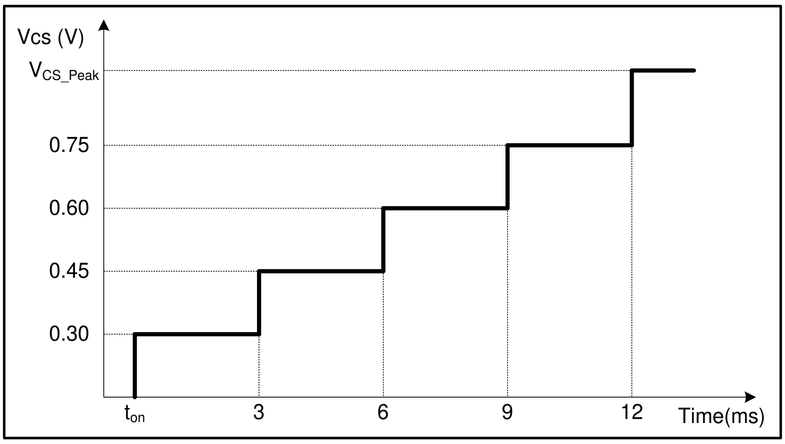

Figure 5 **Maximum current sense voltage during soft start**

3.3 Normal Operation

During normal operation, the ICE5QSAG works with a digital signal processing circuit composing an up/down counter, a zero-crossing counter (ZC counter) and a comparator, and an analog circuit composing a current measurement unit and a comparator. The switch-on and -off time points are each determined by the digital circuit and the analog circuit, respectively. The input information of the zero-crossing signal and the value of the up/down counter are needed to determine the switch-on while the feedback signal V_{FB} and the current sensing signal V_{CS} are necessary for the switch-off determination.

Details about the full operation of the controller in normal operation are illustrated in the following paragraphs.

3.3.1 Digital Frequency Reduction

As mentioned above, the digital signal processing circuit consists of an up/down counter, a ZC counter and a comparator. These three parts are the key to implement digital frequency reduction with decreasing load. In addition, a ringing suppression time controller is implemented to avoid mis-triggering by the high frequency oscillation, when the output voltage is very low under conditions such as soft start period or output short circuit. Functionality of these parts is described as in the following.

3.3.1.1 Minimum ZC Count Determination

To reduce the switching frequency difference between low and high line, minimum ZC count determination is implemented. Minimum ZC count is set to 1 if VIN less than V_{VIN_REF} which represents for low line. For high line, minimum ZC count is set to 3 after VIN higher than V_{VIN_REF}. There is also a hysteresis V_{VIN_REF} with certain blanking time t_{VIN_REF} for stable AC line selection between low and high line.

3.3.1.2 Up/down counter

The up/down counter stores the number of the zero crossing which determines valley numbers to switch-on the main MOSFET after demagnetization of the transformer. This value is fixed according to the feedback voltage, V_{FB}, which contains information about the output power. Indeed, in a typical peak current mode control, a high output power results in a high feedback voltage, and a low output power leads to a low feedback voltage. Hence, according to V_{FB}, the value in the up/down counter is changed to vary the power

MOSFET off-time according to the output power. In the following, the variation of the up/down counter value according to the feedback voltage is explained.

The feedback voltage V_{FB} is internally compared with three threshold voltages V_{FB_LHC}, V_{FB_HLC} and V_{FB_R} at each clock period of 48 ms. The up/down counter counts then upward, keep unchanged or count downward, as shown in 0.

Table 3 Operation of up/down counter

V_{FB}	up/down counter action
Always lower than V_{FB_LHC}	Count upwards till n=8/10[1]
Once higher than V_{F_LHC}, but always lower than V_{FB_HLC}	Stop counting, no value changing
Once higher than V_{FB_HLC}, but always lower than V_{FB_R}	Count downwards till n=1/3[2]
Once higher than V_{FB_R}	Set up/down counter to n=1/3[2]

The number of zero crossing is limited and therefore, the counter varies among 1 to 8 (for low line) or 3 to 10 (for high line) and any attempt beyond this range is ignored. When V_{FB} exceeds V_{FB_R} voltage, the up/down counter is reset to 1 (low line) and 3 (high line) in order to allow the system to react rapidly to a sudden load increase. The up/down counter value is also reset to 1 (low line) and 3 (high line) at the start-up time, to ensure an efficient maximum load start up. Figure 6 shows some examples on how up/down counter is changed according to the feedback voltage over time.

The use of two different thresholds V_{FB_LHC} and V_{FB_HLC} to count upward or downward is to prevent frequency jittering when the feedback voltage is close to the threshold point.

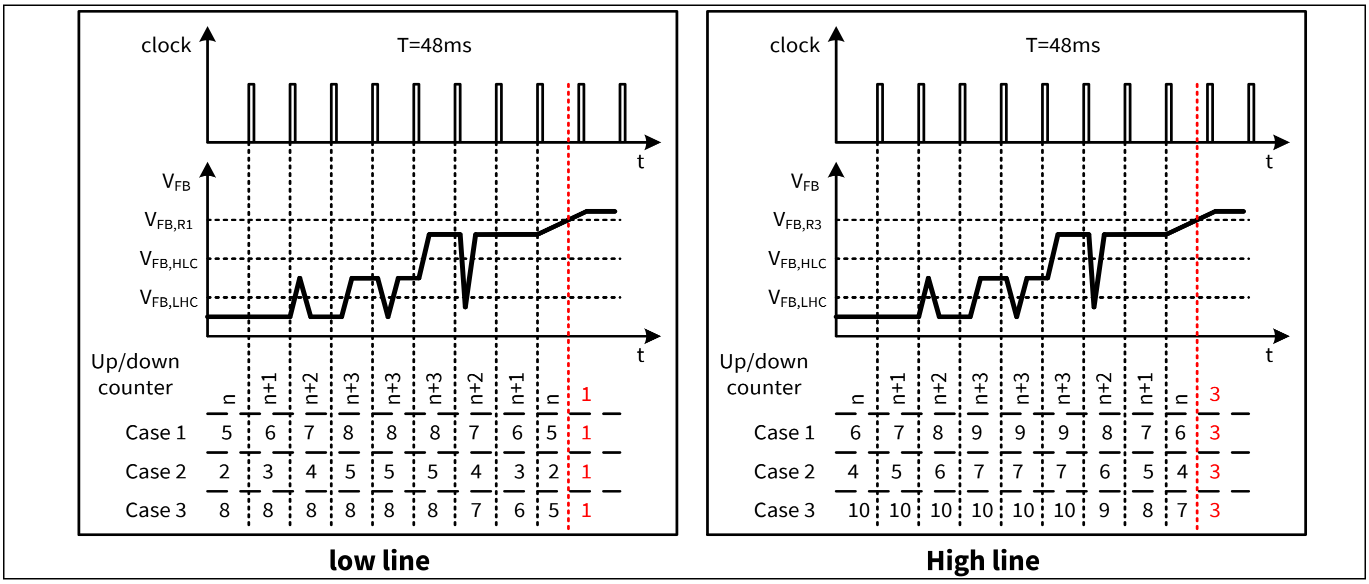

Figure 6 Up/down counter operation

3.3.1.3 Zero crossing (ZC counter)

In the system, the voltage from the auxiliary winding is applied to the ZCD pin through a RC network, which provides a time delay to the voltage from the auxiliary winding. Internally this pin is connected to a clamping network, a zero-crossing detector, an output overvoltage detector and a ringing suppression time controller.

During on-state of the power switch, a positive gate drive voltage is applied to the ZCD pin due to R_{ZCD} resistor, hence external diode D_{ZC} (see Figure 1) is added to block the negative voltage from the auxiliary winding. The ZC counter has a minimum value of 1 (for low line) or 3 (for high line) and maximum value of 8 (for low line) or 10

[1] *n=8 (for low line) and n=10 (for high line)*

[2] *n=1 (for low line) and n=3 (for high line)*

(for high line). After the Q1 (see Figure 1) is turned off, every time when the falling voltage ramp of on ZCD pin crosses the V_{ZCD_CT} threshold, a zero crossing is detected and ZC counter will increase by 1. It is reset every time after the DRIVER output is changed to high.

To achieve the switch on at voltage valley, the voltage from the auxiliary winding is fed to a time delay network (the RC network consists of R_{ZC} and C_{ZC} as shown in Figure 1) before it is applied to the zero-crossing detector through the ZCD pin. The needed time delay to the main oscillation signal Δt should be approximately one fourth of the oscillation period, T_{OSC} (by transformer primary inductor and drain-source capacitor) minus the propagation delay from the detected zero-crossing to the switch-on of the main switch t_{delay}, theoretically:

$$\Delta t = \frac{T_{OSC}}{4} - t_{delay} \tag{2}$$

This time delay should be matched by adjusting the time constant of the RC network which is calculated as:

$$\tau_{td} = C_{ZC} \cdot \frac{R_{ZC} \cdot R_{ZCD}}{R_{ZC} + R_{ZCD}} \tag{3}$$

3.3.2 Ringing suppression time

After Q1 (see **Error! Reference source not found.**) is turned off, there will be some oscillation on V_{DS}, which will also appear on the V_{ZCD}. To avoid mis-triggering by such oscillations to turn on the Q1, a ringing suppression timer is implemented. This suppression time is depended on the voltage V_{ZCD}. If the voltage V_{ZCD} is lower than the threshold V_{ZCD_RS}, a longer preset time t_{ZCD_RS2} is applied. However, if the voltage V_{ZCD} is higher than the threshold, a shorter time t_{ZCD_RS1} is set.

3.3.2.1 Switch on determination

After the gate drive goes to low, it cannot be changed to high during ring suppression time.

After ring suppression time, the gate drive can be turned on when the ZC counter value is equal to up/down counter value.

However, it is also possible that the oscillation between primary inductor and drain-source capacitor damps very fast and IC cannot detect zero crossings event. In this case, a maximum off time is implemented. After gate drive has been remained off for the period of T_{OffMax}, the gate drive will be turned on again regardless of the ZC counter values and V_{ZCD}. This function can effectively prevent the switching frequency from going lower than 20 kHz. Otherwise it will cause audible noise.

3.3.3 Switch off determination

In the converter system, the primary current is sensed by an external shunt resistor, which is connected between source terminal of the internal MOSFET and the common ground. The sensed voltage across the shunt resistor V_{CS} is applied to an internal current measurement unit, and its output voltage V_1 is compared with the feedback voltage V_{FB}. Once the voltage V_1 exceeds the voltage V_{FB}, the output flip-flop is reset. As a result, the main power switch is switched off. The relationship between the V_1 and the V_{CS} is described by (see Figure 3):

$$V_{CS} = I_D \times R_{CS}$$
$$V_1 = G_{PWM} \cdot V_{CS} + V_{PWM} \tag{4}$$

where, V_{CS} : CS pin voltage

I_D : power MOSFET current

R_{CS} : resistance of the current sense resistor

V_1 : voltage level compared to V_{FB}

G_{PWM} : PWM-OP gain

To avoid mis-triggering caused by the voltage spike across the shunt resistor at the turn on of the main power switch, a leading edge blanking time, t_{LEB}, is applied to the output of the comparator. In other words, once the gate drive is turned on, the minimum on time of the gate drive is the leading edge blanking time.

In addition, there is a maximum on time, t_{OnMax}, limitation implemented in the IC. Once the gate drive has been in high state longer than the maximum ON time, it will be turned off to prevent the switching frequency from going too low because of long on time.

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Also, if the voltage at the current sense pin is lower than the preset threshold V_{CS_STG} after the time $t_{CS\_STG\_SAM}$ for three consecutive pulses during on-time of the power switch, this abnormal V_{CS} will trigger IC into auto restart mode.

3.3.4 Modulated gate drive

The drive-stage is optimized for EMI consideration. The switch on speed is slowed down before it reaches the CoolMOS™ turn on threshold. That is a slope control of the rising edge at the output of driver (see Figure 7). Thus the leading switch spike during turn on is minimized.

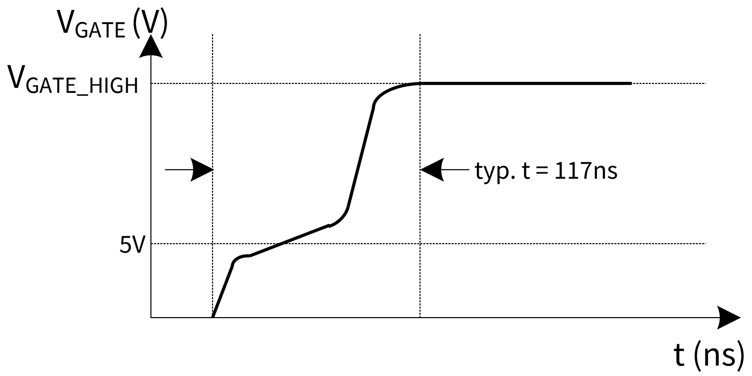


Figure 7 Gate rising waveform

3.4 Current limitation

There is a cycle by cycle current limitation realized by the current limit comparator to provide over-current detection. The source current of the CoolMOS™ is sensed via a sense resistor R_{CS}. By means of R_{CS} the source current is transformed to a sense voltage V_{CS} which is fed into the pin CS. If the voltage V_{CS} exceeds an internal voltage limit, adjusted according to the Line voltage, the comparator immediately turns off the gate drive.

When the main bus voltage increases, the switch on time becomes shorter and therefore the operating frequency is also increased. As a result, for a constant primary current limit, the maximum possible output power is increased which is beyond the converter design limit.

To compensate such effect, both the internal peak current limit circuit (V_{CS}) and the ZC count varies with the bus voltage according to Figure 8.

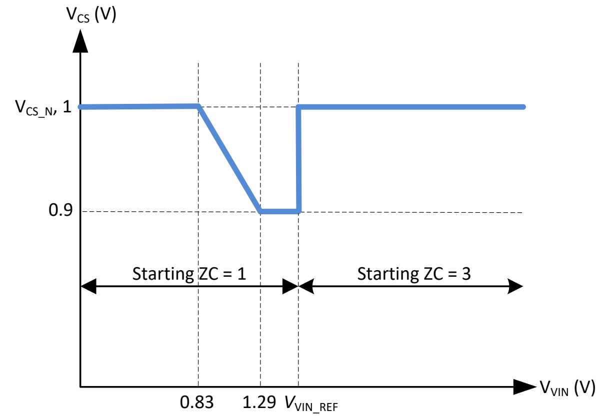


Figure 8 Variation of the V_{CS} limit voltage according to the V_{IN} voltage

3.5 Active Burst Mode with selectable power level

At light load condition, the IC enters Active Burst Mode operation to minimize the power consumption. Details about Active Burst Mode operation are explained in the following paragraphs.

The burst mode entry level can be selected by changing the different resistor R_{Sel} at FB pin. There are 2 levels to be selected with different resistor which are targeted for low range of active burst mode power (Level 1) and high range of active burst mode power (Level 2). The following table shows the control logic for the entry and exit level with the FB voltage.

Table 4 Two levels entry and exit active burst mode power

Level	V_{FB}	V_{CS}	Entry level	Exit level
			V_{FB_EBLX}	V_{FB_LB}
1	$V_{FB} > V_{REF\_B}$	$V_{CS\_BL1} = 0.31$ V	0.90 V	2.75 V
2	$V_{FB} < V_{REF\_B}$	$V_{CS\_BL2} = 0.35$ V	1.05 V	2.75 V

During IC first startup, the internal Ref_{GOOD} signal is logic low when $V_{CC} < 4$ V. It will reset the Burst Mode level Detection latch. When the Burst Mode Level Detection latch is low and IC is in OFF state, the IC internal R_{FB} resistor is disconnected from the FB pin and a current source I_{sel} is turned on instead.

From Vcc=4 V to Vcc on threshold, the FB pin will start to charge to a voltage level associated with R_{Sel} resistor. When Vcc reaches Vcc on threshold, the FB voltage is sensed. The burst mode thresholds are then chosen according to the FB voltage level. The Burst Mode Level Detection latch is then set to high. Once the detection latch is set high, any change of the FB level will not change the threshold selection. The current source I_{sel} is turned off in 2 µs after V_{CC} reaches V_{CC} on threshold and the R_{FB} resistor is re-connected to FB pin (see Figure 9).

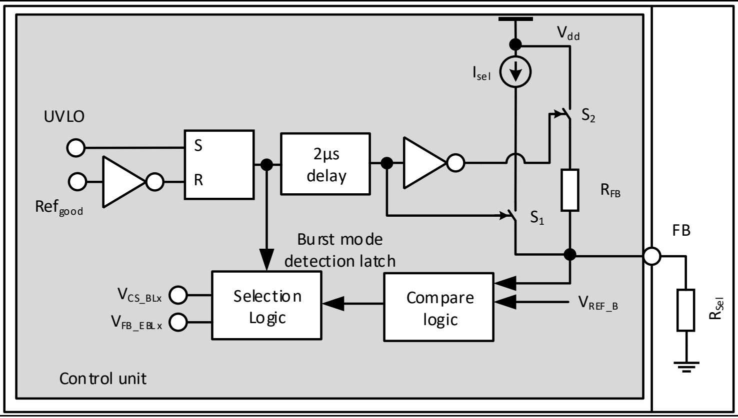


Figure 9 Burst mode detect and adjust

3.5.1 Entering Active Burst Mode Operation

For determination of entering Active Burst Mode operation, three conditions apply:

- the feedback voltage is lower than the threshold of V_{FB_EBLX}
- the up/down counter is 8 for low line or 10 for high line and
- the above two conditions remain after a certain blanking time t_{FB_BEB} (20 ms).

Once all of these conditions are fulfilled, the Active Burst Mode flip-flop is set and the controller enters Active Burst Mode operation. This multi-condition determination for entering Active Burst Mode operation prevents mis-triggering of entering Active Burst Mode operation, so that the controller enters Active Burst Mode operation only when the output power is really low during the preset blanking time.

3.5.2 During Active Burst Mode Operation

After entering the Active Burst Mode the feedback voltage rises as V_O starts to decrease due to the inactive PWM section. One comparator observes the feedback signal if the voltage level V_{FB_BOn} is exceeded. In that case the internal circuit is power up to restart with switching.

Turn-on of the power MOSFET is triggered by ZC counter with a fixed value of 8 ZC for low line and 10 ZC for high line. Turn-off is resulted if the voltage across the shunt resistor at CS pin hits the threshold V_{CS_BLX}.

If the output load is still low, the feedback signal decreases as the PWM section is operating. When feedback signal reaches the low threshold V_{FB_BOff}, the internal circuit is reset again and the PWM section is disabled until next time V_{FB} signal increases beyond the V_{FB_BOn} threshold. In Active Burst Mode, the feedback signal is changing like a saw tooth between V_{FB_BOff} and V_{FB_BOn} (see Figure 10).

3.5.3 Leaving Active Burst Mode Operation

The feedback voltage immediately increases if there is a high load jump. This is observed by a comparator with threshold of V_{FB_LB}. As the current limit is V_{CS_BLX} (31% or 35%) during Active Burst Mode, a certain load is needed so that feedback voltage can exceed V_{FB_LB}. After leaving active burst mode, normal peak current control through V_{FB} is re-activated. In addition, the up/down counter will be set to 1 (low line) or 3 (high line) immediately after leaving Active Burst Mode. This is helpful to minimize the output voltage undershoot.

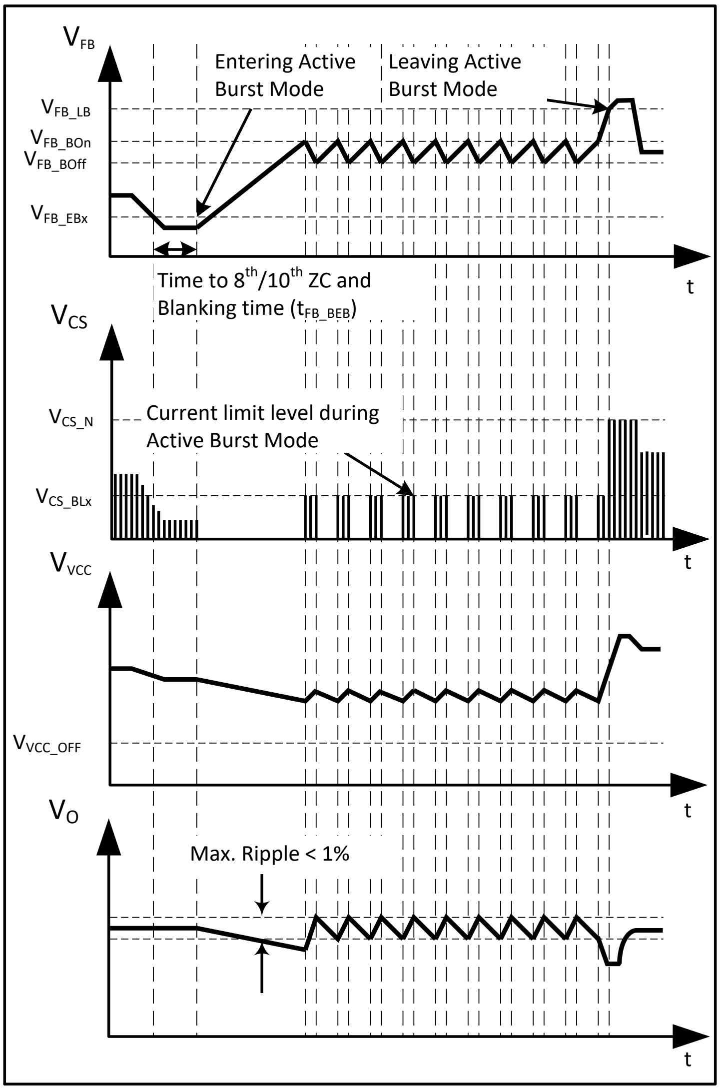


Figure 10 Signals in Active Burst Mode

3.6 Protection Functions

The ICE5QSAG provides numerous protection functions which considerably improve the power supply system robustness, safety and reliability. The following table summarizes these protection functions. There are 3 different kinds of protection mode; non switch auto restart, auto restart and odd skip auto restart. The details can refer to the Figure 11, Figure 12 and Figure 13.

Table 5 Protection functions

Protection Functions	Normal Mode	Burst Mode		Protection Mode
		Burst ON	Burst OFF	
Line Over Voltage	√	√	√	Non switch Auto Restart
Brownout	√	√	√	Non switch Auto Restart
V_{CC} Over Voltage	√	√	NA[1]	Odd skip Auto Restart
V_{CC} Under Voltage	√	√	√	Auto Restart

[1] Not Applicable

Protection Functions	Normal Mode	Burst Mode		Protection Mode
		Burst ON	Burst OFF	
Over Load	√	NA[1]	NA[1]	Odd skip Auto Restart
Output Over Voltage	√	√	NA[1]	Odd skip Auto Restart
Over Temperature	√	√	√	Non switch Auto Restart

3.6.1 Line Over Voltage

The AC **Line Over Voltage** Protection is detected by sensing bus capacitor voltage through VIN pin via 2 potential divider resistors, R_{l1} and R_{l2} (see Figure 1). Once V_{VIN} voltage is higher than the line over voltage threshold V_{VIN_LOVP}, the controller enters Line Over Voltage Protection and it releases the protection mode after V_{VIN} is lower than V_{VIN_LOVP}.

3.6.2 Brownout

The **Brownout** protection is observed by VIN pin similar to line over voltage Protection method with a different voltage threshold level. When V_{VIN} voltage is lower than the brownout threshold (V_{VIN_BO}), the controller enters Brownout Protection and it releases the protection mode after V_{VIN} higher than brownin threshold (V_{VIN_BI}).

3.6.3 V_{CC} Ovder Voltage or Under Voltage

During operation, the V_{CC} voltage is continuously monitored. In case of a **V_{CC} Over Voltage** or **Under Voltage**, the IC is reset and the main power switch is then kept off. After the V_{CC} voltage falls below the threshold V_{VCC_OFF}, the new start up sequence is activated. The V_{CC} capacitor is then charged up. Once the voltage exceeds the threshold V_{VCC_ON}, the IC begins to operate with a new soft-start.

3.6.4 Over Load

In case of open control loop or output **Over Load**, the feedback voltage will be pulled up and exceed V_{FB_OLP}. After a blanking time of $t_{FB\_OLP\_B}$, the IC enters auto restart mode. The blanking time here enables the converter to operate for a certain time during a sudden load jump.

3.6.5 Output Over Voltage

During off-time of the power MOSFET, the voltage at the ZCD pin is monitored for **Output Over Voltage** detection. If the voltage is higher than the preset threshold V_{ZCD_OVP} for 10 consecutive pulses, the IC enters Output Over Voltage Protection.

3.6.6 Over Temperature

If the junction temperature of controller chip exceeds T_{jcon_OTP}, the IC enters into **Over Temperature** protection (OTP) Non switch auto restart mode. The controller implements with a 40˚C hysteresis. In another word, the controller/IC can only resume from OTP if its junction temperature drops 40˚C from OTP trigger point. The over temperature protection of the controller chip shall prevent turn-on of the power supply if the component temperature is too high. For appropriate system protection, additional measures may have to be taken by the designer.

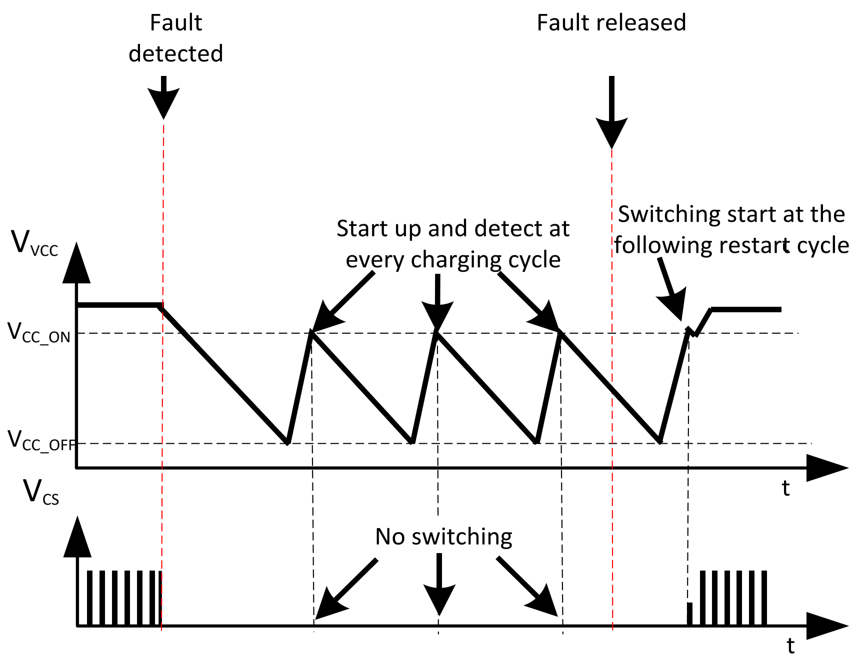


Figure 11 Non switch Auto Restart Mode

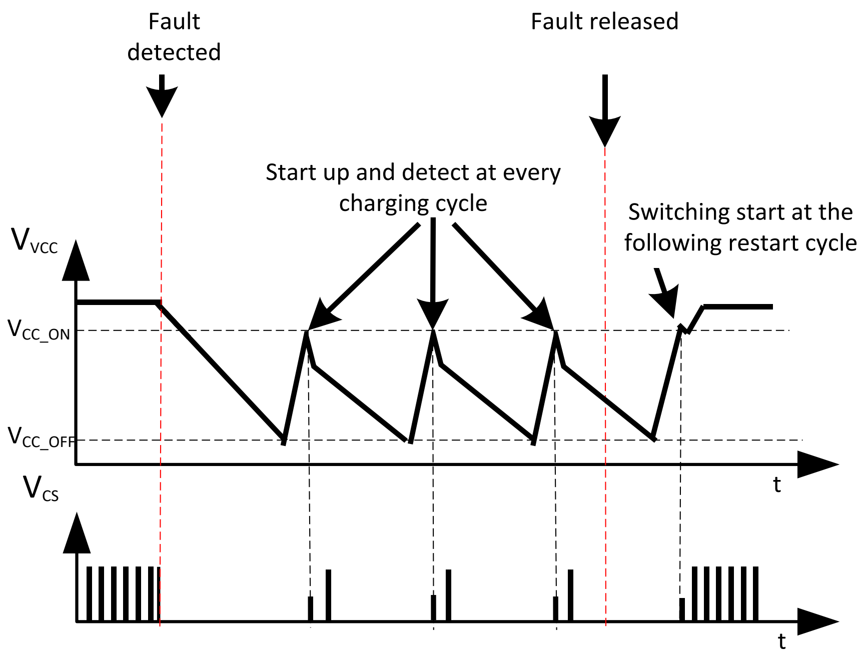


Figure 12 Auto Restart Mode

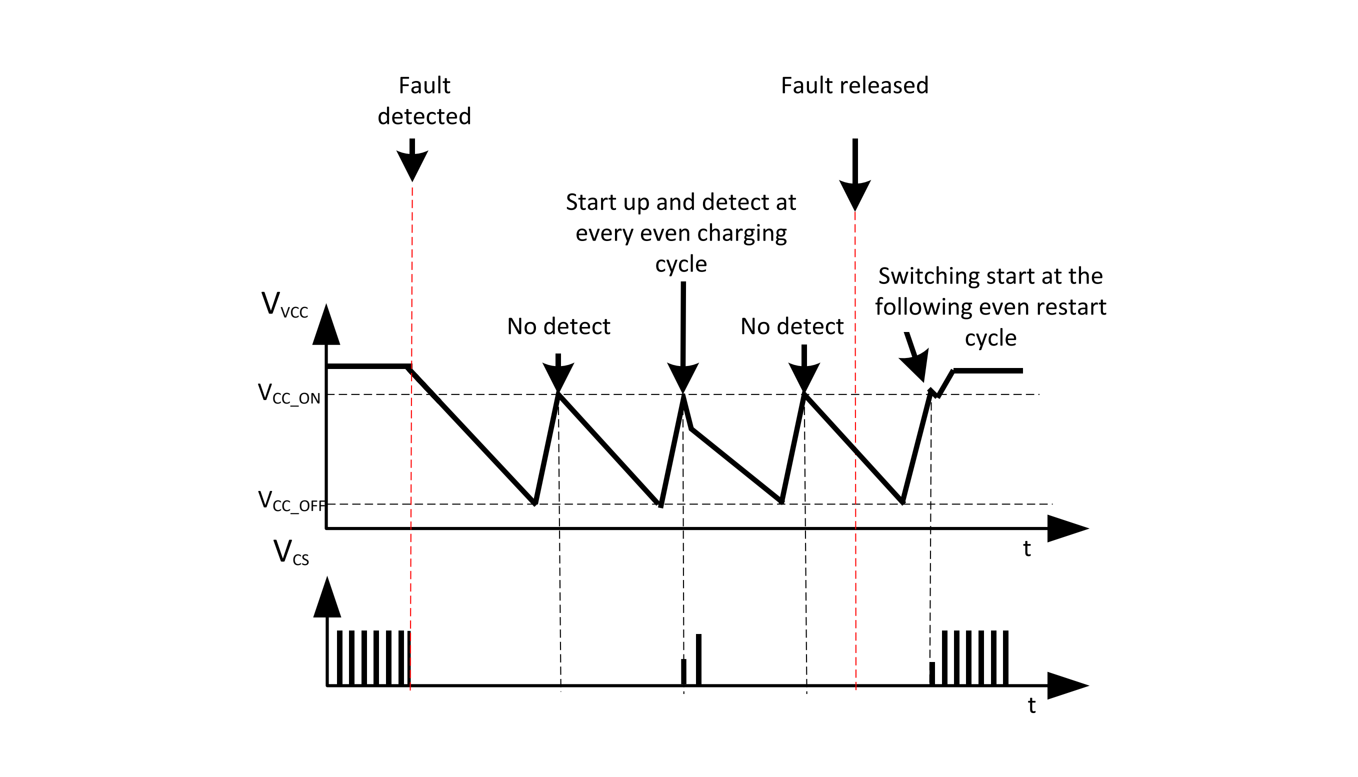


Figure 13 Odd skip Auto Restart Mode

4 Electrical Characteristics

Attention: *All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.*

4.1 Absolute Maximum Ratings

Attention: *Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. System design needs to ensure not to exceed the maximum limit. Ta=25°C unless otherwise specified.*

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Note / Test Condition
		Min.	Max.		
VCC Supply Voltage	V_{CC}	-0.3	27	V	
GATE Voltage	V_{GATE}	-0.3	27	V	
SOURCE Voltage	V_{SOURCE}	-0.3	27	V	
FB Voltage	V_{FB}	-0.3	3.6	V	
ZCD Voltage	V_{ZCD}	-0.3	27	V	
CS Voltage	V_{CS}	-0.3	3.6	V	
VIN Voltage	V_{IN}	-0.3	3.6	V	
Maximum DC current at SOURCE pin	I_{SOURCE}	-	0.9	A	Limited by $T_{j,Max}$
Single pulse source current at SOURCE pin	I_{S_pulse}	-	5.8	A	Pulse width t_P=20 µs and limited by $T_{j,Max}$
ESD robustness HBM	V_{ESD_HBM}	-	2000	V	According to EIA/JESD22
ESD robustness CDM	V_{ESD_CDM}	-	500	V	
Junction temperature range	T_J	-40	150	°C	
Storage Temperature	T_{STORE}	-55	150	°C	
Thermal Resistance Junction-Ambient	R_{thJA}	-	185	K/W	Setup according to the JESD51 standard

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Table 7 Operating Range

Parameter	Symbol	Limit Values		Unit	Remark
		Min.	Max.	V	
VCC Supply Voltage	V_{VCC}	V_{VCC_OFF}	V_{VCC_OVP}		
Junction Temperature of controller	T_{jCon_op}	-40	T_{jCon_OTP}	˚C	Max value limited due to OTP of controller chip

4.3 Operating Conditions

Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from – 40 °C to 125 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 18 V is assumed.

Table 8 Operating Conditions

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC Charge Current	$I_{VCC\_Charge1}$	-0.35	-0.2	-0.09	mA	V_{VCC}=0 V, $R_{StartUp}$=50 MΩ and V_{DRAIN}=90 V
	$I_{VCC\_Charge2}$	-	-3.2	-	mA	V_{VCC}=3 V, $R_{StartUp}$=50 MΩ and V_{DRAIN}=90 V
	$I_{VCC\_Charge3}$	-5	-3	-1	mA	V_{VCC}=15 V, $R_{StartUp}$=50 MΩ and V_{DRAIN}=90 V
Current Consumption, Startup Current	$I_{VCC\_Startup}$	-	0.19	-	mA	V_{VCC}=15 V
Current Consumption, Normal	I_{VCC_Normal}	-	0.9	-	mA	I_{FB}=0 A (No gate switching)
Current Consumption, Auto Restart	I_{VCC_AR}	-	320	-	µA	
Current Consumption, Burst Mode	$I_{VCC\_Burst Mode}$	-	0.5	-	mA	V_{FB}=1.8 V
VCC Turn-on Threshold Voltage	V_{VCC_ON}	15.3	16	16.5	V	
VCC Turn-off Threshold Voltage	V_{VCC_OFF}	9.5	10	10.5	V	
VCC Short Circuit Protection Voltage	V_{VCC_SCP}	-	1.1	1.9	V	
VCC Turn-off blanking	$t_{VCC\_OFF\_B}$	-	50	-	µs	

4.4 Internal Voltage Reference

Table 9 Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Internal Reference Voltage	V_{REF}	3.2	3.3	3.4	V	Measured at pin FB I_{FB}=0

4.5 Gate Driver

Table 10 Gate Driver

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage at logic low	V_{GATE_LOW}	-	-	1.00	V	
Output voltage at logic high	V_{GATE_HIGH}	7.5	10	13	V	
Rise Time	t_{GATE_RISE}	-	117	-	ns	Cout = 1nF
Fall Time	t_{GATE_FALL}	-	27	-	ns	Cout = 1nF

4.6 PWM Section

Table 11 PWM Section

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Feedback Pull-Up Resistor	R_{FB}	11	15	20	kΩ	
PWM-OP Gain	G_{PWM}	1.95	2.05	2.15	-	
Offset for Voltage Ramp	V_{PWM}	0.42	0.5	0.58	V	
Maximum on time in normal operation	t_{OnMax}	20	35	60	µs	
Maximum off time in normal operation	t_{OffMax}	24	42.5	71	µs	

4.7 Current Sense

Table 12 Current Sense

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Peak current limitation in normal operation	V_{CS_N}	0.94	1.00	1.06	V	
Leading Edge Blanking time	t_{CS_LEB}	118	220	462	ns	
Peak Current Limitation in Active Burst Mode – Level 1	V_{CS_BL1}	0.26	0.31	0.36	V	
Peak Current Limitation in Active Burst Mode – Level 2	V_{CS_BL2}	0.3	0.35	0.4	V	
Abnormal CS voltage threshold	V_{CS_STG}	0.06	0.10	0.15	V	
Abnormal CS voltage Consecutive Trigger	P_{CS_STG}	-	3	-	cycle	
Abnormal CS voltage Sample period	$t_{CS\_STG\_SAM}$	2.3	5	-	µs	

4.8 Soft Start

Table 13 Soft Start

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Soft-Start time	t_{SS}	8.5	12	-	ms	
Soft-start time step	t_{SS_S}[1]	-	3	-	ms	

[1] The parameter is not subjected to production test - verified by design/characterization

Internal regulation voltage at first step	V_{SS1}[1]	-	0.30	-	V	CS peak voltage
Internal regulation voltage step at soft start	V_{SS_S}[1]	-	0.15	-	V	CS peak voltage

4.9 Digital Zero Crossing

Table 14 Digital Zero Crossing

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Zero crossing threshold voltage	V_{ZCD_CT}	60	100	150	mV	
Zero crossing Ringing suppression threshold	V_{ZCD_RS}	-	0.45	-	V	
Minimum ringing suppression time	t_{ZCD_RS1}	1.5	2.5	4.1	µs	$V_{ZCD} > V_{ZCD\_RS}$ (except 1st 3 ms of soft-start)
Maximum ringing suppression time	t_{ZCD_RS2}	-	25	-	µs	$V_{ZCD} < V_{ZCD\_RS}$
Threshold to reset Up/Down Counter	V_{FB_R}	-	2.80	-	V	
Threshold for downward counting	V_{FB_HLC}	-	2.05	-	V	
Threshold for upward counting	V_{FB_LHC}	-	1.55	-	V	
Counter Time	t_{COUNT}	-	48	-	ms	
ZCD resistance	R_{ZCD}	2.5	3.0	3.5	kΩ	Internal resistor at ZCD pin
VIN voltage threshold for line selection	V_{VIN_REF}	1.48	1.52	1.58	V	
Blanking time for VIN voltage threshold for line selection	t_{VIN_REF}	-	16	-	ms	

4.10 Active Burst Mode

Table 15 Active Burst Mode

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Charging current to select burst mode	I_{sel}	2.1	3	3.9	µA	
Burst mode selection reference voltage	V_{REF_B}	2.65	2.75	2.85	V	
Feedback voltage for entering Active Burst Mode for level 1	V_{FB_EBL1}	0.86	0.9	0.94	V	

Feedback voltage for entering Active Burst Mode for level 2	V_{FB_EBL2}	1.0	1.05	1.1	V	
Blanking time for entering Active Burst Mode	t_{FB_BEB}	-	20	-	ms	
Feedback voltage for leaving Active Burst Mode	V_{FB_LB}	2.65	2.75	2.85	V	
Feedback voltage for burst-on	V_{FB_BOn}	2.3	2.4	2.5	V	
Feedback voltage for burst-off	V_{FB_BOff}	1.9	2.0	2.1	V	

4.11 Line Over Voltage Protection

Table 16 Line OVP

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line Over Voltage threshold	V_{VIN_LOVP}	2.8	2.9	3.0	V	
Line Over Voltage Blanking	$t_{VIN\_LOVP\_B}$	-	250	-	µs	

4.12 Brownout Protection

Table 17 Brownout Protection

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
BrownIn threshold	V_{VIN_BI}	0.63	0.66	0.69	V	
BrownIn Blanking	$t_{VIN\_BI\_B}$	-	250	-	µs	
BrownOut threshold	V_{VIN_BO}	0.37	0.40	0.43	V	
BrownOut Blanking	$t_{VIN\_BO\_B}$	-	250	-	µs	

4.13 V_{CC} Over Voltage Protection

Table 18 Vcc Over Voltage Protection

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC Over Voltage threshold	V_{VCC_OVP}	24	25.50	27	V	
VCC Over Voltage blanking	$t_{VCC\_OVP\_B}$	-	50	-	µs	

4.14 Over Load Protection

Table 19 Overload Protection

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		

Over Load Detection threshold for OLP protection at FB pin	V_{FB_OLP}	2.65	2.75	2.85	V	
Over Load Protection Blanking Time	$t_{FB\_OLP\_B}$	-	30	-	ms	

4.15 Output Over Voltage Protection

Table 20 Output OVP

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output Over Voltage threshold	V_{ZCD_OVP}	1.9	2	2.1	V	
Output Over Voltage Blanking Pulse	$P_{ZCD\_OVP\_B}$	-	10	-	pulse	Consecutive Pulse

4.16 Thermal Protection

Table 21 Thermal Protection

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Over temperature protection[1]	T_{jcon_OTP}	129	140	150	°C	Junction temperature of the controller chip
Over temperature Hysteresis[1]	T_{jHYS_OTP}	-	40	-	°C	
Over temperature Blanking Time	$t_{jcon\_OTP\_B}$	-	50	-	µs	

4.17 Low side MOSFET

Table 22 Low side MOSFET

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain Source On-Resistance	R_{DSon}	-	0.22	0.29	Ω	Tj = 25°C
		-	0.31[1]	-	Ω	Tj = 125°C

[1] The parameter is not subjected to production test - verified by design/characterization

5 Output power curve

The calculated output power curves versus ambient temperature are shown below. The curves are derived based on a typical DCM flyback in an open frame design setting the maximum T_J at 125 °C, using minimum pin copper area in a 2 oz copper single sided PCB and steady state operation only (no design margins for abnormal operation modes are included).

The output power figure is for reference only. The actual power can vary depending on a particular design. In a power supply system, appropriate thermal design margins must be considered to make sure that the operation of the device is within the maximum ratings given in section 4.1.

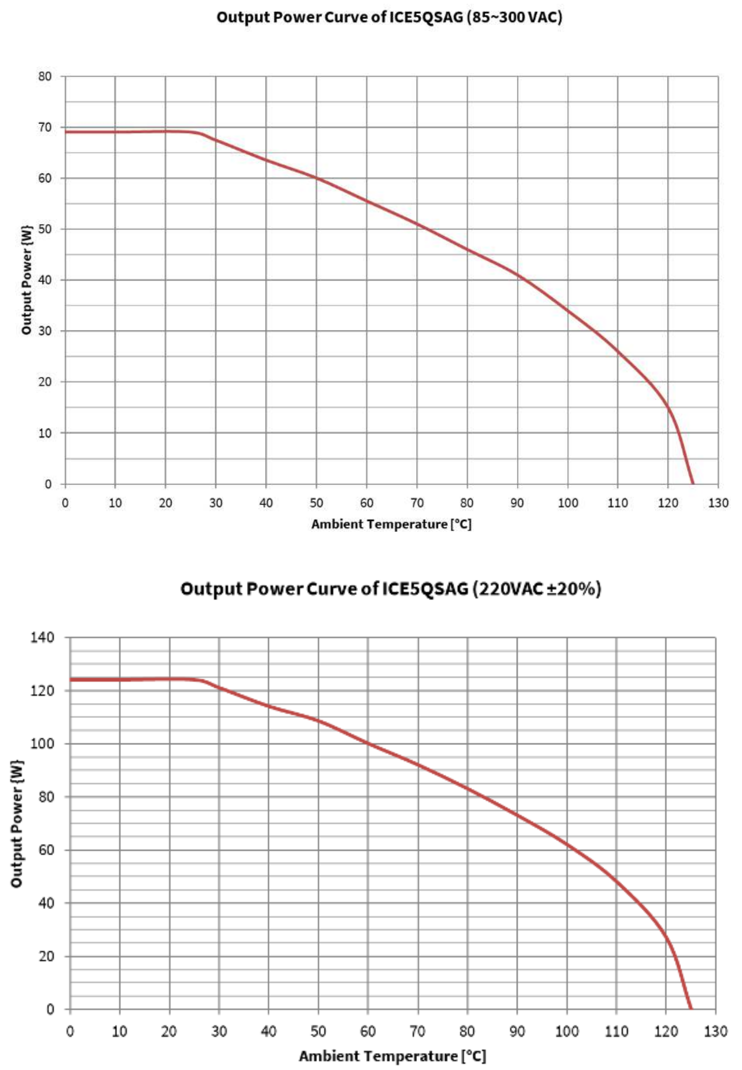
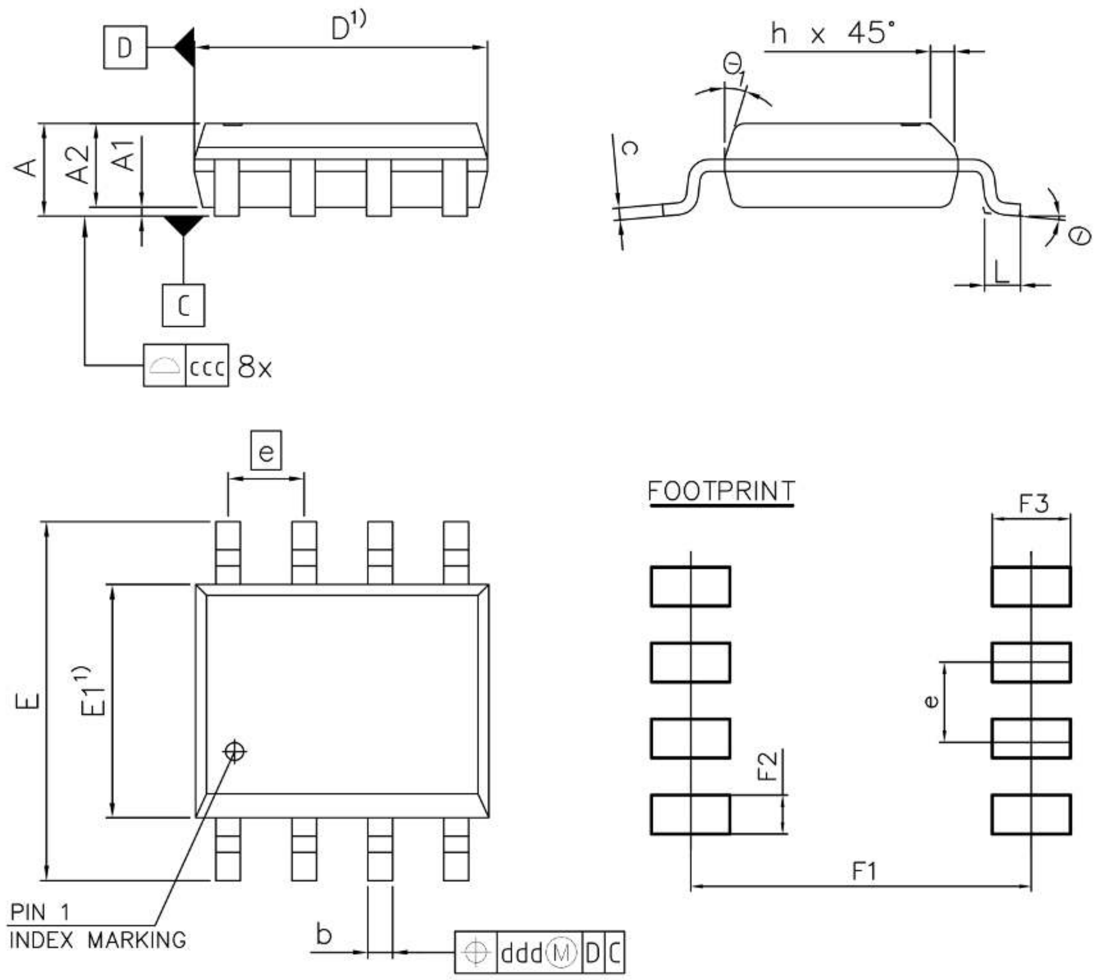


Figure 14 Output power curve of ICE5QSAG

6 Outline Dimension



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

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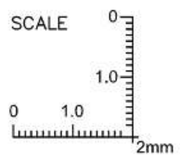

EUROPEAN PROJECTION

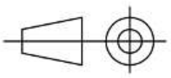

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Figure 15 **PG-DSO-8**

7 Marking

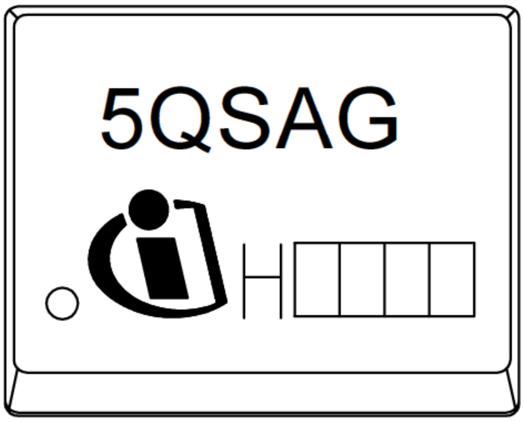

Figure 16 Marking for ICE5QSAG

Revision history

Document version	Date of release	Description of changes
V 1.2	10 Mar 2017	Page 1, 3 Updated features and description Page 6 ~ 14 Typo error
V 2.0	11 Aug 2017	Page 7 ~16 Text content revised
V 2.1	3 Feb 2020	Update of CS pin function and description (refer to errata sheet ES_2001_PL83_2002_024629)

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