REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added vendor CAGE 1ES66 to devices 03 and 04. Made changes to table I. Editorial changes throughout.	90-12-03	Michael Frye
B	Drawing updated to reflect current requirements. - lgt	01-07-16	Raymond Monnin

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	B	B	B																	
SHEET	15	16	17																	

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Rick C. Officer

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Raymond Monnin

APPROVED BY
Michael Frye

DRAWING APPROVAL DATE
12 July 1989

MICROCIRCUIT, LINEAR, CMOS 8-BIT A/D CONVERTER, MONOLITHIC SILICON

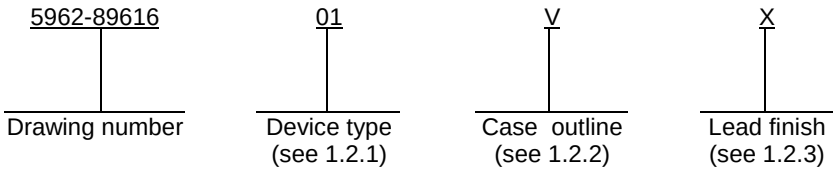
REVISION LEVEL	SIZE	CAGE CODE	
B	A	**67268**	**5962-89616**

SHEET 1 OF 17

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD-908A	CMOS microprocessor-compatible FAST 8-bit A/D converter
02	AD-908B	CMOS microprocessor-compatible FAST 8-bit A/D converter
03	PM-7574A	CMOS microprocessor-compatible 8-bit A/D converter
04	PM-7574B	CMOS microprocessor-compatible 8-bit A/D converter

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
V	GDIP1-T18 or CDIP2-T18	18	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V_{DD} to AGND ..... 0 V dc to +7.0 V dc
V_{DD} to DGND ..... 0 V dc to +7.0 V dc
AGND to DGND ..... ±0.3 V dc
Digital input voltage ($\overline{RD}$, $\overline{CS}$ pins) to DGND ..... -0.3 V dc to V_{DD}
Digital output voltage (D_{B0} – D_{B7}, $\overline{BUSY}$ pins) to DGND ..... -0.3 V dc to V_{DD}
Clock input voltage to (CLK pins) DGND ..... -0.3 V dc to V_{DD}
Voltage at V_{REF} ..... -0 V dc to -20 V dc
Voltage at V_{BOFS} ..... ±20 V dc
Voltage at V_{AIN} ..... ±20 V dc
Power dissipation (P_D) :
  To +75°C ..... 450 mW
  Derate above +75°C (cases V and 2) ..... 6.0 mW/°C
Ambient operating temperature range (T_A) ..... -55°C to +125°C
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction to case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, junction to ambient (θ_{JA})
  Cases V and 2 ..... 35°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{DD}) ..... +5 V dc
Reference voltage (V_{REF}) ..... -10 V dc
Ground ..... AGND = DGND = 0 V dc
Clock resistance (R_{CLK}) :
Devices 01 and 02 ..... 43 kΩ
Devices 03 and 04 ..... 150 kΩ
Clock capacitance (C_{CLK}) 100pF

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{DD} = +5 V, V_{REF} = -10 V AGND = DGND = 0 V Unipolar configuration unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Integral nonlinearity 1/	INL		1, 2, 3	01, 03		±0.5	LSB
				02, 04		±0.75	
Differential nonlinearity 1/	DNL		1, 2, 3	01, 03		±0.75	LSB
				02, 04		±0.875	
Gain error 2/	AE		1	01, 03		±3.0	LSB
				02, 04		±5.0	
			2, 3	01, 03		±4.5	
				02, 04		±6.5	
Offset error	VOS		1	01, 03		±30.0	mV
				02, 04		±60.0	
			2, 3	01, 03		±50.0	
				02, 04		±80.0	
Resistance mismatch B_{OFS} to A_{AIN}	ΔR_{AB}		1, 2, 3	01, 02		±1.0	%
				03, 04		±1.5	
Input resistance	R_{IN}	V_{REF} pins	1, 2, 3	ALL	5	15	kΩ
		B_{OFS} pins			10	30	
		A_{IN} pins			10	30	
Digital input high level	V_{IH}	$\overline{RD}$, $\overline{CS}$ 3/	1, 2, 3	ALL	2.4		V
Digital input low level	V_{IL}	$\overline{RD}$, $\overline{CS}$ 3/	1, 2, 3	ALL		0.8	V
Digital input current	I_{IN}	V_{IN} = 0 V or V_{DD}	1	ALL		±1.0	μA
			2, 3			±10.0	
Clock input high level	V_{IH}	Clock 3/	1, 2, 3	01, 02	2.4		V
				03, 04	3.0		
Clock input low level	V_{IL}	Clock 3/	1, 2, 3	01, 02		0.8	V
				03, 04		0.4	
Clock input high current	I_{IH}	Clock, V_{IN} = V_{DD}	1	ALL		±2.0	mA
Clock input low current	I_{IL}	Clock, V_{IN} = 0 V	1	ALL		±1.0	mA
			2, 3			±10.0	
Digital output high level D_{B7} – D_{B0}; $\overline{BUSY}$	V_{OH}	I_{SOURCE} = 40 μA	1, 2, 3	ALL	4.0		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{DD} = +5 V, V_{REF} = -10 V AGND = DGND = 0 V Unipolar configuration unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital output low level $D_{B7} - D_{B0}$; $\overline{BUSY}$	V_{OL}	I_{SINK} = 1.6 mA	1, 2, 3	ALL		0.4	V
Floating state leakage current ($D_{B7} - D_{B0}$)	I_{LKG}	V_0 = 0 V or V_{DD}	1	ALL		±1.0	µA
			2, 3			±10.0	
Supply current from V_{DD}	I_{DD}	A_{IN} = 0 V, $\overline{BUSY}$ and RD high	1, 2, 3	01, 02		2.5	mA
				03, 04		5.0	
Digital input capacitance	C_{IN}	See 4.3.1c	4	ALL		5.0	pF
Floating state output capacitance ($D_{B7} - D_{B0}$)	C_{OUT}	See 4.3.1c	4	ALL		7.0	pF
Functional test		See 4.3.1d	7, 8	ALL			
$\overline{CS}$ pulse width 4/	t_{CS}		9	01, 02	60		ns
			10, 11		90		
			9, 10, 11	03, 04	150		
$\overline{RD}$ to $\overline{CS}$ setup time 5/	t_{WSCS}		9, 10, 11	ALL	0		ns
$\overline{CS}$ to $\overline{BUSY}$ 5/ propagational delay	t_{CBPD}	$\overline{BUSY}$ load = 20 pF	9	01, 02		120	
				03, 04		180	ns
			10, 11	01, 02		150	
				03, 04		180	
		$\overline{BUSY}$ load = 100 pF	9	01, 02		150	
				03, 04		200	
			10, 11	ALL		200	
$\overline{BUSY}$ to $\overline{RD}$ 4/ setup time	t_{BSR}		9, 10, 11	ALL	0		ns
$\overline{BUSY}$ to $\overline{CS}$ 4/ setup time	t_{BSCS}		9, 10, 11	ALL	0		ns
Data valid 4/ propagational delay	t_{RAD}	Load = 20 pF	9	01, 02		140	ns
			10, 11			200	
			9, 10, 11	03, 04		220	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{DD} = +5 V, V_{REF} = -10 V AGND = DGND = 0 V Unipolar configuration unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data valid propagational delay 5/	t_{RAD}	Load = 100 pF	9	01, 02		170	ns
			10, 11			230	
			9, 10, 11	03, 04		400	
Data valid hold time 4/	t_{RHD}		9	01, 02	30	100	ns
			10, 11		40	140	
			9, 10, 11	03, 04	80	180	
$\overline{CS}$ to $\overline{RD}$ hold time 4/	t_{RHCS}		9	01, 02		200	ns
			10, 11			250	
			9, 10, 11	03, 04		500	
Reset time requirement 4/	t_{RESET}		9	01, 02	450		ns
			10, 11		500		
			9, 10, 11	03, 04	3.0		µs
$\overline{RD}$ to $\overline{BUSY}$ propagation delay 4/	t_{WBPD}	$\overline{BUSY}$ load = 20 pF	9	01, 02		600	ns
			10, 11			800	
			9, 10, 11	03, 04		2	µs
Conversion time 1/ 5/	t_C		9, 10, 11	01, 02		6	µs
				03, 04		15	

1/ Devices 01 and 02 measured using external clock frequency of 1.35 MHz. Devices 03 and 04 measured using external clock frequency of 550 kHz. See timing waveforms on figure 3.

2/ Gain error is measured after calibration out offset error.

3/ Guaranteed by functional pattern testing in external clock RAM, ROM, and SLOW modes.

4/ Static RAM interface mode.

5/ If not tested, shall be guaranteed to the limits specified in table I.

Device type	01, 02, 03, and 04	
Case outline	V	2
Terminal Number	Terminal symbol	
1	V_{DD}	NC
2	V_{REF}	V_{DD}
3	B_{OFS}	V_{REF}
4	A_{IN}	B_{OFS}
5	AGND	A_{IN}
6	D_{B7}	AGND
7	D_{B6}	D_{B7}
8	D_{B5}	D_{B6}
9	D_{B4}	D_{B5}
10	D_{B3}	D_{B4}
11	D_{B2}	NC
12	D_{B1}	D_{B3}
13	D_{B0}	D_{B2}
14	$\overline{BUSY}$	D_{B1}
15	$\overline{RD}$	D_{B0}
16	$\overline{CS}$	$\overline{BUSY}$
17	CLK	$\overline{RD}$
18	DGND	$\overline{CS}$
19	-------	CLK
20	-------	DGND

NC = No connection

FIGURE 1. Terminal connections.

Device types 01 and 02.

Truth table, static RAM mode

Inputs		Outputs		Operation
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	$D_{B7} - D_{B0}$	
L	H	H	High Z	Start convert (write cycle)
L	↓	H	High Z to Data	Read data (read cycle)
L	↑	H	Data to High Z	Reset converter
H	X (See note)	X	High Z	No effect (not selected)
L	H	L	High Z	No effect (converter busy)
L	↓	L	High Z	No effect (converter busy)
L	↑ (See note)	L	High Z	Conversion error not allowed

L = Low H = High X = Don't care ⌐ = Low to high transition ⌐ = High to low transition

NOTE: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

FIGURE 2. Truth tables.

Device types 03 and 04.

Static RAM mode

Inputs		Outputs		Operation
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	$D_{B7} - D_{B0}$	
↓	H	↓	High Z	Start convert (write cycle)
L	↓	H	High Z to Data	Read data (read cycle)
L	↑	H	Data to High Z	Reset converter
H	X (See note)	X	High Z	No effect (not selected)
L	H	L	High Z	No effect (converter busy)
L	↓	L	High Z	No effect (converter busy)
L	↑ (See note)	L	High Z	Conversion error not allowed

L = Low H = High X = Don't care ↑ = Low to high transition ↓ = High to low transition

NOTE: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

FIGURE 2. Truth tables – Continued.

Device types 01, 02, 03, and 04.

Slow-memory mode

Inputs	Outputs		Operation
$\overline{CS}$ and $\overline{RD}$	$\overline{BUSY}$	$D_{B7} - D_{B0}$	
H	H	High Z	No effect (not selected)
⎍	⎍	High Z	Start conversion
L	L	High Z	Conversion in progress μP in WAIT state
L	⎍ (See note)	High Z to Data	Conversion complete read data
⎍ (See note)	H	Data to High Z	Reset and deselect converter

L = Low H = High ⎍ = Low to high transition ⎍ = High to low transition

NOTE: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

FIGURE 2. Truth tables – Continued.

Device types 01, 02, 03, and 04.

ROM mode

Inputs		Outputs		Operation
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	$D_{B7} - D_{B0}$	
L	↓	H	High Z to Data	Read data
L	↑	↓	Data to High Z	Reset and start new converter
L	↓	L	High Z	No effect (converter busy)
L	↑ (See note)	L	High Z	Conversion error not allowed

L = Low H = High ⌐¬ = Low to high transition ¬⌐ = High to low transition

NOTE: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

FIGURE 2. Truth tables – Continued.

STATIC RAM MODE

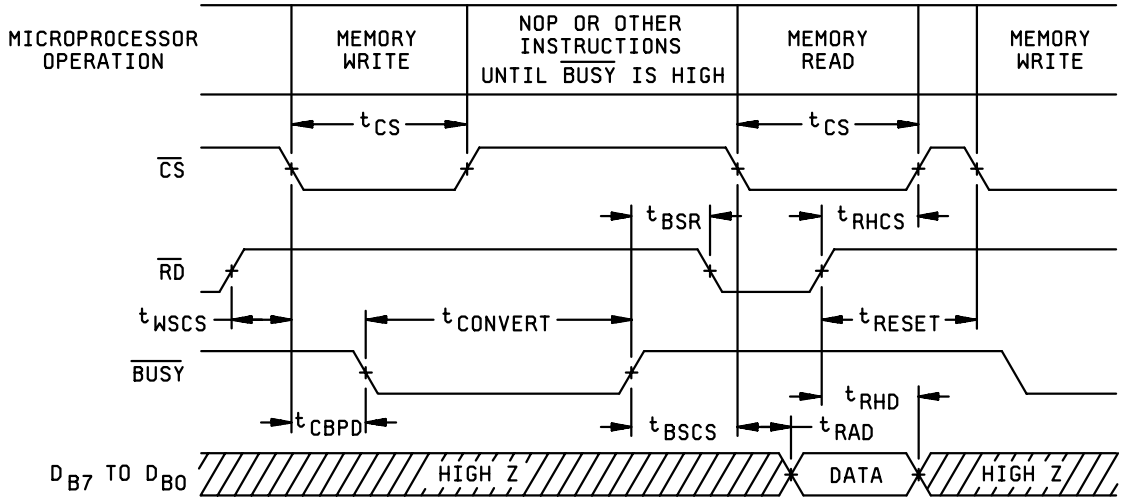
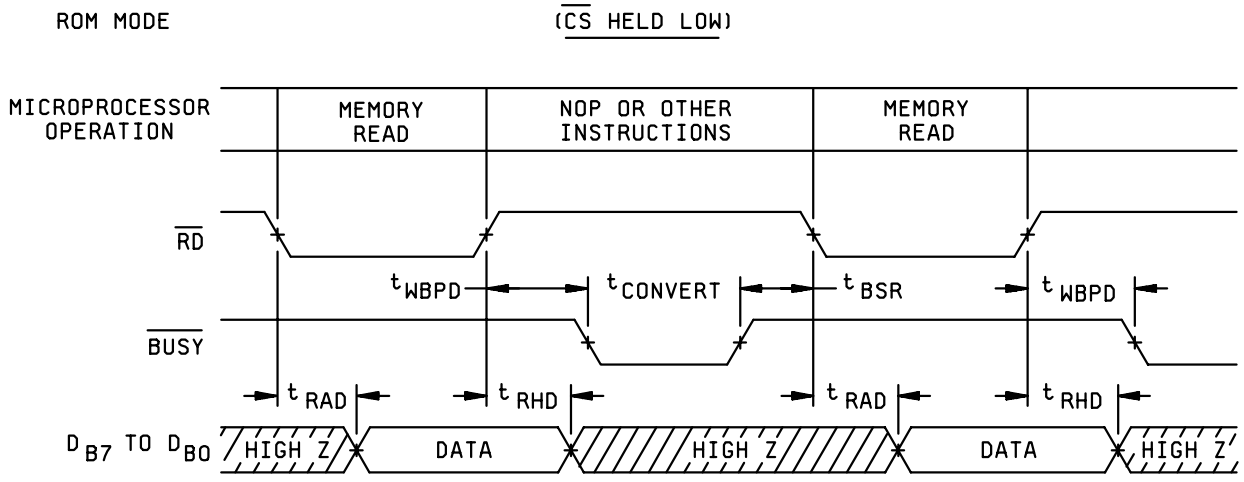
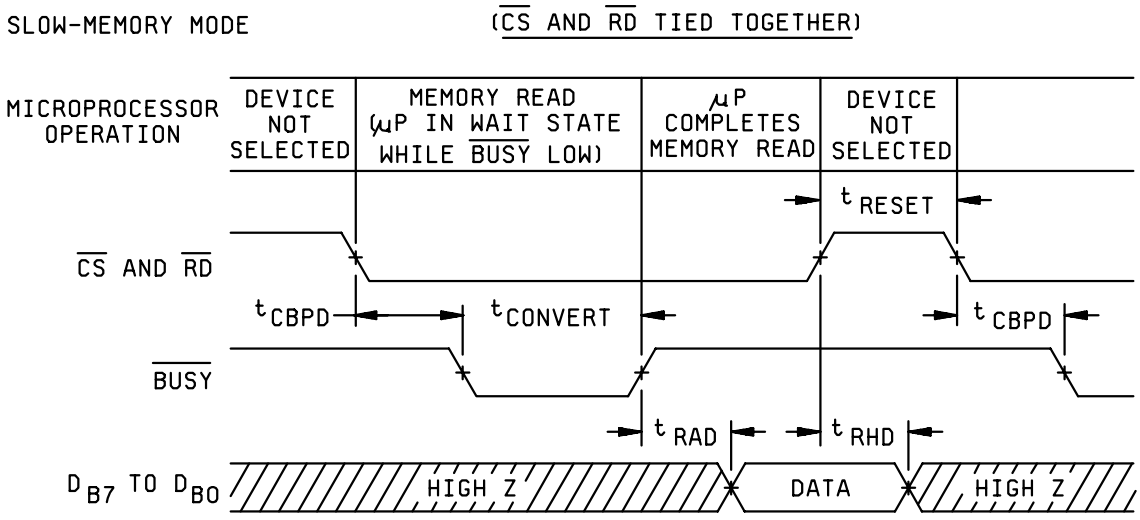


FIGURE 3. Timing waveforms.



NOTE: For device types 01 and 02, t_{RAD} timing is measured at +2 V and +0.8 V.

FIGURE 3. Timing waveforms - Continued.



Note: For device types 01 and 02, t_{RAD} timing is measured at +2 V and +0.8 V.

FIGURE 3. Timing waveforms - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3
Group A test requirements (method 5005)	1, 2, 3, 4, 7**, 8**, 9, 10***, 11***
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** See 4.3.1d
*** Subgroups 10 and 11 are guaranteed if not tested.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-07-16

Approved sources of supply for SMD 5962-89616 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8961601VA	24355	ADC-908AX
5962-8961602VA	24355	ADC-908BX
5962-89616022A	24355	ADC-908RC
5962-8961603VA	24355	PM-7574AX
	1ES66	MX7574TQ/883B
5962-89616032C	1ES66	MX7574TE/883B
5962-8961604VA	24355	PM-7574BX
	1ES66	MX7574SQ/883B
5962-89616042A	24355	PM-7574BRC
5962-89616042C	1ES66	MX7574SE/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices, Inc. Rt. 1 Industrial Park P.O. Box 9106 Norwood, Ma. 02062 Point of Contact: 1500 Space Park Dr. P.O. Box 58020 Santa Clara, Ca. 95050-8020
1ES66	Maxim Integrated Products 120 San Gabriel DR Sunnyvale, CA 94086