Dual High-Efficiency PWM Step-Down DC/DC Converter

General Description

The RT8020 is a dual high-efficiency Pulse-Width-Modulated (PWM) step-down DC/DC converter. It is capable of delivering 1A output current over a wide input voltage range from 2.5V to 5.5V, the RT8020 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources within the range such as cellular phones, PDAs and other hand-held devices.

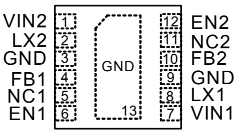
Two operational modes are available : PWM/Low-Dropout auto-switch and shutdown modes. Internal synchronous rectifier with low $R_{DS(ON)}$ dramatically reduces conduction loss at PWM mode. No external Schottky diode is required in practical application.

The RT8020 enters Low-Dropout mode when normal PWM cannot provide regulated output voltage by continuously turning on the upper PMOS. The RT8020 enter shutdown mode and consumes less than 0.1μA when EN pin is pulled low.

The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operation frequency of 1.5MHz. This along with small WDFN-12L 3x3 package provides small PCB area application. Other features include soft start, lower internal reference voltage with 2% accuracy, over temperature protection, and over current protection.

Pin Configurations

(TOP VIEW)



WDFN-12L 3x3

Features

- **2.5V to 5.5V Input Range**
- **Adjustable Output From 0.6V to V_{IN}**
- **1.2V, 1.3V, 1.8V, 2.5V and 3.3V Fixed/ Adjustable Output Voltage**
- **1A Output Current**
- **95% Efficiency**
- **No Schottky Diode Required**
- **50μA Quiescent Current per Channel**
- **1.5MHz Fixed Frequency PWM Operation**
- **Small 12-Lead WDFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Mobile Phones
- Personal Information Appliances
- Wireless and DSL Modems
- MP3 Players
- Portable Instruments

Ordering Information

RT8020☐☐☐

Package Type
QW : WDFN-12L 3x3 (W-Type)
(Exposed Pad-Option 1)

Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)

Output Voltage : VOUT1/VOUT2
Default : Adjustable
A : 3.3V/1.8V
B : 3.3V/1.3V
C : 3.3V/1.2V
D : 2.5V/1.8V

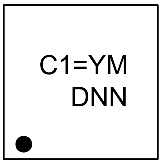
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT8020GQW



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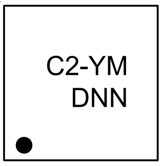
YMDNN : Date Code

RT8020APQW



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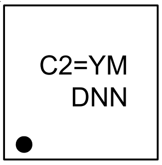
RT8020AGQW



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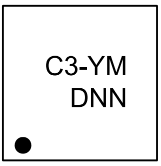
RT8020BPQW



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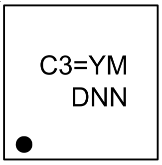
RT8020BGQW



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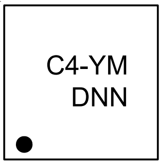
RT8020CPQW



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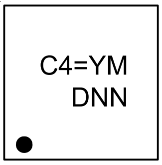
YMDNN : Date Code

RT8020CGQW



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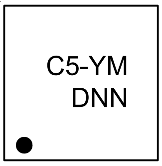
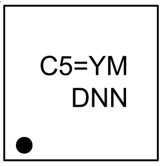
RT8020DPQW



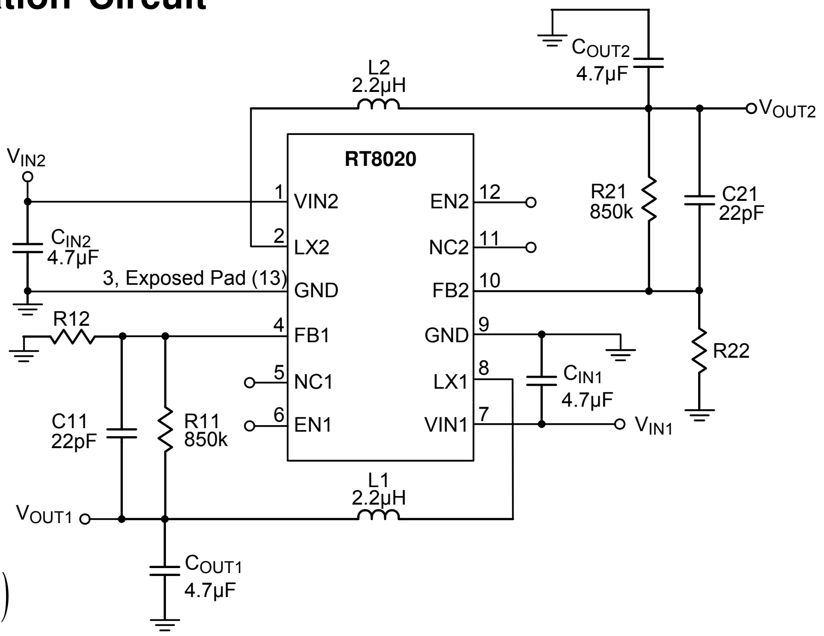
C5- : Product Code
YMDNN : Date Code

RT8020DGQW



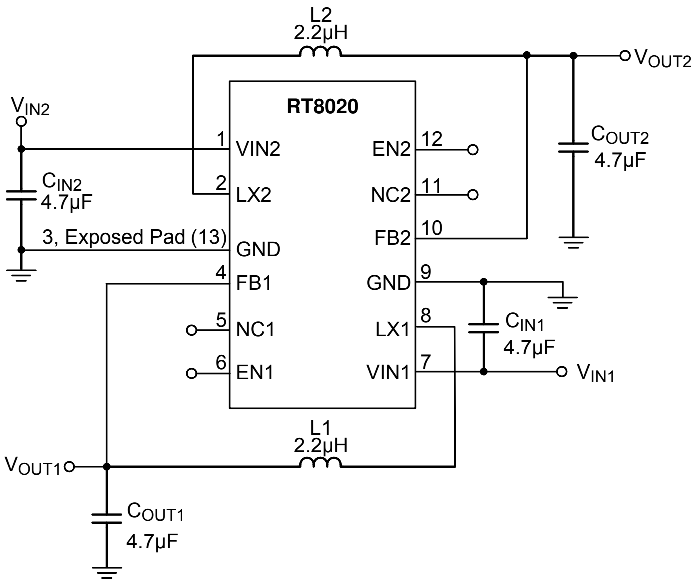
C5=: Product Code
YMDNN : Date Code

Typical Application Circuit



$$V_{OUTx} = V_{REF} \times \left(1 + \frac{Rx1}{Rx2}\right)$$

Figure 1. Adjustable Voltage Regulator



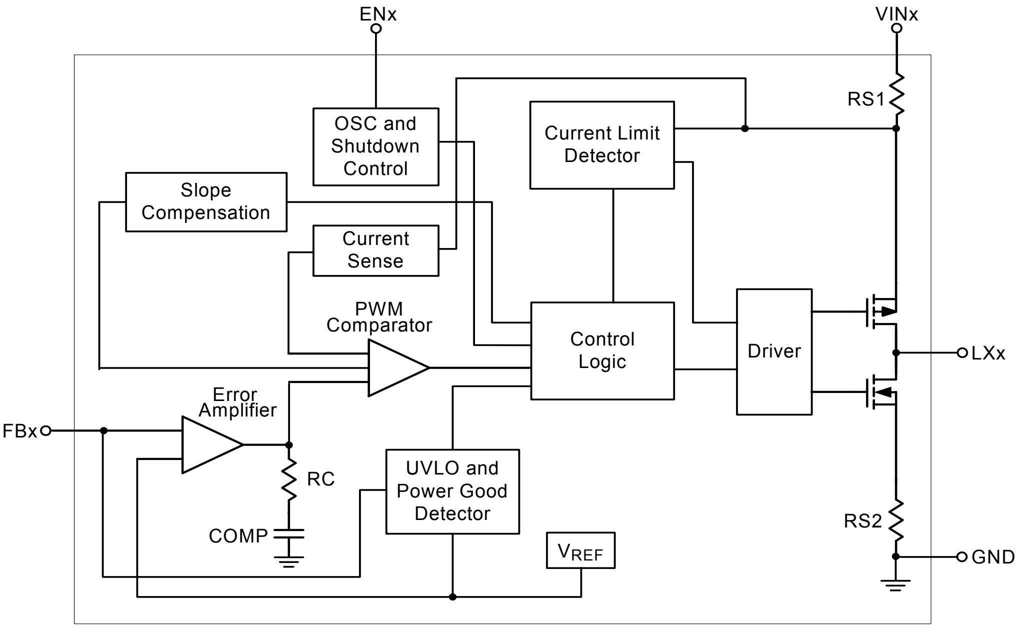
V_{OUTx} = 1.2V, 1.3V, 1.8V, 2.5V or 3.3V

Figure 2. Fixed Voltage Regulator

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN2	Power Input of Channel 2.
2	LX2	Pin for Switching of Channel 2.
3, 9, Exposed Pad (13)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	FB1	Feedback of Channel 1.
5, 11	NC1, NC2	No Connection or Connect to V_{IN}.
6	EN1	Chip Enable of Channel 1 (Active High). $V_{EN1} \leqq V_{IN1}$.
7	VIN1	Power Input of Channel 1.
8	LX1	Pin for Switching of Channel 1.
10	FB2	Feedback of Channel 2.
12	EN2	Chip Enable of Channel 2 (Active High). $V_{EN2} \leqq V_{IN2}$.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN1}, V_{IN2}	–0.3V to 6.5V
- EN1, FB1, LX1, EN2, FB2 and LX2 Pin Voltage	–0.3V to (V_{IN} + 0.3V)
- LX1 to GND, LX2 to GND (<200ns)	–1.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C	
WDFN-12L 3x3	1.667W
- Package Thermal Resistance (Note 2)	
WDFN-12L 3x3, θ_{JA}	60°C/W
WDFN-12L 3x3, θ_{JC}	8.2°C/W
- Lead Temperature (Soldering, 10 sec.)	260°C
- Junction Temperature	150°C
- Storage Temperature Range	–65°C to 150°C
- ESD Susceptibility (Note 3)	
HBM (Human Body Model)	2kV
MM (Machine Model)	200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage	2.5V to 5.5V
- Junction Temperature Range	–40°C to 125°C
- Ambient Temperature Range	–40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 2.5V, V_{REF} = 0.6V, L = 2.2uH, C_{IN} = 4.7μF, C_{OUT} = 10μF, T_A = 25°C, I_{MAX}= 1A unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Channel 1 and Channel 2							
Input Voltage Range		V_{IN}		2.5	--	5.5	V
Under Voltage Lock Out threshold		UVLO		--	1.8	--	V
Hysteresis				--	0.1	--	V
Quiescent Current		I_Q	I_{OUT} = 0mA, V_{FB} = V_{REF} + 5%	--	50	70	μA
Shutdown Current		I_{SHDN}	EN = GND	--	0.1	1	μA
Reference Voltage		V_{REF}	For Adjustable Output Voltage	0.588	0.6	0.612	V
Adjustable Output Voltage Range		V_{OUT}	(Note 6)	V_{REF}	--	$V_{IN} - \Delta V$	V
Output Voltage Accuracy	Fix	ΔV_{OUT}	V_{IN} = 2.5V to 5.5V, V_{OUT} = 1.2V 0A < I_{OUT} < 1A	–3	--	3	%
		ΔV_{OUT}	V_{IN} = 2.5V to 5.5V, V_{OUT} = 1.3V 0A < I_{OUT} < 1A	–3	--	3	%
		ΔV_{OUT}	V_{IN} = 2.5 to 5.5V, V_{OUT} = 1.8V 0A < I_{OUT} < 1A	–3	--	3	%
		ΔV_{OUT}	V_{IN} = V_{OUT} + ΔV to 5.5V (Note 5) V_{OUT} = 2.5V, 0A < I_{OUT} < 1A	–3	--	3	%
		ΔV_{OUT}	V_{IN} = V_{OUT} + ΔV to 5.5V (Note 5) V_{OUT} = 3.3V, 0A < I_{OUT} < 1A	–3	--	3	%

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage Accuracy	Adjustable	ΔV_{OUT}	V_{IN} = V_{OUT} + ΔV to 5.5V (Note 5) 0A < I_{OUT} < 1A		–3	--	3	%
FB Input Current		I_{FB}	V_{FB} = V_{IN}		–50	--	50	nA
$R_{DS(ON)}$ of P-MOSFET		$R_{DS(ON)\_P}$	I_{OUT} = 200mA	V_{IN} = 2.5V	--	0.38	--	Ω
				V_{IN} = 3.6V	--	0.28	--	
$R_{DS(ON)}$ of N-MOSFET		$R_{DS(ON)\_N}$	I_{OUT} = 200mA	V_{IN} = 2.5V	--	0.35	--	Ω
				V_{IN} = 3.6V	--	0.25	--	
P-Channel Current Limit		I_{LIM_P}	V_{IN} = 2.5V to 5.5 V		1.4	1.5	--	A
EN Input Voltage	Logic-High	V_{EN_H}	V_{IN} = 2.5V to 5.5V		1.5	--	V_{IN}	V
	Logic-Low	V_{EN_L}	V_{IN} = 2.5V to 5.5V		--	--	0.4	
Oscillator Frequency		f_{OSC}	V_{IN} = 3.6V, I_{OUT} = 100mA		1.2	1.5	1.8	MHz
Thermal Shutdown Temperature		T_{SD}			--	160	--	°C
Maximum Duty Cycle					100	--	--	%
LX Leakage Current		I_{LX}	V_{IN} = 3.6V, V_{LX} = 0V or V_{LX} = 3.6V		–1	--	1	μA

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

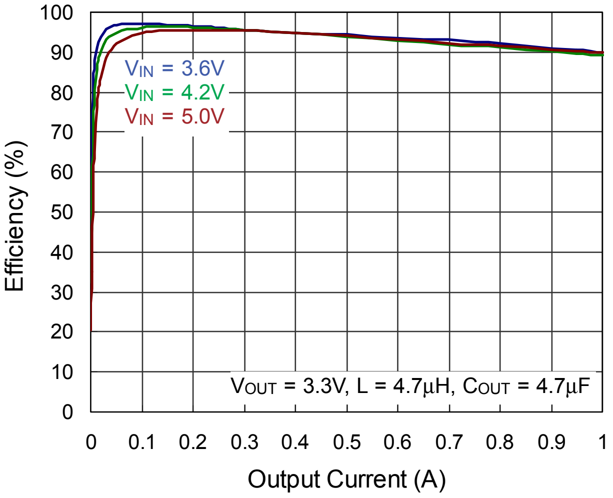
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. $\Delta V = I_{OUT} \times P_{RDS(ON)}$

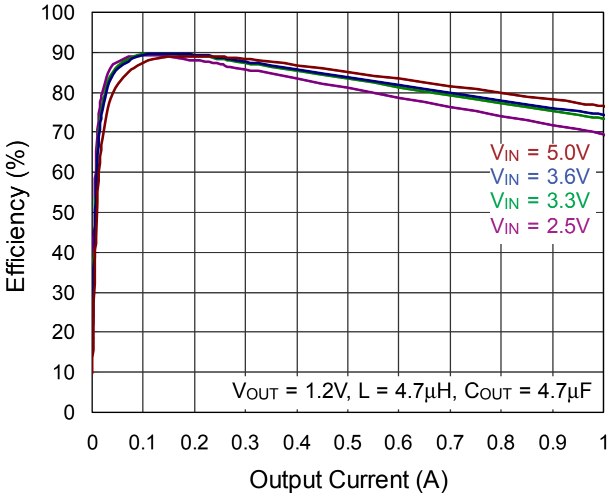
Note 6. Guarantee by design.

Typical Operating Characteristics

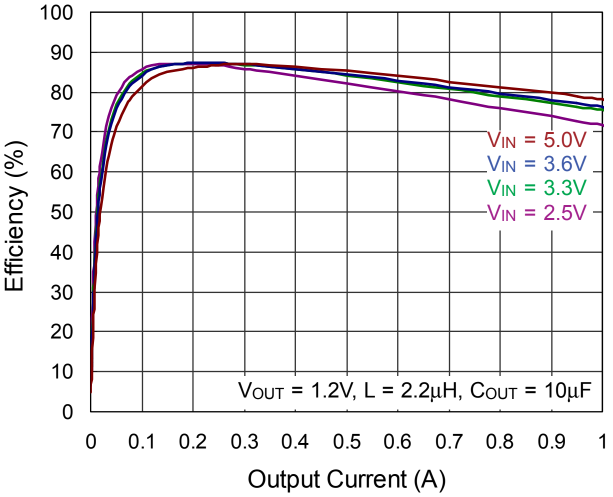
Efficiency vs. Output Current



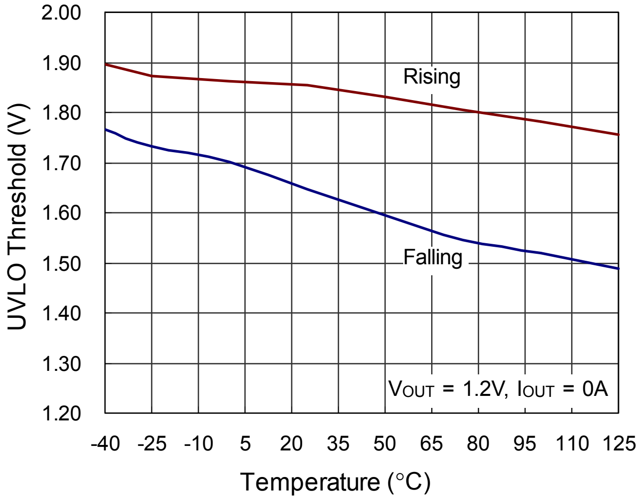
Efficiency vs. Output Current



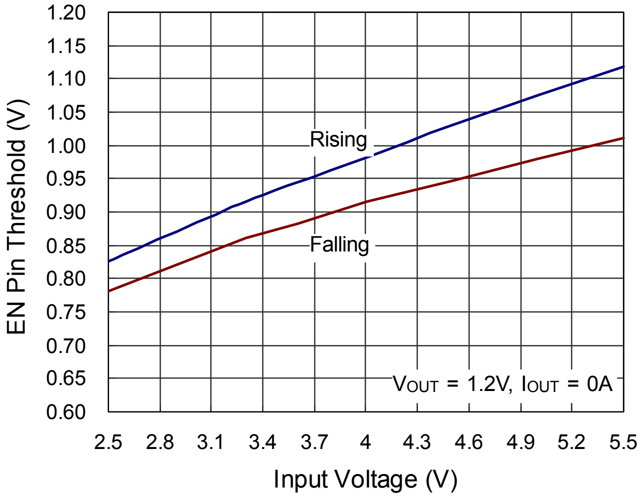
Efficiency vs. Output Current



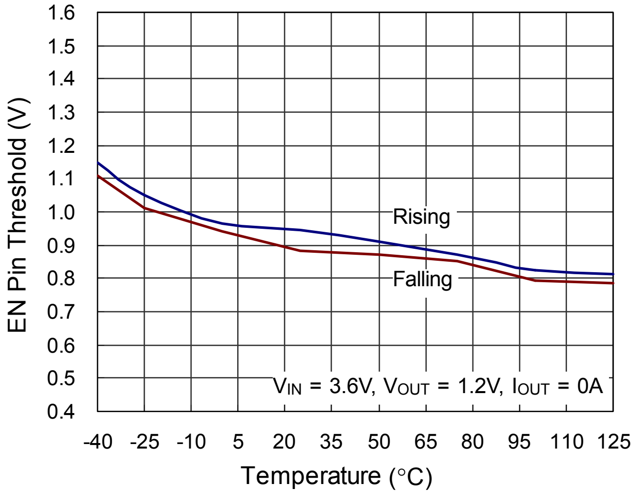
UVLO Threshold vs. Temperature

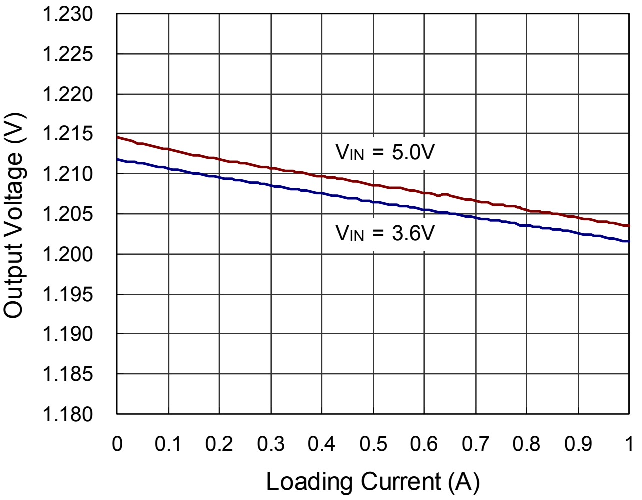


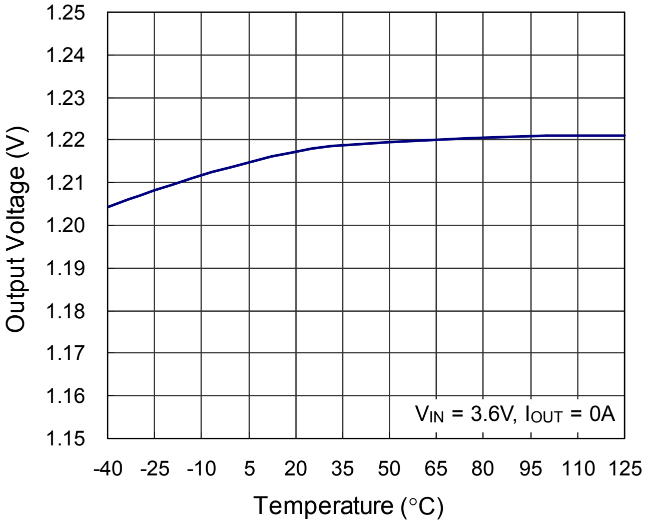
EN Pin Threshold vs. Input Voltage

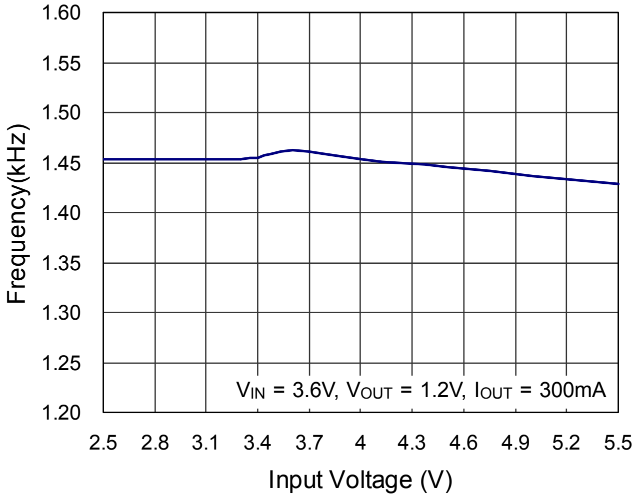


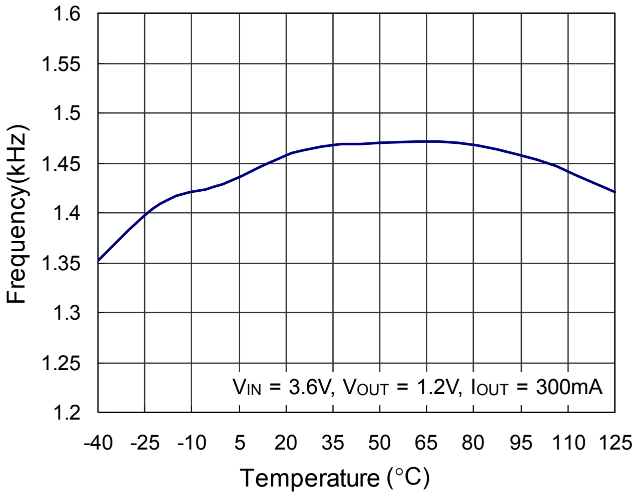
EN Pin Threshold vs. Temperature

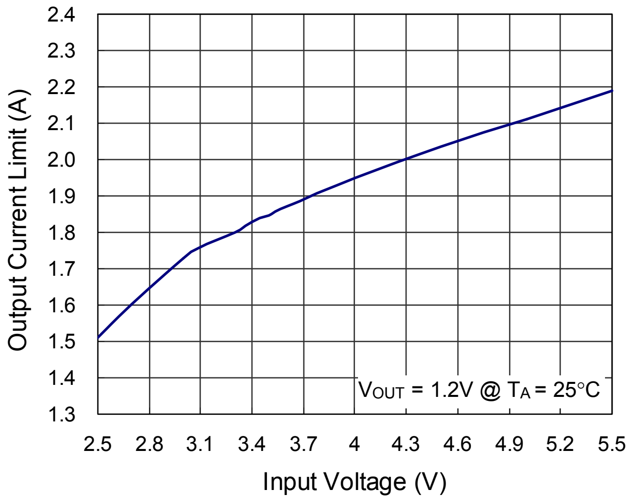


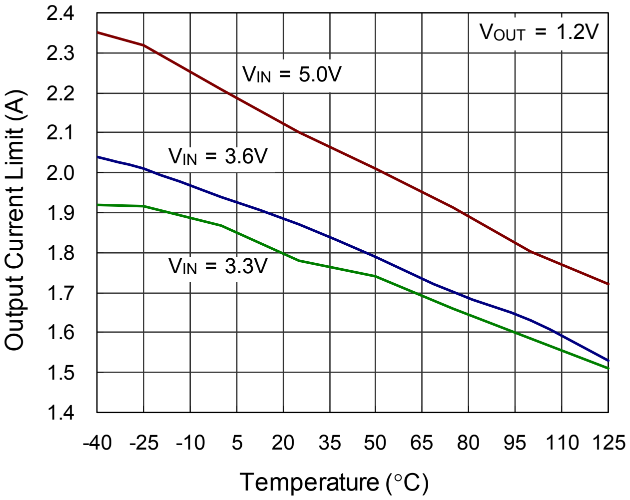

Output Voltage vs. Loading Current


Output Voltage vs. Temperature

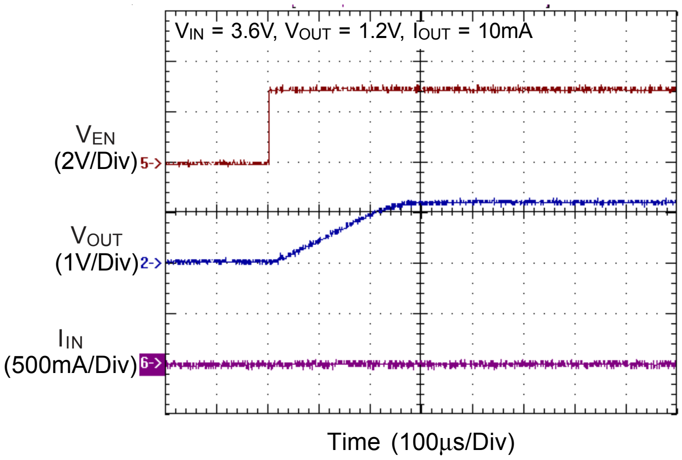

Switching Frequency vs. Input Voltage


Switching Frequency vs. Temperature

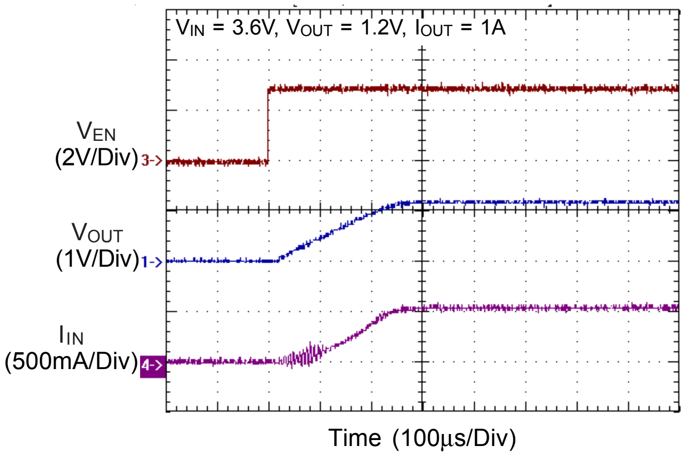

Output Current Limit vs. Input Voltage


Output Current Limit vs. Temperature

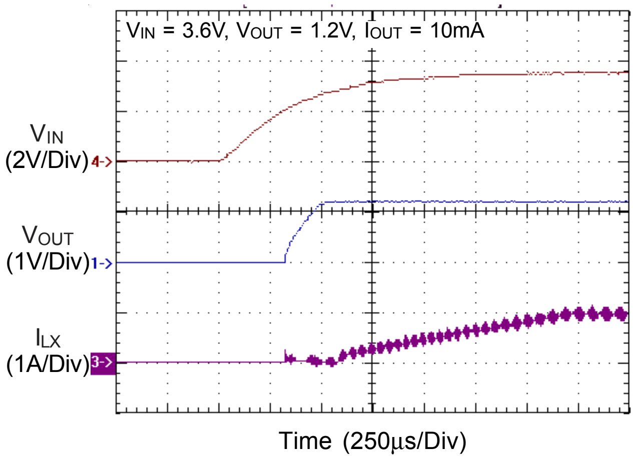
Power On from EN



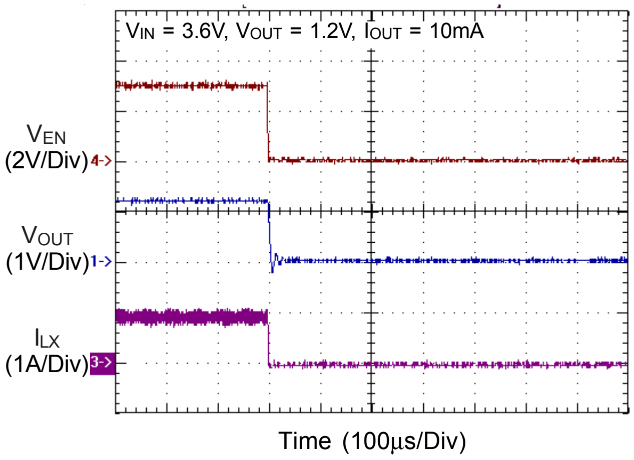
Power On from EN



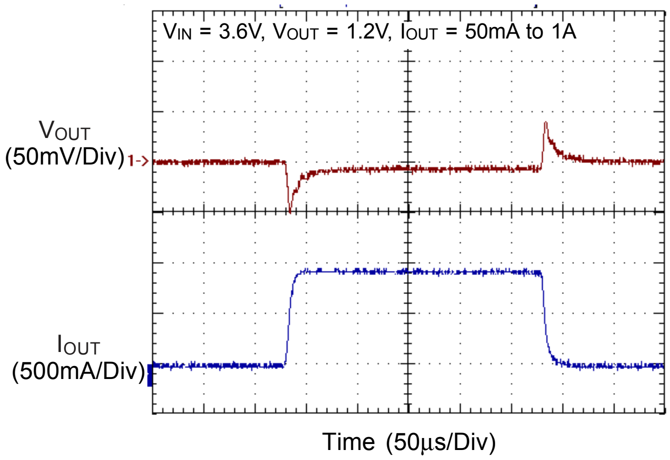
Power On from V_{IN}



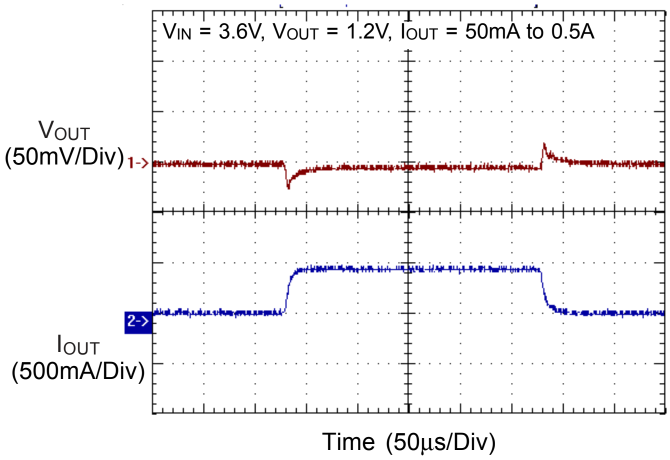
Power Off from EN



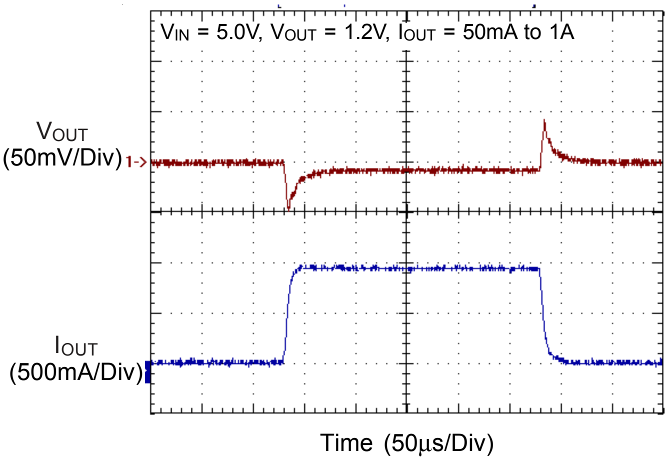
Load Transient Response



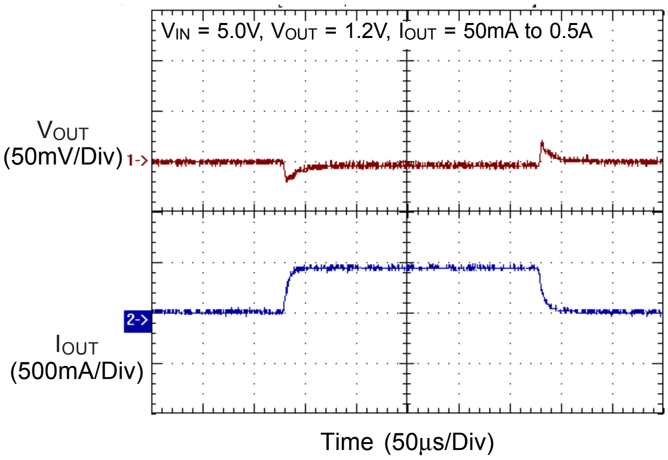
Load Transient Response



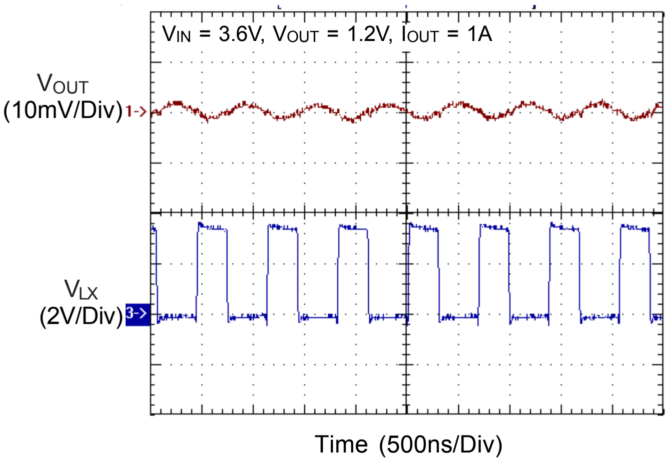
Load Transient Response



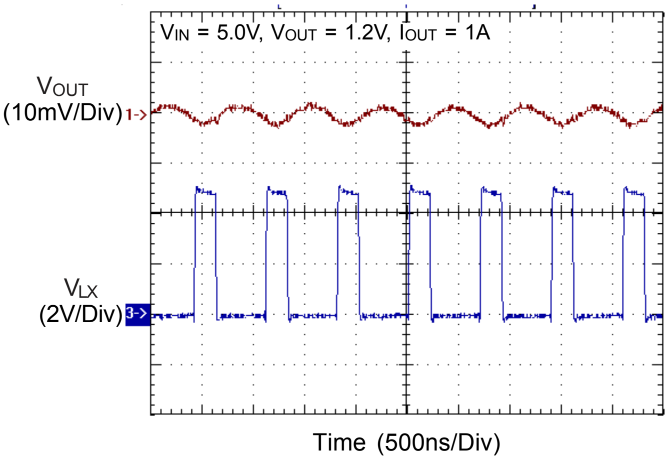
Load Transient Response



Ripple



Ripple



Applications Information

The basic RT8020 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or permalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. However, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates " hard" , which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depend on the price vs. size requirements and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Programming

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 3.

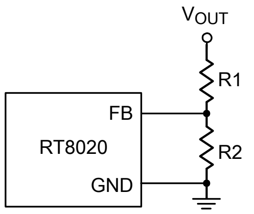


Figure 3. Setting the Output Voltage

For adjustable voltage mode, the output voltage is set by an external resistive divider according to the following equation :

$V_{OUT} = V_{REF} \times (1 + R1/R2)$

Where V_{REF} is the internal reference voltage (0.6V typical)

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as :

Efficiency = 100% − (L1+ L2+ L3+...)

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I^2R losses.

The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1.The V_{IN} quiescent current appears due to two components : the DC bias current and the gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ moves from V_{IN} to ground.

The resulting $\Delta Q/\Delta t$ is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode,

$I_{GATECHG} = f(Q_T + Q_B)$

where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. In continuous mode the average output current flowing

through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) is shown as follows :

$R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1 - DC)$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current. Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Thermal Considerations

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating conditions specification of RT8020 DC/DC converter, where $T_{J(MAX)}$ is the maximum junction temperature of the die and T_A is the ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WDFN-12L 3x3 packages, the thermal resistance θ_{JA} is 60°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (60°C/W) = 1.667W for WDFN-12L 3x3 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. The Figure 4 of de-rating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

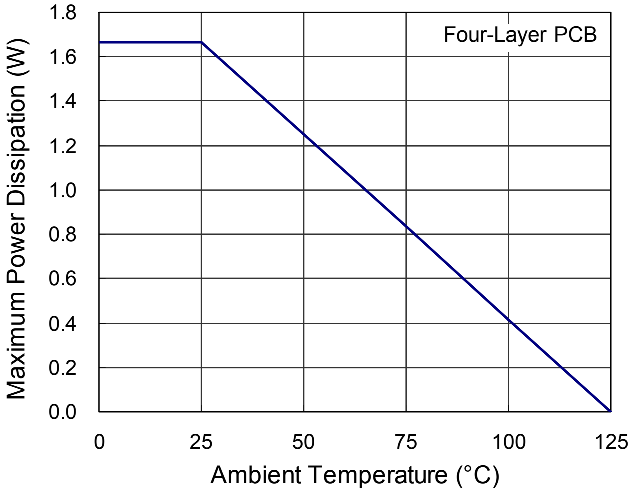


Figure 4. Derating Curve of Maximum Power Dissipation

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Layout Considerations

Follow the PCB layout guidelines for optimal performance of RT8020.

- For the main current paths, keep their traces short and wide.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8020.
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

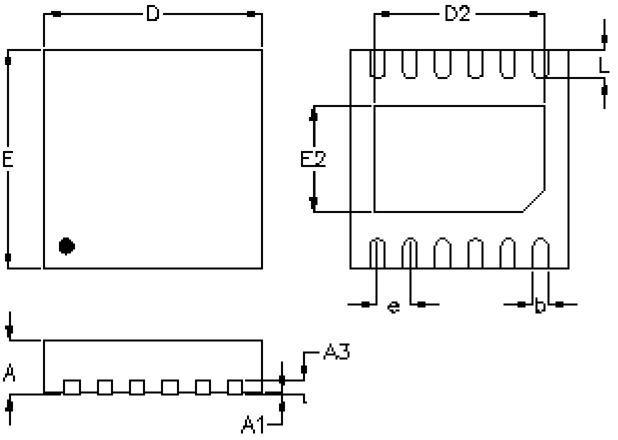
Table 1. Recommended Inductors

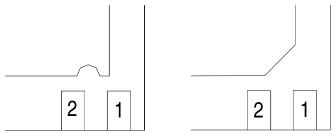
Component Supplier	Series	Inductance (μH)	DCR (mΩ)	Current Rating (mA)	Dimensions (mm)
TAIYO YUDEN	NR 3015	2.2	60	1480	3 x 3 x 1.5
TAIYO YUDEN	NR 3015	4.7	120	1020	3 x 3 x 1.5
Sumida	CDRH2D14	2.2	75	1500	4.5 x 3.2 x 1.55
Sumida	CDRH2D14	4.7	135	1000	4.5 x 3.2 x 1.55
GOTREND	GTSD32	2.2	58	1500	3.85 x 3.85 x 1.8
GOTREND	GTSD32	4.7	146	1100	3.85 x 3.85 x 1.8

Table 2. Recommended Capacitors for C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (μF)	Case Size
TDK	C1608JB0J475M	4.7	0603
TDK	C2012JB0J106M	10	0805
MURATA	GRM188R60J475KE19	4.7	0603
MURATA	GRM219R60J106ME19	10	0805
TAIYO YUDEN	JMK107BJ475RA	4.7	0603
TAIYO YUDEN	JMK107BJ106MA	10	0603
TAIYO YUDEN	JMK212BJ106RD	10	0805

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		2.950	3.050	0.116	0.120
D2	Option1	2.300	2.650	0.091	0.104
	Option2	1.970	2.070	0.078	0.081
E		2.950	3.050	0.116	0.120
E2	Option1	1.400	1.750	0.055	0.069
	Option2	1.160	1.260	0.046	0.050
e		0.450		0.018	
L		0.350	0.450	0.014	0.018

W-Type 12L DFN 3x3 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789