Evaluation Board User Guide
UG-566

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240 W Evaluation Board Kit for the ADP1051, Digital Controller for Isolated Power Supply with PMBus Interface

FEATURES

- Full support evaluation kit for the ADP1051
- 240 W full bridge topology (adjustable to phase shifted full bridge topology or half bridge topology)
- Input voltage range: 36 V dc to 75 V dc
- Output voltage: 12 V dc
- Nominal output current: 20 A
- Direct paralleling with multiple boards connected to a common bus
- Synchronization as master device and slave device
- Droop current sharing and analog current sharing extension
- On-board tests for housekeeping functions
- LED indicated key status
- PMBus™ communication
- Graphical user interface (GUI) software

EVALUATION KIT CONTENTS

- ADP1051-240-EVALZ evaluation board
- ADP1051DC1-EVALZ daughter card
- CD with ADP1051 GUI installer, ADP1051 data sheet, UG-566 user guide, project sample files, schematics and BOMs for the ADP1051-240-EVALZ, ADP1051DC1-EVALZ, and current share daughter card

ADDITIONAL EQUIPMENT/SOFTWARE NEEDED

- ADP-I2C-USB-Z USB-to-I²C connector
- ADP-I2C-USB-Z drivers CD

GENERAL DESCRIPTION

The ADP1051-240-EVALZ evaluation board, together with a ADP1051DC1-EVALZ daughter card, allows the user to evaluate the ADP1051 in a power supply unit (PSU) environment. The boards are fully compatible with the ADP1051 GUI software. With the ADP-I2C-USB-Z USB-to-I²C connector and the GUI software, the ADP1051 on the evaluation board can be interfaced with a PC via a USB port.

The evaluation board allows the ADP1051 to be exercised without the need of external components. The board is set up to act as an isolated PSU, outputting a rated load of 12 V, 20 A from a 36 V dc to 75 V dc source.

Two parallel connectors on the evaluation board provide synchronization, share bus, and PMBus interfaces. They allow the direct paralleling evaluation when multiple evaluation boards are connected in parallel to a common bus. One analog current share daughter card connector allows analog current share extension.

Multiple test points allow easy access to all critical points/pins. Three LEDs give the user a direct visual indication of variations in the board status, such as the system input voltage, PGOOD output, and FLAGIN input.

Full performance details are provided in the ADP1051 data sheet, and the ADP1051 data sheet should be consulted in conjunction with this user guide.

EVALUATION BOARD SETUP

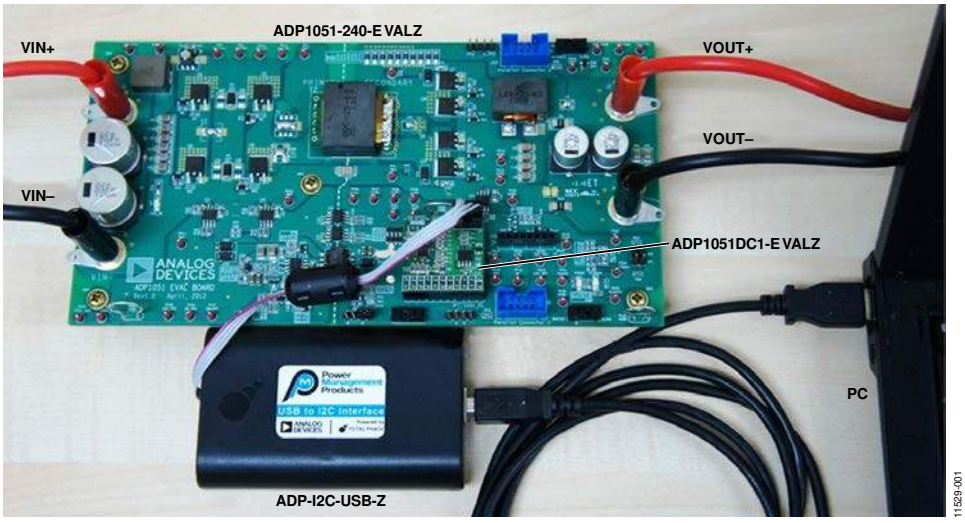

Figure 1. ADP1051 Evaluation Board Setup

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REVISION HISTORY

7/13—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADP1051-240-EVALZ evaluation board and the ADP1051DC1-EVALZ daughter card feature the ADP1051 in a dc-to-dc switching power supply in full bridge topology with synchronous rectification. Figure 2 shows a hardware photo of the evaluation board. Figure 3 shows a block diagram of the main components on the board. The circuit is designed to provide a rated load of 12 V, 20 A from a dc input voltage source of 36 V dc to 75 V dc. The ADP1051 provides functions such as output voltage regulation, synchronization, constant current control, prebias start up, direct paralleling, and comprehensive protection.

The main transformer on the evaluation board breaks the dc-to-dc power supply into primary side and secondary side; therefore, creating isolation. On the primary side, the full bridge stage switches and inverts the dc voltage derived from the input terminals (J1 and J5) into ac voltage. The control signals for the full bridge stage come from the ADP1051 through the digital isolators (ADuM3210) and the half bridge drivers. There is also a current transformer (CT) sensing and transmitting the primary side current information to the ADP1051 on the secondary side.

On the secondary side, the full wave synchronous rectifiers (SR) rectify the ac voltage to dc voltage. An LC filter smooths the pulsated dc voltage. The current information is sensed through a current sense resistor and fed to the CS2+ and CS2− pins in the ADP1051. Output terminals, J2 and J6, are used for the load connection.

The ADP1051DC1-EVALZ daughter card shown in Figure 4 can be plugged into the daughter card connector (J8). It provides the signals that are used to regulate the output voltage, limit the output current, and control the on/off switch of the evaluation board. A 4-pin connector (J2) on the daughter card is used for I²C/PMBus communication through a USB-to-I²C connector, ADP-I2C-USB-Z. This allows the GUI software to communicate with the evaluation board through the USB port of the PC. If the J17 or J18 parallel connector is connected, the GUI can visit all the evaluation boards through a single USB-to-I²C connector. With this interface, users can monitor and program the ADP1051.

An auxiliary power supply on the evaluation board is used to generate a 10V_PRI bias power for full bridge drivers, a 5V_PRI bias power for the primary side power supply of the ADuM3210, and a 10V_SEC bias power for the ADP3654 driver. A 10V_VCC bias power is generated from an OR-diode network using a 10V_SEC bias power and 5 V voltage source from the USB-to-I²C connector. This allows the GUI access to the ADP1051 when the auxiliary power circuit is not powered up. The ADP3303 LDO converts 10V_VCC to a 3V3_SEC bias power for the ADP1051 and the secondary side power of the ADuM3210. Alternatively, the auxiliary power input can also come from an independent dc source through TP47 and TP50.

An analog current share connector (J15) allows an external current share daughter card to be used for analog current sharing control. Two parallel connectors (J17 and J18) allow the synchronization, current share, and PMBus communication between multiple evaluation boards.

There are wholly three blue color LEDs in the evaluation board to provide the status of the evaluation board. D7 indicates the input voltage signal. D17 indicates the PGOOD output (PG/$\overline{\text{ALT}}$ pin output signal). D18 indicates the FLAGIN signal.

There are three complete switches on the evaluation board. The SW1 switch is used to control the voltage level of the hardware CTRL pin. The SW2 and SW3 switches are used to change the part operating state between as master device and as slave device when the synchronization is enabled.

Figure 2. ADP1051-240-EVALZ Evaluation Board

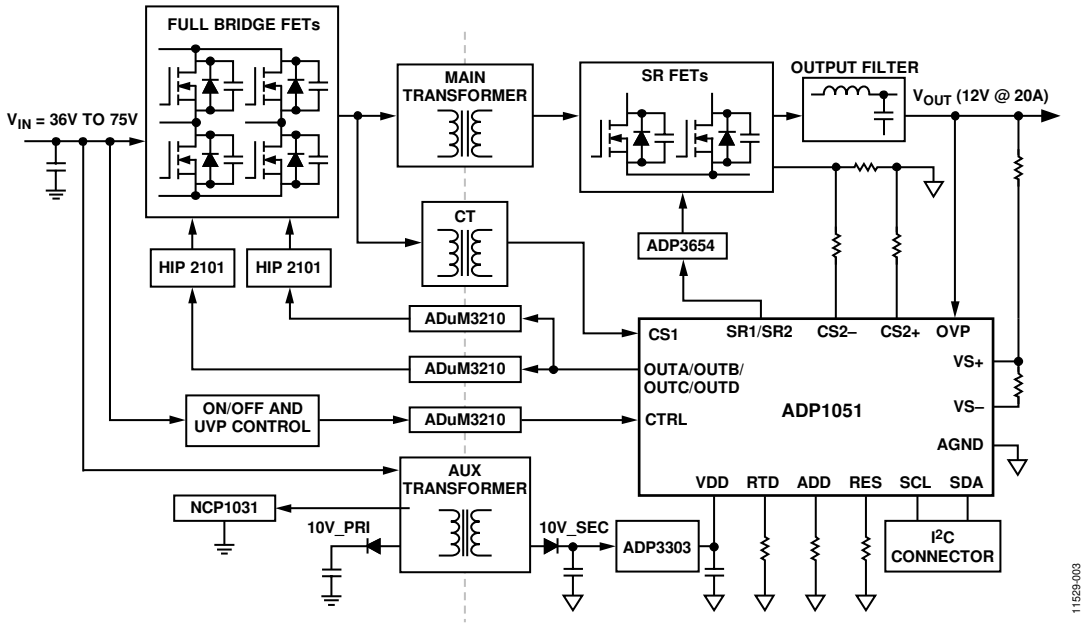


Figure 3. Block Diagram of ADP1051-240-EVALZ Evaluation Board

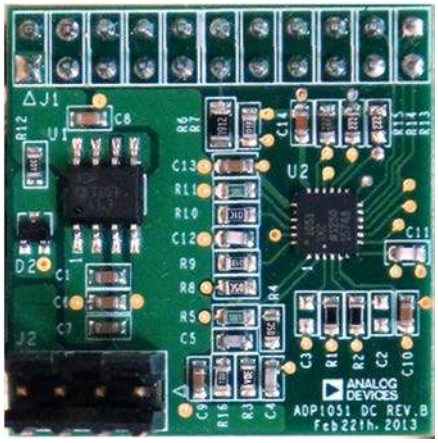


Figure 4. ADP1051DC1-EVALZ Daughter Card

EVALUATION BOARD CHARACTERISTICS

Table 1. Evaluation Board Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comment
INPUT VOLTAGE	V_{IN}	36	48	75	V dc	
OUTPUT VOLTAGE SETPOINT	V_{OUT}		12		V dc	
V_{OUT} OV Fault Limit (Default)			14		V dc	
Output Voltage Ripple			200		mV	V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 20 A
OUTPUT CURRENT	I_{OUT}	0		20	A	
I_{OUT} OC Fault Limit (Default)			25			
OPERATION TEMPERATURE	T_A		25	50	°C	Natural convection
			25	85	°C	Airflow = 200 LFM or above
OT Fault Limit (Default)	T_{OT_FAULT}		110		°C	
EFFICIENCY	η		94.5		%	V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 20 A
SWITCHING FREQUENCY	f_{SW}		120		kHz	
DIMENSION						
Width	W		210		mm	
Length	L		110		mm	
Component Height	H		40		mm	

CONNECTORS

The connections to the ADP1051-240-EVALZ evaluation board are shown in Table 2. Table 3 to Table 6 show the details about these connectors.

Table 2. Evaluation Board Connections

Connector	Function
J1	VIN+, dc input
J5	VIN−, ground return for dc input
J2	VOUT+, dc output
J6	VOUT−, ground return for dc output
J8	ADP1051 daughter card connector
J15	Analog current share daughter card connector
J17	Parallel Connector 1
J18	Parallel Connector 2

Daughter Card Connector J8

The connections to J8 are shown in Table 3.

Table 3. J8 Connections

Pin	Function
1	10V_VCC
2	VS−
3	VS+
4	CS2−
5	CS2+
6	VF
7	CS1
8	SR1
9	SR2
10	OUTA
11	OUTB
12	OUTC
13	OUTD
14	SCL
15	SDA
16	CTRL
17	PG/$\overline{\text{ALT}}$
18	SYNI/FLGI
19	3V3_SEC
20	AGND
21	RTD
22	OVP

Analog Current Share Connector J15

The connections to J15 are shown in Table 4.

Table 4. J15 Connections

Pin	Function
1	CS2+
2	CS2−
3	10V_SEC
4	3V3_SEC
5	IBUS
6	VF_ISHARE
7	AGND
8	AGND

Parallel Connector J17 and J18

The connections to J17 and J18 are shown in Table 5.

Table 5. J17 and J18 Connections

Pin	Function
1	SCL
2	SDA
3	SYNC
4	CTRL
5	AGND
6	10V_VCC
7	IBUS
8	AGND

Daughter Card I²C/PMBus Connector

The connections to J2 in the ADP1051 daughter card are shown in Table 6.

Table 6. J2 Connections

Pin	Function
1	5V
2	SCL
3	SDA
4	AGND

HARDWARE CONNECTION

Caution

This evaluation board is supplied with high voltages and currents. Take extreme caution, especially on the primary side, to ensure safety for the user. It is strongly advised to switch off the evaluation board when not in use. A current-limit dc source is recommended to use as the input.

Required Equipment

- DC power supply capable of 36 V dc to 75 V dc, 10 A output
- Electronic load capable of 12 V, 25 A input
- Oscilloscope capable of 500 MHz bandwidth or higher
- PC with Microsoft Windows XP (32-bit), Vista (32-bit), Windows 7 (32-bit), or Windows 8 (32-bit)
- Precision digital multimeters (6-digit HP34401 or equivalent)
- Portable digital multimeters (fluke) for measuring up to 25 A dc current
- ADP-I2C-USB-Z USB-to-I²C connector (see Figure 5) available from Analog Devices, Inc.

Figure 5. ADP-I2C-USB-Z USB-to-I²C Interface Connector

Evaluation Board Configurations

There are a series of jumpers used for ADP1051-240-EVALZ hardware settings. All the jumper configurations have been completed during the evaluation board assembly. Table 7 shows the details of jumper configurations.

J3 and J4 are short pins for configuring the low-side output current sense method and high-side output current sense method. The low-side current sense method is used by default. T1 and T4 are current transformers for primary side current sense. Typically, T4 is used while T1 is not connected by default.

Users do not need to complete any hardware configuration unless special test items will be conducted.

Table 7. Jumpers Configuration

Jumper	Function
JP1	Short this jumper to short the R46. This jumper can be used as signal injection point during the control loop test. It is open by default.
JP2	Short this jumper to short R53. It is open by default.
JP3	When SW1 is used to control the PSU, short this jumper. It is shorted by default.
JP4	When multiple evaluation boards are connected in parallel, proper configuration of this jumper allows a single switch to control all evaluation boards. It is shorted by default.
JP5	Short this jumper to configure the on/off pin at an off state. It is open by default.
JP11	Short this jumper to select OUTD as a SYNO signal to J17 connector. It is open by default.
JP12	Short this jumper to select OUTC as a SYNO signal to J17 connector. It is open by default.
JP13	Short this jumper to select OUTD as a SYNO signal to J18 connector. It is open by default.
JP14	Short this jumper to select OUTC as a SYNO signal to J18 connector. It is open by default.

Connecting the Hardware

Do not connect the ADP-I2C-USB-Z connector to the evaluation board until after the GUI software has been installed.

Figure 6 shows the test configuration of the evaluation board. The digital multimeters are optional. An independent dc source can be applied on TP47 and TP50 to generate all bias power supplies even if the dc input is lower than 30 V. The board evaluation can start when the dc input voltage is increased from 0 V.

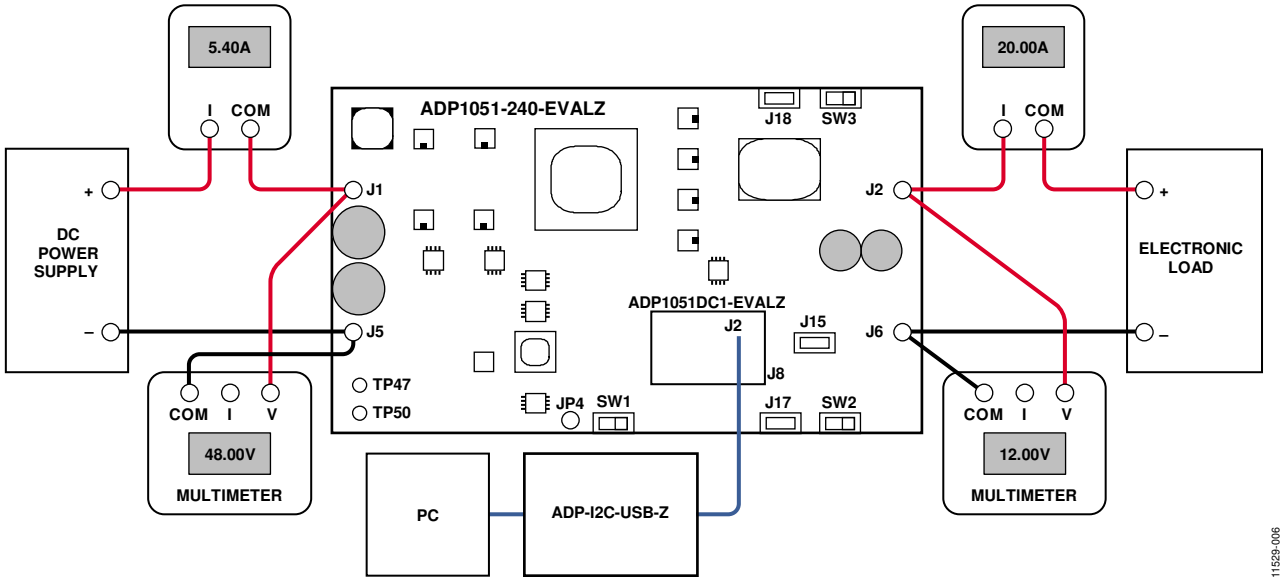


Figure 6. Test Configuration for the Evaluation Board

EVALUATION BOARD GUI SOFTWARE

OVERVIEW

The ADP1051 GUI is a free software tool for programming and configuring the ADP1051. For more information on the GUI, refer to the ADP1051 GUI user guide.

DOWNLOADING THE GUI

The ADP1051 GUI setup file is included on the CD in the ADP1051 evaluation kit.

Users can also visit http://www.analog.com/ADP1051 to obtain the latest version of GUI software.

INSTALLING THE GUI

Warning

Do not connect the USB cable to the evaluation board until the software has been installed.

Installation Steps

To install the ADP1051 GUI software, use the following steps:

1. Insert the CD.
2. Double click **ADP1051 Setup.msi** installation file to start the installation.
3. Click through the following windows (such as Figure 7).
4. In the **Total Phase USB Setup** window, click **Next**.
5. Check **I accept the terms in the License Agreement** after reading it and click **Next**.
6. Check the **Install USB drivers** option when the driver is not installed. If the driver has been installed, uncheck the **Install USB drivers** option. Then click **Install**.
7. After the installation, click **Close** to complete the driver installation.
8. When the **Adobe Flash Player Installer** window appears, check **I have read and agree to the terms of the Flash Player License Agreement** after reading it. Click **INSTALL**. If a newer version of Adobe Flash Player is already installed in the system, click **Quit** and continue.
9. Click **Close** to exit setup.

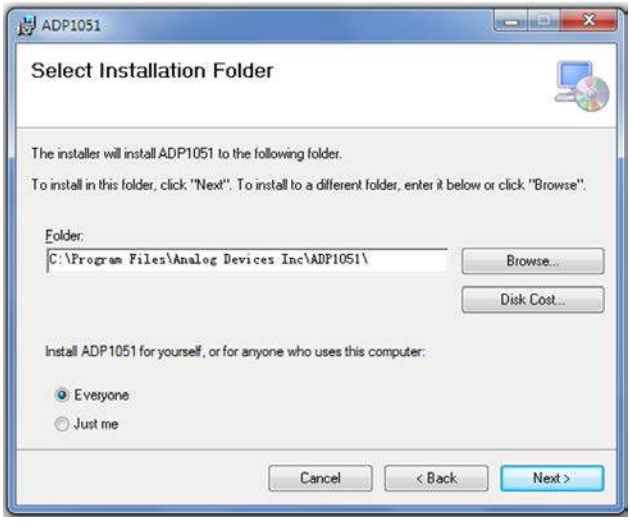


Figure 7. GUI Installation

LAUNCHING THE GUI

To launch the GUI, use the following steps:

1. Plug the ADP1051 daughter card into the J8 connector.
2. Ensure that the CTRL switch (SW1) is turned to the off position. The off position is the left side by default.
3. Plug the ADP-I2C-USB-Z connector into the USB port in the PC.
4. If the **Found New Hardware - Total Phase Aardvark I2C/SPI Host Adapter** window appears, the PC automatically installs the hardware driver. Wait until the installation is finished. If this window does not appear, skip this step.
5. Connect the ADP-I2C-USB-Z connector to J2 on the ADP1051 daughter card.
6. Launch the **ADP1051.exe** file. The GUI software should report that the ADP1051 has been located on the board as shown in Figure 8.
7. Click **Finish** to proceed to the **Monitor** window (see Figure 10).
8. Click **Unlock Chip Password** (Button I in Figure 10) and enter the chip password in the following pop-up window. The default chip password is 0xFFFF. Click **Enter** after keying in the password to process the **Setup** tab as shown in Figure 11.

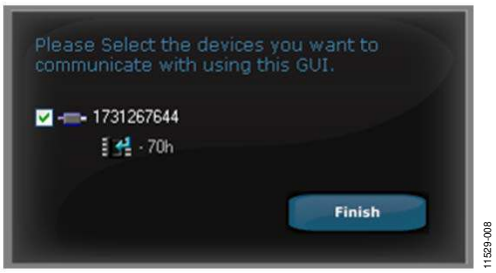


Figure 8. Getting Started.

If the user wants to load the default command and board settings file from a local folder, click **Load Command and Board settings from a '.51s' file to ADP1051** (Button A in Figure 11) and select the **ADP1051-240W-EVALZ-Default.51s** file when specifying the folder as shown in Figure 9. Because the ADP1051 in the evaluation kit is preprogrammed with the board and command settings, this step is optional.

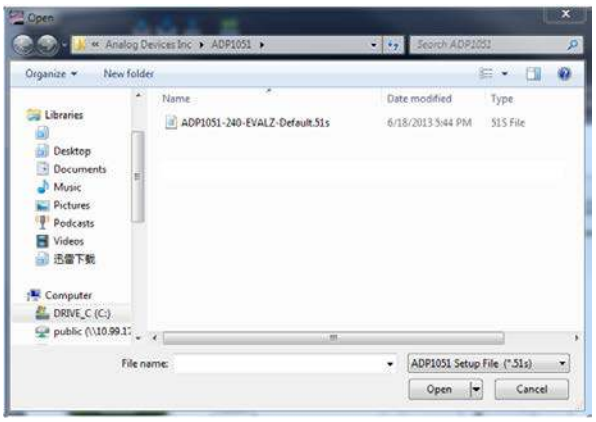


Figure 9. Load Board and Command Settings File

Table 8. shows a list of key buttons in the GUI. For more information about the ADP1051 GUI, refer to the ADP1051 GUI user guide.

Table 8. Key Buttons in the GUI

Button Letter	Button	Description
A		Load command and board settings from a '.51s' file to the ADP1051 device.
B		Save command and board settings from the ADP1051 device to a '.51s' file.
C		Generate a hex file of the command and board settings.
D		Access to the EEPROM.
E		Scan for the ADP1051 device.
F		Open a spy window to monitor I²C communication between the GUI and the ADP1051 device.
G		Program command and board settings into the EEPROM.
H		Unlock/lock the trim password.
I		Unlock/lock the chip password.

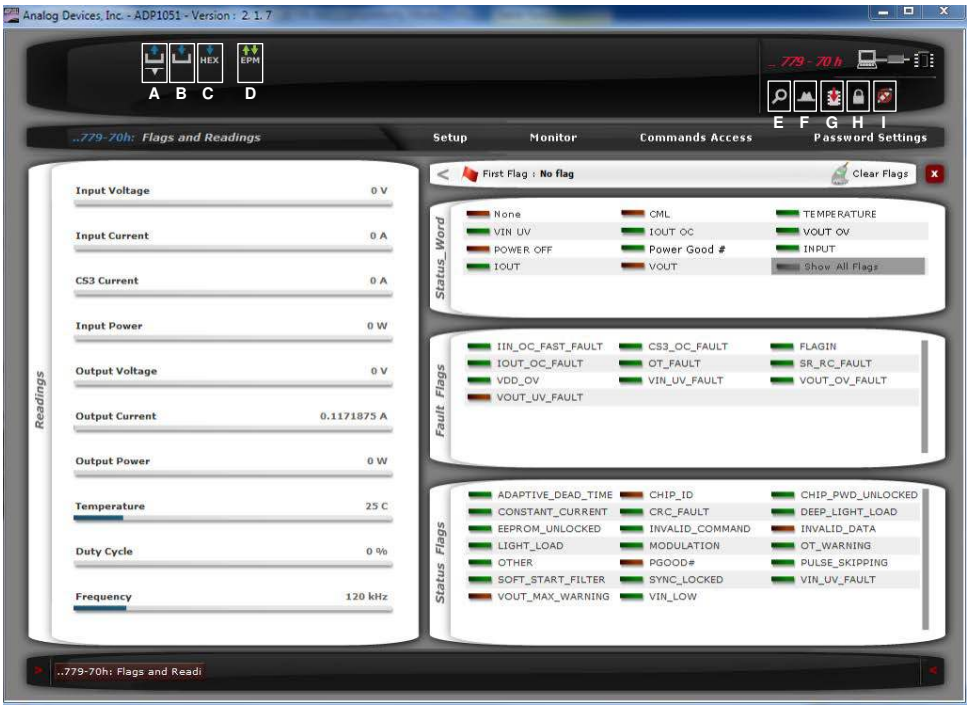


Figure 10. Monitor Window in the GUI

GETTING STARTED

Connect a dc source (voltage range of 36 V dc to 75 V dc) at the J1 and J5 input terminals and connect an electronic load at the J2 and J6 output terminals. See Figure 6 for the correct configuration.

Connect the multimeters on the input terminals and output terminals separately as shown in Figure 6.

Connect the voltage probes at different test pins. Ensure that the differential probes are used and that the grounds of the probe are isolated if the measurements are made on the primary and secondary side of the transformer simultaneously.

Turn the CTRL switch (SW1) to the on position.

The evaluation board is now up and running, and ready for evaluation. The output should read 12 V dc.

After a successful startup, the PSU is in a steady state. The board's LEDs provide the status of the board. D17 is turned on indicating that there are no faults detected. In case of a fault, the PGOOD LED will be turned off indicating that a flag has tripped. The **Monitor** tab in the GUI displays the appropriate state of the PSU.

After completing the programming of ADP1051, click **Program command and board settings into EEPROM** (Button G in Figure 11) to program the command and board settings into the EEPROM once the user wants to save the settings in the device.

Moreover, the user can use the **Save Command and Board settings from ADP1051 to a '.51s' file** button (Button B in Figure 11) to generate a .51s file for the command and board settings.

Software Main Window

Figure 11 shows the main window. There are four tabs total in the main window:

- **Setup** tab: All the setting windows are in this tab. It includes the board settings and command setting windows.
- **Monitor** tab: The readings and flags are monitored in this tab.
- **Commands Access** tab: This tab provides the command maps for direct access.
- **Password Settings** tab: The PMBus command WRITE_ PROTECT and chip password can be configured in this tab.

PROJECT SAMPLE FILES

There are a series of project sample files on the CD. Using the GUI software, the user can load the different project sample file from the CD to do different types of evaluation. The evaluation board hardware should be configured to half bridge topology if the half bridge sample settings are to be evaluated.

The default settings file is also stored as ADI_Default.51s in the GUI. After the GUI is stalled, the user can load the ADI_Default.51s file in the default folder to learn the default settings of the evaluation board.

Table 9. Project Sample Files

File Name	Description
ADP1051-240-EVALZ-Default.51s	ZVS full bridge converter sample file. This is the default settings file.
ADP1051-240-EVALZ-HSFB-SAMPLE.51s	Hard-switched full bridge converter sample file.
ADP1051-240-EVALZ-FSFB-SAMPLE.51s	Phase-shifted full bridge converter sample file.
ADP1051-240-EVALZ-HB-SAMPLE.51s	Half bridge sample file.
ADP1051-240-EVALZ-OLFB-SAMPLE.51s	Open-loop full bridge converter sample file.
ADP1051-240-EVALZ-OLFF-SAMPLE.51s	Open-loop input voltage feed forward converter sample file.

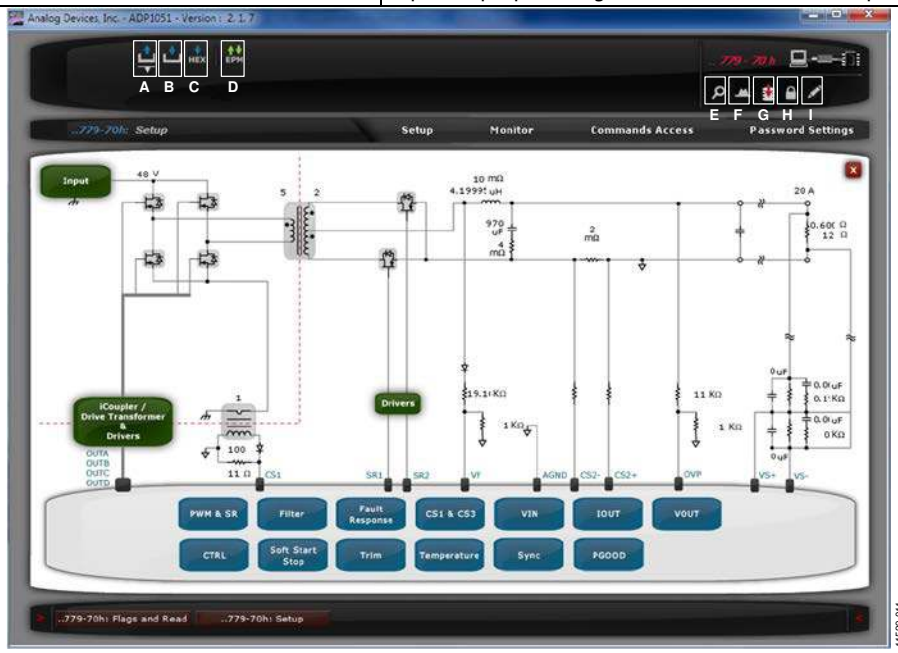


Figure 11. Main Setup Window of the ADP1051 GUI (See Also Table 8)

EVALUATING THE BOARD

This ADP1051 evaluation kit allows the user to get an insight into the flexibility offered by the extensive ADP1051 programming options. The following sections provide an overview of evaluation items to evaluate the key features of the ADP1051. Unless otherwise specified, use the project sample file ADP1051-240-EVALZ-Default.51s (it is preprogrammed in the ADP1051 of the daughter card) to do all the evaluation.

ON/OFF CONTROL AND SOFT START

This section specifies the power-on control behavior, power-off control behavior, and the soft start timing of the PSU. By default, the AND logic of the hardware CTRL pin logic and software OPERATION command are used to turn on the ADP1051, as shown in the **CTRL Settings** window of the **Setup** tab (Figure 12). It is recommended that Switch SW1 be used to control the operation state of the PSU.

The turn-on delay time, turn-on rise time, and the turn-off delay time can be programmed in **Soft Start and Stop** window of the **Setup** tab (see Figure 13). Additional soft start settings are programmed in Figure 14. Figure 15 and Figure 16 show the results of soft start at 0 A load and 20 A load separately. The soft start rise time is programmed to 40 ms. Figure 17 gives an example of soft start with disabled synchronous rectifiers during soft start ramp.

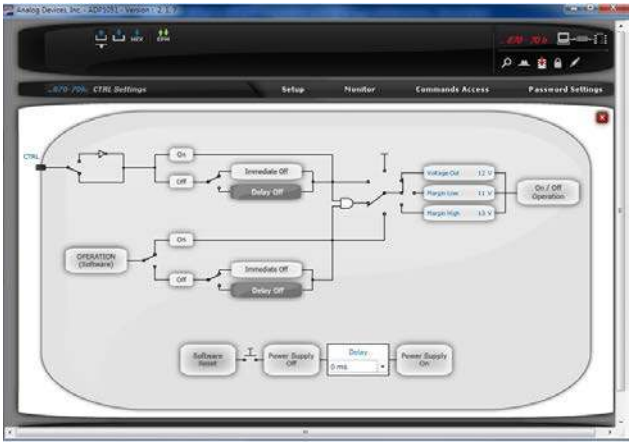


Figure 12. CTRL Settings Window

Figure 13. Soft Start and Stop Settings Window

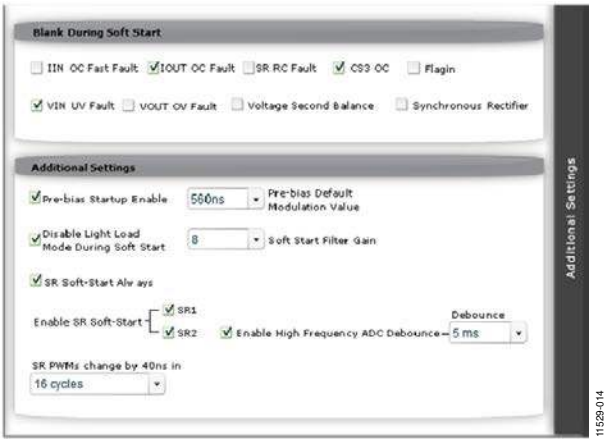


Figure 14. Additional Soft Start Settings Window

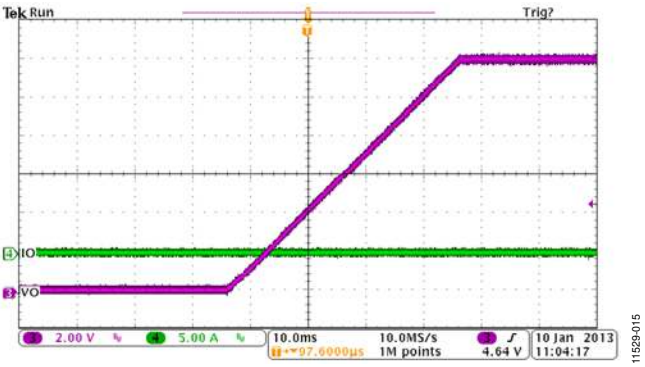


Figure 15. Soft Start at 48 V DC Input, 0 A Load

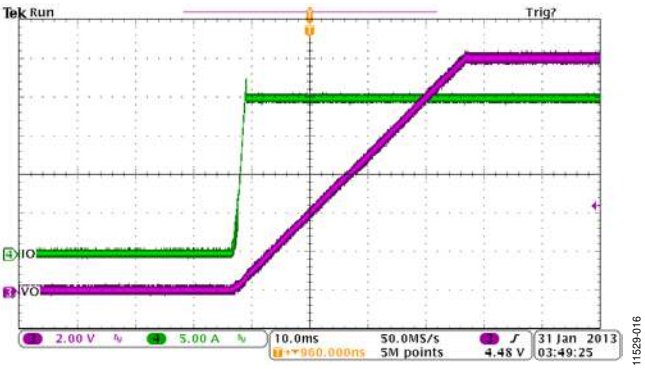


Figure 16. Soft Start at 48 V DC Input, 20 A Load

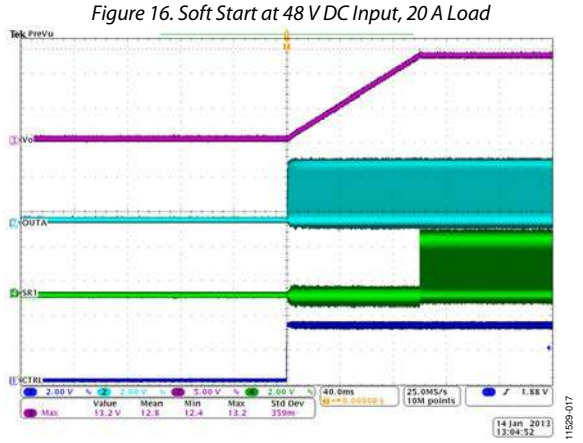


Figure 17. Soft Start with Disabled SRs

Prebias Start Up

The prebias start-up function provides the capability to start up with a prebiased voltage on the output. To set up the prebias startup, use the following steps:

1. Enable the prebias start up and program the appropriate nominal modulation value for prebias startup through the additional soft start settings window shown in Figure 14.
2. Select the type of prebias start up as shown in Figure 18:
    - If the closed-loop input voltage feed forward operation is enabled and the input voltage information is available for the ADP1051 before the PSU starts up, select the **Feed Forward always Activated** option (Option A).
    - If the closed-loop input voltage feedforward operation is disabled and the input voltage information is available for the ADP1051 before the PSU starts up, select the **Feed Forward only during Startup** option (Option B).
    - If the closed-loop feed forward operation is disabled and the input voltage information is not aviable for ADP1051 before the PSU starts up, select the **Feed Forward always Disabled** option (Option C).

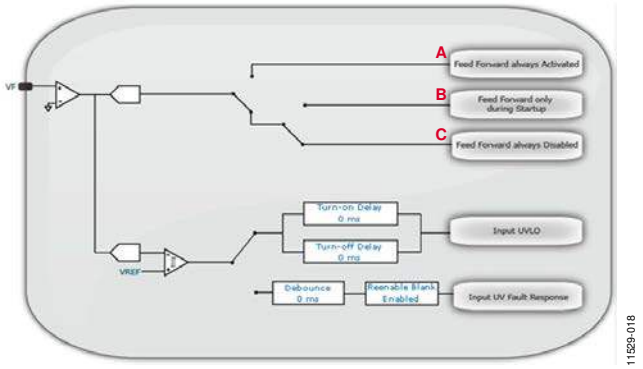


Figure 18. Feed Forward Selection Option

Figure 19 and Figure 20 show the prebias start up waveforms when the **Feed Forward always Activated** option (Option A) is selected.

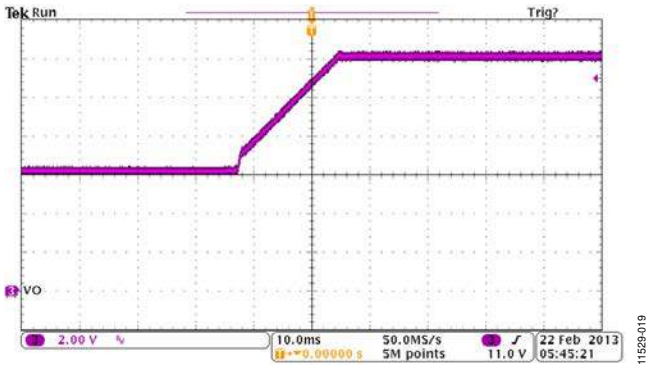


Figure 19. Prebias Start Up at 36 V DC Input and Low Residual Voltage

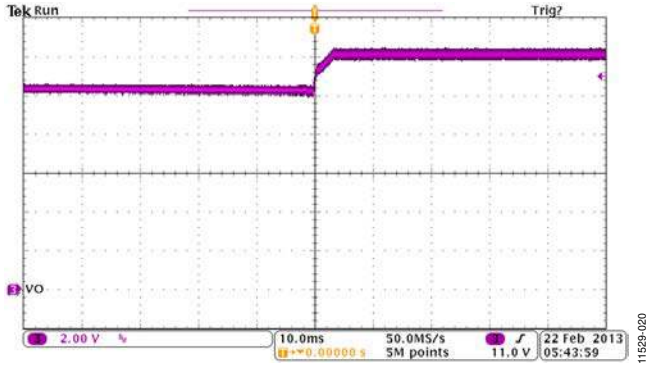


Figure 20. Prebias Start Up at 60 V DC Input and High Residual Voltage

Because the input voltage cannot be sensed through the windings of auxiliary power supply in this evaluation board, it is recommended that the **Feed Forward always Disabled** option (Option C) be selected for evaluation.

Other evaluation options are:

- Program different turn-on rise time in combination with different turn-on delay time.
- Blank different flags during soft start ramp as shown in Figure 14.
- Choose different soft start gains to derive a best soft start ramp.
- Enable the SR soft start and select a different SR soft start speed to prevent a glitch at the output voltage ramp.

PWM SETTINGS

The PWM timings for the primary side switches and secondary side synchronous rectifiers are programmed in the **PWM SR Settings** window of the **Setup** tab as shown in Figure 21. This window allows the programming of the switching frequency, rising edge and falling edge timings, the type of modulating edge (rising edge or falling edge), modulation type (positive or negative), and modulation limit. Figure 21 shows the gate drive signals at the output pins of the ADP1051. The QA, QB, QC, QD, Q7/Q8, and Q3/Q4 switches in the evaluation board ADP1051-240-EVALZ are driven separately by PWM outputs OUTA, OUTB, OUTC, OUTD, SR1, and SR2.

Although the switching frequency can be adjusted, the GUI software does not account for the dead times and the PWM timings have to be programmed manually to guarantee the normal operation of the PWM outputs.

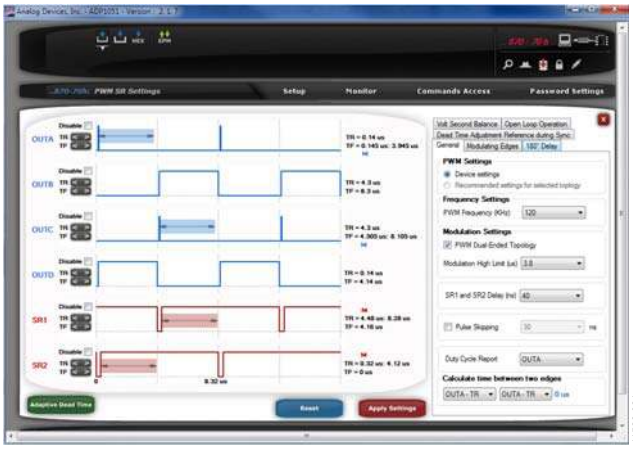


*Figure 21. **PWM SR Settings** Window*

Additional PWM and SR evaluation options are:

- Enable and disable the pulse skipping mode and measure the standby power of the PSU.
- Double the switching frequency from 120 kHz to 240 kHz. The board is designed to operate at a switching frequency of up to 240 kHz with airflow cooling.
- Program an imbalance in the on time of the QA and QC switches, and evaluate the volt-second balance control function.
- Run the software in simulation mode and program the PWM settings for different topologies such as zero-voltage-switched full bridge, hard-switched full bridge, phase shifted full bridge, half bridge, push-pull, two-switch forward, or active clamp forward converters. The project sample files listed in Project Sample Files section can also be loaded.
- Align all SR edges to OUTA, OUTB, OUTC, OUTD edges and adjust the primary-secondary propagation delay by programming the SR1 and SR2 delay.
- Program the adaptive dead time compensation function as shown in Figure 22 to improve the efficiency at light load condition.

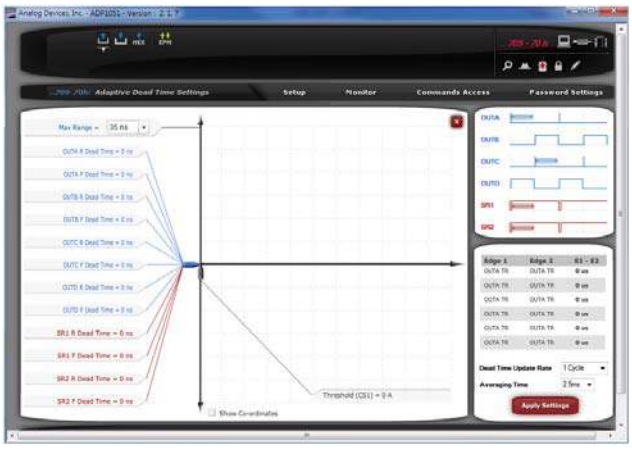


Figure 22. Adaptive Dead Time Compensation Settings Window

DIGITAL COMPENSATOR AND LOAD TRANSIENT RESPONSE

The digital compensator can be configured by the **Filter Settings** window of the **Setup** tab as shown in Figure 23. The digital compensator can be changed by manipulating the position of the poles and zeros in the s-domain. The ADP1051 allows two different sets of compensator responses to be programmed. One is normal mode compensator and the other is light load mode compensator.

The digital compensator is a Type III compensator. The first pole is placed at a dc position to eliminate the steady state error. The second pole can be freely placed (ideally at the ESR zero position). However, the third pole is fixed at half of the switching frequency.

*Figure 23. **Filter Settings** Window*

Warning

While varying the compensator's parameters is possible when the part is running, the wrong combination of parameters can cause the system to become unstable.

Control Loop Configuration

To configure the control loop, use the following steps:

1. Make sure the board parameters are set correctly, including the topology, the turn ratio of the main transformer, the output LC filter parameters, and the output voltage sense network parameters. Using the information, the GUI software generates the Bode plots of the power stage and output voltage sense network separately.
2. The switching frequency is determined in the **PWM SR Settings** window. Changing of the switching frequency changes the low frequency gain and the third pole position.
3. The user can start to place the zeros and poles, and set the low frequency gain and high frequency gain of the digital compensator, based on the stability rules.
4. The GUI then displays the full loop gain crossover frequency, the phase margin, the gain margin, and the phase crossover frequency.
5. Using the loop analyzer, the user can verify the programmed control loop as shown in Figure 24. During the test on the control loop, the test signal from the loop analyzer can be easily injected in JP1 of the evaluation board.

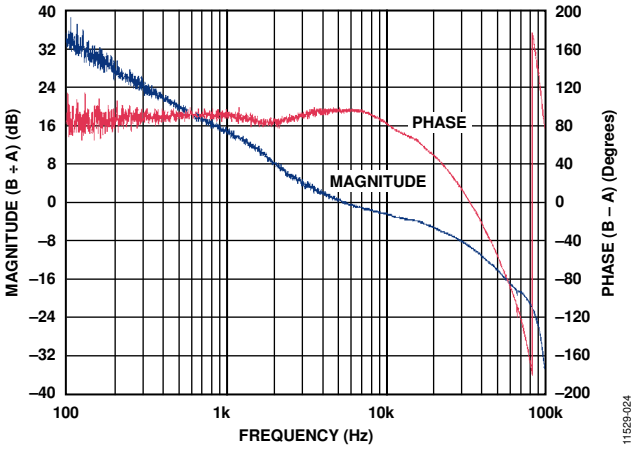


Figure 24. Control Loop Test by AP300 Loop Analyzer

Transient Response for the Load Step

A dynamic electronic load can be connected to the output of the evaluation board to evaluate the load transient response. Set up an oscilloscope to capture the transient waveforms of the PSU output. Figure 25 and Figure 26 show an example of the load transient response.

The user can vary the digital compensator via the GUI software to change the transient response. This evaluation kit allows the digital compensator to be easily programmed to optimize the load transient response of the PSU.

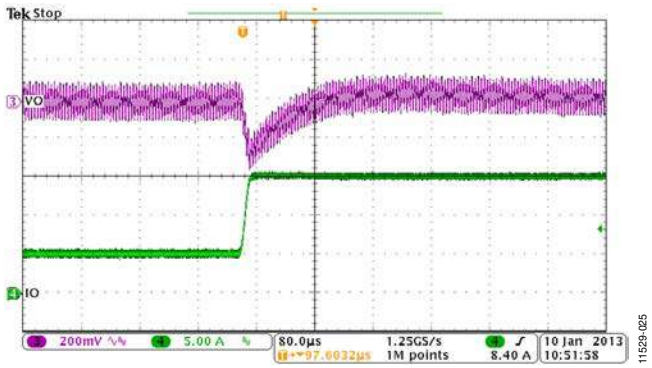


Figure 25. Transient Response with Load Steps: 25% to 50% to 25%

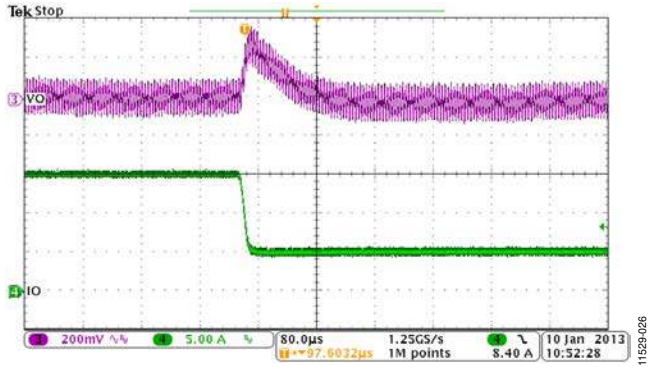


Figure 26. Transient Response with Load Steps: 50% to 75% to 50%

INPUT VOLTAGE SETTINGS

If the input voltage can be sensed by ADP1051 before the PSU is turned on (for example, the input voltage is sensed through the transformer windings of the auxiliary power circuit), the VIN on and VIN off limits can be programmed to control the input UVLO protection. Using the **VIN Settings** window in the **Setup** tab as shown in Figure 27, the user can program the **V_{IN} On** limit and **V_{IN} Off** limit.

By proper selection of the input voltage feed forward options as shown in Figure 18, the input voltage feed forward can be evaluated in different ways. Figure 28 gives a result of the input voltage transient with the feed forward being disabled (Option C—**Feed Forward always Disabled** in Figure 18). While Figure 29 gives a result of the input voltage transient with the input voltage feed forward being enabled (Option A—**Feed Forward always Activated** in Figure 18).

Additional input voltage related evaluation options are:

- Apply a different input voltage compensation multiplier (Register 0xFE59) to get an accurate input voltage sense at both no load and heavy load conditions.
- Select the input voltage signal to trigger the VIN_LOW flag or the VIN_UV_FAULT flag in the feed forward selection window shown in Figure 18.

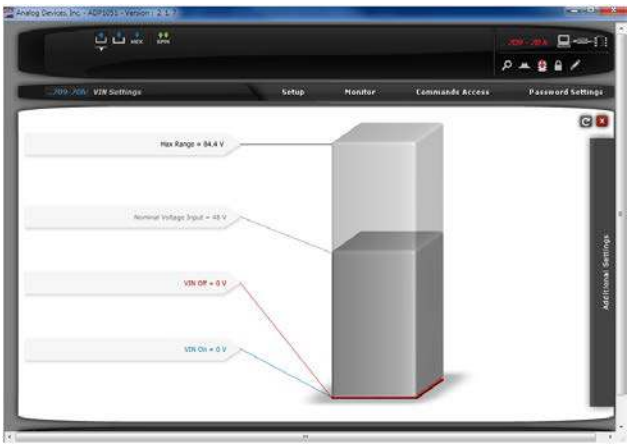


Figure 27. VIN Settings Window

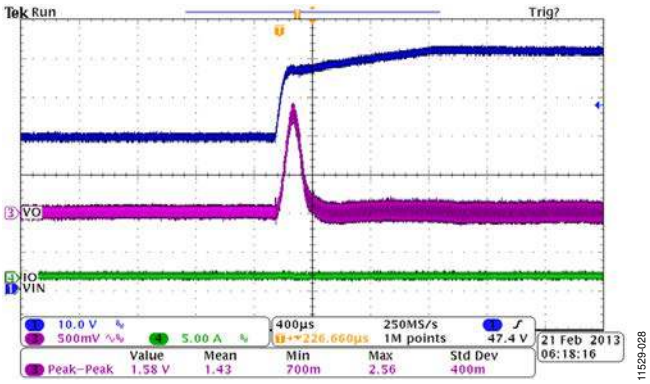


Figure 28. Input Voltage Transient Response with Feed Forward Disabled

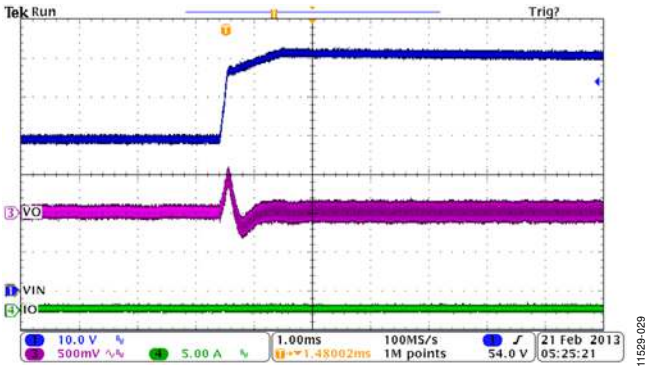


Figure 29. Input Voltage Transient Response with Feed Forward Enabled

OUTPUT VOLTAGE SETTINGS

The **VOUT Settings** windows (shown in Figure 30 and Figure 31) set all the output voltage related parameters, such as the output voltage settings, the droop resistor (through the VOUT_DROOP command), the output voltage transition rate (through the VOUT_TRANSITION_RATE), and conditional overvoltage protection setting. Figure 32 and Figure 33 provide results of output voltage adjustment when the V_{OUT} transition rate is programmed as 3.125 µV/µs.

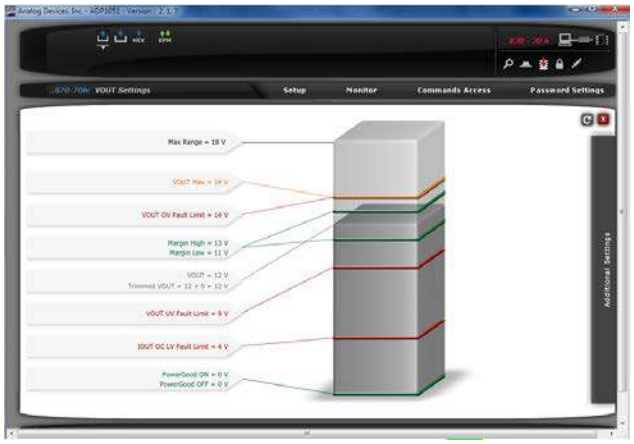


Figure 30. VOUT Settings Window 1

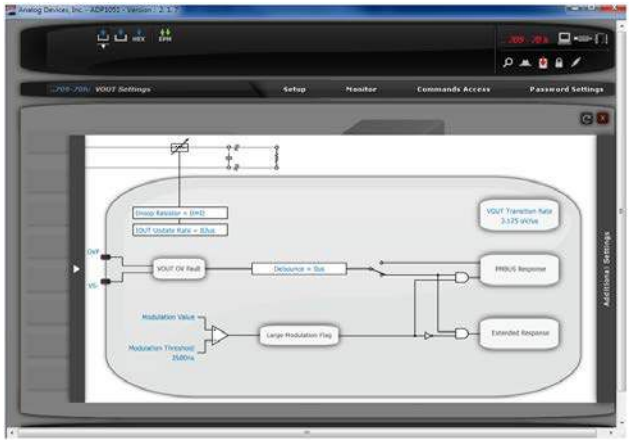


Figure 31. VOUT Settings Window 2

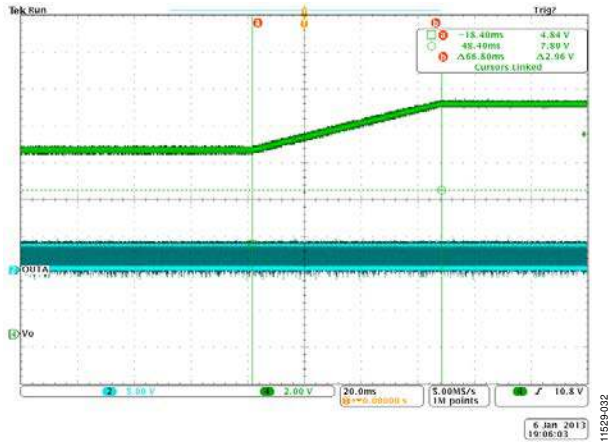


Figure 32. V_{OUT} Adjusted from 10 V to 12.5 V with 3.125 µV/µs Transition Rate

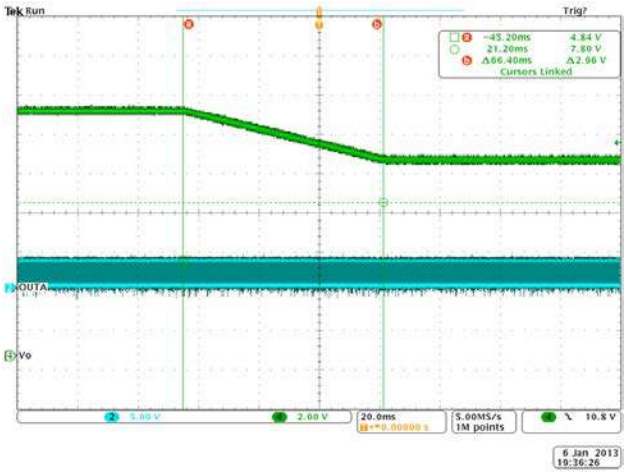


Figure 33. V_{OUT} Adjusted from 12.5 V to 10 V with 3.125 µV/µs Transition Rate

Droop Current Sharing

This test can be conducted by plotting the V-I curve when the load current is gradually increased from 0 A to 20 A. It can also be conducted by applying a dynamic load to test the transient performance. Moreover, the drooping current share test can be conducted using two or more evaluation boards connected in parallel. The settings of drooping current sharing are shown in Figure 31. The droop resister is programmed as 20 mΩ and the I_{OUT} update rate is programmed as 82 µs. Figure 34 gives drooping current sharing accuracy using two ADP1051-240-EVALZ evaluation boards connected in parallel.

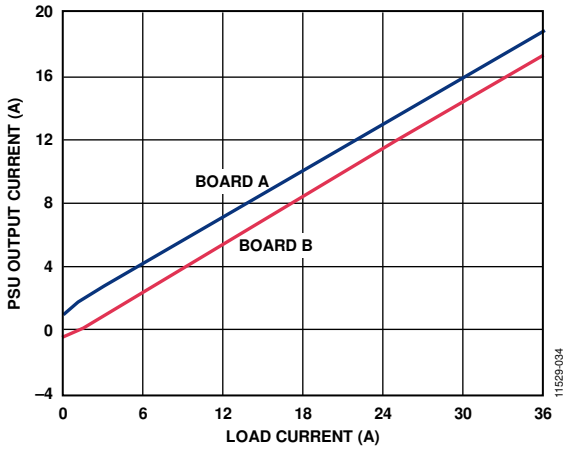


Figure 34. Droop Current Sharing Accuracy

Output Overvoltage Protection

This test can be conducted in a number of ways. The simplest way is to set the output voltage to a value higher than the V_{OUT} OV fault limit shown in Figure 30. Alternatively, shorting of the VS+ pin to AGND in the ADP1051 daughter card can cause a fast output overvoltage condition. The responses of the fault conditions can be programmed in the Flags and Fault Response Configurations section (see Figure 48). Figure 35 shows the waveforms when the response to an output overvoltage condition occurred.

The ADP1051 also supports the conditional overvoltage protection. The settings of conditional output overvoltage protection are shown in Figure 31. Figure 36 shows a result of conditional overvoltage protection when the outputs of two evaluation boards are connected to a common bus.

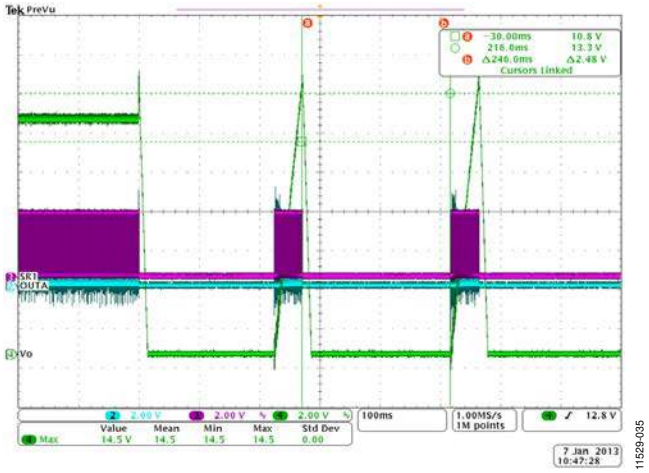


Figure 35. Overvoltage Protection Waveform

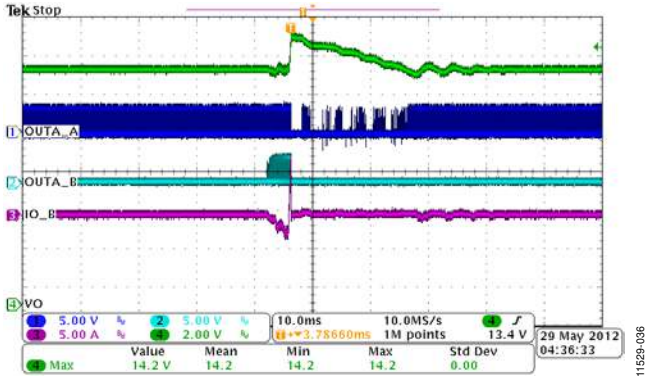


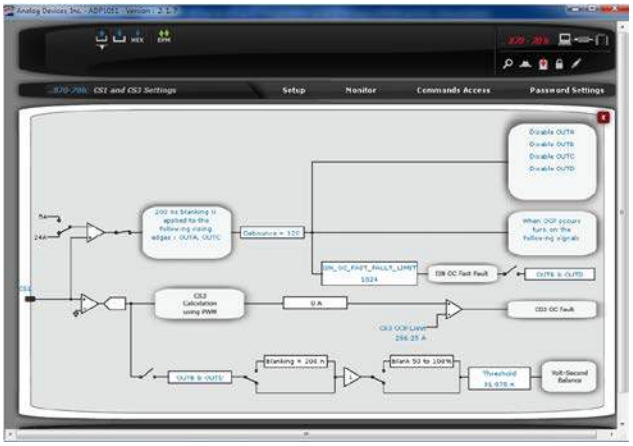
Figure 36. Conditional Overvoltage Protection with Two Evaluation Boards Connected to a Common Bus

Output Undervoltage Protection

This test can be done in a number of ways. The simplest way is to set the output voltage to a value lower than the V_{OUT} UV fault limit value shown in Figure 30. Even a shorted load or an internal short (such as shorting of the synchronous rectifiers) can cause an output undervoltage condition. The response of the fault condition can be programmed in the Flags and Fault Response Configurations section.

INPUT CURRENT SETTINGS

The input current settings are accessed using the **CS1 and CS3 Settings** window as shown in Figure 37. This window is used to program the cycle-by-cycle current limiting, the input overcurrent fast fault protection, the CS3 overcurrent protection and the volt-second balance control.



11529-037

Figure 37. CS1 and CS3 Settings Window

CS1 Cycle-by-Cycle Current Limiting

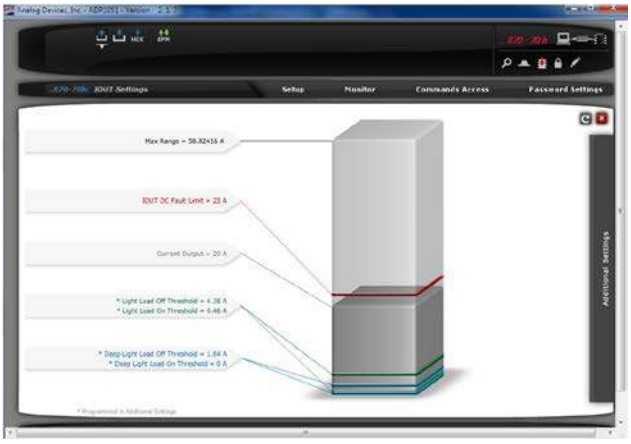
The leading edge blanking time, the leading edge blanking reference, debounce time, the PWM disabling selection, and the matched cycle-by-cycle current limiting can be programmed in **CS1 Settings** window shown in Figure 37.

Input Overcurrent Fast Fault Protection

This test can be conducted by shorting the load. Using the setting window shown in Figure 37, the user can specify the I_{IN} OC fast fault limit value by 2, 8, 16, 64, 128, 256, 512, or 1024. The fault response can be configured in the Flags and Fault Response Configurations section.

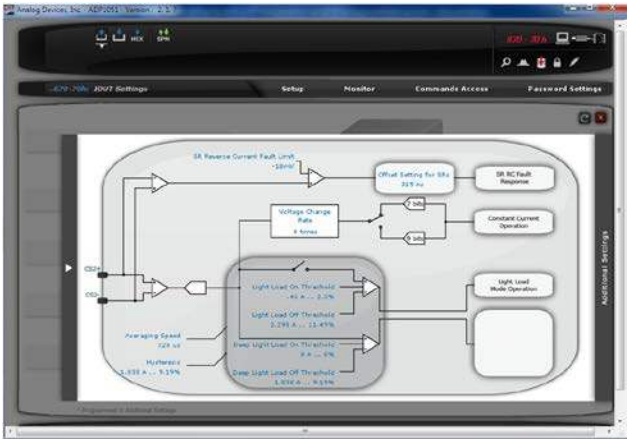
OUTPUT CURRENT SETTING

The output current settings window is accessed using the **IOUT Settings** window. This window features the output overcurrent fault limit, the thresholds for the light load threshold and the deep light load, the responses for the light load threshold and the deep light load, the constant current mode, and the SR reverse current control.



11529-038

Figure 38. IOUT Settings Window 1



11529-039

Figure 39. IOUT Settings Window 2

Output Overcurrent Protection

This test can be conducted by applying a load current larger than the value programmed by the I_{OUT} OC fault limit (shown in Figure 38). The fault response is programmed in the **Fault Response** window shown in Figure 48.

Figure 40 gives an experimental result by setting the I_{OUT} OC fault limit at 25 A and enabling soft start after every 250 ms.

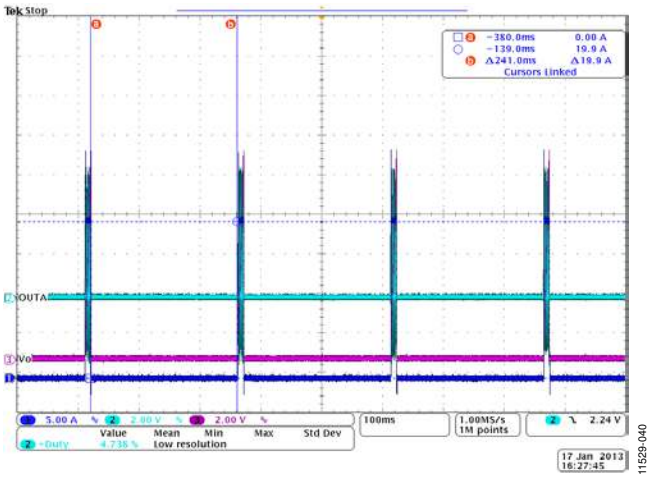


Figure 40. I_{OUT} OC Response Experimental Result

Constant Current Mode

Prior to the constant current mode test, the user needs to configure the constant current mode settings in Figure 39, including the output voltage change rates and the output current averaging speeds.

This test can be conducted in multiple ways:

- The constant current mode happens during a soft start at a CR load. The test is done on a standalone evaluation board.
- The constant current mode happens during a soft start at a CV load. The test is done on a standalone evaluation board.
- The constant current mode happens during a CR load transient. The test is done on a standalone evaluation board.
- The constant current mode happens during a CV load transient. The test is done on a standalone evaluation board.
- The constant current mode happens during a soft start when two or more evaluation board are connected in parallel. The load is a CR load.
- The constant current mode happens during a soft start when two or more evaluation boards are connected in parallel. The load is a CC load.

Figure 41 shows a result that the constant current mode happens during a soft start at a CR load. The test is done on a standalone evaluation board.

Figure 42 and Figure 43 show results that the constant current mode happens during a soft start when two evaluation boards are connected in parallel. The load is a CR load.

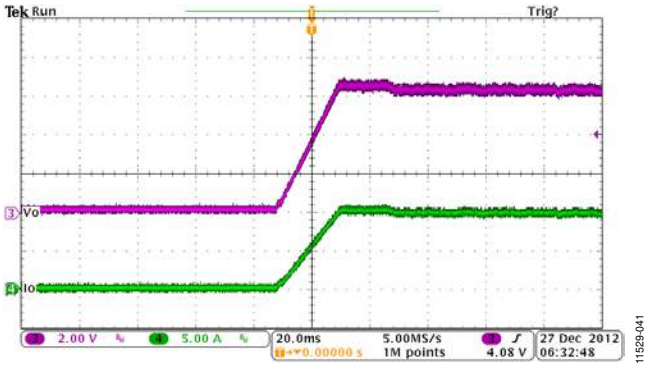


Figure 41. Constant Current Control During Startup; Constant Current Threshold is 10 A

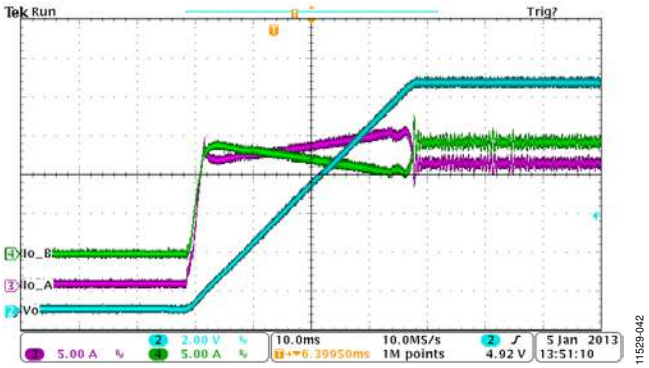


Figure 42. Constant Current Control with Two Evaluation Boards in Parallel; Turn-On Timing is the Same

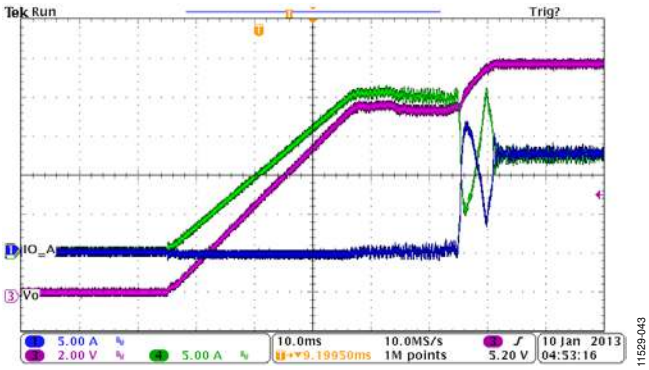


Figure 43. Constant Current Control with Two Evaluation Boards in Parallel; Turn-On Timing Difference is 50 ms

SR Reverse Current Protection

This test can be conducted by several ways:

- At a no load condition, the V_{OUT} voltage is adjusted from a higher voltage to a lower voltage with the fastest V_{OUT} transition rate. Up to 10,000 µF capacitance is connected at output terminals.
- Switch the load current between full load and no load with the fastest current slew rate programmed by E-load.
- At a no load condition, use an air switch to short the input terminals. A capacitor with up to 10,000 µF capacitance can be connected at the output terminals. This is a typical input voltage dip test.

Figure 44 shows a result where the output voltage is adjusted from a higher voltage to a lower voltage. Figure 45 shows a result that the input is shorted by an air switch.

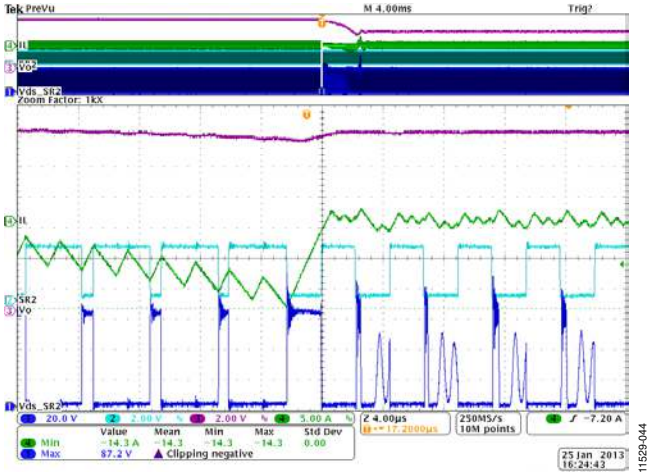


Figure 44. SR Reverse Current Protection During Output Voltage Adjustment

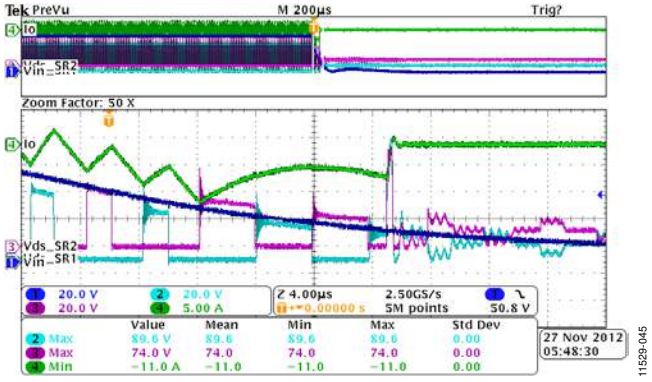


Figure 45. SR Reverse Current Protection During Input Dip Test; 10,000 µF Capacitance is Connected at Output Terminal

Light Load Efficiency Optimization

The ADP1051 can be programmed to optimize performance when the output current drops below a certain level. The light load mode threshold and deep light load mode threshold are programmed in a manner to reduce the losses and increase the efficiency. A hysteresis for the light load mode and the deep light load mode is provided on the thresholds to avoid the current oscillations. The thresholds for light load mode and deep light load mode can also be programmed in the **IOUT** window as shown in Figure 39.

When operating in the light load mode or deep light load mode, the mode flag is set in the **Monitor** tab. In combination with the pulse skipping mode, the standby power consumption can be reduced.

The user can try the test items as follows:

- Try different thresholds for light load mode and deep light load mode to test the efficiency improvement.
- Try different averaging speed for light load mode and deep light load mode to test the transient response by applying a dynamic load.
- Program the threshold for the pulse skipping mode to test the efficiency improvement during standby mode.
- Select the PWM channels to be disabled during the deep light load mode as shown in Figure 46.

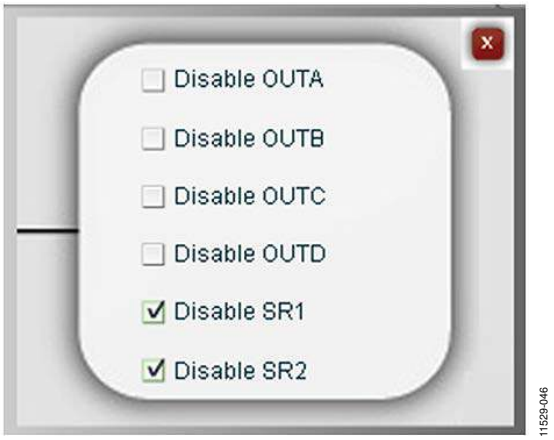


Figure 46. Deep Light Load Response Check Box

TEMPERATURE SETTINGS

This test can be conducted by enclosing the evaluation board in a thermal chamber at the desired ambient temperature to simulate the operating condition. The user can program the OT fault limit and OT warning limit through the **Temperature Settings** window shown in Figure 47. The OT hysteresis is the value difference of OT fault limit and OT warning limit.

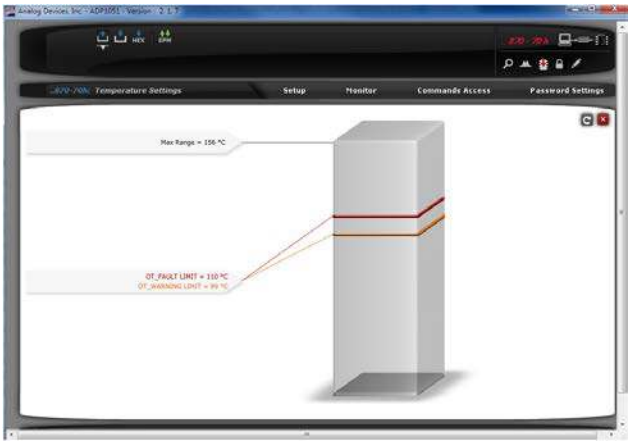


Figure 47. Temperature Settings Window

FLAGS AND FAULT RESPONSE CONFIGURATIONS

The fault responses can be programmed in the **Fault Response** window of the **Setup** tab as shown in Figure 48. The state of faults can be monitored in the **Monitor** tab as shown in Figure 11. There are two groups of fault responses:

- PMBus faults responses, including I_{OUT} OC, V_{OUT} OV, V_{OUT} UV, and OT.
- Manufacturer specific fault responses, including I_{IN} OC FAST, CS3 OC, V_{IN} UV, Flagin, SR RC, VDD OV. There is a global reenabling timing for all manufacturer specific fault responses.

The user can test this section by applying a fault condition. By changing the settings of the debounce timing, delay timings, responses and reenable timings, the user can see different protection performance.

When there is a fault causing the power supply to be shut down and a soft start is required if the PWM outputs are reenabled, the first fault ID information is shown in the **Monitor** tab. The first flag ID register gives the user more information for fault diagnosis than a simple flag.

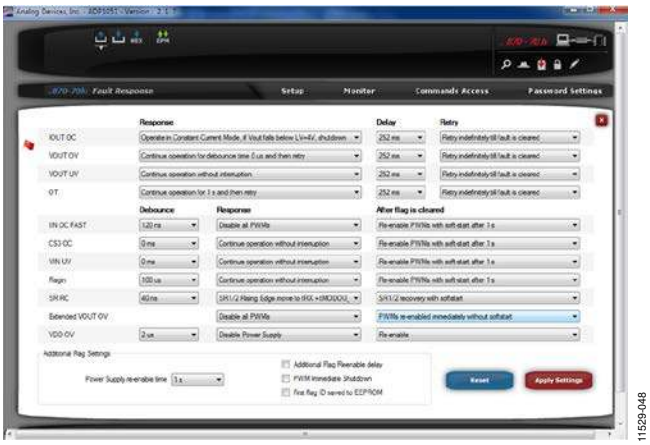


Figure 48. Fault Response Window

TRIMMING

This test allows the entire power supply to be calibrated and trimmed digitally through the ADP1051 in the production environment.

All the ADP1051 parts are factory calibrated. The trimming is not needed if the voltage and current sense resistors have a high enough accuracy (see the ADP1051 data sheet for details). However, the ADP1051 can be retrimmed by the user to compensate for the errors introduced by external components. All the trimming can be done in the **Trim Settings** window of the **Setup** tab as shown in Figure 49.

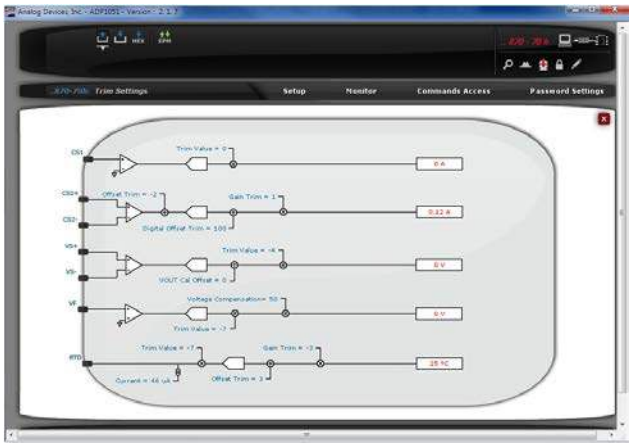


Figure 49. Trimming Window

SYNCHRONIZATION

Synchronization as a Master Device

This test can be done by specifying OUTC or OUTD as a SYNO signal using the **Sync Settings** window of the **Setup** tab as shown in Figure 50. The SYNO signal should be stable to constantly represent the internal switching frequency once the ADP1051 V_{DD} voltage is applied.

Jumper JP11 to Jumper JP13 can be used to configure OUTC or OUTD connected to SYNO. The user can test the SYNO clock through the test point TP35 or the SYNC pin in the JP17 and JP18 connectors.

Synchronization as a Slave Device

This test can be done by applying an external clock signal in the TP25 test point. Alternatively, the external clock signal (such as SYNO signal in the master device) can be applied in the SYNC pin of the J17 or J18 connector.

The settings can be programmed in the **Sync Settings** window (see Figure 50). To view the synchronization performance, try the following items:

- Enable and disable synchronization.
- Set different delays to see the phase shift between master device and slave device.
- Program the different phase capture range.
- If the external clock signal is generated by a signal generator, the user can try to program the clock signal in sweep mode or burst mode to see the synchronization locking or unlocking.

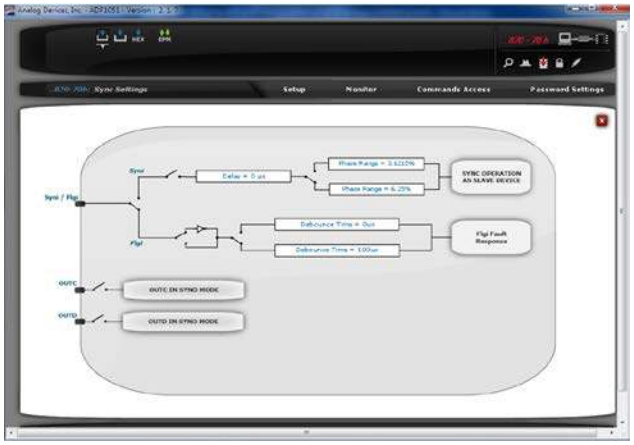


Figure 50. Synchronization Configurations

POWER GOOD SIGNAL

This test can be conducted by applying a fault condition, which is used to trigger a PGOOD flag and pull down the PG/ALT pin. The user can follow the **PGOOD Settings** window shown in Figure 51 to program which fault signal asserts the PGOOD flag. In the case of a fault to trigger the PGOOD flag, the D17 LED is turned off indicating that the power supply is not good. Figure 52 shows that a VOUT_UV_FAULT flag triggers the PGOOD output (PG/ALT pin).

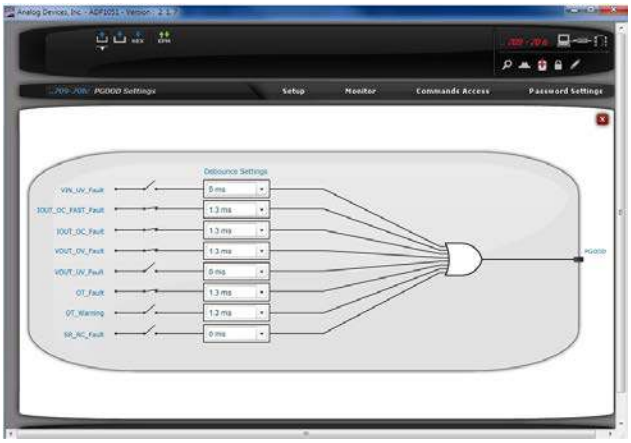


Figure 51. PGOOD Configurations

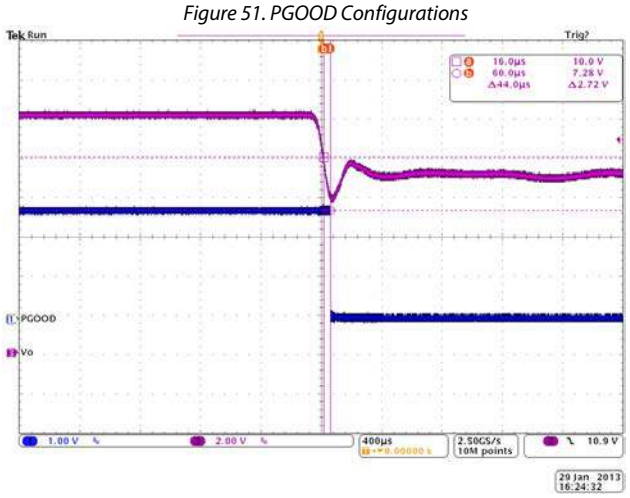


Figure 52. A VOUT_UV_FAULT Flag to Trigger PGOOD

PHASE SHIFTED FULL BRIDGE OPERATION

The PWM settings for phase shifted full bridge operation is highly flexible. Either the QA/QB leg (controlled by OUTA/OUTB PWM outputs) or the QC/QD leg (controlled by OUTC/OUTD PWM outputs) can be configured to run in modulation mode. Figure 53 provides a PWM setting example of the QA/QB leg in positive modulation mode. In this case, the QA/QB leg is the leading leg and the QC/QD leg is the lagging leg.

All the test items are similar to the general full bridge operation. The only difference is the SR reverse current protection. In case of SR reverse current, configure the synchronous rectifier to be disabled. The user can load the phase shifted full bridge project sample file, ADP1051-240-EVALZ-FSFB-SAMPLE.51s, to do the evaluation.

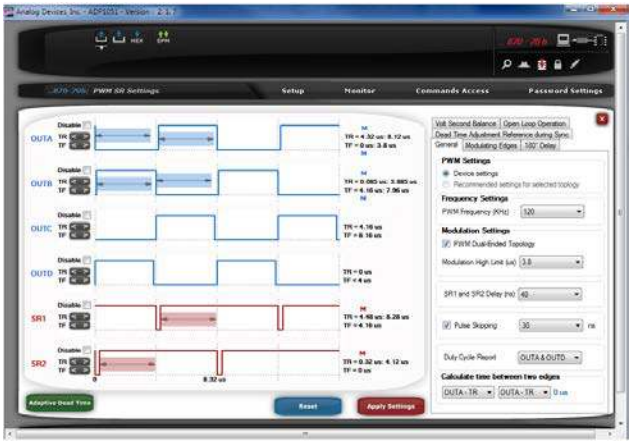


Figure 53. Phase Shifted Full Bridge PWM Setting Window

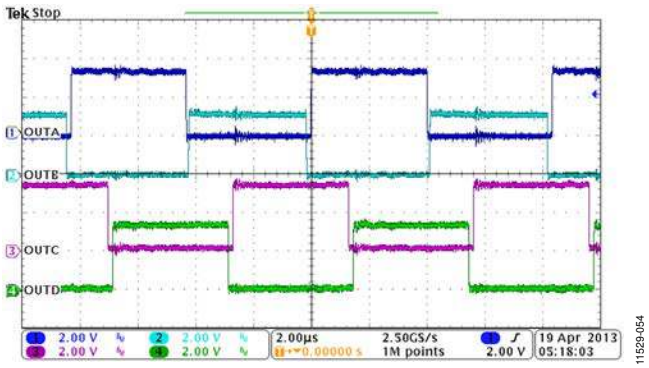


Figure 54. PWM Waveforms under PSFB Operation

DIRECT PARALLELING

The direct paralleling function is that multiple power supplies output rails are connected directly to a common bus without the existing of OR'ing devices. To overcome the challenges for direct paralleling, implement the following series of features:

- Prebias start up.
- Current sharing. Use drooping current sharing or active current sharing (through the current share daughter card).
- Synchronous rectifiers reverse current protection to avoid sinking current in a power supply.
- Constant current control and hot-switching control.
- Synchronization to reduce the output voltage ripple.
- Conditional overvoltage protection for redundant control.

All the previous features are implemented in the ADP1051-240-EVALZ evaluation board.

Figure 56 shows the setup of two ADP1051-240-EVALZ evaluation boards connected in parallel for direct paralleling test. Each board can be controlled by SW1 on each board (R73 should be removed). Alternatively, the SW1 on Board B can be configured to control both Board A and Board B. In this case, remove the JP4 jumper on Board A. For synchronization, if the ADP1051 in Board A is assigned as a slave device, then assign the ADP1051 in Board B as a master device. In this case, the SW2 in Board A should be turned to the slave position and the SW3 in Board B should be turned to the master position.

All the features listed in this section can be conducted in this direct paralleling system.

Figure 55. Parallel Cable to Connect Two Evaluation Boards

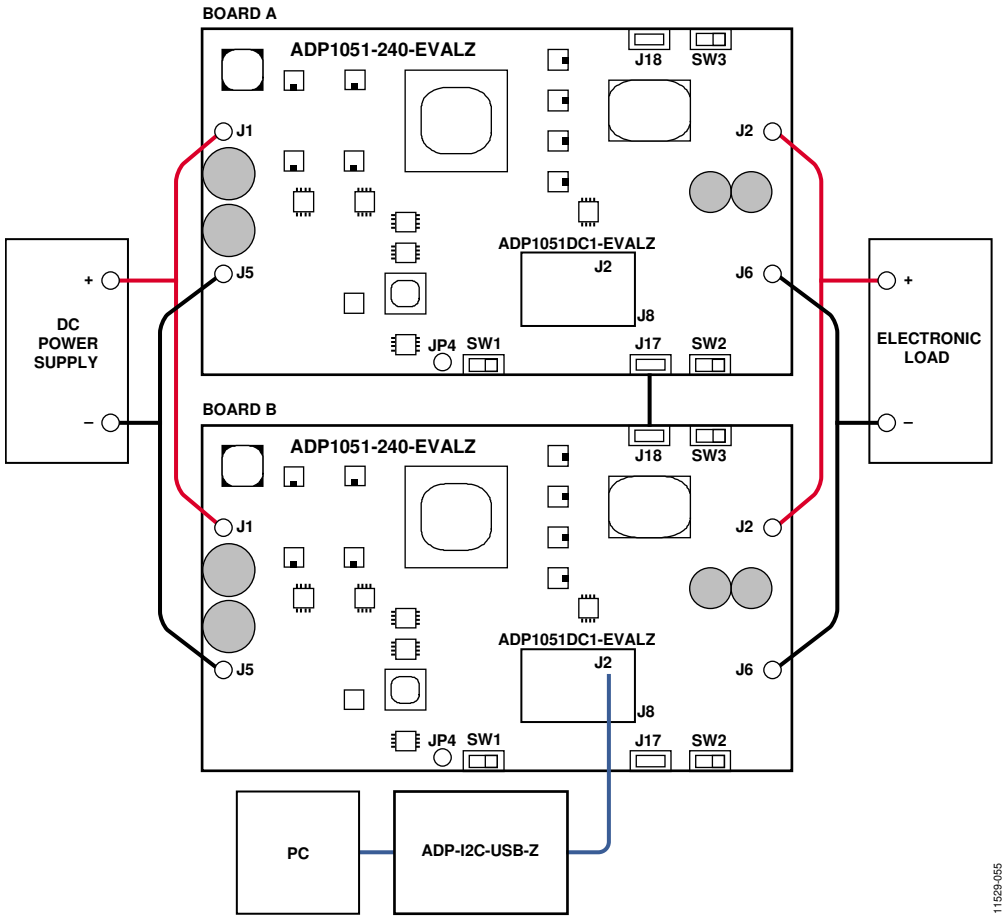


Figure 56. Direct Paralleling Configuration when Two Evaluation Boards are Connected in Parallel

ADDITIONAL GRAPHS

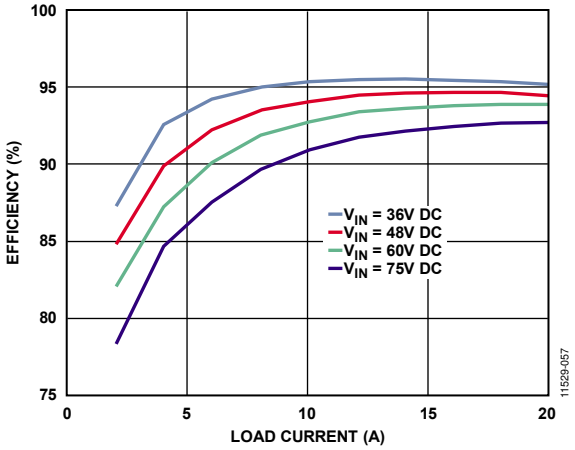


Figure 57. Efficiency Curve at 36 V DC, 48 V DC, 60 V DC and 75 V DC Input

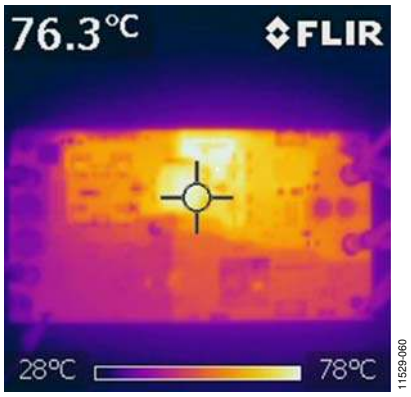


Figure 60. Thermal Image at 60 V DC Input, 20 A Load, No Airflow

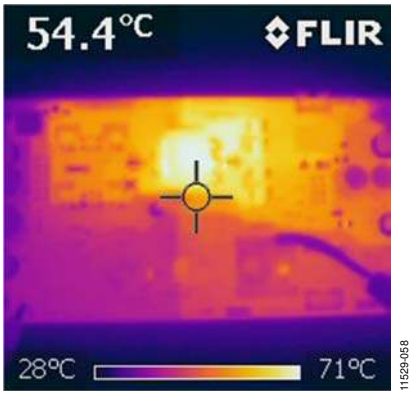


Figure 58. Thermal Image at 36 V DC Input, 20 A load, No Airflow

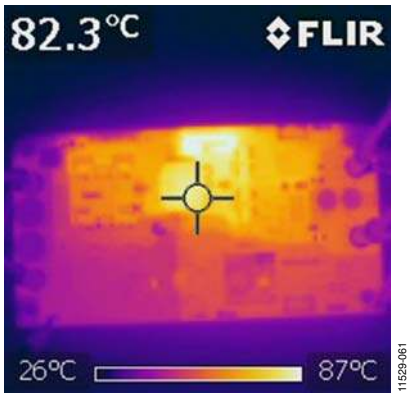


Figure 61. Thermal Image at 75 V DC Input, 20 A Load, No Airflow

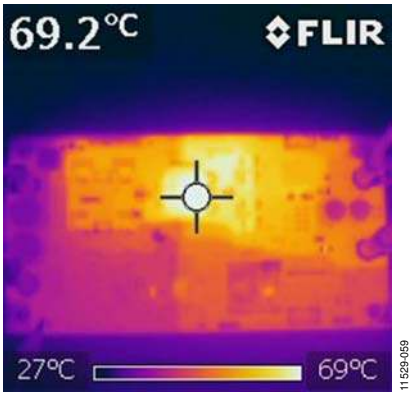


Figure 59. Thermal Image at 48 V DC Input, 20 A Load, No Airflow

SCHEMATICS AND ARTWORK

ADP1051-240-EVALZ

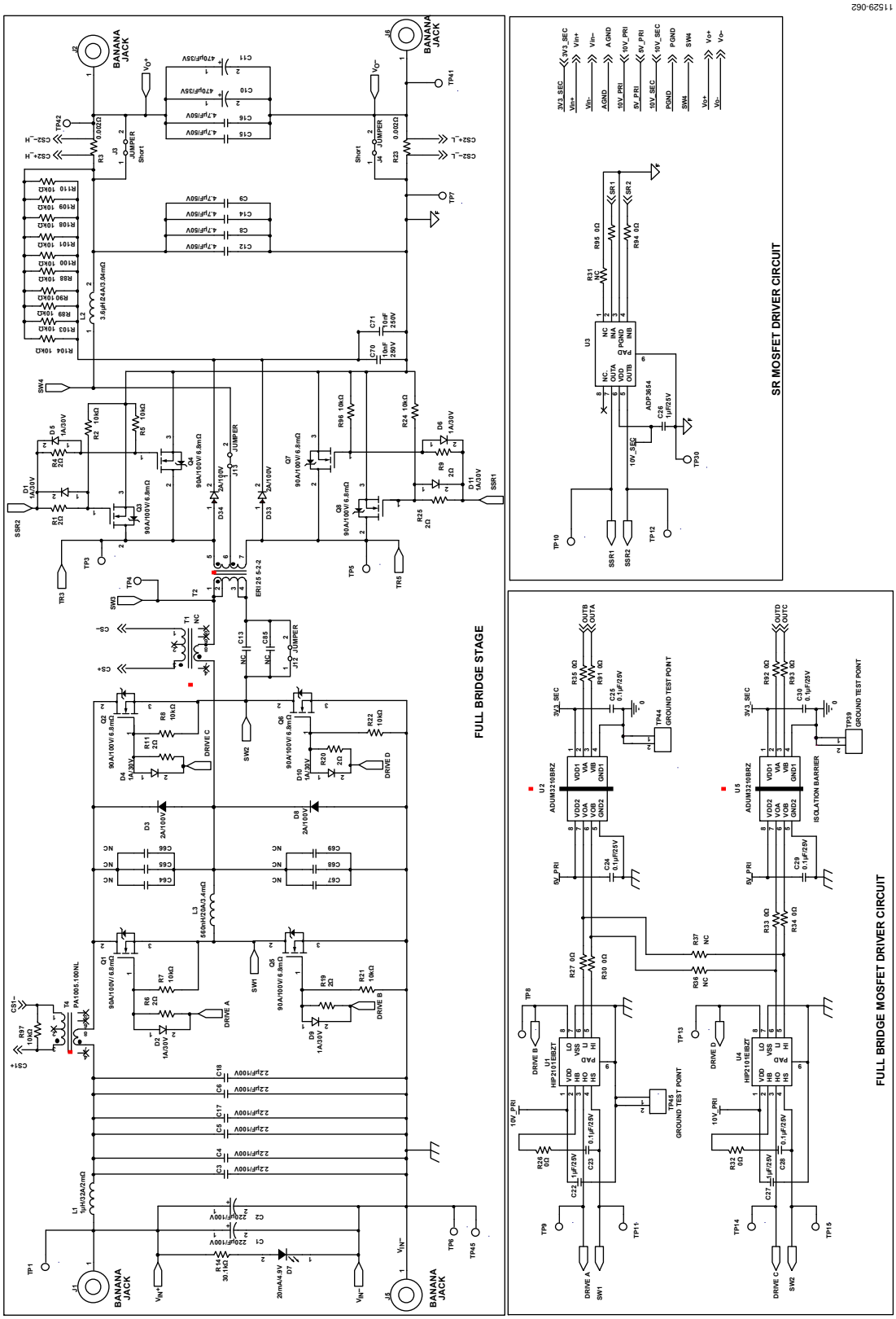


Figure 62. ADP1051 Evaluation Board Schematic—Part I

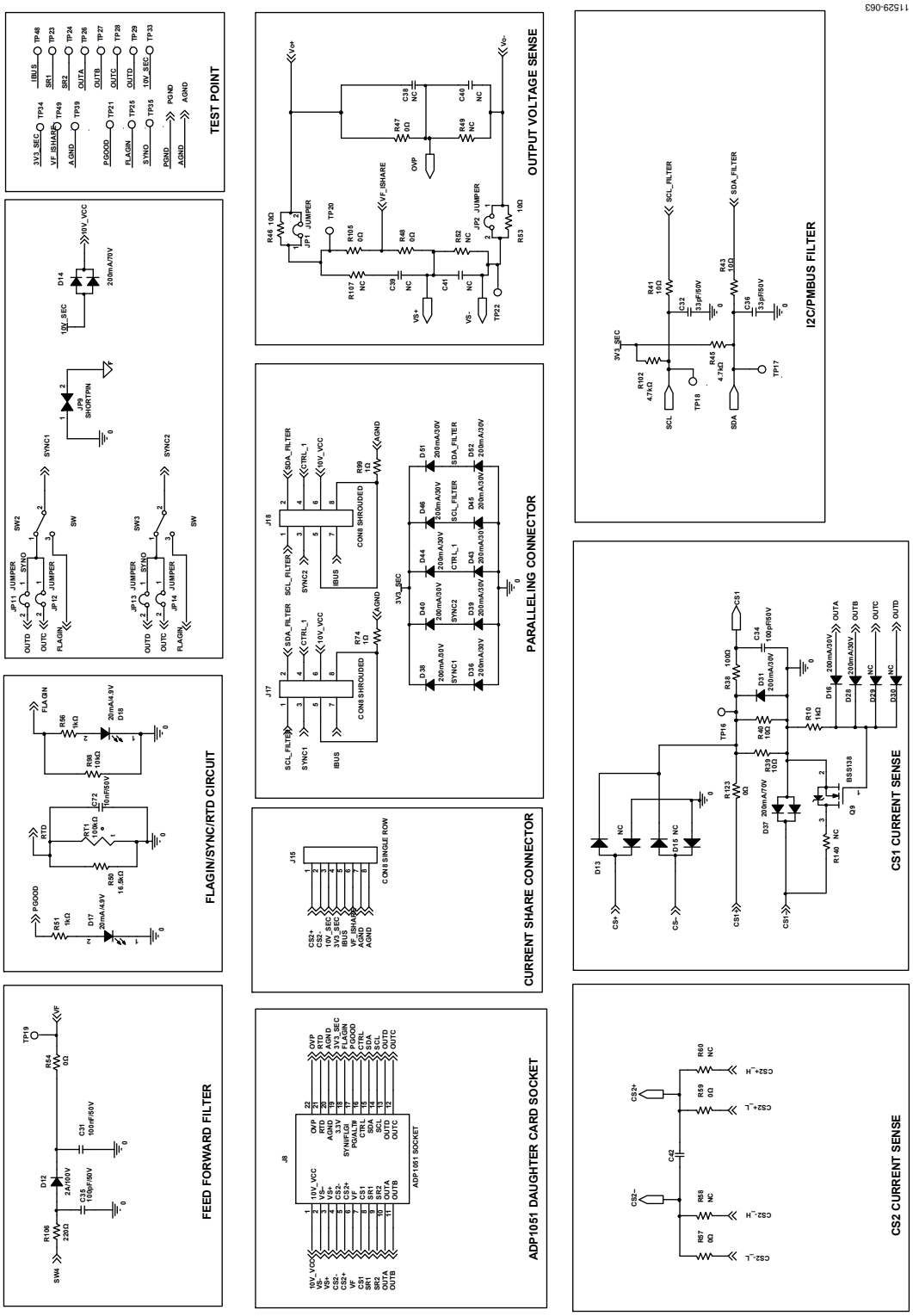


Figure 63. ADP1051 Evaluation Board Schematic—Part II

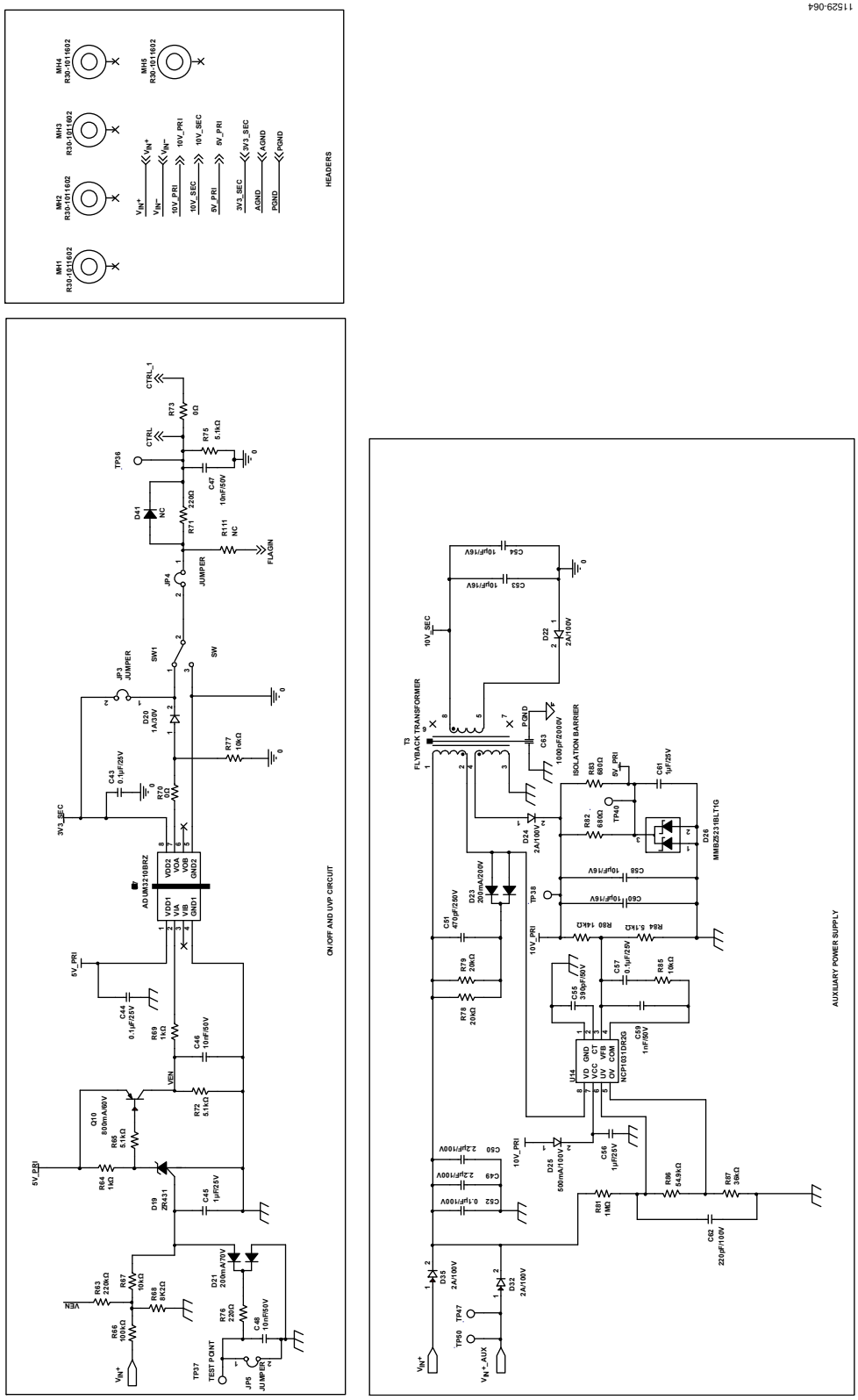


Figure 64. ADP1051 Evaluation Board Schematic—Part III

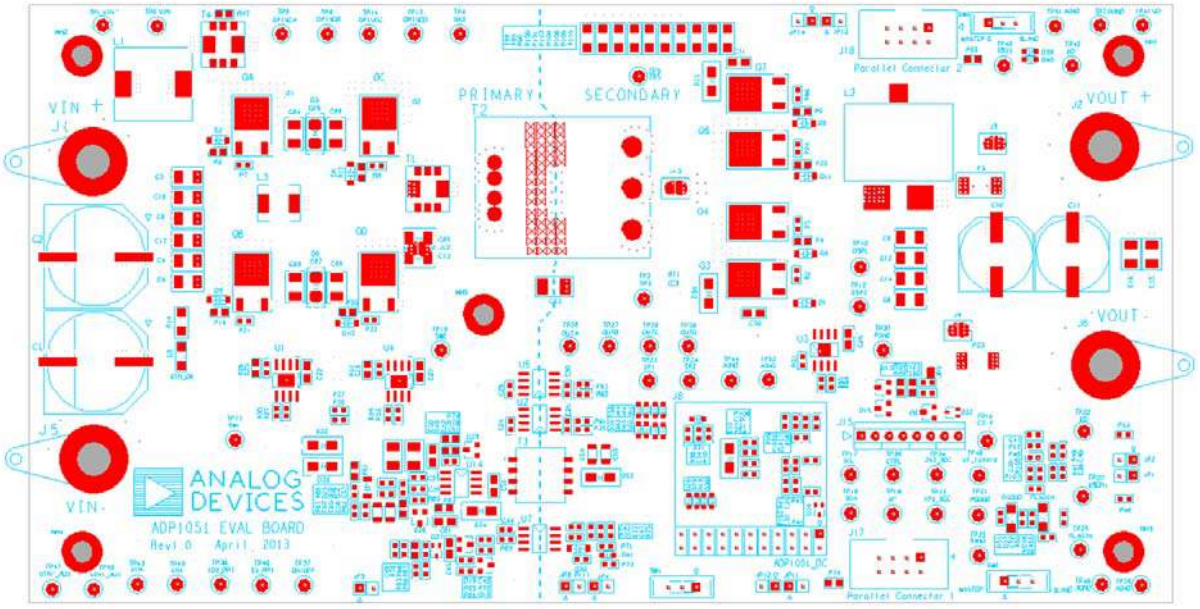


Figure 65. PCB Layout, Silkscreen Layer

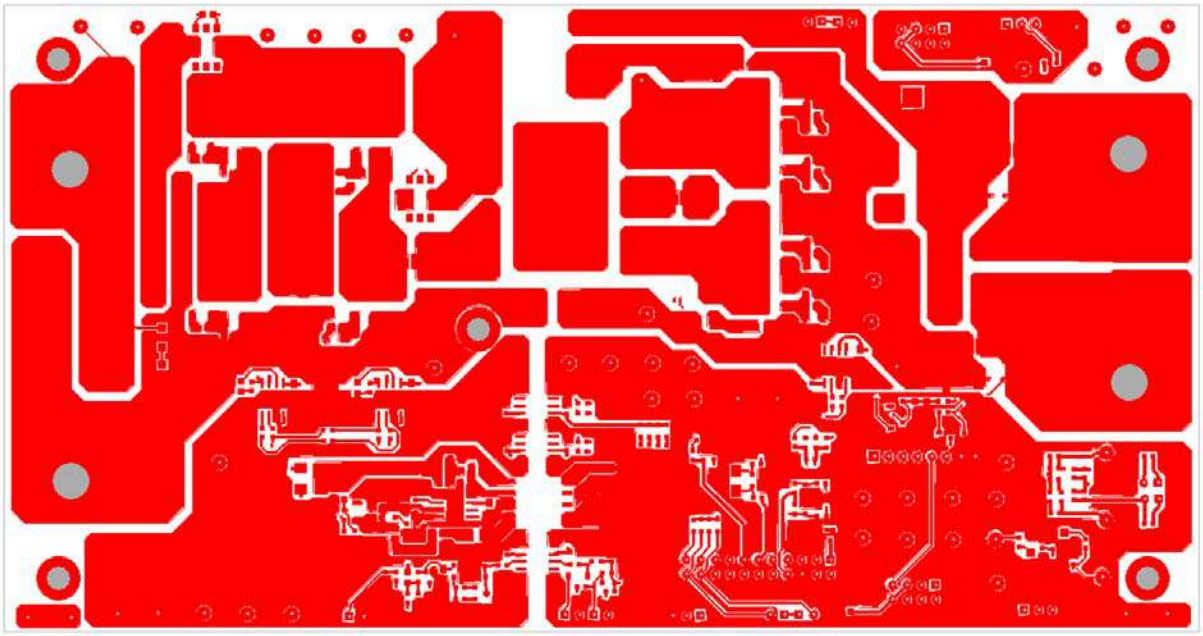


Figure 66. PCB Layout, Top Layer

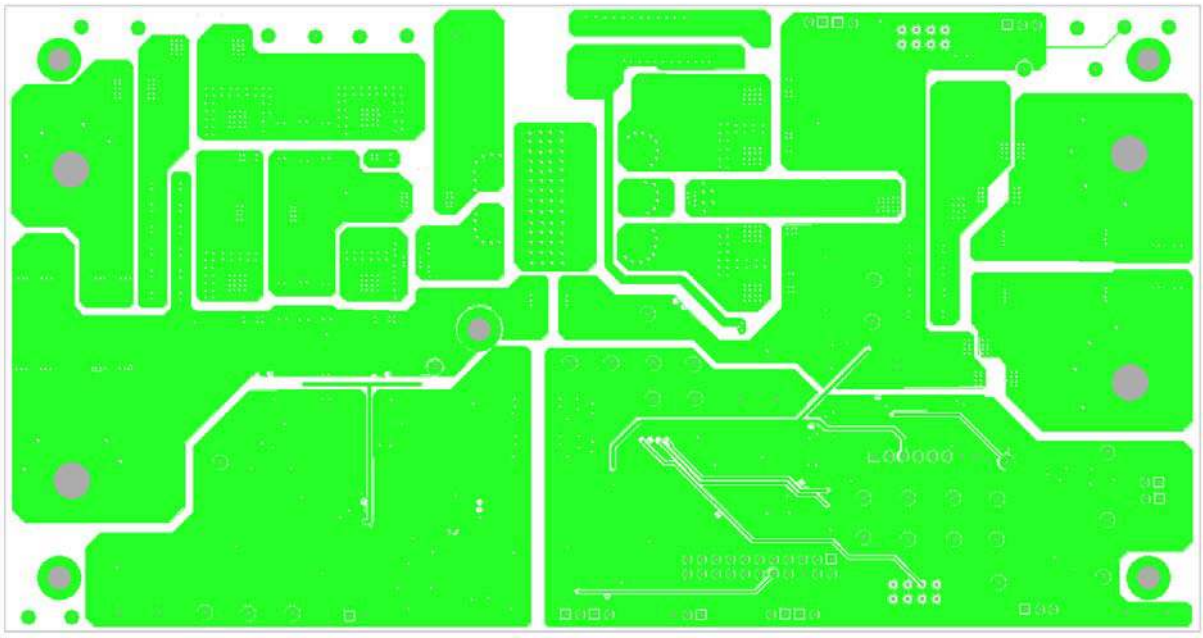


Figure 67. PCB Layout, Layer 2

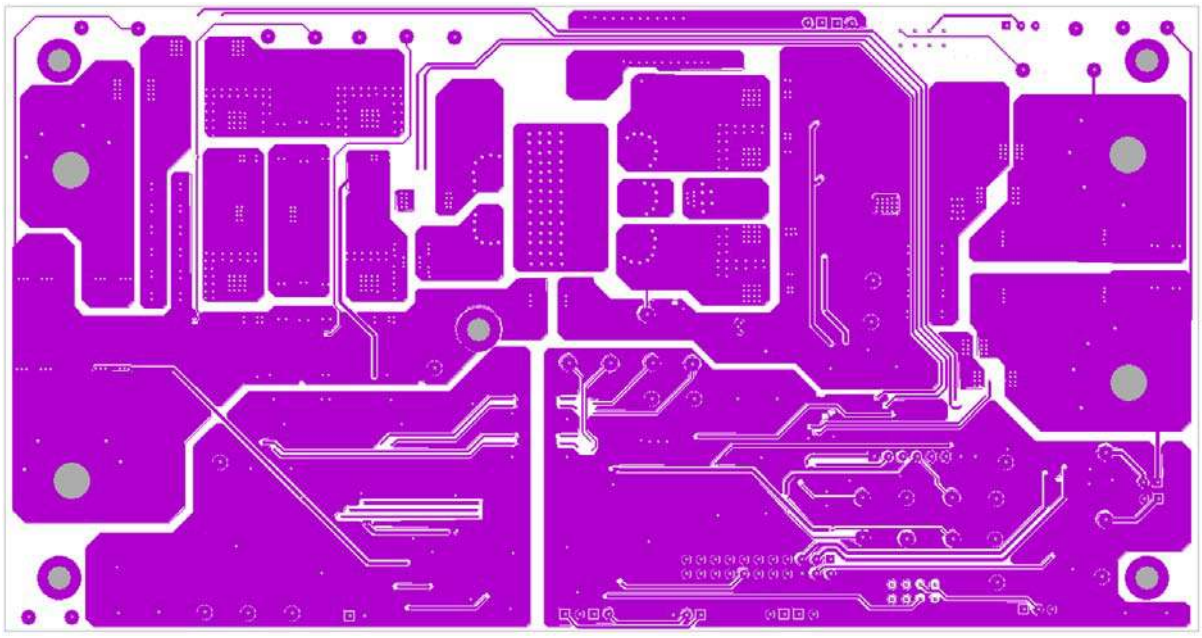


Figure 68. PCB Layout, Layer 3

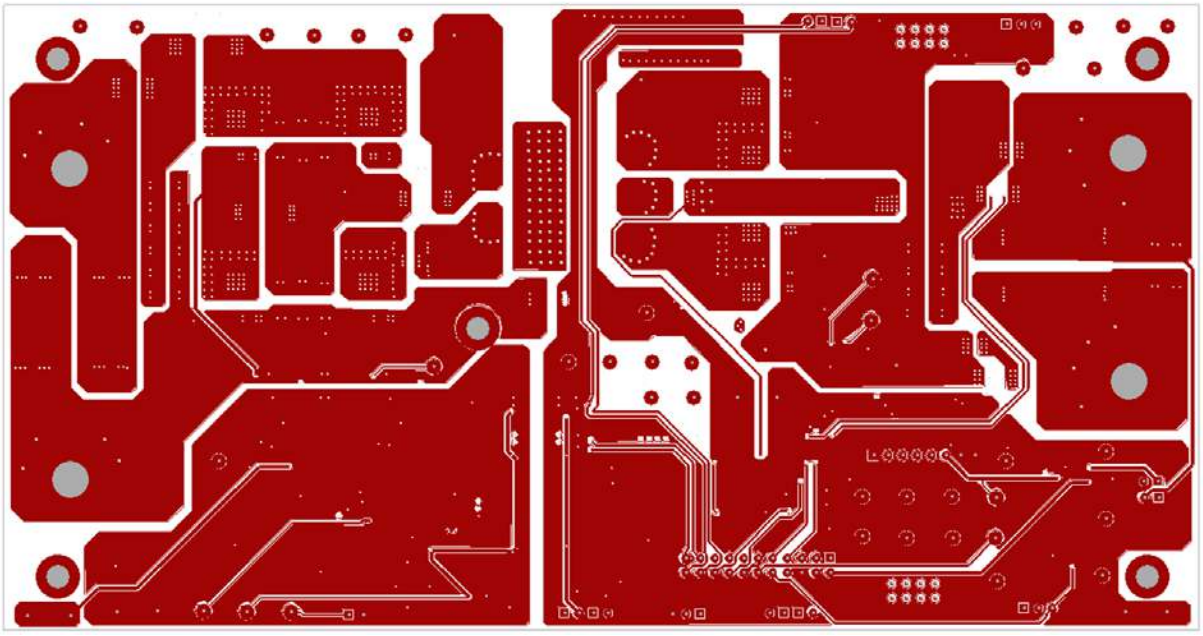


Figure 69. PCB Layout, Layer 4

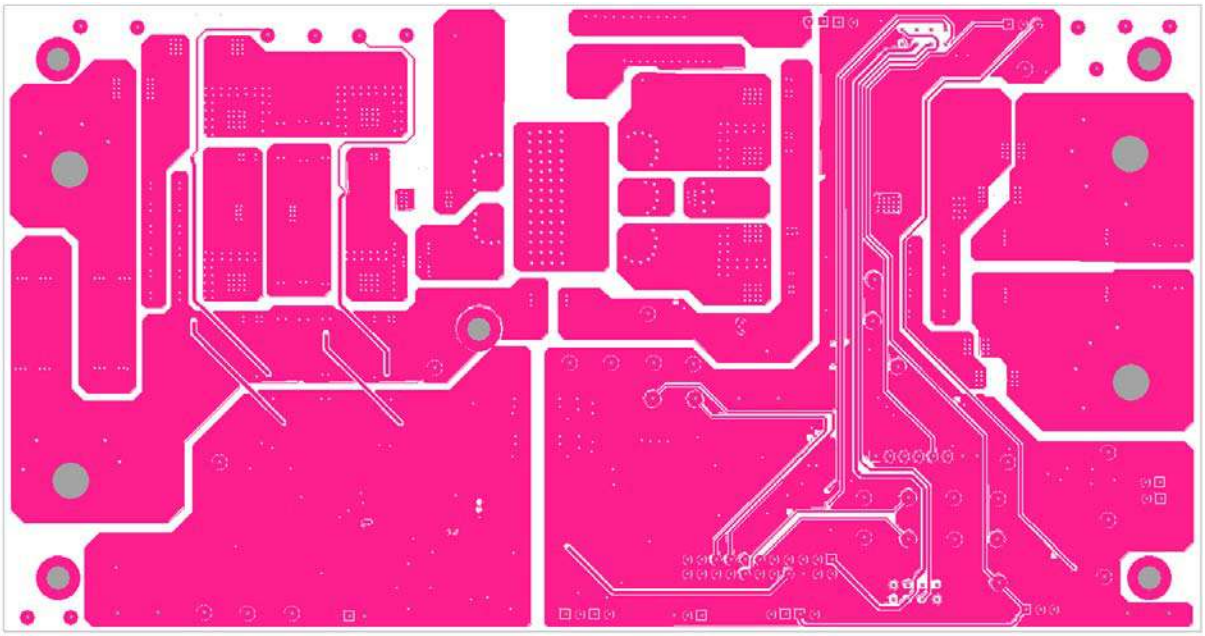


Figure 70. PCB Layout, Layer 5

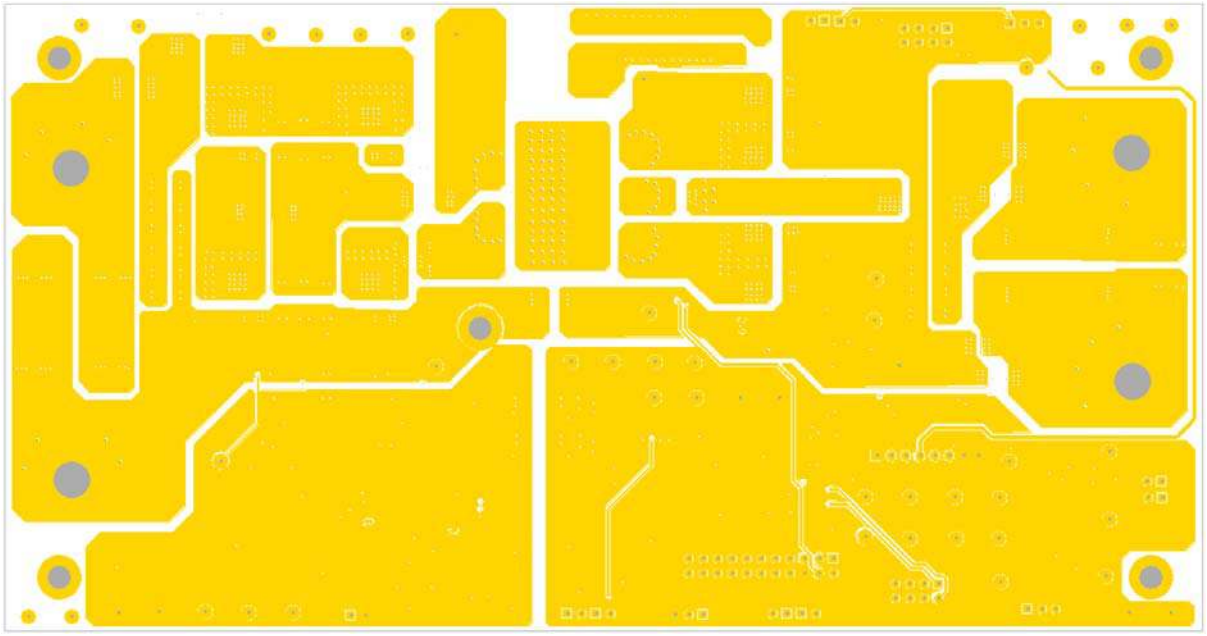


Figure 71. PCB Layout, Bottom Layout

ADP1051DC1-EVALZ

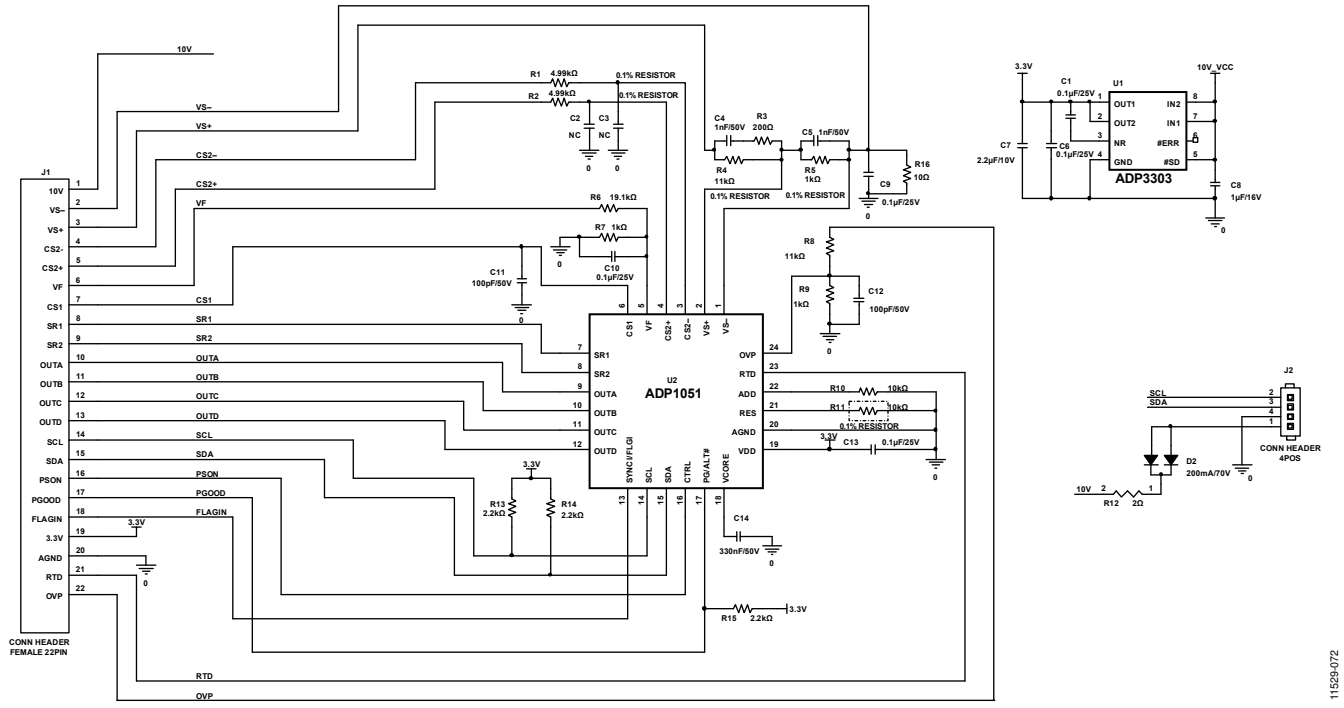


Figure 72. ADP1051 Daughter Schematic

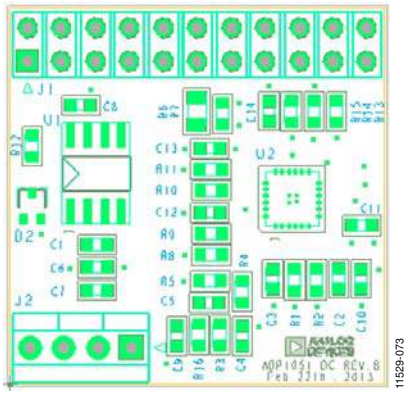


Figure 73. PCB Layout, Silkscreen Layer

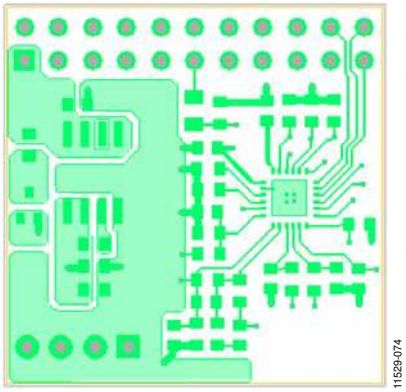


Figure 74. PCB Layout, Top Layer

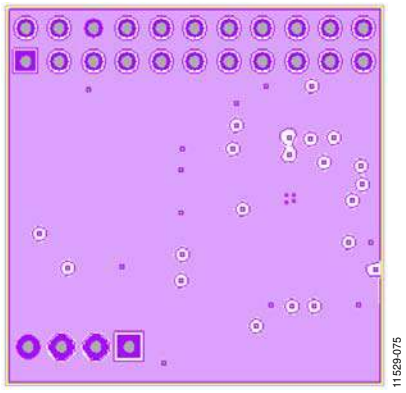


Figure 75. PCB Layout, Layer 2

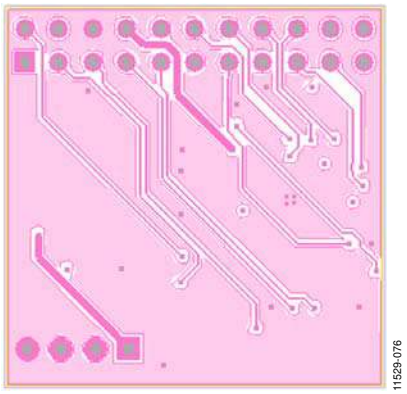


Figure 76. PCB Layout, Layer 3

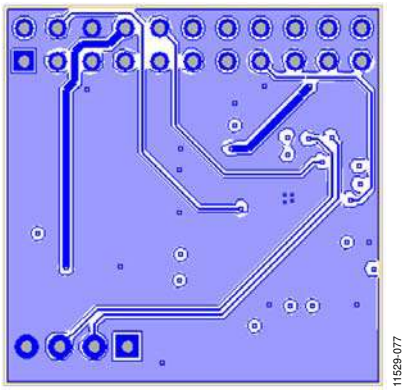


Figure 77. PCB Layout, Bottom Layer

CURRENT SHARE DAUGHTER CARD

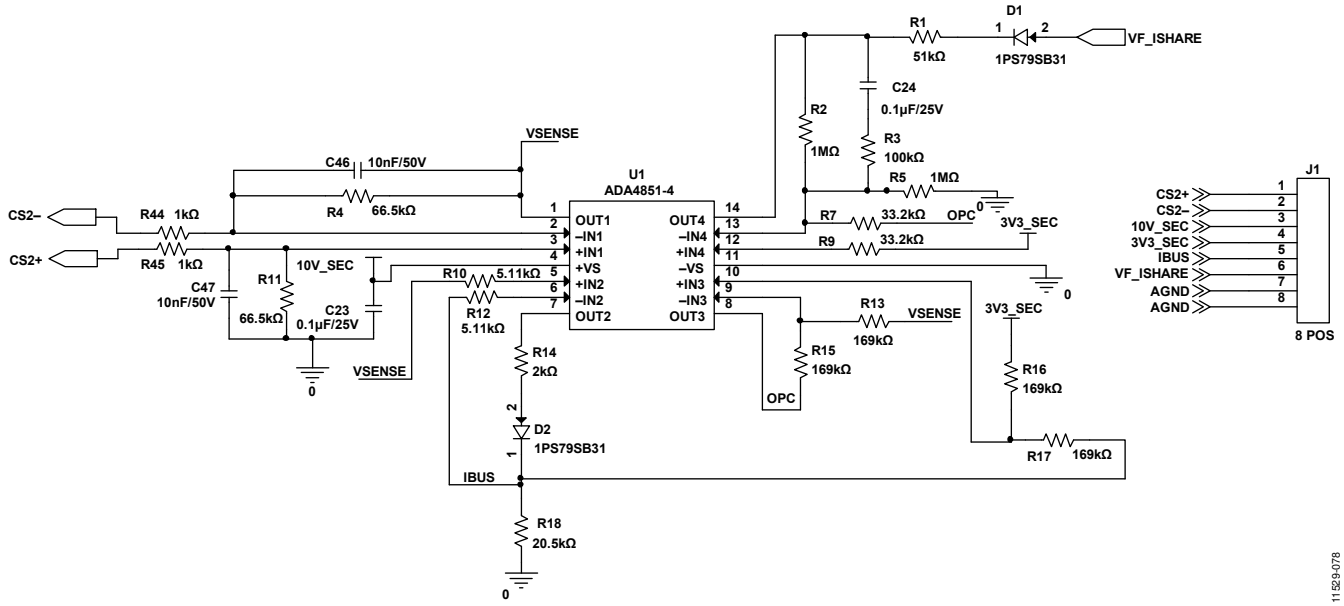


Figure 78. Current Share Daughter Card Schematic

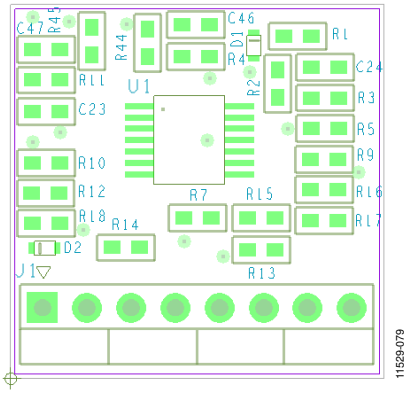


Figure 79. PCB Layout, Silkscreen Layer

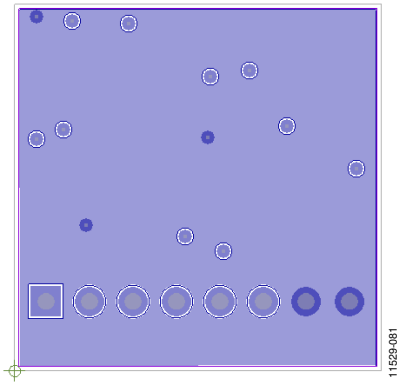


Figure 81. PCB Layout, Layer 2

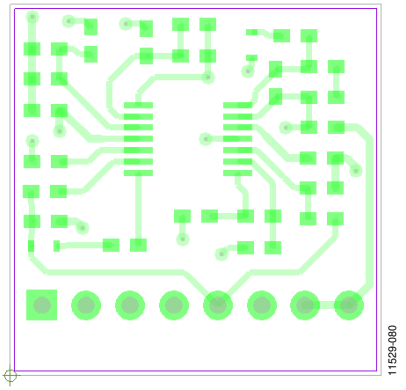


Figure 80. PCB Layout, Top Layer

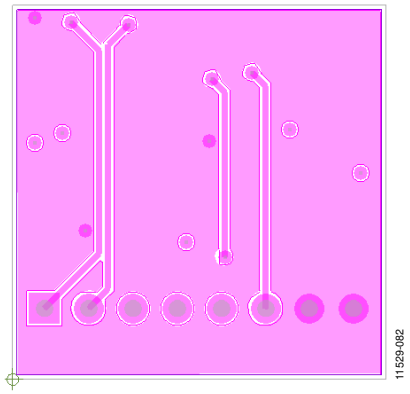


Figure 82. PCB Layout, Layer 3

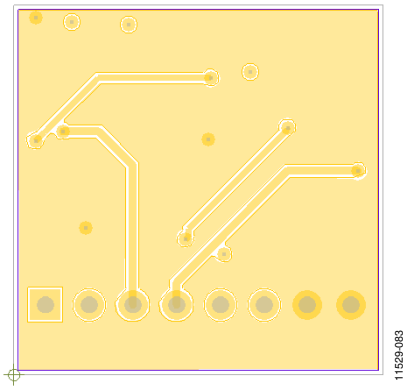


Figure 83. PCB Layout, Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 10. ADP1051 Evaluation Board

Qty	Reference Designator	Part Number		Footprint	Description
		Manufacturer	Digi-Key[1]		
2	C1, C2	EEEFK2A221AM	PCE4866TR-ND	SMC-AEC-TG-K16	Capacitor ALUM 220 µF 100 V 20% SMD
8	C3, C4, C5, C6, C17, C18, C49, C50	C3225X7R2A225K	445-4497-2-ND	C1210	Capacitor 2.2 µF/100 V X7R 1210
6	C8, C9, C12, C14, C15, C16	GRM32ER71H475KA88	490-1864-2-ND	C1210	Capacitor ceramic 4.7 µF 50 V 10% X7R 1210
2	C10, C11	EEEFK1V471AQ	PCE4862TR-ND	AL_CAP_H13	Capacitor ALUM 470 µF 35 V 20% SMD
2	C13, C85	C3225X7R2A225K	445-4497-2-ND	C1210	Capacitor ceramic 2.2 µF 100 V 10% X7R 1210
6	C22, C26, C27, C45, C56, C61	C2012X7R1E105K	445-1354-2-ND	C0805	Capacitor ceramic 1 µF 25 V 10% X7R 0805
9	C23, C24, C25, C28, C29, C30, C43, C44, C57	C1608X7R1E104K	445-1316-2-ND	C0603	Capacitor ceramic 0.1 µF 25 V 10% X7R 0603
1	C31	C1608X7R1H104K	445-1314-2-ND	C0603	Capacitor ceramic 0.1µF 50 V 10% X7R 0603
2	C32, C36	C1608COG1H330J	445-1257-2-ND	C0603	Capacitor ceramic 33 pF 50 V 5% NP0 0603
2	C34, C35	C1608COG1H101J	445-1281-2-ND	C0603	Capacitor ceramic 100 pF 50 V 5% NP0 0603
4	C38, C39, C40, C41	C1608COG1H102J	445-1293-2-ND	C0603	Capacitor ceramic 1000 pF 50 V 5% NP0 0603
1	C42	C1608X7R1H104K	445-1314-2-ND	C0603	Capacitor ceramic 0.1 µF 50 V 10% X7R 0603
4	C46, C47, C48, C72	C1608X7R1H103J	445-5089-2-ND	C0603	Capacitor ceramic 10 nF 50 V 5% X7R 0603
1	C51	C1608C0G2E471J	445-2318-2-ND	C0603	Capacitor ceramic 470 pF 250 V 5% NP0 0603
1	C52	C2012X7R2A104K	445-1418-2-ND	C0805	Capacitor ceramic 0.1 µF 100 V 10% X7R 0805
4	C53, C54, C58, C60	C3216X7R1C106K	445-4042-2-ND	C1206	Capacitor ceramic 10 µF 16 V 10% X7R 1206
1	C55	C1608C0G1H391J	445-1288-2-ND	C0603	Capacitor ceramic 390 pF 50 V 5% NP0 0603
1	C59	C1608COG1H102J	445-1293-2-ND	C0603	Capacitor ceramic 1 nF 50 V 5% NP0 0603
1	C62	C1608COG2A221J	445-2308-2-ND	C0603	Capacitor ceramic 220 pF 100 V 5% NP0 0603
1	C63	202S43W102KV4E	709-1053-2-ND	C1812	Capacitor ceramic 1 nF 2 KV 10% X7R 1812
6	C64, C65, C66, C67, C68, C69	C3225X7R1H335K	445-3936-2-ND	C1210	Capacitor ceramic 3.3 µF 50 V 10% X7R 1210
2	C70, C71	C2012X7R2E103K	445-2280-2-ND	C0805	Capacitor ceramic 10 nF 250 V X7R 0805
9	D1, D2, D4, D5, D6, D9, D10, D11, D20	MBR130LSFT1G	MBR130LSFT1GOSTR-ND	SOD123	Schottky diode 1 A 30 V SOD-123FL
9	D3, D8, D12, D22, D24, D32, D33, D34, D35	MURA110T3G	MURA110T3GOSTR-ND	SMA	Diode ultrafast 2 A 100 V SMA
3	D7, D17, D18	CMD15-21UBC/TR8	L62206CT-ND	D1206	LED blue clear 1206 SMD
2	D13, D15	BAV99	BAV99FSTR-ND	SOT23	Diode ultrafast HI COND 70 V SOT-23
3	D14, D21, D37	BAV70WT1G	BAV70WT1GOSTR-ND	SOT323	Diode switch dual CC 70 V SOT323
13	D16, D28, D31, D36, D38, D39, D40, D43, D44, D45, D46, D51, D52	BAT42WS-7	BAT42WSDITR-ND	SOD323	Schottky diode 30 V 200MW SOD-323
1	D19	ZR431F01TA	ZR431F01TR-ND	SOT23-IC	IC VREF shunt PREC ADJ SOT-23
1	D23	MMBD1504A	MMBD1504ATR-ND	SOT23	Diode SS 200 V 200 MA SOT23
1	D25	EGL34B-E3/83	EGL34B-E3/83-ND	DO-213AA	Diode 0.5A 100 V 50 NS MELF
1	D26	MMBZ5231BLT1G	MMBZ5231BLT1GOSTR-ND	SOT23	Diode Zener 5.1 V 225 MW SOT-23
3	D29, D30, D41	BAT42WS-7	BAT42WSDITR-ND	SOD323	Schottky diode 30 V 200 MW SOD-323
9	JP1, JP2, JP3, JP4, JP5, JP11, JP12, JP13, JP14	STC02SYAN	S9000-ND	HEADER-SR-2	Connector jumper shorting tin
1	JP9	N/A	N/A	Shortpin	Single connect point of AGND and PGND
4	J1, J2, J5, J6	108-0740-001	J147-ND	B-JACK	Connector jack banana
4	J3, J4, J12, J13	N/A	N/A	PADJUMPER	Power connector jumper on PCB
1	J8	TSW-111-14-T-D	SAM1058-11-ND	HEADER-DR-22	Connector header 22POS 0.100 dual tin 22 male pin 2.54
1	J15	PPC081LFBN-RC	S4108-ND	HEADER-I-SR-8	Single row 8 female pin 2.54 mm
2	J17, J18	75869-132LF	609-3530-ND	313-208-s2	Connector header 8POS dual vert PCB
1	L1	IHLP5050FDER1R0M01	541-1032-2-ND	IND-IHLP-5050FD	Power inductor 1.0 µH 32 A SMD
1	L2	#7443630420	N/A	LER-20-63	Power inductor 4.2uH 24 A 3.04 mΩ SMD
		LER-20-63	N/A		Power Inductor 3.6 µH 30 A 2.3 mΩ SMD
1	L3	IHLP2525EZERR56M01	IHLP2525EZERR56M01-ND	2525ez	power Inductor 0.56 µH 20 A SMD

Qty	Reference Designator	Part Number		Footprint	Description
		Manufacturer	Digi-Key[1]		
5	MH1, MH2, MH3, MH4, MH5	R30-1011602	952-1492-ND	MH	Standoff HEX M3 THR Brass 16 mm
8	QA, QB, QC, QD, Q3, Q4, Q7, Q8	IPD068N10N3 G	IPD068N10N3 G-ND	DPAK	MOSFET N-CH 100 V 90 A TO252-3
1	Q9	BSS138	BSS138TR-ND	SOT23	MOSFET N-CH 50 V 220 MA SOT-23
1	Q10	MMBT2907A	MMBT2907AFSTR-ND	SOT23	Transistor GP PNP AMP SOT-23
1	RT1	NCP15WF104F03RC	490-4803-2-ND	R0402	Thermistor 100 kΩ NTC 0402 SMD resistance 1% beta
12	R2, R5, R7, R8, R21, R22, R24, R67, R77, R85, R96, R98	CRCW060310K0JNTA	CRCW060310K0JNTA-ND	R0603	Resistor 10 kΩ 5% 1/10 W 0603 SMD
2	R3, R23	ERJ-M1WTF2M0U	P2.0NDTR-ND	R2512	Resistor 0.002 Ω 1 W 1% 2512
8	R1, R4, R6, R9, R11, R19, R20, R25	CRCW08052R00JNEA	541-2.0ATR-ND	R0805	Resistor 2 Ω 5% 1/8 W 0805 SMD
1	R10	CRCW060310K0JNTA	CRCW060310K0JNTA-ND	R0603	Resistor 10 kΩ 5% 1/10 W 0603 SMD
1	R14	CRCW120630K1FKEA	541-30.1KFTR-ND	R1206	Resistor 30.1 kΩ 1/4 W 1% 1206 SMD
2	R26, R32	CRCW08050000Z0EA	541-0.0ATR-ND	R0805	Resistor 0.0 Ω 1/8 W 0805 SMD
19	R27, R30, R33, R34, R35, R47, R48, R54, R57, R59, R70, R73, R91, R92, R93, R94, R95, R105, R123	CRCW06030000Z0EA	541-0.0GTR-ND	R0603	Resistor 0.0 Ω 1/10 W 0603 SMD
9	R31, R36, R37, R49, R58, R60, R107, R111, R140	CRCW06030000Z0EA	541-0.0GTR-ND	R0603	Resistor 0.0 Ω 1/10 W 0603 SMD
1	R38	CRCW0603100RFKEA	541-100HCT-ND	R0603	Resistor 100 Ω 1/10 W 1% 0603 SMD
2	R39, R40	CRCW080510R0FKEA	541-10.0CTR-ND	R0805	Resistor 10.0 Ω 1/8 W 1% 0805 SMD
4	R41, R43, R46, R53	CRCW060310R0FKEA	541-10.0HTR-ND	R0603	Resistor 10.0 Ω 1/10 W 1% 0603 SMD
2	R45, R102	CRCW06034K10JNEA	541-4.7KGCT-ND	R0603	Resistor 4.7 kΩ 1/10 W 5% 0603 SMD
1	R50	CRCW060316K5FKTA	CRCW060316K5FKTA-ND	R0603	Resistor 16.5 kΩ 1% 1/10 W 0603 SMD
4	R51, R56, R64, R69	CRCW06031K00FKEA	541-1.00KHCT-ND	R0603	Resistor 1.00 kΩ 1/10 W 1% 0603 SMD
1	R52	CRCW06031K00FKEA	541-1.00KHCT-ND	R0603	Resistor 1.00 kΩ 1/10 W 1% 0603 SMD
1	R63	CRCW0603220KFKEA	541-220KHTR-ND	R0603	Resistor 220 kΩ 1/10 W 1% 0603 SMD
3	R65, R72, R75	CRCW06035K10JNEA	541-5.1KGCT-ND	R0603	Resistor 5.1 kΩ 1/10 W 5% 0603 SMD
1	R66	CRCW0805100KJNEA	541-100KATR-ND	R0805	Resistor 100 kΩ 1/8 W 5% 0805 SMD
1	R68	CRCW06038K20FKEA	541-8.20KHCT-ND	R0603	Resistor 8.20 kΩ 1/10 W 1% 0603 SMD
3	R71, R76, R106	CRCW0603220RJNEA	541-220GCT-ND	R0603	Resistor 220 Ω 1/10W 5% 0603 SMD
2	R74, R99	CRCW08051R00JNEA	541-1.0ATR-ND	R0805	Resistor 1 Ω 5% 1/8W 0805
2	R78, R79	CRCW080520R0JNEA	541-20ACT-ND	R0805	Resistor 20 Ω 1/8 W 5% 0805 SMD
1	R80	CRCW060314K0FKEA	541-14.0KHTR-ND	R0603	Resistor 14.0 kΩ 1/10 W 1% 0603 SMD
1	R81	CRCW08051M00FKEA	541-1.00MCTR-ND	R0805	Resistor 1.00 M Ω 1/8 W 1% 0805 SMD
2	R82, R83	CRCW0805680RJNEA	541-680ACT-ND	R0805	Resistor 680 Ω 1/8 W 5% 0805 SMD
1	R84	CRCW06035K10FKEA	541-5.10KHTR-ND	R0603	Resistor 5.10 kΩ 1/10 W 1% 0603 SMD
1	R86	CRCW060354K9FKEA	541-54.9KHTR-ND	R0603	Resistor 54.9 kΩ 1/10 W 1% 0603 SMD
1	R87	CRCW060336K0FKEA	541-36.0KHTR-ND	R0603	Resistor 36.0 kΩ 1/10 W 1% 0603 SMD
10	R88, R89, R90, R100, R101, R103, R104, R108, R109, R110	CRCW120620K0JNEA	541-20KETR-ND	R1206	Resistor 20 kΩ 1/4 W 5% 1206 SMD
1	R97	CRCW080510K0JNEA	541-10KATR-ND	R0805	Resistor 10 kΩ 1/8 W 5% 0805 SMD
3	SW1, SW2, SW3	EG1218	EG1903-ND	SPDT-SLSW	Switch slide SPDT 30 V.2A PC MNT

Qty	Reference Designator	Part Number		Footprint	Description
		Manufacturer	Digi-Key[1]		
43	TP1, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP33, TP34, TP35, TP36, TP37, TP38, TP40, TP41, TP42, TP47, TP48, TP49, TP50, TP51	5010	5010K-ND	TP-70	Test point PC
3	TP39, TP44, TP45	GTP002	N/A	TP-70 dual	Ground test point
1	T1	PA1005.100NL	553-1529-2-ND	P820X	XFRMR current sense 2.0 MH 1:100 SMD
1	T2	#750341378	N/A	BDC_2512	Transformer ER25 5:2:2
		BDC-25-69	N/A		Transformer ER25 5:2:2
1	T3	#750341379	N/A	PBSER9-77	36 V to 75 V input, 12 V 0.25 A pri output, 12 V, 0.25 A sec output, ER9.5 22:8:8
		BSER9-77	N/A		36 V to 75 V input, 12 V pri output, 12 V sec output, ER9.5 22:8:8
1	T4	PA1005.100NL	553-1529-2-ND	P820X	XFRMR current sense 2.0 MH 1:100 SMD
2	U1, U4	HIP2101EIBZT	HIP2101EIBZTTR-ND	8-SOIC-EP	IC driver half bridge 100 V 8EPSOIC
3	U2, U5, U7	ADUM3210BRZ-RL7	ADUM3210BRZ-RL7TR-ND	8-SOIC	*i*Coupler 2CH 8-SOIC
1	U3	ADP3654ARDZ-R7	ADP3654ARDZ-R7-ND	8-SOIC_N_EP	IC MOSFET DVR 4 A dual HS SOIC_N_EP
1	U14	NCP1031DR2G	NCP1031DR2GOSTR-ND	8-SOIC	IC CTRLR PWM OTP OVD HV 8SOIC

[1] N/A = not applicable.

Table 11. ADP1051 Daughter Card

Qty	Reference Designator	Part Number		Footprint	Description
		Manufacturer	Digi-Key[1]		
5	C1, C6, C9, C10, C13	C1608X7R1H104K	445-1316-2-ND	C0603	Capacitor ceramic 0.1 µF 25 V 10% X7R 0603
2	C2, C3	C1608X7R1H104K	445-1316-2-ND	C0603	Capacitor ceramic 0.1 µF 25 V 10% X7R 0603
2	C4, C5	C1608COG1H102J	445-1293-2-ND	C0603	Capacitor ceramic 1 nF 50 V 5% NP0 0603
1	C7	C1608X7R1A225K	445-5958-6-ND	C0603	Capacitor ceramic 2.2 µF 10 V 10% X7R 0603
1	C8	C1608X7R1C105K	445-1604-2-ND	C0603	Capacitor ceramic 1 µF 16 V 10% X7R 0603
2	C11, C12	C1608COG1H101J	445-1281-2-ND	C0603	Capacitor ceramic 100 pF 50 V 5% NP0 0603
1	C14	C1608X7R1H334K	445-5950-2-ND	C0603	Capacitor ceramic 330 nF 50 V 10% X7R 0603
1	D2	BAV70WT1G	BAV70WT1GOSTR-ND	SOT323	Diode switch dual CC 70 V SOT323
1	J1	PPPC112LFBN-RC	S7114-ND	Header-dr-22	Connector header FMAL 22PS.1" DL gold
1	J2	69167-104HLF	609-2411-ND	HEADER-L-SR-4	Connector header 4POS SGL PCB 30GOLD
2	R1, R2	9-1879360-4	9-1879360-4-ND	R0603	Resistor 4.99 kΩ 1/16 W 0.1% 0603 10PPM
1	R3	CRCW0603200RFKEA	541-200HTR-ND	R0603	Resistor 200 Ω 1/10 W 1% 0603 SMD
1	R4	TNPW060311K0BEEA	TNP11.0KAATR-ND	R0603	Resistor 11 kΩ 1/10 W 0.1% 0603 SMD
1	R5	TNPW06031K00BEEA	TNP1.00KAATR-ND	R0603	Resistor 1.00 kΩ 1/10 W 0.1% 0603 SMD
1	R6	CRCW080519K1FKEA	541-19.1KCTR-ND	R0805	Resistor 19.1 kΩ 1/8 W 1% 0805 SMD
2	R7, R9	CRCW06031K00FKEA	541-1.00KHCT-ND	R0603	Resistor 1.00 kΩ 1/10 W 1% 0603 SMD
1	R8	CRCW060311K0FKEA	541-11.0KHTR-ND	R0603	Resistor 11 kΩ 1/10 W 1% 0603 SMD
1	R10	CRCW060310K0FKEA	541-10.0KHTR-ND	R0603	Resistor 10 kΩ 1% 1/10 W 0603 SMD
1	R11	TNPW060310K0BEEA	TNP10.0KAATR-ND	R0603	Resistor 10 kΩ 0.1% 1/10 W 0603 SMD
1	R12	CRCW06032R00FKEA	541-2.00HHTR-ND	R0603	Resistor 2 Ω 1% 1/10 W 0603 SMD
3	R13, R14, R15	CRCW06032K20FKEA	541-2.20KHTR-ND	R0603	Resistor 2.2 kΩ 1% 1/10 W 0603 SMD
1	R16	CRCW060310R0FKEA	541-10.0HTR-ND	R0603	Resistor 10 Ω 1% 1/10 W 0603 SMD
1	U1	ADP3303ARZ-3.3	ADP3303ARZ-3.3-ND	SO8	IC regulator LDO 200 MA 3.3 V 8-SOIC
1	U2	ADP1051ACPZ	N/A	CP-24-7	Digital controller ADP1051 CP-24-7

[1] N/A = not applicable.

Table 12. Current Share Daughter Card

Qty	Reference Designator	Part Number		Footprint	Description
		Manufacturer	Digi-Key		
2	C23, C24	C1608X7R1H104K	445-1316-2-ND	C0603	Capacitor ceramic 0.1 µF 25 V 10% X7R 0603
2	C46, C47	C1608X7R1H103J	445-5089-2-ND	C0603	Capacitor ceramic 10000 pF 50 V 5% X7R 0603
2	D1, D2	1PS79SB31	1PS79SB31,315-ND	SOD523	Diode Schottky 30 V 200 mA SC-79
1	J1	PPC081LFBN-RC	09-3321-ND	HEADER-SR-8	CONN HEADER 8POS 0.100 R/A 15AU
1	R1	CRCW060351K0FKEA	541-51.0KHTR-ND	R0603	Resistor 51.0 kΩ 1/10 W 1% 0603 SMD
2	R2, R5	CRCW06031M00FKEA	541-1.00MHTR-ND	R0603	Resistor 1.00 MΩ 1/10 W 1% 0603 SMD
1	R3	CRCW0603100KFKEA	541-100KHTR-ND	R0603	Resistor 100 kΩ 1/10 W 1% 0603 SMD
2	R4, R11	CRCW060366K5FKEA	541-66.5KHTR-ND	R0603	Resistor 66.5 kΩ 1/10 W 1% 0603 SMD
2	R7, R9	CRCW060333K2FKEA	541-33.2KHTR-ND	R0603	Resistor 33.2 kΩ 1/10 W 1% 0603 SMD
2	R10, R12	CRCW06035K11FKEA	541-5.11KHTR-ND	R0603	Resistor 5.11 kΩ 1/10 W 1% 0603 SMD
4	R13, R15, R16, R17	CRCW0603169KFKEA	541-169KHTR-ND	R0603	Resistor 169 kΩ 1/10 W 1% 0603 SMD
1	R14	CRCW06032K00FKEA	541-2.00KHTR-ND	R0603	Resistor 2.00 kΩ 1/10 W 1% 0603 SMD
1	R18	CRCW060320K5FKEA	541-20.5KHTR-ND	R0603	Resistor 20.5 kΩ 1/10 W 1% 0603 SMD
2	R44, R45	CRCW06031K00FKEA	541-1.00KHCT-ND	R0603	Resistor 1.00 kΩ 1/10 W 1% 0603 SMD
1	U1	ADA4851-4YRUZ	ADA4851-4YRUZ-ND	TSSOP14	IC op amp VF R-R quad LP 14-lead TSSOP

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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