

## MPC5748G Low Cost EVB User Guide

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# 1. Introduction

This user guide details the setup and configuration of the NXP MPC5748G Low Cost Evaluation Board (hereafter referred to as the LCEVB). The LCEVB is intended to provide a mechanism for easy evaluation of the MPC5748G family of microcontrollers, and to facilitate basic hardware and software development.

Note that the LCEVB has a limited feature set compared to the main MPC574xG customer EVB and is intended for evaluation purposes. Customers moving to serious development activities are recommended to purchase the fully functional customer EVB which also has device specific daughter cards.

The LCEVB is intended for bench / laboratory use and has been designed using normal temperature specified components (+70° C).

This product contains components that may be damaged by electrostatic discharge. Observe precautions for handling electrostatic sensitive devices when using the LCEVB.

The user guide is intended to be read alongside the respective MCU documentation available at [www.nxp.com](http://www.nxp.com) and includes:

- Reference Manuals
- Product Data Sheets
- Application notes
- Device Errata

## 2. LCEVB Features

The LCEVB provides the following key features:

- Single 5 V DC external power supply input with on-board 3.3 V regulator. Power is supplied via a 2.1 mm barrel style power jack.
- Simple jumperless configuration (enhanced configuration is possible via 0 Ohm Resistors and optional jumpers if required).
- Master power switch and regulator status LED.
- USB Serial interface.
- 2 x High Speed CAN transceiver routed to 3-way headers.
- 2 x LIN interfaces routed to 3-way headers.
- Main clock supplied from on board crystal.
- User reset switch with reset status LED's.
- Ethernet PHY and RJ45 socket (configured for MII mode).
- USB Type A Host interface.
- 2 x FlexRay interfaces with standard 2-pin connectors.
- 14-pin JTAG connector.

- 4 user LED's wired to MCU ports.
- 2 user pushbutton switches wired to MCU ports.
- Hexadecimal encoded switch wired to 4 MCU ports.
- Simple potentiometer connected to analogue input channel.

## 2.1. Differences to the Customer EVB

Note that the GPIO pins used for peripherals on the LCEVB are the same as those used on the customer EVB. This ensures maximum code compatibility between the 2 boards, making it easy to migrate from one board to the other

**Table 1. Customer EVB vs LCEVB features**

Feature	Customer EVB	LCEVB
MCU Support	Custom MCU Daughtercards for multiple devices (socketed)	Soldered 176QFP MPC5748G
Power Supply	External 12 V	<b>External 5 V (Caution)</b>
On Board Regulators (and LED's)	5 V, 3.3 V, 1.25 V (combination of Linear and /or Switching regulators)	3.3 V Switching Regulator
Master Power Switch	Yes	Yes
Reset Control	Reset button with MCU and External Reset LED's	Reset button with MCU and External Reset LED's
USB FTDI Serial Interface	Yes	Yes
CAN Physical Interfaces	2 (routed to 0.1" headers)	2 (routed to 0.1" headers)
LIN Physical Interfaces	2 (routed to Molex headers)	2 (routed to 0.1" headers)
FlexRay Physical Interfaces	2 (routed to 0.1" headers)	2 (routed to 0.1" headers)
Ethernet Physical Interface	1 (MII and RMII Support)	1 (MII only mode)
USB Physical Interface	2 (USB Host and OTG)	1 (USB Host)
MLB Daughtercard Connector	Yes	No
SAI Audio / TWRPI Connectors	Yes	No
SDHC Connector	Full Size SDHC Socket	No
Fast External Osc (FXOSC)	Daughtercard Crystal * and SMA input connector	40 MHz Crystal
Slow External Osc (SXOSC)	Daughtercard Crystal *	32.768 KHz Crystal
CLKOUT signals available	Yes (GPIO Matrix)	Yes (Standalone pads)
User LEDS	4	4
User Pushbutton Switches	4	2
Hex Encoded Switch	Yes	Yes
Test Potentiometer for ADC	Yes	Yes
GPIO Matrix	All Available Pins not otherwise used for peripherals	Selection of Pins available from 5 GPIO Ports
Debug	14 Pin JTAG and 50 pin Nexus	14 Pin JTAG
Configuration	Highly configurable via jumper shunts	Fixed (limited configuration via 0 ohm resistors)

\* Daughtercard crystals are typically 40 MHz for FXOSC and 32.768 KHz for SXOSC but may vary between daughtercards.

The figure below shows the customer EVB (left) next to the LCEVB(right).

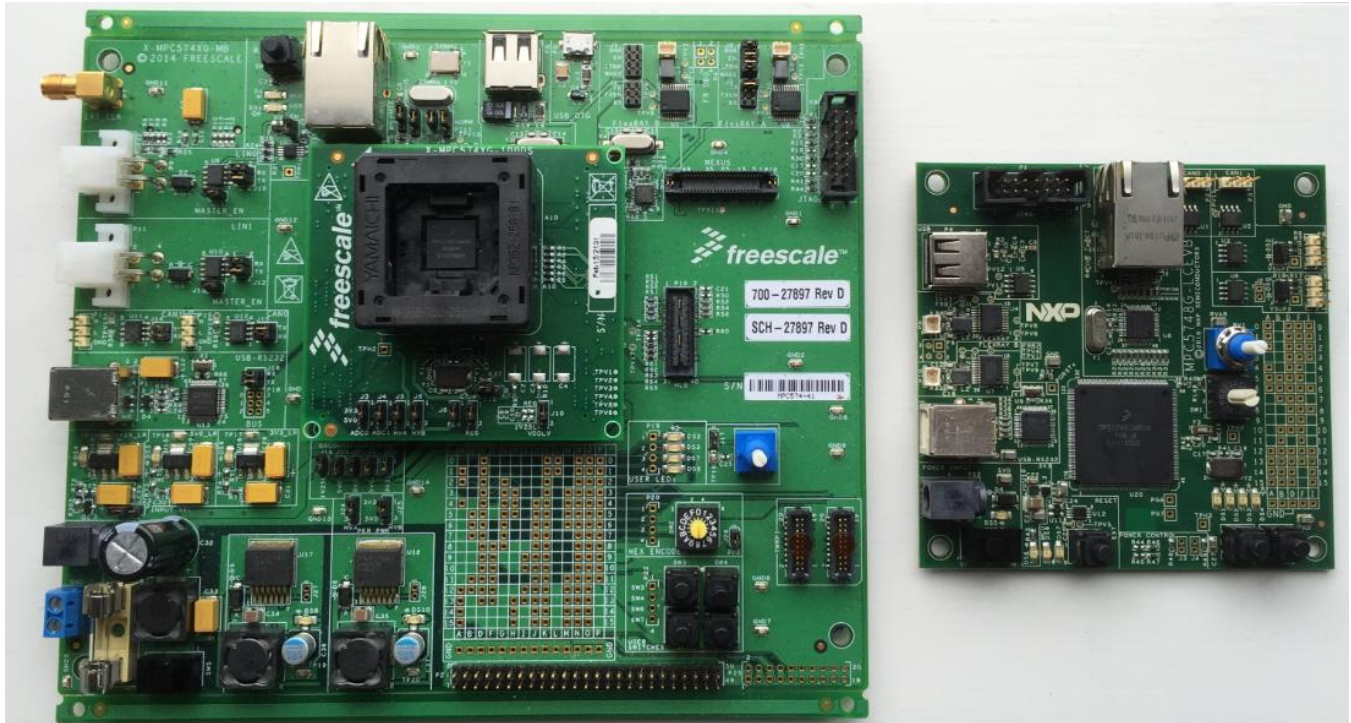


Figure 1. Customer and LCEVB side by side



### 3. Configuration Overview

Out of the box, there is no configuration required for the LCEVB to function. Unlike the customer EVB, the LCEVB is primarily designed for a single mode of operation with no requirement for user configuration. If you wish to have a more flexible configuration the recommendation is that the fully configurable customer EVB is purchased.

There are however some jumper footprints and zero ohm resistors populated in positions that would normally have jumper headers fitted (for example on the MCU power supply lines and tracking to the peripheral interfaces). If required these can be de-soldered to modify functionality. Any such modification is done at the full risk of the user and no support or warranty repairs will be provided for a board that has been modified. Modifications should only be attempted by appropriately trained personnel using the correct equipment and Personal Protective Apparel

The diagram below gives an overview of the functional blocks of the LCEVB

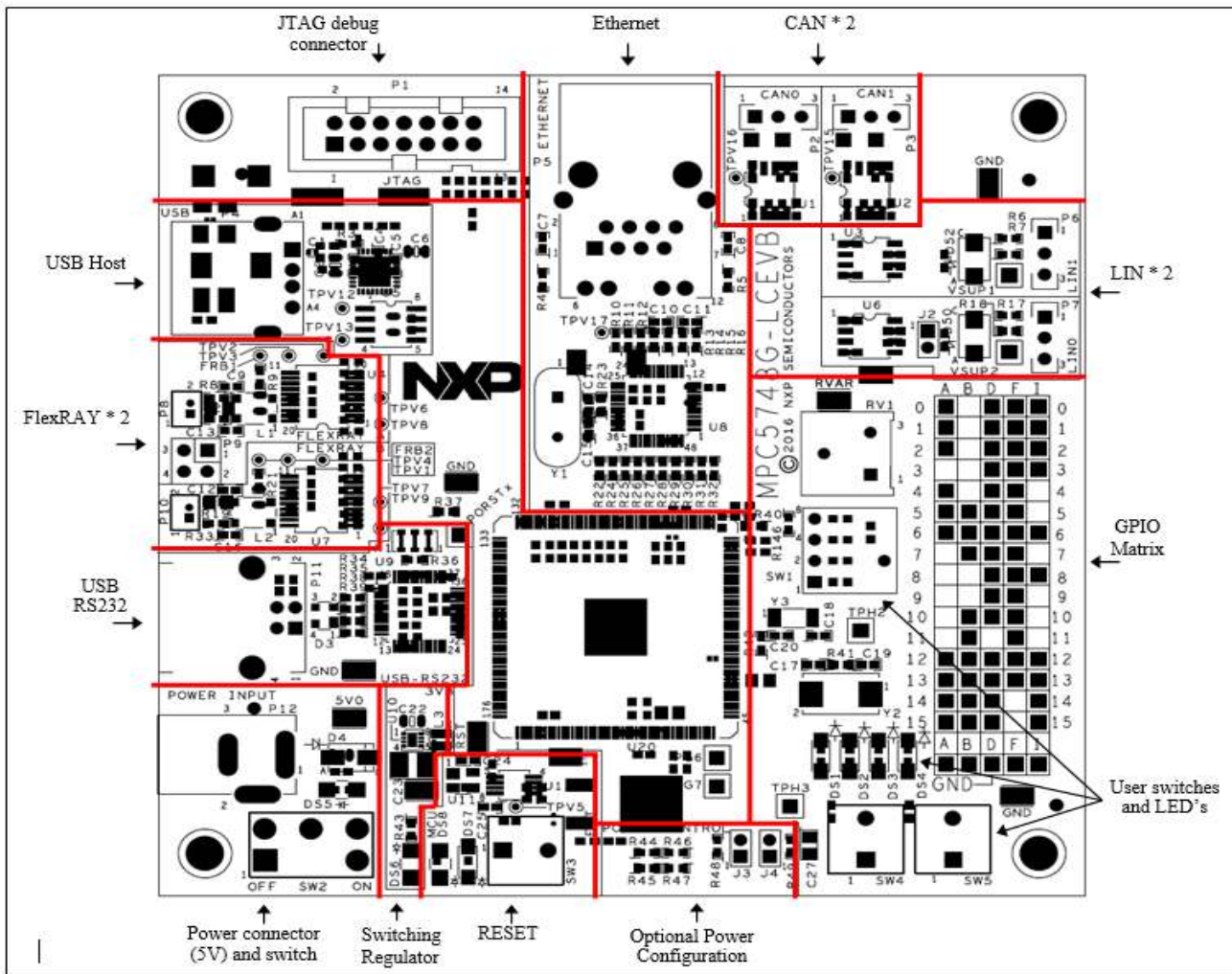


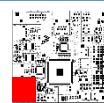
Figure 2. EVB Functional Blocks

## 4. Initial Setup

This section details the power, reset, clocks, and debug configuration which is the minimum configuration needed in order to power ON the LCEVB.

### 4.1. Power Supply Configuration

*The Power supply section is located in the bottom left corner of the LCEVB*



The LCEVB requires an external power supply voltage of 5 V DC, minimum 1 A. There is a single 3.3 V switching regulator on the LCEVB providing MCU and peripheral power.

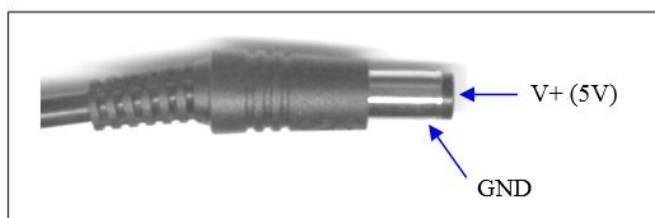
#### CAUTION

**Connecting a power supply with a voltage greater than 5 V will result in irrecoverable board damage. Check the power supply voltage before connecting the plug to the LCEVB.**

#### 4.1.1. Power Input Connector

Power is supplied to the LCEVB via a 2.1 mm connector from the wall-plug mains adapter as shown below. Note – if a replacement or alternative adapter is used, care must be taken to ensure the 2.1 mm plug uses the correct polarisation as shown below:

**Figure 3. 2.1 mm Power Connector**



#### 4.1.2. Power Switch

Slide switch SW2 can be used to isolate the power supply input from the EVB voltage regulators if required.

- Moving the slide switch to the right (away from the power connector) will turn the EVB ON.
- Moving the slide switch to the left (towards the power connector) will turn the EVB OFF.

### 4.1.3. Power Status LED

When power is applied to the LCEVB, two green LED's adjacent to the regulator and power connector show the presence of the supply voltages as follows:

- LED DS5 – Indicates that the 5.0 V supply voltage is present
- LED DS6 – Indicates that the 3.3 V switching regulator is functioning

If no LED's are illuminated when power is supplied to the LCEVB and the power switch is in the “ON” position, the power adapter may be faulty or there may be a fault with the LCEVB. If only one LED is illuminated there may be a short in that power supply rail – check there is nothing shorting on the EVB. If you continue to have problems, contact NXP for support.

#### CAUTION

In the event of a short on the regulator output (in which case one of the LED's would be off or dimly illuminated), the regulator and/or the shorted component will likely be hot.

### 4.1.4. MCU and Peripheral Voltage Configuration

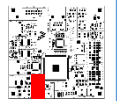
The following MCU supply rails are connected to the 3.3 V switching regulator:

- VDD\_HV\_ADC0
- VDD\_HV\_ADC1
- VDD\_HV\_ADC1\_REF
- VDD\_HV\_A
- VDD\_HV\_B
- VDD\_HV\_FLTA
- External Ballast Transistor Supply

Similarly all of the peripheral interfaces (or the I/O power in the peripheral interface) are supplied from 3.3 V as is the reset circuitry and the voltage sense wire on the JTAG connector.

## 4.2. Reset Control (SW3)

*The reset circuitry is located in the bottom left quarter of the LCEVB next to the power switch*



The MCU has a single bi-directional open drain Reset pin. Rather than connect multiple devices to the reset pin directly, a reset-in and reset-out buffering scheme has been implemented on the LCEVB as shown in [Figure 4](#). The reset “in” from the reset switch (SW3) and the debug connectors are logically OR'd together using an AND gate and then connected to the buffer to provide an open-drain output.

The “reset-out” circuitry provides a buffered reset signal that can be used to drive any circuitry requiring a reset control from the MCU.



This scheme is not required if it is guaranteed that anything driving the reset pin has an open drain drive and that there is no significant output load on the MCU reset pin.

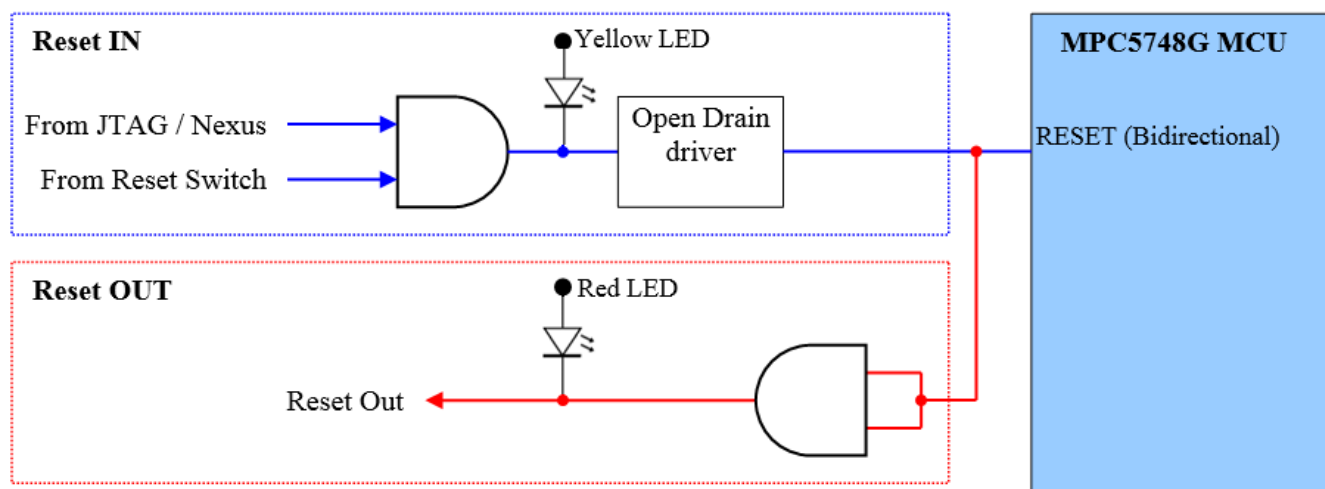


Figure 4. EVB Reset Control

#### 4.2.1. Reset LEDs

As can be seen above, there are two reset LED's that can be used to identify the source / cause of a reset: RED LED DS8 (titled "MCU") will illuminate if:

- The MCU issues a reset (in this condition ONLY this LED will be illuminated and LED DS1 will be off)
- There is a target reset (ie from the reset switch or from the debugger in which case LED DS1 will be ON)

YELLOW LED DS7 (titled "EXT") will illuminate when an external hardware device issues a reset to the MCU:

- The reset switch is pressed
- There is a reset being driven from one of the debug connectors

Table 2. Reset LED Decoding

LED DS7 (Yellow)	LED DS8 (Red)	Description
OFF	OFF	No Reset being issued from MCU or external logic
OFF	ON	MCU has issued a reset
ON	OFF	External reset issued from switch or debug BUT not being issued to MCU (check R137 has not been removed)
ON	ON	External reset issued from reset switch or debug and has been issued to MCU.

## 4.3. MCU Clock Configuration

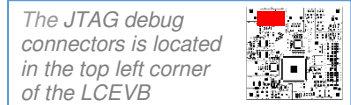
There is an external 40MHz crystal connected to the MCU Fast External Oscillator (FXOSC) pins EXTAL and XTAL.

There is also a 32.768 crystal connected to the MCU Slow External Oscillator (SXOSC) pins OSC32K\_EXTAL and OSC32K\_XTAL. This can be used for accurate time keeping.

There are 2 pads PG6 and PG7 (located just below the MCU) on the LCEVB to facilitate measurement of the CLKOUT1 and CLKOUT0 signals.

Note – there is no external clock input on the LCEVB

## 4.4. Debug Connector (P1)



The LCEVB has a single 14-pin keyed JTAG connector for connection to an external debugger.

Before attaching or removing the debug cable from the LCEVB remove power from the EVB to prevent damage to the LCEVB or debug hardware.

### 4.4.1. Debug Connector Pinout

The following tables list the pinout for the JTAG connector used on the LCEVB

**Table 3. 14-Pin JTAG Debug Connector Pinout**

Pin No	Function	Connection	Pin No	Function	Connection
1	TDI	PC0	2	GND	GND
3	TDO	PC1	4	GND	GND
5	TCLK	PH9	6	GND	GND
7	EVTI	PL8	8	N/C	---
9	RESET	JTAG-RSTx	10	TMS	PH10
11	VREF	PER_HVA	12	GND	GND
13	RDY	---	14	JCOMP	10K Pulldown

TDI, TDO and TMS have 10K pullup resistors on the LCEVB. TCLK has a 10K pulldown (R147) to facilitate STANDBY exit without any additional code (at the sacrifice of slightly higher STANDBY current), however this can be changed to a pullup if required by removing R147 and fitting the resistor on R56.

Table 4. JTAG Pins Pull State (from MPC5748G Reference Manual)

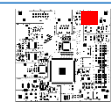
TERMINAL TYPE <sup>1</sup>	POWERUP pad state <sup>2</sup>	RESET pad state	DEFAULT pad state <sup>3</sup>
RESET	strong pull-down	strong pull-down	weak pull-up
PORST <sup>4</sup>	Weak pull down	Weak pull up	weak pull-up
GPIO	high impedance	high impedance	high impedance
ANALOG	high impedance	high impedance	high impedance
EOUT0, EOUT1	high impedance	high impedance	high impedance
TCK	high impedance	weak pull-up	weak pull-up
TMS	high impedance	weak pull-up	weak pull-up
TDI	high impedance	weak pull-up	weak pull-up
TDO	high impedance	high impedance	high impedance

## 5. Communications & Memory Interfaces:

This section details the communication interface and storage peripherals that are implemented on the LCEVB.

### 5.1. CAN Interfaces (P2, P3)

*The CAN circuitry is located on the top right edge of the LCEVB*



The LCEVB incorporates two identical CAN interface circuits connected to MCU CAN0 and CAN1 using MC33901 transceivers. Both transceivers are configured for high speed operation by pulling pin 8 to GND via a 4.7 KOhm resistor. There are test points to allow the Select pin to be driven high if desired. The MC33901 is pin compatible with other CAN transceivers supporting full CAN FD data rates.

For flexibility, the CAN transceiver I/O is connected to a 0.1" header (P2 for CAN0 / P3 for CAN1) rather than using non-standard DB9 connectors. The pinout of these headers is shown below.

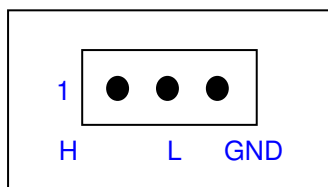
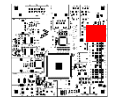


Figure 5. CAN Physical Interface Connectors

## 5.2. LIN Interfaces (P6, P7)

The LIN Physical interface circuits are located on the right edge of the LCEVB



The LCEVB incorporates two LIN transceiver circuits connected to MCU LIN0 and LIN1, using an NXP MC33662 transceiver. The MPC5748G LIN0 supports both master and slave modes whereas LIN1 only supports master mode.

On the LCEVB, the LIN0 transceiver is configured as slave mode by default. Master mode operation is possible by either populating a zero ohm resistor (R143) or by fitting a jumper header (J2) – see the schematics for details. The LIN0 transceiver is hard wired for master mode.

To save on board space and cost, both LIN transceivers are connected to 0.1” pitch 3x1 headers as shown below rather than the usual LIN Molex header.

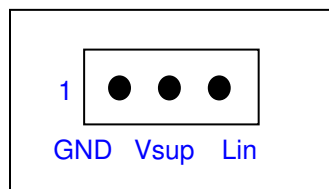
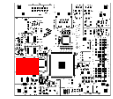


Figure 6. LIN Physical Interface Connector

*Note that in order for the LIN transceiver to function, external 12v must be supplied via pin 2 of the connector*

## 5.3. USB RS232 Serial Interface (P11)

The USB RS232 interface is on the left hand edge of the board (USB Type B)

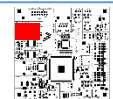


The LCEVB incorporates a USB RS232 serial interface providing RS232 connectivity via a direct USB connection between the PC and the EVB. The circuit contains an FTDI FT232D USB to Serial interface which should automatically install the drivers for two additional COM ports on your PC. Note that only one of these ports is used so you will need to try both (usually the higher numbered COM port is the active one). For more information on the USB drivers and general fault finding, consult the FTDI website at <http://www.ftdichip.com/>

The MCU LIN2 signals are routed to the FTDI transceiver (UART TX and RX). No handshaking signals are implemented and no board configuration is required.

## 5.4. USB HOST Interface (P4)

The USB Host interface is on the top left corner of the LCEVB on the left



The LCEVB includes a Type A (Host) USB interface, routed to a USB type A female connector. The USB circuit contains a USB83340 transceiver with a MIC2026-1YM USB power switch. There is no hardware user configuration required to use the USB circuit.

## 5.5. Ethernet Interface (P5)

*The Ethernet interface is mid-way along the top edge of the LCEVB*



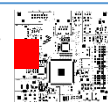
The EVB incorporates a single DP83848c Ethernet transceiver with the circuitry configured for MII mode. The transceiver is connected to a pulse J1011F21PNL RJ45 connector which includes a built-in isolation transformer. There is no hardware configuration needed.

If you require RMII mode or access to both Ethernet ports on the MPC5748G, please purchase the MPC5748G customer EVB and appropriate daughter cards.

Note that the MCU Ethernet signals are all in the VDD\_HV\_B domain. The Ethernet PHY will only function with 3.3 V I/O so if you have made any modifications to the EVB power domain configuration (via the zero ohm resistors), you need to ensure the VDD\_HV\_B domain is at 3.3 V before attempting to use the Ethernet module. If VDD\_HV\_B is set to 5 V, the signals routed to the Ethernet PHY (see the EVB schematics) must be left as tristate to prevent damage to the transceiver.

## 5.6. FlexRay (P8, P9, P10)

*The FlexRay interfaces are midway down the left hand edge of the LCEVB*



The LCEVB incorporates two FlexRay TJA1080TS/N interfaces connected to MCU FlexRay channels A and B and routed to two Molex 1.25 mm pitch PicoBlade shrouded headers (standard on many NXP EVB's). There is no hardware configuration required to use FlexRay.

Note that the LCEVB is supplied with a 40 MHz crystal by default. If FlexRay is configured to use the external clock source, then the crystal should be left at 40 MHz.

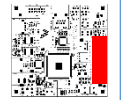


## 6. User Interface (I/O)

This section details the user I/O available on the LCEVB and includes the GPIO matrix, switches, LED's and the ADC variable resistor.

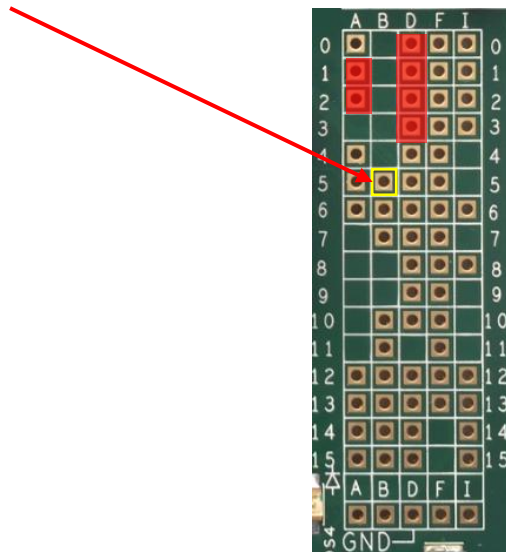
### 6.1. GPIO Matrix

*The GPIO matrix is on the right hand edge of the LCEVB*



A sub-set of available GPIO pins (available pins being those not already routed to LCEVB peripherals) are available at the GPIO matrix as detailed below. The matrix provides an easy to follow, intuitive, space saving grid of 0.1" header through-hole pads. Users can solder wires, fit headers or simply insert a scope probe into the respective pad.

To use the matrix, simply read the port letter from the top or bottom row of text then the pad number from the columns on the left or right of the matrix. For example, the 1<sup>st</sup> pad available on Port B is PB5 as outlined below.



**Figure 7. GPIO Matrix**

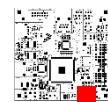
If a pad is populated in the matrix, it means this is available for exclusive use as GPIO. The exception to this are the port pins detailed below which are also shared with switches or user LED's (shaded red in the matrix diagram above).

- PD0, PD1, PD2, PD3 – HEX Encoder Switch
- PA1, PA2 – User pushbutton Switches

If you require access to all of the available GPIO pads, the customer EVB and daughtercard provides this additional functionality.

## 6.2. User Switches (SW4, SW5)

The user pushbutton switches are in the bottom right corner of the LCEVB



There are two active high (pulled low, driven to 3.3 V) pushbutton switches on the LCEVB connected directly to MCU GPIO ports. No configuration is required to use the switches.

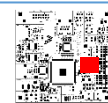
SW4 is connected to port PA1 (which is also the NMI pin) and SW5 is connected to port PA2

### NOTE

The MCU ports used on the user pushbutton switches are also routed to the GPIO matrix.

## 6.3. Hex Encoded Switch (SW1)

The hex encoder switch is located to the left of the GPIO Matrix



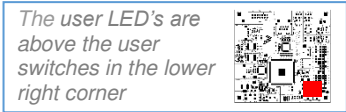
There is a single hex encoded 16 position rotary switch on the LCEVB. This outputs a binary encoded hex value (active high) on four MCU ports (Port D[0..3]).

Table 5. Hex Encoder Switch (SW2)

Position	HEX_SW4 (PD3)	HEX_SW3 (PD2)	HEX_SW2 (PD1)	HEX_SW1 (PD0)
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

Note that POSN 0 will ensure that no voltage is applied to the pads. This allows the pads to be used as normal GPIO (with 10K pulldown) and accessed at the respective pads on the GPIO matrix area.

## 6.4. User LED's (DS1, DS2, DS3, DS4)

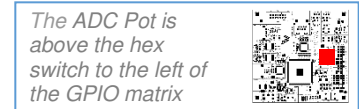


There are four **active low** user LED's, DS1 to DS4, connected directly to 4 MCU ports (PG[2..5]) as shown below. No configuration is required to use the LED's.

**Table 6. Use LED's (DS1, DS2, DS3 and DS4)**

User LED	MCU Pin
DS1	PG2
DS2	PG3
DS3	PG4
DS4	PG5

## 6.5. ADC Input Potentiometer (RVAR, RV1)



There is a small variable resistor RV1 on the LCEVB which routes a voltage between 0v and 3.3 V to MCU pin PB4. This is useful for quick ADC testing. Test point RVAR can be used to probe the voltage with a voltmeter.

Note that this circuit provides a very rough way to evaluate the ADC. There is a small current limiting series resistor network to limit the injection current to around 4.4 mA.

## 7. MCU Port Pin LCEVB Functions

The table below shows what each MCU pin is used for on the LCEVB.

**Table 7. LCEVB 176QFP Port Pin Functions**

No	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H
0	GPIO	CAN0	JTAG	GPIO <sup>3</sup>	---	GPIO	Ethernet	Ethernet
1	GPIO <sup>2</sup>	CAN0	JTAG	GPIO <sup>3</sup>	---	GPIO	Ethernet	Ethernet
2	GPIO <sup>2</sup>	LIN0	USB1	GPIO <sup>3</sup>	FlexRay A	GPIO	GPIO <sup>4</sup>	Ethernet
3	Ethernet	LIN0	USB1	GPIO <sup>3</sup>	FlexRay A	GPIO	GPIO <sup>4</sup>	---
4	GPIO	ADC Pot	FlexRay B	GPIO	FlexRay B	GPIO	GPIO <sup>4</sup>	---
5	GPIO	GPIO	FlexRay A	GPIO	FlexRay B	GPIO	GPIO <sup>4</sup>	---
6	GPIO	GPIO	LIN1	GPIO	---	GPIO	GPIO	---
7	Ethernet	GPIO	LIN1	GPIO	---	GPIO	GPIO	---
8	Ethernet	EXTAL32	RS232	GPIO	---	GPIO	---	---
9	Ethernet	XTAL32	RS232	GPIO	---	GPIO	---	JTAG
10	Ethernet	SAI Audio	CAN1	GPIO	---	GPIO	USB1	JTAG
11	Ethernet	GPIO	CAN1	---	---	GPIO	USB1	USB1
12	GPIO	GPIO	FlexRay	GPIO	Ethernet	GPIO	Ethernet	USB1
13	GPIO	GPIO	FlexRay	GPIO	Ethernet	GPIO	Ethernet	---
14	GPIO	GPIO	FlexRay	GPIO	USB1	Ethernet	USB1	---
15	GPIO	GPIO	FlexRay	GPIO	USB1	Ethernet	USB1	---

No	Port I	Port J
0	GPIO	---
1	GPIO	---
2	GPIO	---
3	GPIO	---
4	USB1	---
5	USB1	
6	GPIO	
7	USB1	
8	GPIO	
9		
10		
11	Ethernet	
12	GPIO	
13	GPIO	
14	GPIO	
15	GPIO	

Key:	
---	Pin not bonded out on 176QFP package
---	Pin not accessible on LCEVB

<sup>2</sup> Shared with user switches

<sup>3</sup> Shared with Hex Encoder Switch

<sup>4</sup> Shared with user LED's

## 8. Appendix

The MPC5748G LCEVB schematics, Rev B are shown below.



# MPC5748G Low Cost Evaluation Board (MPC5748G-LCEVB)

## Table Of Contents:

Power - Main input and 3.3V regulator	Sheet 2
Power - MCU Power	Sheet 3
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Reset and JTAG	Sheet 5
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MCU GPIO 1	Sheet 7
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Comms1 - CAN and LIN	Sheet 9
Comms 2 - FTDI RS232 Interface	Sheet 10
Comms 3 - USB Host Interface (device footprints only)	Sheet 11
Comms 4 - Ethernet (MII Mode)	Sheet 12
Comms 5 - FlexRay	Sheet 13
User - Switches, LED's and Potentiometer	Sheet 14
User - GPIO Pin Matrix	Sheet 15

## Revision Information

Rev	Date	Designer	Comments
x1	14 Apr 2015	Alasdair Robertson	Start of capture, Working version (256BGA)
x2	08 May 2015	Alasdair Robertson	Changed to 176 QFP Package and changed peripherhal Matrix
x3	18 May 2015	Alasdair Robertson	Changes required for initial placement
x4	19 May 2015	Alasdair Robertson	Tidy Up, Replaced some "hard to source" components
x5	26 May 2015	Alasdair Robertson	Re-number and Back Annotated from Layout
x6	27 May 2015	Alasdair Robertson	Correction to GND on 3v3 Regulator circuit
x7	29 May 2015	Alasdair Robertson	Correction to CAN Test points
x8	31 May 2015	Alasdair Robertson	Few refdes changes after layout tweaks
x9	01 Jun 2015	Alasdair Robertson	Correction to user LED Refdes after re-number
x10	01 Jun 2015	Alasdair Robertson	DNP Jumpers. 0 Ohm resistors added across LIN jumpers
A	11 Jun 2015	Andrew MacDonald	Prototype Manufacture Release
AX1	29 Sep 2015	Alasdair Robertson	Prodn Build changes (LIN0 default to Slave, LIN1 Master only) PN Changed to MPC5748G-LCEVB
AX2	26 Oct 2015	Alasdair Robertson	Change to JTAG Pulls to meet latest RM Spec
AX3	29 Oct 2015	Alasdair Robertson	Changed RV1 current limit resistor. SW4 / SW5 refdes swap
AX4	09 Dec 2015	Alasdair Robertson	Pull DOWN on TCLK to mitigate against STANDBY exit issue.
AX5	20 Jan 2016	Alasdair Robertson	Updated NXP Logos
B	12 Feb 2016	Alasdair Robertson	Updated NXP Logos

## Caution:

These schematics are provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and NXP does not assume any liability for such a hardware design.

## Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

**Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.**

User notes are given throughout the schematics.

*Specific PCB LAYOUT notes are detailed in ITALICS*

3 Different test points used in design:

TPVx - Through Hole Pad small


TPHx - Through Hole Pad Large (for standard 0.1" header).  
Also used on IO Matrix (IOMx)

TPx - Surface Mount Wire Loop

 TPV?

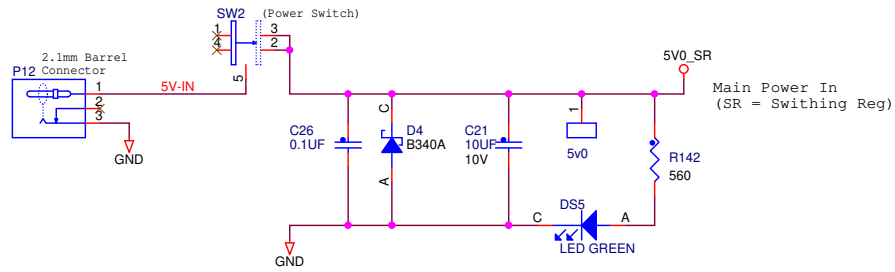
 TPH5

 TP?

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This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
Designer: A. Robertson	Drawing Title: <b>MPC5748G-LCEVB</b>		
Drawn by: A. Robertson	Page Title: <b>Index and Title Page</b>		
Approved: A. Robertson	Size B	Document Number SCH-27897 PDF: SPF-27897	Rev B
Date:	Friday, February 12, 2016	Sheet	1 of 15

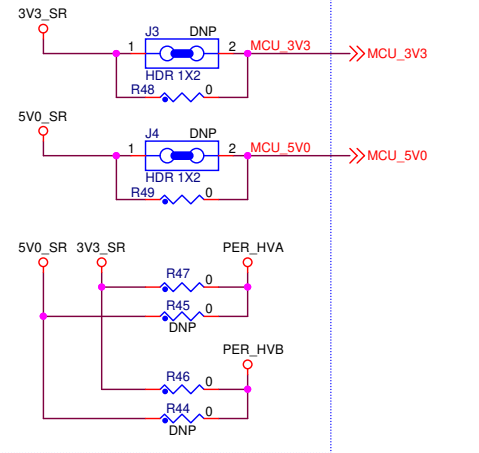
# Power Input and Linear Voltage Regulators

## Power Supply Input

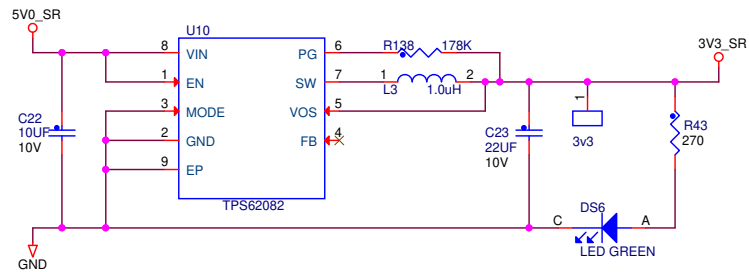


## Power Control

Jumpers can be fitted to facilitate power measurements

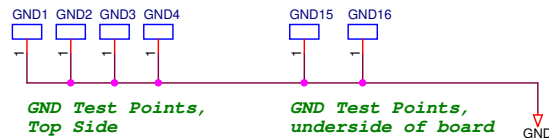


## 3.3v Switching Regulator



Inoput Voltage 5V, Output 3.3V at 700mA. Ripple 1.4mV, Approx 90% efficient

## Test and reference points



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<b>Power Input and Linear Voltage Regulators</b>			
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# Calypso MCU Power Connections

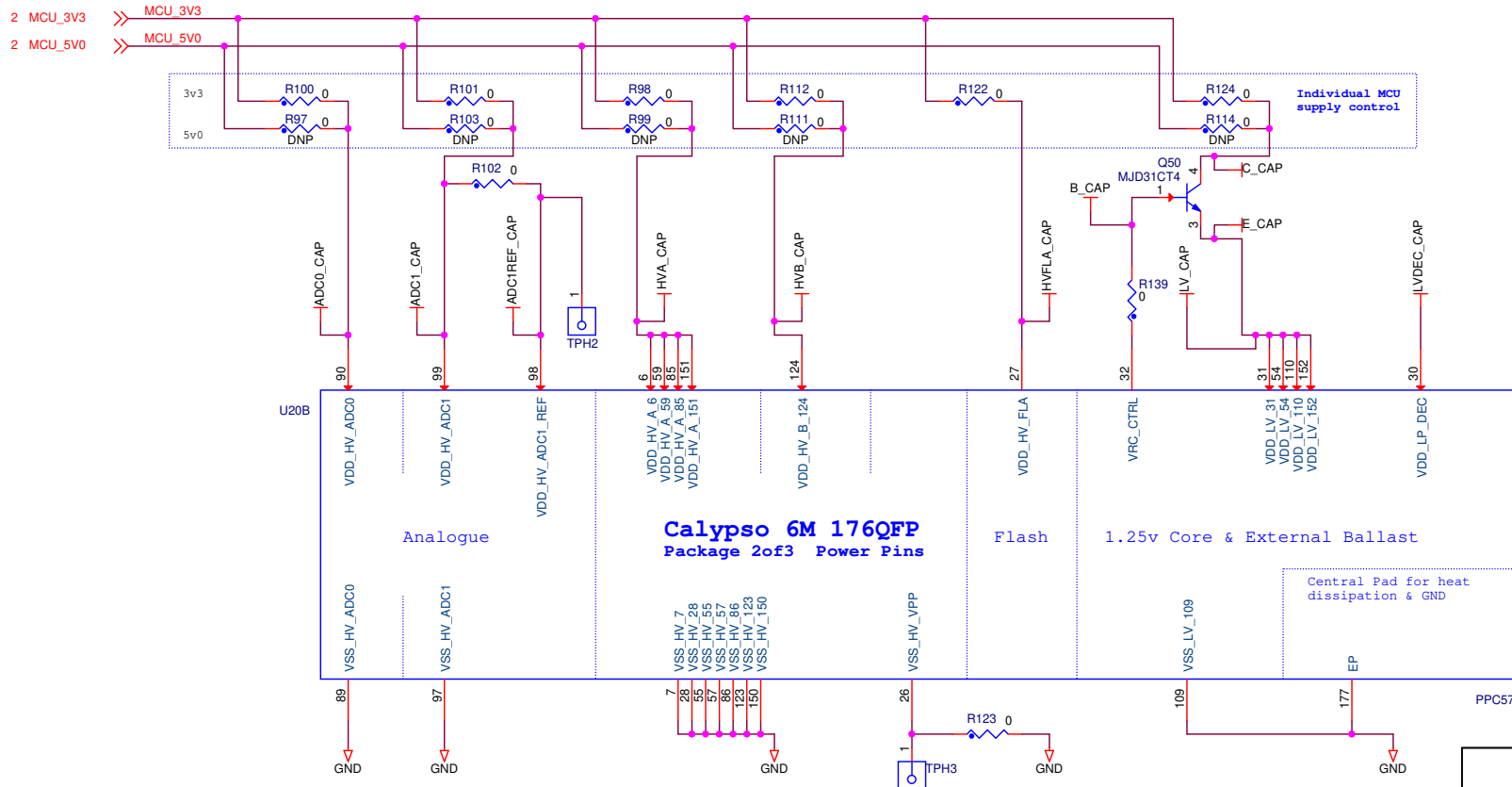
## Power Supply Constraints:

- If VDD\_HV\_A is driven from 3.3V, VDD\_HV\_FL A must also be supplied from 3.3V
- If VDD\_HV\_A is driven from 5V, the VDD\_HV\_FL A pin must be disconnected from 3.3V
- Don't attempt to over drive an analogue pad to 5V when the digital VDD\_HV\_x supply is set to 3.3V. This will trigger the ESD protection on that pad. For example if VDD\_HV\_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD\_HV\_A domain

## Default Configuration:

- ALL MCU supply voltages are set to 3.3V (ADC0, ADC1, VDD\_HV\_A, VDD\_HV\_B, VDD\_HV\_C, VBallast)
- VDD\_HV\_FL A = External 3.3V supplied (jumper fitted)


The analogue pins can only be driven to the same voltage as the VDD\_HV\_x domain they are situated in (ie max 3.3V) so makes sense for the analogue supply and reference to be 3.3V



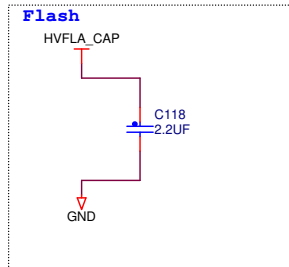
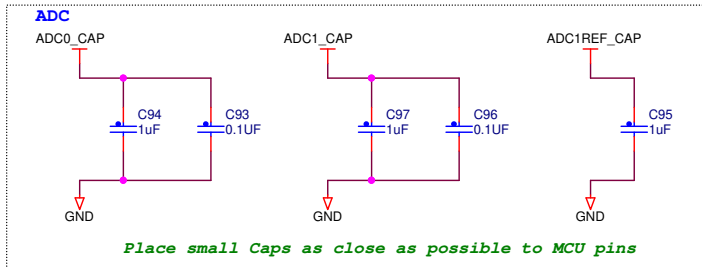
PPC5748GSK0MKU6

## Notes on signal Grounds:

- The scheme shown has the analogue and digital grounds connected to the same plane
- This results in better ADC performance than using an analogue ground plane with single point (or ferrite) to digital ground plane.

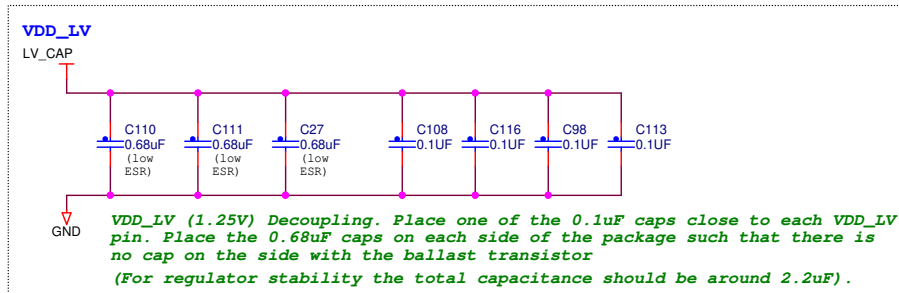
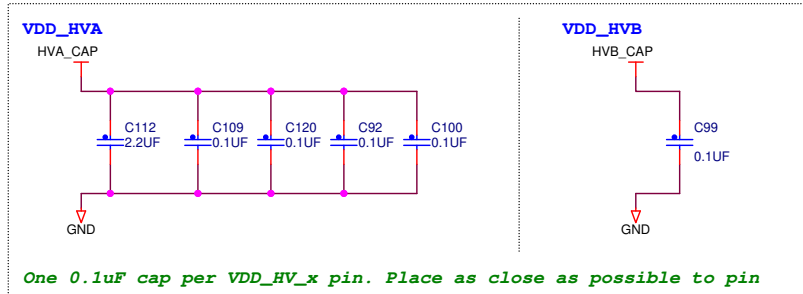
		Automotive Microcontroller Applications	
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Drawing Title: <b>MPC5748G-LCEVB</b>			
Page Title: <b>Calypso MCU Power</b>			
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# Calypso MCU Decoupling and bulk storage

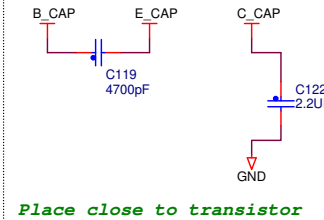


**Capacitor Types:**

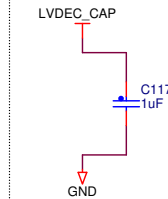
- 4700pF - Ceramic X7R, 50V 10% 0402
- 0.1uF - Ceramic X7R, 16V 10% 0402 (Kemet C0402C104K4RAC)
- 0.68uF - Ceramic X7R, 16V 10% 0805 (Murata GCM219R71C684KA37)
- 1uF - Ceramic X7R, 10V 10% 0603 Low ESR (Taiyo Yuden LMK107B7105KA-T)
- 2.2uF - Ceramic X7R, 10V 10% 0603 Low ESR (Taiyo Yuden LMK107B7225KA-TR)



**Ballast Transistor**



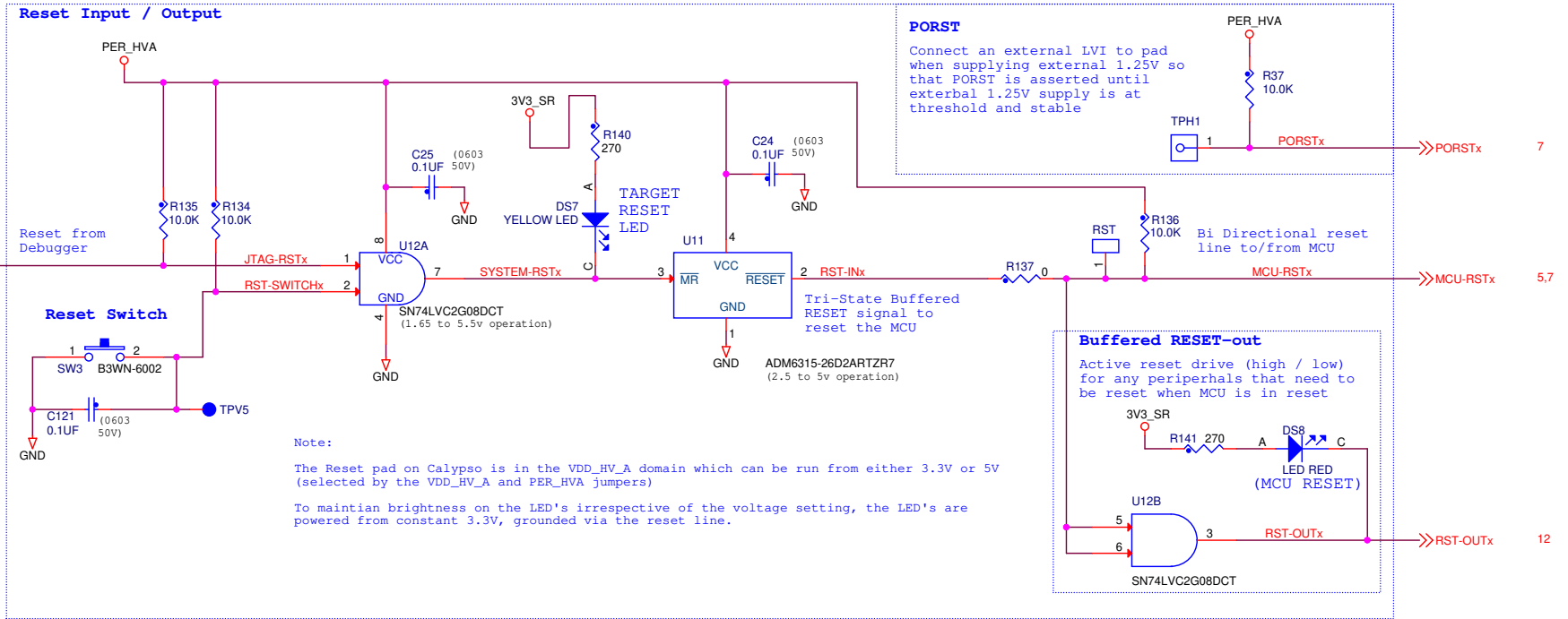
**LP Internal Reg Cap**



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Page Title: <b>Calypso MCU Decoupling</b>			
Size B	Document Number	SCH-27899 PDF: SPF-27899	Rev B
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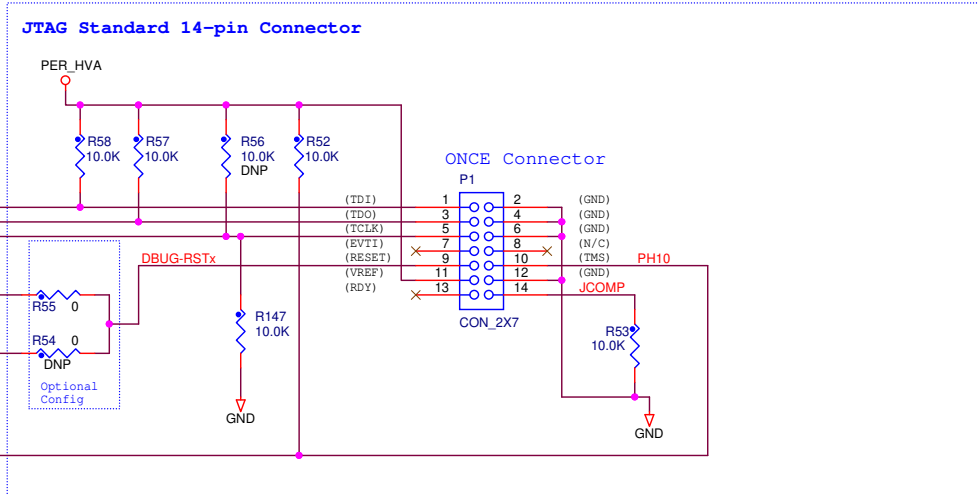
# Reset and External Clock In

Reset is in the VDD\_HVA domain.



**PORST**

Connect an external LVI to pad when supplying external 1.25V so that PORST is asserted until external 1.25V supply is at threshold and stable



**Table 13-3. Functional terminal state during power-up and reset**

TERMINAL TYPE <sup>1</sup>	POWERUP pad state <sup>2</sup>	RESET pad state	DEFAULT pad state <sup>3</sup>	Comments
RESET	strong pull-down	strong pull-down	weak pull-up	functional reset pad
PORST <sup>4</sup>	Weak pull down	Weak pull up	weak pull-up	power on reset pad
GPIO	high impedance	high impedance	high impedance	by default, but configurable for STANDBY exit
ANALOG	high impedance	high impedance	high impedance	-
EOUT0, EOUT1	high impedance	high impedance	high impedance	-
TCK	high impedance	weak pull-up	weak pull-up	-
TMS	high impedance	weak pull-up	weak pull-up	-
TDI	high impedance	weak pull-up	weak pull-up	-
TDO	high impedance	high impedance	high impedance	-
TCK_ALT	high impedance	weak pull-up	weak pull-up	-
TMS_ALT	high impedance	weak pull-up	weak pull-up	-
TDI_ALT	high impedance	weak pull-up	weak pull-up	-
TDO_ALT	high impedance	high impedance	high impedance	-

*Note TCLK needs to be pulled down to allow exit from STANDBY in some corner cases*

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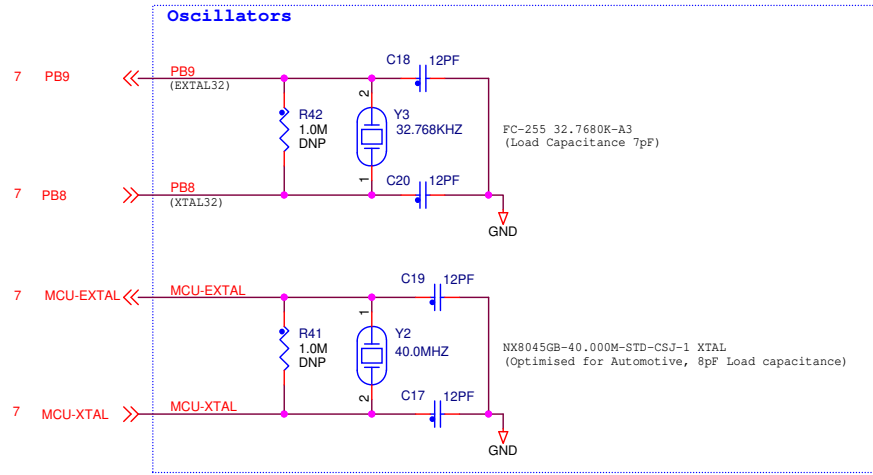
Drawing Title: **MPC5748G-LCEVB**

Page Title: **Reset Circuitry & External Clock In**

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# Clocks



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Page Title: **Clocks**

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# Calypso GPIO 1 of 2

U20A

## Calypso 176QFP Package 1of3 GPIO Pins1

Key to text colours:  
 Purple - Comms Physical Interfaces  
 Orange - Other Peripherals and I/O  
 Blue - Debug (JTAG & Nerves)  
 Black - Clock, Reset and Control  
 RED - I/O Matrix and other functions (eg LED)  
 Green - I/O Matrix (dedicated)

PA 12..15 has SPI

PD has ADC0 and ADC1

15	PA0	(GPIO)	PA0	24	
(WKPU2 / NMIO)	14,15	PA1	(SW1 & GPIO)**	PA1	19
(WKPU3)	14,15	PA2	(SW2 & GPIO)	PA2	17
	12	PA3	(MII_RXCLK)	PA3	114
	12	PA4	(GPIO)	PA4	51
	15	PA5	(GPIO)	PA5	146
	15	PA6	(GPIO)	PA6	147
	12	PA7	(MII_RXD2)	PA7	128
	12	PA8	(MII_RXD1)	PA8	129
	12	PA9	(MII_RXD0)	PA9	130
	12	PA10	(MII_CS)	PA10	131
	12	PA11	(MII_RXER)	PA11	132
	15	PA12	(GPIO)	PA12	53
	15	PA13	(GPIO)	PA13	52
	15	PA14	(GPIO)	PA14	50
	15	PA15	(GPIO)	PA15	48

(GPIO)	PA0	24
(SW1 & GPIO)**	PA1	19
(SW2 & GPIO)	PA2	17
(MII_RXCLK)	PA3	114
(GPIO)	PA4	51
(GPIO)	PA5	146
(GPIO)	PA6	147
(MII_RXD2)	PA7	128
(MII_RXD1)	PA8	129
(MII_RXD0)	PA9	130
(MII_CS)	PA10	131
(MII_RXER)	PA11	132
(GPIO)	PA12	53
(GPIO)	PA13	52
(GPIO)	PA14	50
(GPIO)	PA15	48

PA0	24
PA1	19
PA2	17
PA3	114
PA4	51
PA5	146
PA6	147
PA7	128
PA8	129
PA9	130
PA10	131
PA11	132
PA12	53
PA13	52
PA14	50
PA15	48

PE0	18
PE1	20
PE2	156 PE2 (FR_A_TX_EN)
PE3	157 PE3 (FR_A_RX)
PE4	160 PE4 (FR_B_TX)
PE5	161 PE5 (FR_B_RX)
PE6	167
PE7	168
PE8	21
PE9	22
PE10	25
PE11	133 PE12 (MII CRS)
PE12	127 PE13 (MII_RXD3)
PE13	136 PE14 (USB1_D2)
PE14	137 PE15 (USB1_D3)
PE15	

PE2	13
PE3	13
PE4	13
PE5	13
PE12	12
PE13	12
PE14	11
PE15	11

9	PB0	(CAN0_TX)	PB0	39
9	PB1	(CAN0_RX)	PB1	40
9	PB2	(LIN0_TX)	PB2	176
9	PB3	(LIN0_RX)	PB3	1
14	PB4	(ADC_P01)	PB4	88
15	PB5	(GPIO)	PB5	91
15	PB6	(GPIO)	PB6	92
15	PB7	(GPIO)	PB7	93
15	PB8	(XTAL32)	PB8	61
6	PB9	(EXTAL32)	PB9	60
15	PB10	(GPIO)	PB10	62
15	PB11	(GPIO)	PB11	96
15	PB12	(GPIO)	PB12	101
15	PB13	(GPIO)	PB13	103
15	PB14	(GPIO)	PB14	105
15	PB15	(GPIO)	PB15	107

(CAN0_TX)	PB0	39
(CAN0_RX)	PB1	40
(LIN0_TX)	PB2	176
(LIN0_RX)	PB3	1
(ADC_P01)	PB4	88
(GPIO)	PB5	91
(GPIO)	PB6	92
(GPIO)	PB7	93
(XTAL32)	PB8	61
(EXTAL32)	PB9	60
(GPIO)	PB10	62
(GPIO)	PB11	96
(GPIO)	PB12	101
(GPIO)	PB13	103
(GPIO)	PB14	105
(GPIO)	PB15	107

PB0	39
PB1	40
PB2	176
PB3	1
PB4	88
PB5	91
PB6	92
PB7	93
PB8	61
PB9	60
PB10	62
PB11	96
PB12	101
PB13	103
PB14	105
PB15	107

PF0	63 PF0 (GPIO)
PF1	64 PF1 (GPIO)
PF2	65 PF2 (GPIO)
PF3	66 PF3 (GPIO)
PF4	67 PF4 (GPIO)
PF5	68 PF5 (GPIO)
PF6	69 PF6 (GPIO)
PF7	70 PF7 (GPIO)
PF8	42 PF8 (GPIO)
PF9	41 PF9 (GPIO)
PF10	46 PF10 (GPIO)
PF11	47 PF11 (GPIO)
PF12	43 PF12 (GPIO)
PF13	49 PF13 (GPIO)
PF14	126 PF14 (RMII_MDIO)
PF15	125 PF15 (RMII_RXDV)

PF0	15
PF1	15
PF2	15
PF3	15
PF4	15
PF5	15
PF6	15
PF7	15
PF8	15
PF9	15
PF10	15
PF11	15
PF12	15
PF13	15
PF14	12
PF15	12

5	PC0	(TDI)	PC0	154
5	PC1	(TDO)	PC1	149
11	PC2	(USB1_CLK)	PC2	145
11	PC3	(USB1_DIR)	PC3	144
13	PC4	(FR_B_TX_EN)	PC4	159
13	PC5	(FR_A_TX)	PC5	158
9	PC6	(LIN1_TX)	PC6	44
9	PC7	(LIN1_RX)	PC7	45
10	PC8	(RS232_TX)	PC8	175
10	PC9	(RS232_RX)	PC9	2
9	PC10	(CAN1_TX)	PC10	36
9	PC11	(CAN1_RX)	PC11	35
13	PC12	(FR_DBG0)	PC12	173
13	PC13	(FR_DBG1)	PC13	174
13	PC14	(FR_DBG2)	PC14	3
13	PC15	(FR_DBG3)	PC15	4

(TDI)	PC0	154
(TDO)	PC1	149
(USB1_CLK)	PC2	145
(USB1_DIR)	PC3	144
(FR_B_TX_EN)	PC4	159
(FR_A_TX)	PC5	158
(LIN1_TX)	PC6	44
(LIN1_RX)	PC7	45
(RS232_TX)	PC8	175
(RS232_RX)	PC9	2
(CAN1_TX)	PC10	36
(CAN1_RX)	PC11	35
(FR_DBG0)	PC12	173
(FR_DBG1)	PC13	174
(FR_DBG2)	PC14	3
(FR_DBG3)	PC15	4

PC0	154
PC1	149
PC2	145
PC3	144
PC4	159
PC5	158
PC6	44
PC7	45
PC8	175
PC9	2
PC10	36
PC11	35
PC12	173
PC13	174
PC14	3
PC15	4

PG0	122 PG0 (RMII_MDC)
PG1	121 PG1 (RMII_TXCLK)
PG2	16 PG2 (LED1 & GPIO)
PG3	15 PG3 (LED2 & GPIO)
PG4	14 PG4 (LED3 & GPIO)
PG5	13 PG5 (LED4 & GPIO)
PG6	38 PG6 (CLKOUT1 GPIO)
PG7	37 PG7 (CLKOUT0 GPIO)
PG8	34
PG9	33
PG10	138 PG10 (USB1_D4)
PG11	139 PG11 (USB1_D5)
PG12	116 PG12 (MII_TXD2)
PG13	115 PG13 (MII_TXD3)
PG14	134 PG14 (USB1_D0)
PG15	135 PG15 (USB1_D1)

PG0	12
PG1	12
PG2	14 (eMIOS ELUC_12_H)
PG3	14 (eMIOS ELUC_13_H)
PG4	14 (eMIOS ELUC_14_H)
PG5	14
PG6	1
PG7	1
PG10	11
PG11	11
PG12	12
PG13	12
PG14	11
PG15	11

14,15	PD0	(HEX1 & GPIO)	PD0	77
14,15	PD1	(HEX2 & GPIO)	PD1	78
14,15	PD2	(HEX3 & GPIO)	PD2	79
14,15	PD3	(HEX4 & GPIO)	PD3	80
15	PD4	(GPIO)	PD4	81
15	PD5	(GPIO)	PD5	82
15	PD6	(GPIO)	PD6	83
15	PD7	(GPIO)	PD7	84
15	PD8	(GPIO)	PD8	87
15	PD9	(GPIO)	PD9	94
15	PD10	(GPIO)	PD10	95
15	PD12	(GPIO)	PD12	100
15	PD13	(GPIO)	PD13	102
15	PD14	(GPIO)	PD14	104
15	PD15	(GPIO)	PD15	106

(HEX1 & GPIO)	PD0	77
(HEX2 & GPIO)	PD1	78
(HEX3 & GPIO)	PD2	79
(HEX4 & GPIO)	PD3	80
(GPIO)	PD4	81
(GPIO)	PD5	82
(GPIO)	PD6	83
(GPIO)	PD7	84
(GPIO)	PD8	87
(GPIO)	PD9	94
(GPIO)	PD10	95
(GPIO)	PD12	100
(GPIO)	PD13	102
(GPIO)	PD14	104
(GPIO)	PD15	106


PD0	77
PD1	78
PD2	79
PD3	80
PD4	81
PD5	82
PD6	83
PD7	84
PD8	87
PD9	94
PD10	95
PD12	100
PD13	102
PD14	104
PD15	106

PH0	117 PH0 (RMII_TXD1)
PH1	118 PH1 (RMII_TXD0)
PH2	119 PH2 (RMII_TXEN)
PH3	120
PH4	162
PH5	163
PH6	164
PH7	165
PH8	166
PH9	155 PH9 (TCK)
PH10	148 PH10 (TMS)
PH11	140 PH11 (USB1_D6)
PH12	141 PH12 (USB1_D7)
PH13	9
PH14	10
PH15	8

PH0	12
PH1	12
PH2	12
PH9	5
PH10	5
PH11	11
PH12	11

5	MCU-RSTx	MCU-RSTx	29	RESET
5	PORSTx	PORSTx	153	PORST
6	MCU-XTAL	MCU-XTAL	56	XTAL
6	MCU-EXTAL	MCU-EXTAL	58	EXTAL

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Drawing Title: <b>MPC5748G-LCEVB</b>			
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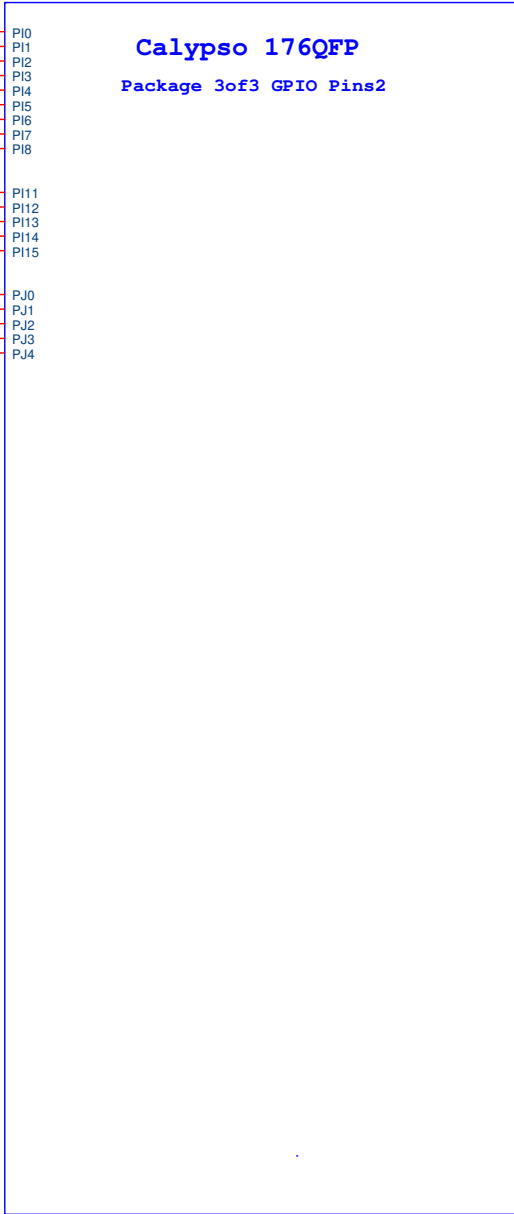
# Calypso GPIO 2 of 2

Key to text colours:  
 Purple - Comms Physical Interfaces  
 Orange - Other Peripherals and I/O  
 Blue - Debug (JTAG & Nexus)  
 Black - Clock, Reset and Control  
 RED - I/O Matrix and other functions (eg LED)  
 Green - I/O Matrix (dedicated)

15	PI0	<<<	(GPIO)	PI0	172	PI0
15	PI1	<<<	(GPIO)	PI1	171	PI1
15	PI2	<<<	(GPIO)	PI2	170	PI2
15	PI3	<<<	(GPIO)	PI3	169	PI2
11	PI4	<<<	(USB1_STF)	PI4	143	PI3
11	PI5	<<<	(USB1_NXT)	PI5	142	PI4
15	PI6	<<<	(GPIO)	PI6	11	PI5
11	PI7	<<<	(USB1_RST)	PI7	12	PI6
15	PI8	<<<		PI8	108	PI7
12	PI11	<<<	(ENET_RST)	PI11	111	PI8
15	PI12	<<<	(GPIO)	PI12	112	PI11
15	PI13	<<<	(GPIO)	PI13	113	PI12
15	PI14	<<<	(GPIO)	PI14	76	PI13
15	PI15	<<<	(GPIO)	PI15	75	PI14


<<<	74	PJ0
<<<	73	PJ1
<<<	72	PJ2
<<<	71	PJ3
<<<	5	PJ4

U20C



Calypso 176QFP  
 Package 3of3 GPIO Pins2

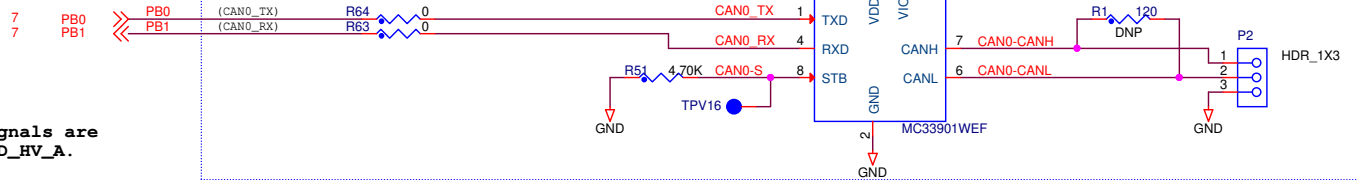
PPC5748GSK0MKU6

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# CAN & LIN Physical

## CAN0 Physical Interface

VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)  
 VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V  
 STB - High for Standby mode, pulled low for normal mode.

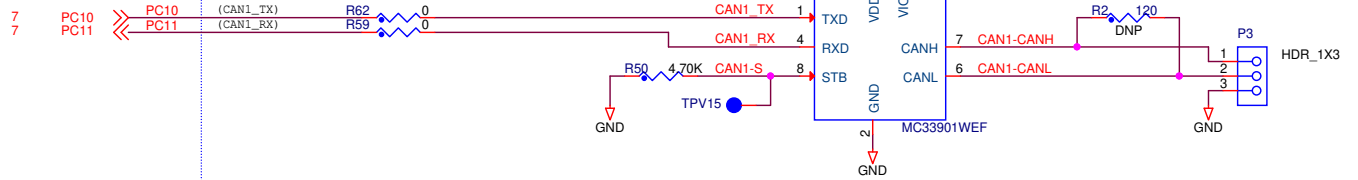


All CAN and LIN signals are in power domain VDD\_HV\_A.

All interfaces will work at 3.3V or 5.0V (PER\_HVA)

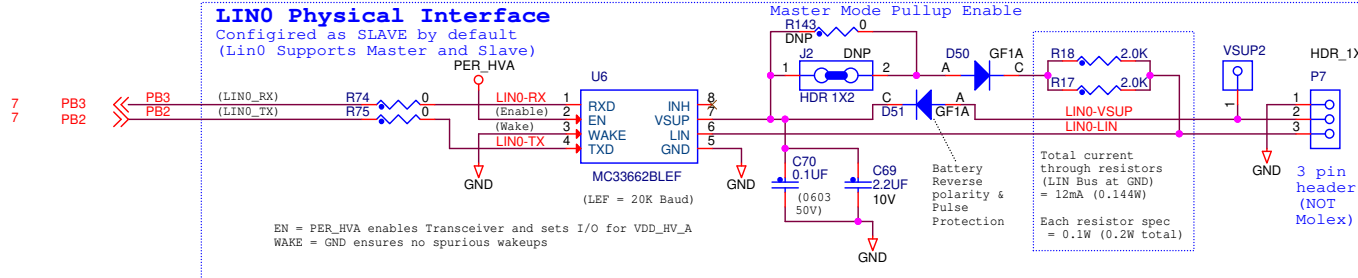
## CAN1 Physical Interface

VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)  
 VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V  
 STB - High for Standby mode, pulled low for normal mode.



## LIN0 Physical Interface

Configured as SLAVE by default  
 (Lin0 Supports Master and Slave)



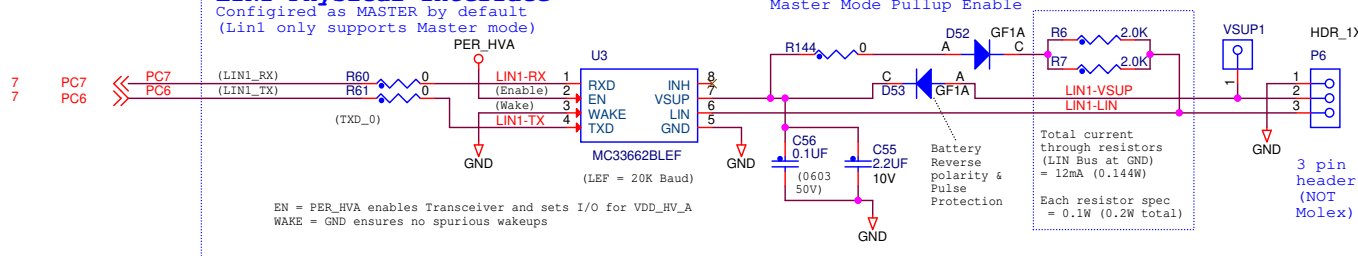
MC33662LEF LIN transceiver is newer version of 33661 offering:

- Full LIN compliance (33661 no longer compliant)
- Improved ESD protection on LIN pin up to 15KV
- Improved ESD on Wake and VSUP Pins
- Other EMC and performance improvements

See freescale.com for more details

## LIN1 Physical Interface

Configured as MASTER by default  
 (Lin1 only supports Master mode)



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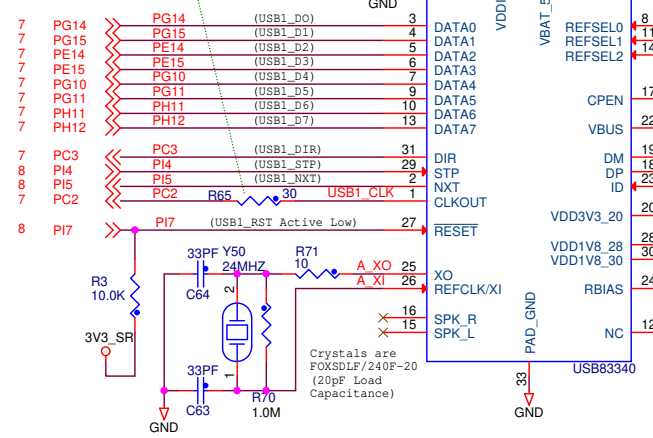


# USB (Type A Host and Type AB OTG)

USB Signals are in power domain VDD\_HV\_A

The USB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD\_HVA is set to 5V, USB MCU pads must be left as tri-state with no pullups.

(Layout Note: Place Series Termination resistor close to USB IC)

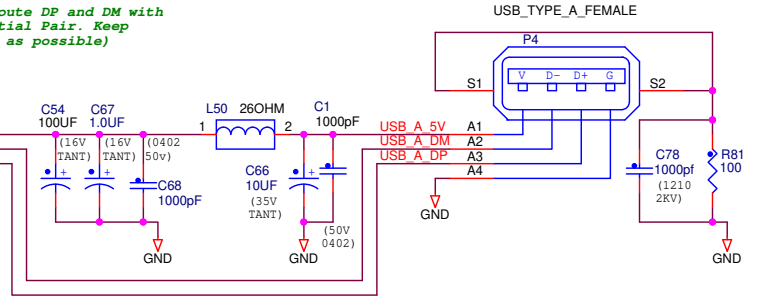


General Layout Note. Recommendation is to keep all tracks between MCU and USB PHI less than 3" See additional SMSC Layout guidelines PDF to the right

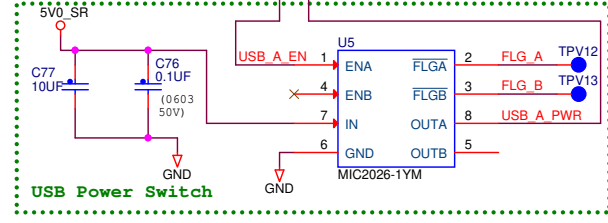


USB Host, Type A (Available on all packages)

(Layout Note: Route DP and DM with 90 Ohm Differential Pair. Keep tracks as short as possible)



Layout Note: Place caps & resistor as close to device as possible



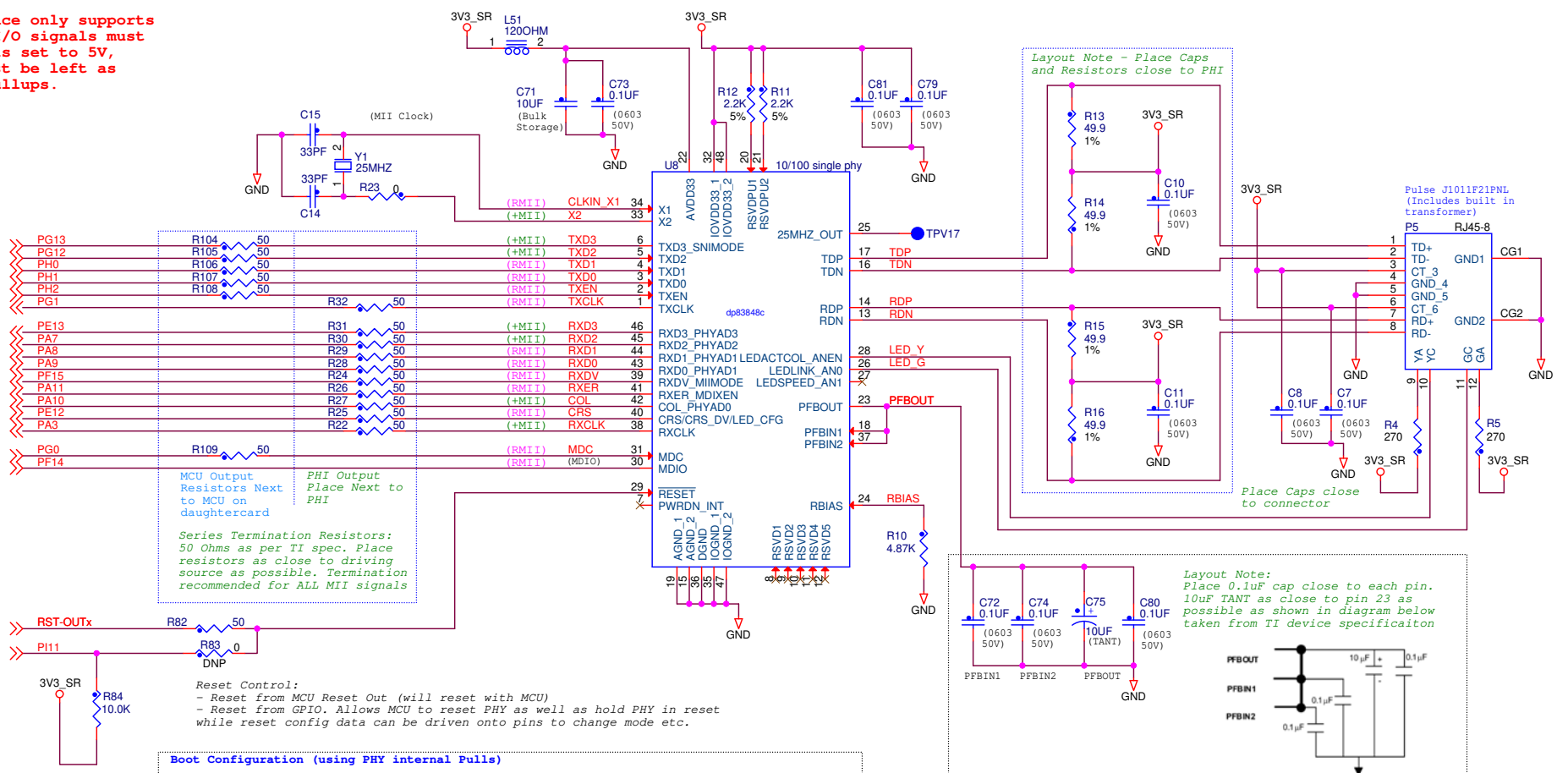
		Automotive Microcontroller Applications	
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Drawing Title: <b>MPC5748G-LCEVB</b>			
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# Ethernet (Configured for MII Mode)

All Ethernet Signals are in power domain VDD\_HV\_B

The Ethernet interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD\_HVA is set to 5V, Ethernet MCU pads must be left as tri-state with no pullups.

- 7 PG13
- 7 PG12
- 7 PH0
- 7 PH1
- 7 PH2
- 7 PG1
- 7 PE13
- 7 PA7
- 7 PA8
- 7 PA9
- 7 PF15
- 7 PA11
- 7 PA10
- 7 PE12
- 7 PA3
- 7 PG0
- 7 PF14



Series Termination Resistors: 50 Ohms as per TI spec. Place resistors as close to driving source as possible. Termination recommended for ALL MII signals

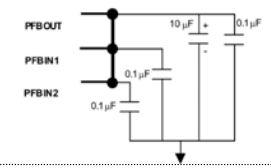
Reset Control:  
 - Reset from MCU Reset Out (will reset with MCU)  
 - Reset from GPIO. Allows MCU to reset PHY as well as hold PHY in reset while reset config data can be driven onto pins to change mode etc.

- Boot Configuration (using PHY internal Pulls)**
- Auto Negotiation Enable (All speeds / duplex supported) (AN\_EN, AN0 and AN1 all Internal PullUP)
  - Operating Mode (MII) (SNI\_Mode Internal PullDown, MII\_Mode control via PF15)
  - LED Configuraiton (Model) (LED\_CFG Internal PullUp)
  - MDIX Enable (Auto MDIX Enabled) (MDIX\_EN Internal PullUP)
  - Physical Address (set to 0b00001) (PHYAD[0] Internal PullUp, PHYAD[1..4] Internal PullDown)

**Layout Note:**  
 MII Mode resistor and the MDIP ullup resistor should be placed as close as possible to the PF15 / PF14 tracks to reduce the effect of a stub on the transmission line.

Layout Note - Place Caps and Resistors close to PHI

Layout Note: Place 0.1uF cap close to each pin. 10uF TANT as close to pin 23 as possible as shown in diagram below taken from TI device specifaicaton



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# FlexRAY Physical Interface

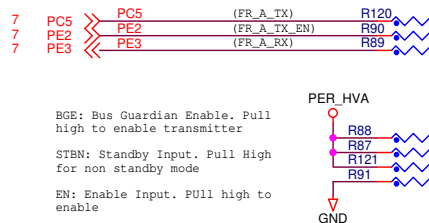
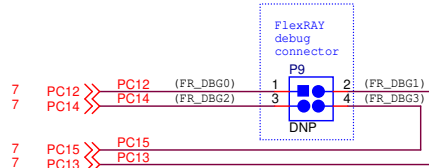
All Signals are in power domain VDD\_HV\_A.

FlexRAY interface will work at 3.3V or 5.0V (PER\_HVA)

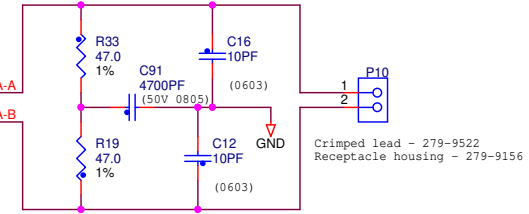
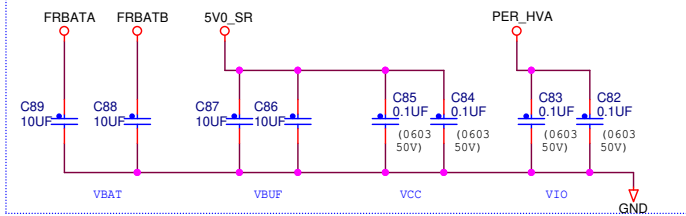
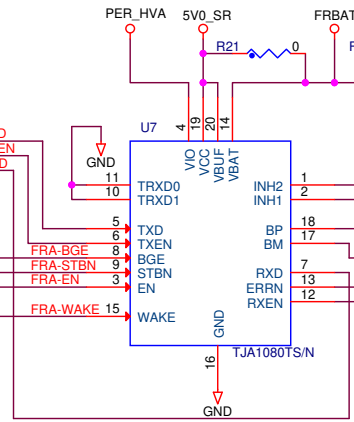
Note on VBAT:  
 - Operational range is 6.5v to 60v  
 - Undervoltage detection is max 4.5v

On EVB this is supplied from 5v, In theory this should be to battery with 60uS delay between applying Vbat and I/O voltages. If necessary, 12V can be externally supplied by removing the resistor and connecting pad to 12v

Decoupling Caps for BOTH IC's. Place next to power pins.



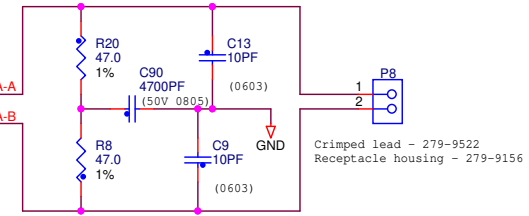
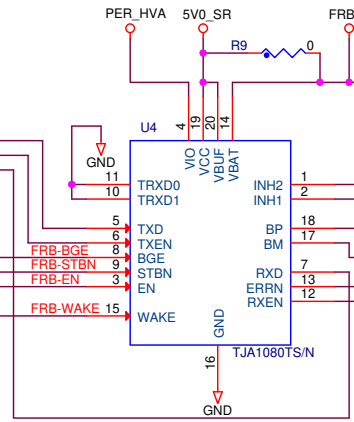
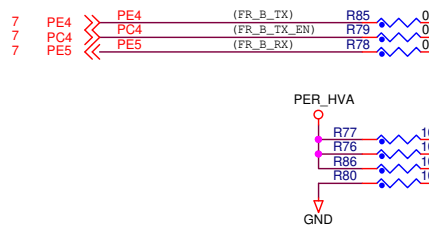
BGE: Bus Guardian Enable. Pull high to enable transmitter  
 STBN: Standby Input. Pull High for non standby mode  
 EN: Enable Input. Pull high to enable



Bus voltage +/- 12V (VBAT = 12v)  
 Components spec'd for 12V operation

## FlexRAY A

## FlexRAY B



Bus voltage +/- 12V (VBAT = 12v)  
 Components spec'd for 12V operation

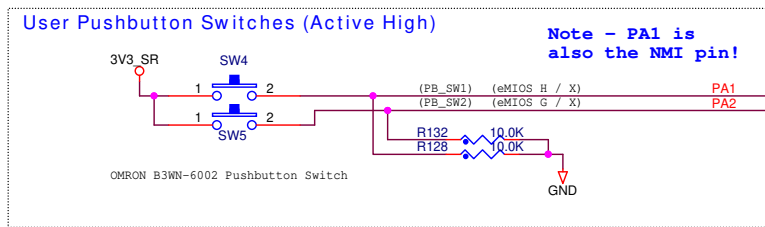
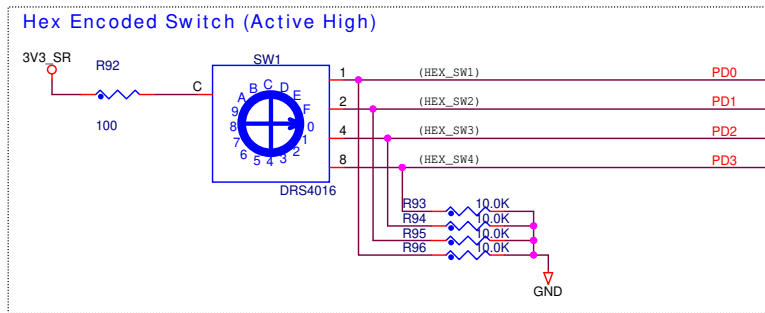
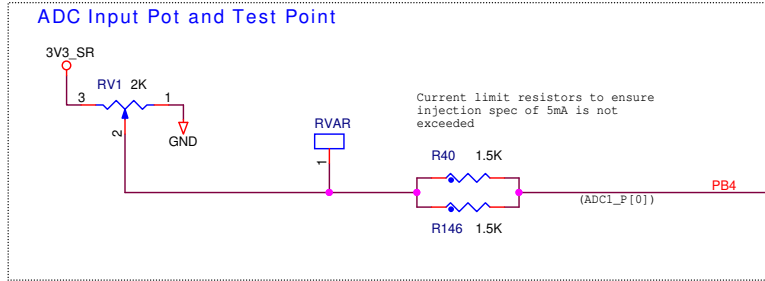
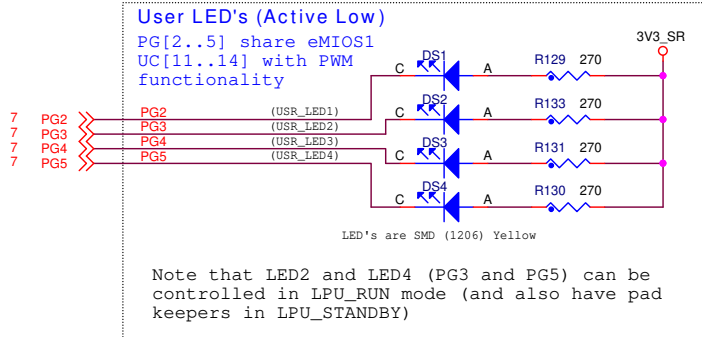
MODE	EN	STBN
Normal	1	1
Rec Only	0	1
Go to Sleep	1	0
Sleep	0	0

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# User Peripherals (Led's, Switches and ADC Pot)

Switches are hard wired to 3.3V rather than 5V so it's not possible to drive 5V into a 3.3V pad (which would cause damage)  
 Similarly, the LED's are active low with 3.3v supply so can be safely coupled to pads on either 3.3V or 5V domains  
 The ADC input is limited to 3.3V, again to prevent driving 5V into a 3.3V pad which would cause damage

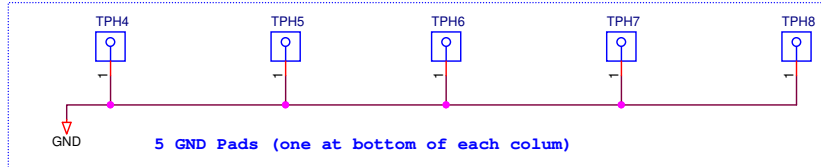
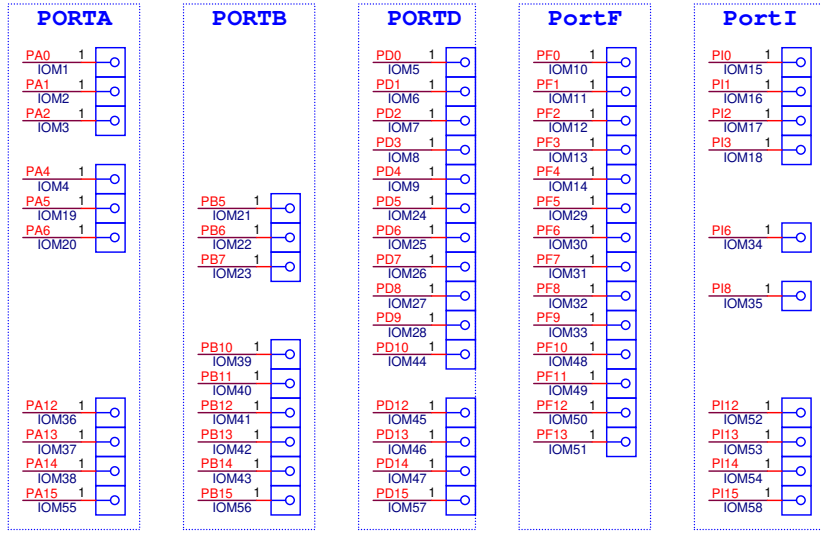


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# GPIO Pin Matrix

All pads are DNP (Do Not Populate) 0.1" pitch headers placed on a 0.1" grid

	7	PA0	PA0
	7,14	PA1	PA1
PA[1,2] shared with user switches	7,14	PA2	PA2
	7	PA4	PA4
	7	PA5	PA5
	7	PA6	PA6
	7	PA12	PA12
	7	PA13	PA13
	7	PA14	PA14
	7	PA15	PA15
	7	PB5	PB5
	7	PB6	PB6
	7	PB7	PB7
	7	PB10	PB10
	7	PB11	PB11
	7	PB12	PB12
	7	PB13	PB13
	7	PB14	PB14
	7	PB15	PB15
	7,14	PD0	PD0
	7,14	PD1	PD1
	7,14	PD2	PD2
	7,14	PD3	PD3
PD[0..3] shared with Hex Switch	7	PD4	PD4
	7	PD5	PD5
	7	PD6	PD6
	7	PD7	PD7
	7	PD8	PD8
	7	PD9	PD9
	7	PD10	PD10
	7	PD12	PD12
	7	PD13	PD13
	7	PD14	PD14
	7	PD15	PD15
	7	PF0	PF0
	7	PF1	PF1
	7	PF2	PF2
	7	PF3	PF3
	7	PF4	PF4
	7	PF5	PF5
	7	PF6	PF6
	7	PF7	PF7
	7	PF8	PF8
	7	PF9	PF9
	7	PF10	PF10
	7	PF11	PF11
	7	PF12	PF12
	7	PF13	PF13
	8	PI0	PI0
	8	PI1	PI1
	8	PI2	PI2
	8	PI3	PI3
	8	PI6	PI6
	8	PI8	PI8
	8	PI12	PI12
	8	PI13	PI13
	8	PI14	PI14
	8	PI15	PI15



**Layout Notes:**  
 Pads must be placed in a 5 (W) x 16(H) matrix pattern, 2.54 mm pitch  
 - one column for each port  
 - 16 tall (1 row for each port number from 0 to 15).  
 - GND pad at bottom of each column  
 - After production, pads should be through hole (not solder filled)

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