# TPS7A7001EVM-065 Evaluation Module

This user's guide describes operational use of the TPS7A7001EVM-065 evaluation module as a reference design for engineering demonstration and evaluation of the TPS7A7001, a low-dropout linear regulator. Included in this document are setup instructions, a schematic diagram, layout and thermal guidelines, a bill of materials, and test results.

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# 1 Introduction

The Texas Instruments TPS7A7001EVM-065 evaluation module (EVM) helps design engineers to evaluate the operation and performance of the TPS7A7001 family of linear regulators for use in their own circuit applications. This particular EVM configuration contains a single linear regulator with internal thermal and current-limit shutdown circuitry in a SOIC-8 package. The regulator is capable of delivering up to 2 A to the load depending on the input/output power dissipation across the part which can be minimized because of the very low-dropout voltage.

# 2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS7A7001EVM-065.

## *2.1 Input/Output Connectors and Jumper Descriptions*

The connectors are shown in Figure 3, Assembly Layer.

### 2.1.1 J1 – VIN

J1 is the input power supply voltage connector. Twist the positive input lead and ground return lead from the input power supply and keep as short as possible to minimize EMI transmission. Add additional bulk capacitance between J1 and J3 if the supply leads are greater than 6 inches. For example, an additional 47-μF electrolytic capacitor connected from J1 to ground can improve the transient response of the TPS7A7001, while eliminating unwanted ringing on the input due to long-wire connections.

### 2.1.2 J2 – VOUT

J2 is the regulated output voltage connector.

### 2.1.3 J3 – GND

J3 is the ground-return connector for the input power supply.

### 2.1.4 J4 – GND

J4 is the output ground-return connector.

## *2.2 Soldering Guidelines*

Any solder rework to modify the EVM for the purpose of repair or other application reasons must be performed using a hot-air system to avoid damaging the integrated circuit (IC).

## *2.3 Equipment Setup*

- Turn off the input power supply after verifying that its output voltage is set to less than 7 V. Connect the positive voltage lead from the input power supply to VIN at the J1 connector of the EVM. Connect the ground lead from the input power supply to GND at the J3 connector of the EVM.
- Connect a 0-A to 2-A load between the output, VOUT, at connector J2, and ground, GND, at connector J4.

# 3 Operation

- Turn on the input power supply. For initial operation set the input power supply, VIN – J1, to 5 V.
- Vary the respective loads and VIN voltages as necessary for test purposes.

# 4 Test Results

This section provides typical performance waveforms for the TPS7A7001EVM-065 printed-circuit board (PCB).



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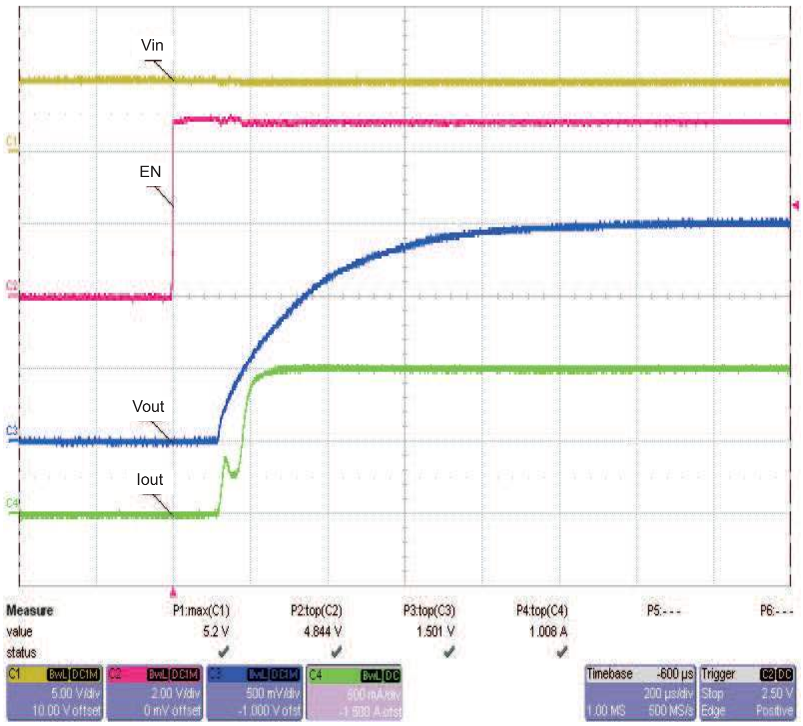
### 4.1 Turnon Sequence

Figure 1 shows the turnon/off characteristic where 3.3 V is quickly applied to VIN. The output drives a 1-A load. The output voltage start-up ramp is not load dependant.




NOTE: Yellow – VIN, Red – EN, Blue – VOUT, Green – IOUT

**Figure 1. Turnon Sequence**

### 4.2 Output Load Transient

Figure 2 shows the load transient response for a load-step transient from 100 mA to 1.6 A (IOUT, green). VIN is set at 5 V.



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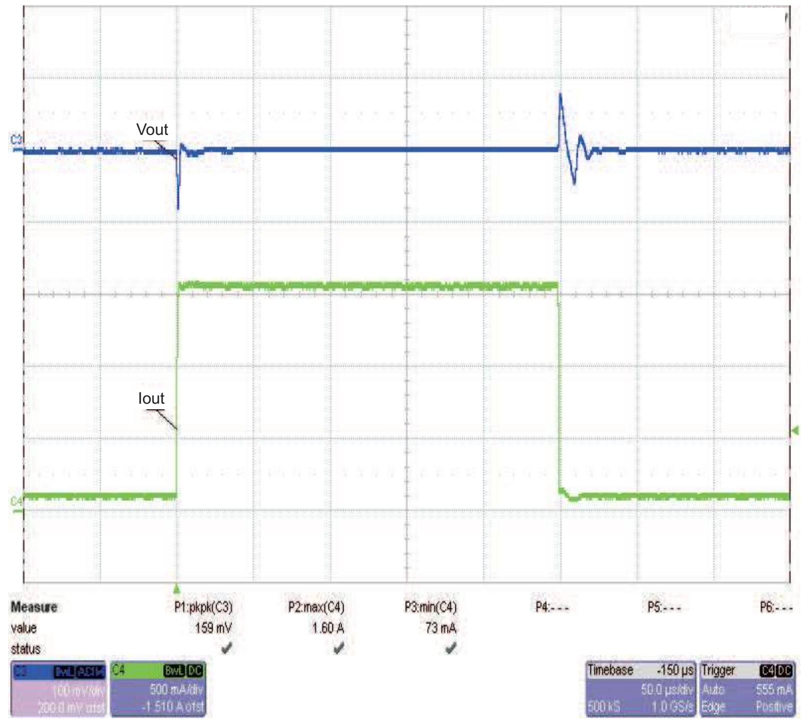


NOTE: Blue – VOUT, Green – IOUT

**Figure 2. Load-Step and Transient Response**

## 5 Thermal Guidelines and Layout Recommendations

Thermal management is a key component of design of any power converter and is especially important when the power dissipation in the low-dropout (LDO) regulator is high. Use the following formula to approximate the maximum power dissipation for the particular ambient temperature:

$T_J = T_A + P_D \times \theta_{JA}$

Where $T_J$ is the junction temperature, $T_A$ is the ambient temperature, $P_D$ is the power dissipation in the device (Watts), and $\theta_{JA}$ is the thermal resistance from junction to ambient. All temperatures are in degrees Celsius. The maximum silicon junction temperature, $T_J$, must not be allowed to exceed 150°C. The layout design must use copper trace and plane areas effectively, as thermal sinks, in order not to allow $T_J$ to exceed the absolute maximum rating under all temperature conditions and voltage conditions across the part.

The layout designer must carefully consider the thermal design of the PCB for optimal performance over temperature. For this EVM, Figure 4 shows that the PCB top VOUT plane has six, 6-mil thermal via connections to the bottom-side copper VOUT plane to dissipate heat. The PCB is a two-layer board with 2-oz. copper on top and bottom layers. The DDA package drawing can be found at the Texas Instruments Web site in the product folder for the TPS7A7001 LDO.

Table 1 repeats information from the Dissipation Ratings Table of the TPS7A7001 (SBVS134) data sheet for comparison with the thermal resistance, $\theta_{JA}$, calculated for this EVM layout to show the wide variation in thermal resistances for given copper areas. The High-K value is determined using a standard JEDEC High-K (2s2p) board having dimensions of 3-inch x 3-inch with 1-oz internal power and ground planes and 2-oz copper traces on top and bottom of the board.



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**Table 1. Thermal Resistance, $\theta_{JA}$, and Maximum Power Dissipation**

| Board | Package | $\theta_{JA}$ | Maximum Dissipation Without Derating ($T_A$ = 25°C) | Maximum Dissipation Without Derating ($T_A$ = 70°C) |
|---|---|---|---|---|
| High-K | DDA | 51.5°C/ W | 1.94 W | 1.06°C/ W |
| TPS7A7001EVM-065 | DDA | 23.6°C/ W | 4.24 W | 2.33 W |


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## 6 Board Layout

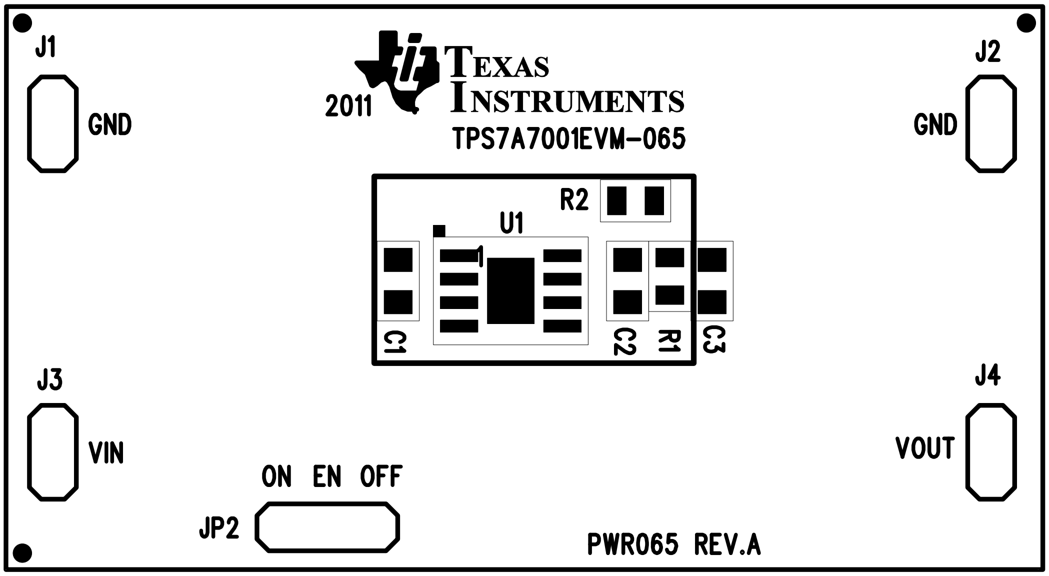


**Figure 3. Assembly Layer**

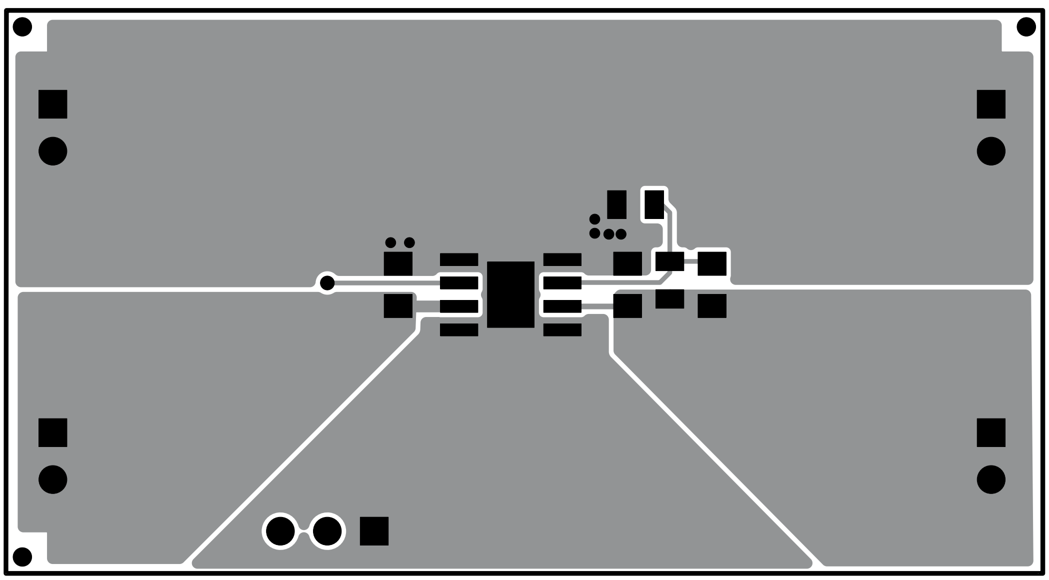

**Figure 4. Top-Layer Routing**



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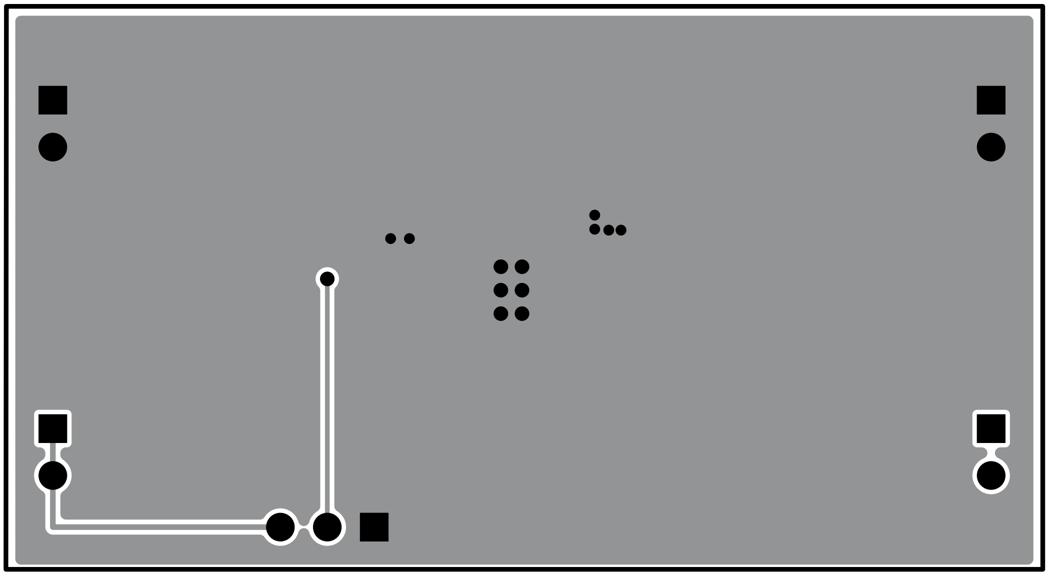

Figure 5. Bottom-Layer Routing

## 7 Schematic and Bill of Materials

### 7.1 Schematic

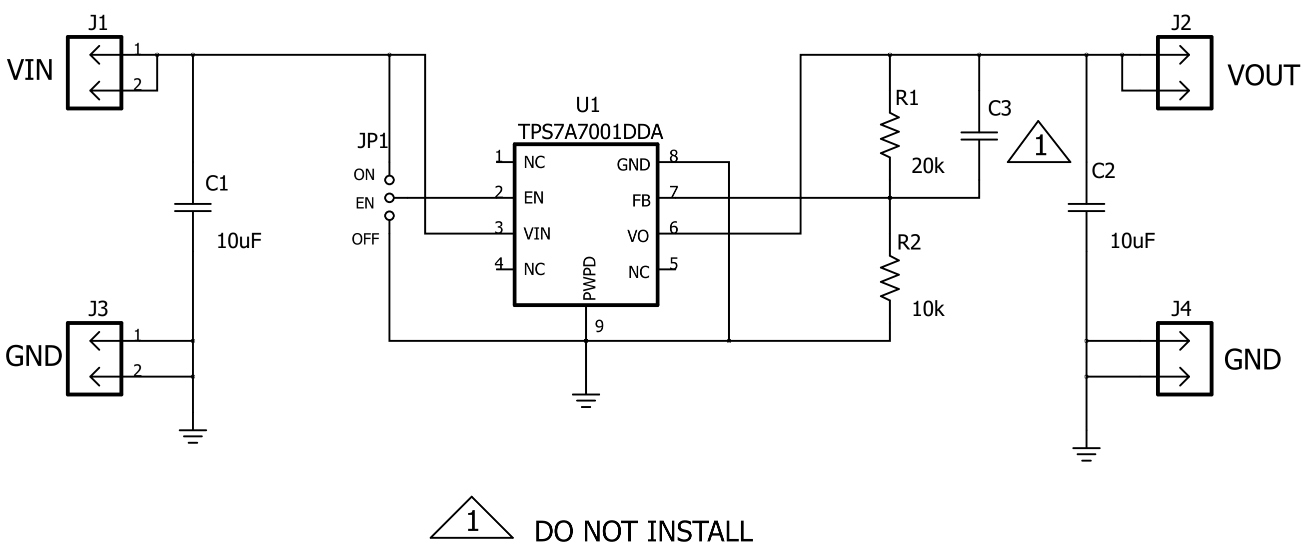


Figure 6. TPS7A7001EVM-065 Schematic

### 7.2 Bill of Materials

Table 2. TPS7A7001EVM-065 Bill of Materials

| Count | RefDes | Value | Description | Size | Part Number | MFR |
|---|---|---|---|---|---|---|
| 2 | C1-2 | 10 µF | Capacitor, Ceramic, 10-V, X7R, 10% | 0805 | STD | STD |
| 0 | C3 | Open | Capacitor, Ceramic, 10-V, X7R, 10% | 0805 | STD | STD |
| 4 | J1-4 | PEC02SAAN | Header, Male 2-pin, 100-mil spacing | 0.100 inch x 2 | STD | Sullins |


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**Table 2. TPS7A7001EVM-065 Bill of Materials (continued)**

| Count | RefDes | Value | Description | Size | Part Number | MFR |
|---|---|---|---|---|---|---|
| 1 | JP1 | PEC03SAAN | Header, Male 3-pin, 100-mil spacing | 0.100 inch x 3 | STD | Sullins |
| 1 | R1 | 20 kΩ | Resistor, Chip, 1/16-W, 1% | 0603 | STD | STD |
| 1 | R2 | 10 kΩ | Resistor, Chip, 1/16-W, 1% | 0603 | STD | STD |
| 1 | U1 | TPS7A7001DDA | IC, Wide Vin, Very Low-Dropout Regulator | HSOP | TPS7A7001DDA | TI |
| 1 | — | | PCB, 1.200 In x 2.200 In x 0.62 In | 1.20 x 2.200 x 0.62 In | PWR065 | Any |


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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125° C. The EVM is designed to operate properly with certain components above 125° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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**General Statement for EVMs including a radio**

*User Power/Frequency Use Obligations*: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

**For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant**

**Caution**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

**FCC Interference Statement for Class B EVM devices**

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

**For EVMs annotated as IC – INDUSTRY CANADA Compliant**

This Class A or B digital apparatus complies with Canadian ICES-003.

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**Concerning EVMs including radio transmitters**

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

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2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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